instruction_timeline

lbi r0, 0

lbi r5, 43

lbi r6, 43

lbi r7, 43

ld r1, r0, 0

st r5, r1, 0

ld r1, r0, 2

st r6, r5, 1

ld r1, r0, 4

st r7, r1, 1

halt

*How the processor should behave

Cycle	What's in write back	Reason to stall
5	lbi r0, 0	
6	lbi r5, 43	
7	lbi r6, 43	
8	lbi r7, 43	
9	ld r1, r0, 0	
10	nop	RAW, no forwarding
11	-	
12	st r5, r1, 0	
13	ld r1, r0, 2	
14	nop	RAW, no forwarding
15	-	
16	st r6, r5, 1	
17	ld r1, r0, 4	
18	nop	RAW, no forwarding
19	-	
20	st r7, r1, 1	
21	halt	