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In This Issue

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AnalogDialogue

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SFDR Considerations in Multi-Octave Wideband Digital Receivers

Benjamin Annino, Applications Director

Introduction

Electronic warfare (EW) receivers must intercept and identify unknown enemy signals among a congested wideband spectrum of multiple interfering signals without the benefit of dynamic range and sensitivity improvement techniques employed in communications and radar receivers. The incident RF band limiting employed in communications receivers is an unwanted trade for the EW receiver that seeks to process ever wider instantaneous bandwidth in less time. In the radar realm, receiver dynamic range benefits from matched filtering, whereby the received radar return is correlated with a copy of the transmitted signal. Alas, the EW receiver has no prior knowledge of the signal to be intercepted and thus nothing with which to correlate! It's like searching a crowd of people for a stranger you've never seen before … and worse yet, he is hiding, or maybe isn't even there!

Now for the good news: over the coming years, high sample rate analog-to-digital converter (ADC) and digital-to-analog converter (DAC) technology will usher in a wideband digital receiver architectural evolution. Most importantly, converters from Analog Devices will maintain the excellent linearity, noise performance, and dynamic range of legacy lower rate digital converters. The workhorse super-heterodyne tuner will give ground to direct sample and direct conversion architectures.[1] Adaptive spectral tuning will continue to shift from the RF to the digital signal processing realm.

This sea change in wideband RF sensing will enable size, weight, power, and cost (SWaP-C) benefits: higher receive and transmit channel counts at lower cost per channel, in the same or smaller sized form factors as today.

Anticipating the coming era of digital EW receivers with multi-octave bandwidth, this article discusses new challenges and considerations when designing for best-in-class dynamic range. In this article, dynamic range refers to instantaneous spur free dynamic range, the key figure of merit for receivers tasked with detecting small signals among a crowded spectrum of larger blockers.

Next-Generation ADC Performance

Many of today's EW receivers feature sub-octave instantaneous bandwidth (IBW) that is limited by the older generation data converter. These will be replaced tomorrow with multi-octave wideband digital receivers spanning several GHz of IBW. For example, in the coming years a growing number of sensing platforms will employ ADI converter chips featuring ADCs and DACs with the ability to process greater than 4 GHz IBW while maintaining SFDR greater than 70 dB.[2,3,4]

A popular low SWaP, wideband digital receiver ADC use case might be:

- An ADC sample rate of ~15 GSPS
- A direct sample of the first Nyquist zone (that is, dc to 6 GHz)
- A direct sample of the second Nyquist zone (that is, 8 GHz to 14 GHz)
- RF block convert middle (6 GHz to 8 GHz) and higher (>14 GHz) bands

EW receivers need to cover higher and higher swaths of spectrum from 18 GHz to 50 GHz and beyond. The ADC's high second Nyquist zone eases the frequency plan, allowing simple RF front-end block converters with relaxed, smaller SWaP RF filters. The following discussion considers an RF front end cascaded with a high sample rate ADC similar to the previous example.

Dynamic Range in Wideband Digital Receivers

Receiver designers optimizing dynamic range must balance sensitivity (NF) with linearity (IP2, IP3) as these RF device attributes usually move against each other. Dynamic range is bound by sensitivity at lower RF levels and linearity at higher RF levels. As a rule of thumb, the maximum allowed receiver operating level is set so that the multisignal intermodulation distortion (IMD) spurious levels are equal to the noise power, as shown in Figure 1. Modern systems use adaptive instantaneous bandwidth channelization and processing bandwidths (B_v), which moves the noise floor up and down $10\text{Log}(B_v)$. The nuanced topic of processing bandwidth is critical and receives its own discussion later.

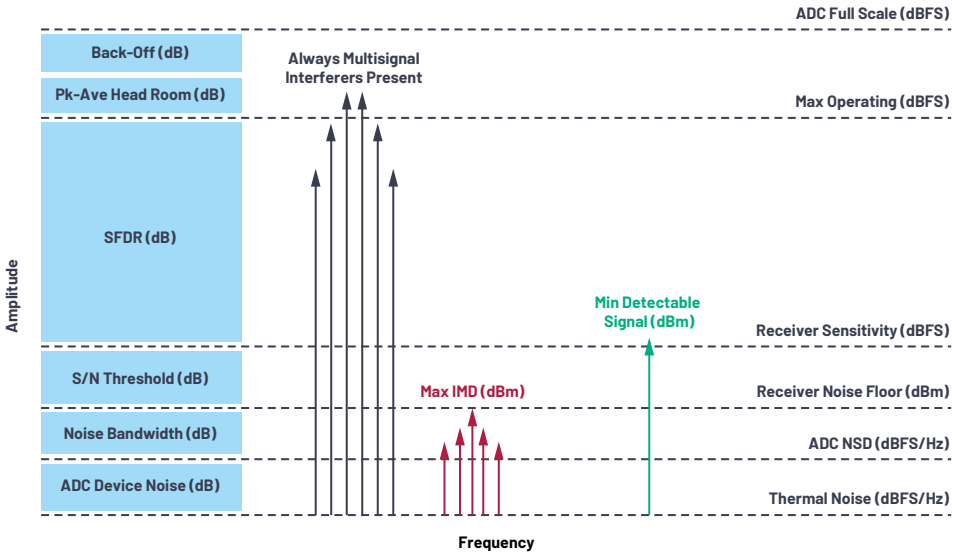


Figure 1. Relating SFDR to ADC operating range, noise, IMD spurs, and detection threshold.

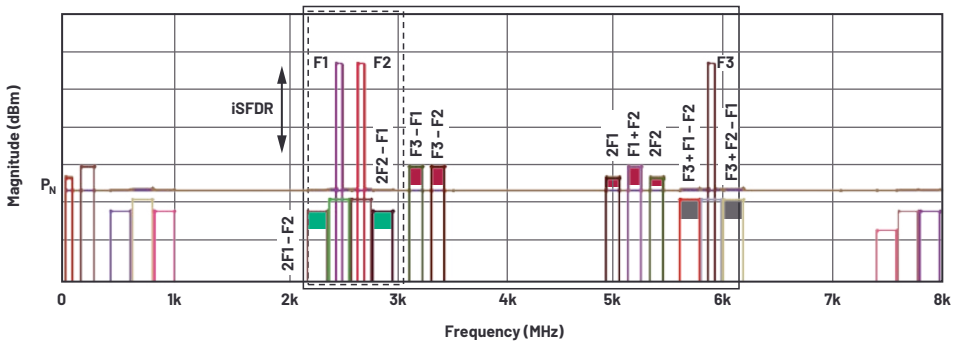


Figure 2. An example of multisignal F1, F2, and F3 (60 MHz each) inducing second-harmonic, IMD2 (red), IMD3 (green), and IMD2/3 combo (gray) spurs. The noise floor (brown) is noted as P_N.

Multi-Octave IMD2 Challenges in Wideband Digital Receivers

The wideband digital receiver evolution introduces new RF challenges. Multisignal second-order intermodulation distortion (IMD2) spurs emerge as problematic dynamic range impairments in the multi-octave wideband digital receiver. While IIP3 has long been a key figure of merit (FOM) in RF device data sheets, IIP2 is harder to track down and can be more problematic to the EW designer. The problem with IMD2 spurs is that they only fall off by 1 dBc for every 1 dB decrease in the incident 2-tone signal power, while third-order intermodulation distortion (IMD3) spurs fall off by 2 dBc.

Of course, multi-octave direct RF sampling at the lower portion of the ADC first Nyquist zone is nothing new. For example, an older system might sample at 500 MSPS and observe dc to 200 MHz in the first Nyquist zone with no IMD2 problems. This is because at these lower frequencies (that is, less than a few hundred MSPS), ADC characteristics are highly linear and the effective IIP2 and IIP3 of the ADC is very high, resulting in benign IMD2 products invisible below the noise floor. Just like in wideband RF devices, however, multi-GHz, multi-octave ADC linearity will degrade with increasing frequency, and IMD2 products will often sit above the noise floor at higher operating frequencies. Going forward, we'll need to deal with IMD2.

Broadened SFDR Definition for Wideband Digital Receivers

IMD2 crashing the party requires a refreshed definition of the popular receiver FOM instantaneous spurious-free dynamic range (SFDR). SFDR specifies how far down a receiver can detect a small signal when there are multiple larger signals creating IMD spurs. SFDR is specified in dB relative to the large signals.

Traditionally, SFDR is defined in terms of IMD3 products, along with NF and processing bandwidth. IMD3-referenced SFDR is derived in many texts, and is sometimes clarified as instantaneous SFDR, which is what we mean in this article.[5,6] We'll call it SFDR3:

$$\begin{aligned} &SFDR3 \text{ dB} = 2/3\ [IIP3 \text{ dBm} - P_N \text{ dBm}] - [S/N \text{ threshold dB}] \\ &P_N = -174 \text{ dBm/Hz} + NF \text{ dB} + 10Log_{10}[B_v/\text{Hz}] \text{ dB} \\ &B_v = \text{processing bandwidth Hz} \end{aligned} \quad (1)$$

Today IMD2-referenced SFDR receives less attention, but it is looming on the horizon as a major impairment needing mitigation. It can be derived in the same manner as SFDR3. Here we'll call it SFDR2:

$$SFDR2 \text{ dB} = 1/2\ [IIP2 \text{ dBm} - P_N \text{ dBm}] - [S/N \text{ threshold dB}] \quad (2)$$

Figure 2 illustrates an RF front-end spectral scenario whereby three simultaneous signals (F1, F2, and F3) create intermodulation products that set the lower bound to dynamic range. Below this level, the wideband digital receiver can't easily tell whether a target is real or a false IMD spur.

The sub-octave IBW receiver of today, notionally shown by the Figure 2 dashed box, worries only about IMD3 because it falls in-band and cannot be filtered. It doesn't worry much about IP2 because of the easily filtered location of IMD2 and the inducing signals. F3 is easily chopped down using input RF filtering, which takes F3 – F1 and F3 – F2 way below the noise floor. Much like the F1 and F2 second harmonics, the F1 + F2 IMD2 is easily attenuated using output filtering. Of course, the second-order performance of the ADC must be considered in relation to Nyquist folding spurs, but the front-end IMD2 performance is easy to deal with.

Enter the multi-octave IBW receiver, notionally shown by the Figure 2 solid box, and the situation turns on its head. IMD2 is the bigger concern vs. IMD3. The IMD2 spurs and inducing interferers are now in-band. Band-pass filtering them defeats the purpose of a multi-octave IBW. This is why tunable notch filtering, despite its limitations, is seeing increased attention as a front-end interference mitigator. It doesn't lop off giant pieces of the multi-octave spectrum.

Figure 3 illustrates the relationship between the fundamental multi-tone large signal, IMD2 and IMD3 level, noise floor, and the resulting SFDR for an example multi-octave wideband digital receiver. The example uses real noise and linearity attributes for an ADC sampling the first Nyquist zone with a 4 GHz IBW from 2 GHz to 6 GHz. A processing bandwidth of 469 kHz is assumed.

Optimal SFDR2 and SFDR3 occur at different P_{in} operating points where the respective IMD level intersects the noise power. If we pretend for a moment that this is a sub-octave receiver with front-end RF band-limiting, SFDR3 sets the overall SFDR, and we can expect a best case SFDR of 79 dB, which is very good. But since the EW receiver requires multi-octave IBW, SFDR2 sets the overall SFDR. At the best SFDR3 input level (P_{in} = –20 dBm), the IMD2 spurs degrade the SFDR by 24 dB, resulting in an SFDR of 55 dB. Fair, albeit disappointing, results.

A useful rule of thumb is that for a specific RF output level = $P_{RF,0}$ to achieve equivalent IMD2 and IMD3 levels:

$$OIP2 \text{ dBm} = 2OIP3 \text{ dBm} - P_{RF,O} \text{ dBm} \quad (3)$$

In other words, this condition will make the SFDR2 and SFDR3 lines intersect the noise floor at the same spot, so that SFDR2 is not limiting performance.

For the previous SFDR example scenario, the RF front end feeds the ADC with –20 dBm and has an OIP3 of 20 dBm. The required OIP2 to get the same level IMD2 and IMD3 spurs, and thereby not limit performance, is:

$$OIP2 \text{ dBm} = 2(20 \text{ dBm}) - (-20 \text{ dBm}) = 60 \text{ dBm} \quad (4)$$

That raw device OIP2 performance is not available today given the balance with other attributes like frequency, bandwidth, noise, and dc power. This explains the increasing interest in next-generation adaptive front-end interferer mitigation techniques.

To mitigate IMD2, the receiver must lower the max input operating level from –20 dBm to –32 dBm, and is then able to achieve an improved SFDR2 of 66 dB best case. In Figure 3, this optimal SFDR2 is where the IMD2 trace intersects the noise floor. Alas, the best case SFDR2 at P_{in} = –32 dBm is still 13 dB worse than the best case SFDR3 at –20 dBm. Since we've now shifted the max operating level down, this puts the spotlight on noise power (sensitivity) limitations, as discussed in the next sections.

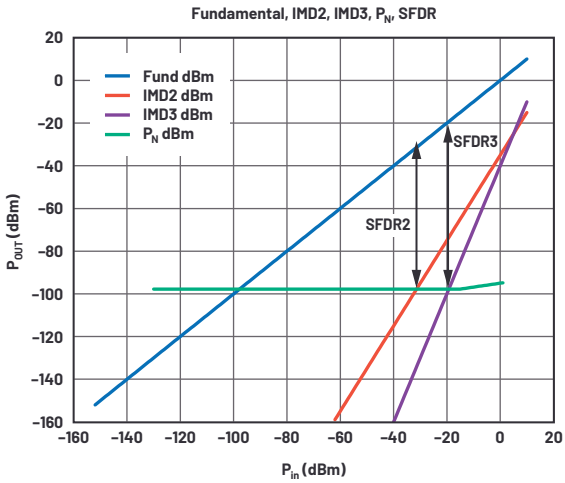
What Sets Processing Bandwidth in the Wideband Digital Receiver?

The sensitivity, or noise power, of the EW receiver gets better as the processing bandwidth narrows. In typical fashion, however, there are trade-offs to balance: we can't just reduce the bandwidth to an arbitrarily small value and head to lunch. What are the competing factors to consider? To answer the question, we need to discuss decimation, the fast Fourier transform (FFT), and their relationship. First, we define a couple variables:

M is the ADC decimation factor of the digital data stream

N is the FFT length, proportional to the sample time duration (5)

ADI's high sample rate ADCs employ on-chip digital signal processor (DSP) blocks that allow configurable filtering and decimation of the raw data stream to a minimum viable payload sent to the downstream FPGA. This process is discussed in detail across ADI literature.[3] The obvious benefit of decimation is reducing the digital payload that must pass over JESD204B/JESD204C to the FPGA. Another benefit is the power consumption savings realized using local on-chip decimation-specific circuitry (that is, ASIC) vs. implementing the same operation in the FPGA fabric. But local on-chip decimation is beneficial beyond just thinning the data stream and saving power. We'll get to that.



Parameter	Value	Units
f_S	15.36	GSPS
IIP3	20	dBm
IIP2	35	dBm
Full scale	–6.5	dBm
NSD	–148	dBFS/Hz
BW_proc	469	kHz
P_N	–98	dBm
iSFDR3	79	dB
iSFDR2	66	dB

Figure 3. SFDR2 and SFDR3 tell you how far down from the largest signal (fundamental) you can easily detect a smaller signal. Because it varies widely, the detection threshold is zero here. In practice, subtract your detection threshold from SFDR.

Figure 4 shows the blocks used in modern wideband digital conversion (as relevant to this discussion). The flow consists of sampling, digital downconverting, digital filtering, decimating, and fast Fourier transforming the data stream.

First, the data sampled at f_S is digital downconverted to baseband (complex I/Q) using a fine-tuned NCO. The data stream is then filtered using a programmable low-pass digital filter. This predecimation digital filtering sets the IF bandwidth and is the first of two different operations to set the receiver noise floor P_N. As the IF bandwidth gets smaller, the integrated in-band noise power decreases as the filtering attenuates the wideband noise.

$$IF\ (noise)\ channel\ bandwidth = f_S/2M \quad (6)$$

Next, decimating by M reduces the effective sampling rate to f_S/M, keeping every M^{th} sample and throwing out the samples in between.

Thus, the downstream FFT processing gets a data stream with rate f_S/M and bandwidth $f_S/2M$. Finally, the FFT length N sets the bin width and capture time, which is the second step in setting the noise floor.

$$FFT\ bin = [IF\ channel\ BW]\ /\ [N/2]\ \text{Hz} = f_S/[MN]\ \text{Hz} \quad (7)$$

Decimation and FFT Impact to Wideband Digital Receiver Noise Floor

Figure 5 relates the wideband digital receiver's processing noise floor (K) to the ADC's noise spectral density (L), which is the widely available data sheet FOM for ADC additive noise. Existing ADI literature does a nice job explaining processing gain, NSD, SNR, and quantization noise.[7]

The most useful relation from Figure 5 is:

$$K = L + F$$
$$Or,\ in\ other\ words$$
$$Processing\ noise\ floor\ (\text{dBFS}) = NSD\ (\text{dBFS/Hz}) + 10Log_{10}[f_S/(MN)/\text{Hz}]\ (\text{dB}) \quad (8)$$

The processing noise floor (Figure 5, K) is the same as P_N and can be dropped into Equation 1 and Equation 2. Note that the designer carefully selects M and N based upon design trade-offs and constraints discussed in the next section.

Even though increasing the decimation factor M has the same proportional effect in reducing the noise floor (Figure 5, C) as increasing the FFT length N (Figure 5, E), it is important to note the mechanisms are entirely different. The decimation step involves band-limiting the channel using digital filtering. This sets the effective noise bandwidth that determines the total integrated noise in the channel (Figure 5, D). It also sets the maximum instantaneous spectral bandwidth of a detectable signal. Compare this to the FFT step, which does not filter per se, but spreads the total integrated noise in the channel over N/2 bins and defines the spectral line resolution. The higher N, the more bins, and the lower the noise content per bin.[8] Together, decimation gain M and FFT gain N define the FFT bin width, and they are often lumped together in discussions of processing bandwidth (Figure 5, F), but their values must be balanced based upon their respective nuanced impact to signal bandwidth, spectral resolution, sensitivity, and latency requirements, as discussed in the next section.

Processing Bandwidth and System Performance Trade-Offs

Relating decimation M and FFT N back to high priority performance attributes:

Latency is the time to sense and process successive spectral captures, and it requires as short a time as possible. Many systems require near real-time operation. This dictates M × N be as small as possible. As the FFT size increases, the spectral resolution improves and noise floor decreases as the integrated noise is spread over more bins. The trade-off is acquisition time, which is a big deal and is simply:

$$Time = N \times M \times t_s\ (seconds) \quad (9)$$

The minimum detectable pulse width (PW) sets the minimum allowable IF channel bandwidth as the spectral content of a shorter time pulse spreads over a relatively wider frequency band. If the IF channel bandwidth is too narrow, the signal spectral content truncates, and the short time pulse isn't detected properly. Minimum IF BW, which sets maximum allowable M, must meet the criteria:

$$f_S/[2M] > [1/PW]\ \text{Hz} \quad (10)$$

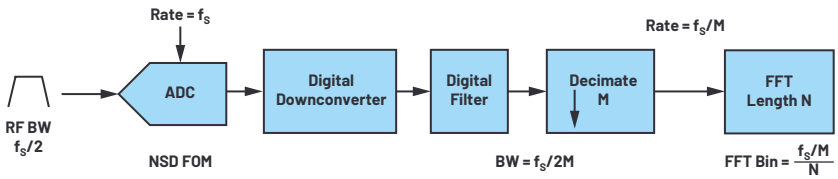


Figure 4. Simple block diagram of ADC data decimation and FFT.

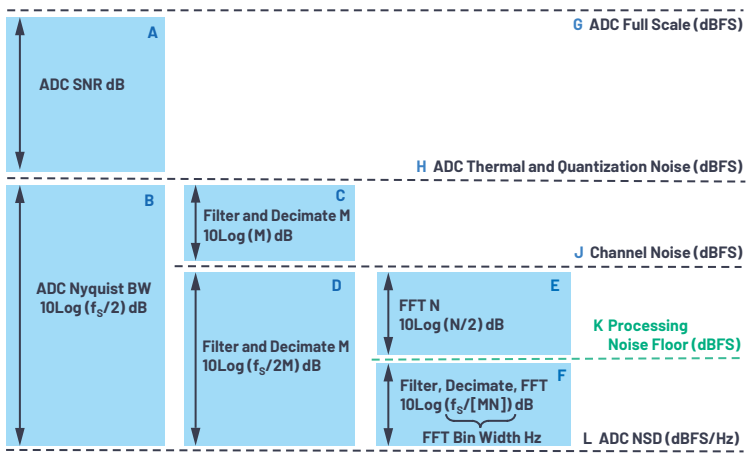


Figure 5. Relationship of decimation and FFT gain operations to commonly referenced noise levels.

Spectral resolution and sensitivity improve as the FFT bin narrows, which requires increasing N. Longer pulse widths and PRIs require finer resolution to resolve closer spectral lines, which means larger N for proper detection. Increasing N improves spectral line resolution, but only within the IF bandwidth defined by M. If too high a decimation is used, increasing N improves the spectral resolution within the IF BW set by M, but cannot recover the missing signal bandwidth. For example, a pulse train with a pulse width below the minimum receiver pulse width will have a frequency domain sinc function whose main lobe exceeds the decimation bandwidth. Increasing N will help resolve the PRF of the train, but will do nothing to resolve the pulse width; that information is lost. The only fix is to decrease decimation M, increasing the IF bandwidth.

Decimation, FFT, and Detection of Pulse Trains

EW wideband digital receivers spend a lot of their effort de-interleaving, identifying, and tracking simultaneous incident radar pulse trains. Carrier frequency, pulse width, and pulse repetition interval (PRI) are radar signatures that are critical in figuring out who's who. Both the time and frequency domain are used in detection schemes.[9] An overarching objective is to sense, process, and react to the pulse trains in as short a time duration as possible. Dynamic range is critical because the EW receiver needs to simultaneously track multiple distant targets while being bombarded with high energy jamming pulses.

Pulse Train FFT Examples

Two pulse train examples are presented. The first represents a pulsed doppler radar exhibiting a very short PW (100 ns) at 10% duty cycle, resulting in very high PRF. The second simulates a pulsed radar exhibiting comparatively longer PW and PRI (lower duty cycle, lower PRF). The following plots and tables illustrate the impact of decimation M and FFT length N on time, sensitivity (noise floor), and spectral resolution. Table 1 summarizes the parameters for easy comparison. The fictional values do not represent specific radars but are nevertheless in a realistic ballpark.[10]

Table 1. Comparison of Example Pulsed Doppler and Pulsed Radar Attributes

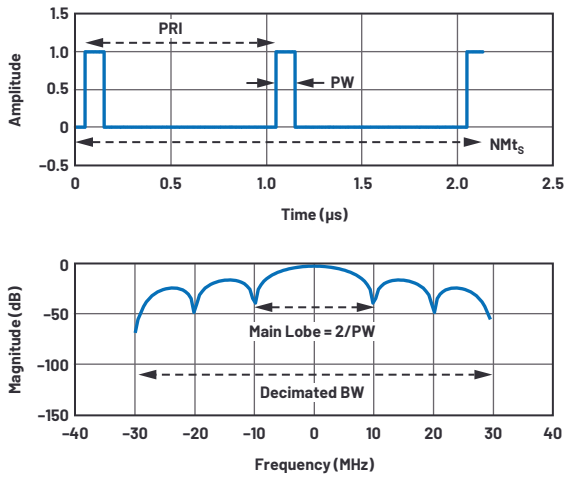
Parameter	Pulsed Doppler Radar		Pulsed Radar	
PW	Short	100 ns	Longer	10 µs
PRI	Short	1 µs	Longer	1 ms
PRF	High	1 MHz	Low	1 kHz
Duty Cycle	Mid/high	10%	Mid/low	1%
Decimation M	Low	256	High	1536
FFT Length N	Low	128 to 512	High	16,384 to 65,536
Time	Quick	2 µs to 9 µs	Longer	2 ms to 7 ms
Sensitivity	Lower	-91 dBFS	Higher	-120 dBFS

The point here is that M and N are not one size fits all, and sophisticated detection algorithms and parallel channelization schemes in any given EW receiver may employ a wide range of values for each. The EW receiver must be able to detect both signals, likely at the same time (not shown here), which is why fast, adaptable configurability is important. Dynamic range and sensitivity are directly dependent on the pulse attributes that must be detected.

Example: Wideband Digital Receiver Sensing Pulsed Doppler Radar

The following two FFTs capture a pulsed doppler scenario.

The first FFT shown in Figure 6 needs just over 2 pulse cycles to determine the pulse width of the signal from the width of the FFT main lobe. The decimation M is set for an IF bandwidth that is adequately wide to capture the main lobe, as well as some sidelobes. The response time is very fast. The trade-off to quick response time is a worse noise floor and spectral resolution. Note that due to the lack of spectral resolution, no PRI information is available in the FFT.



Parameter	Value	Units
F_{SAMPLE}	15.36	GSPS
N	128	
M	256	
M × N	32,768	
FFT Bin	469	kHz
Time (NMt_S)	2	µs
PW	100	ns
Duty	10	%
PRF	1	MHz
PRI	1	µs
Noise Floor	-91	dBFS

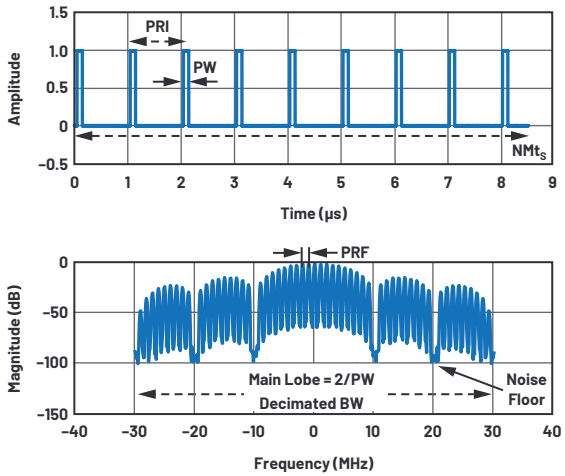
Figure 6. Fast capture of narrow pulse width, high PRF pulse train typical of pulsed doppler radar.

The second FFT in Figure 7 shows an improved noise floor and spectral resolution as sample length N (and time) are increased. M remains the same. By around nine pulse cycles, the spectral resolution improves enough to determine the PRI (1/PRF) from the FFT. The noise floor can be seen between sidelobes.

Example: Wideband Digital Receiver Sensing Pulsed Radar

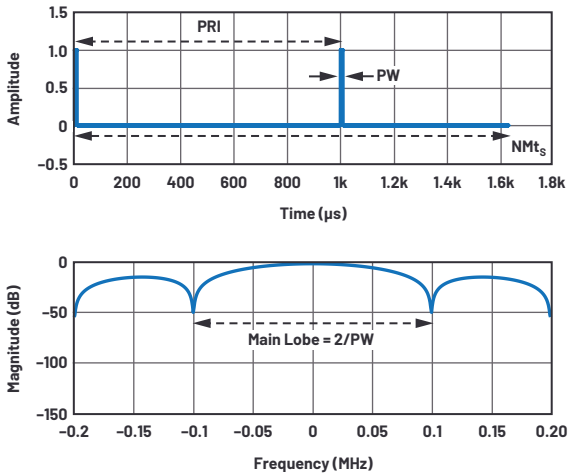
The following two FFTs capture a wider pulsed scenario.

The much wider PRI, or lower pulse density, in the pulsed radar example in Figure 8 requires much higher N. Adjusting M is entirely system dependent. If the short pulse must be detected simultaneously with the long pulse in the same IF channel, then M must be set to accommodate the short pulse spectral bandwidth and cannot be increased. Considered on its own, the long pulse requires a lower IF bandwidth, so M could be set higher to improve the channel noise and resulting sensitivity. The capture time, or FFT length N, required is a lot longer, however. So it's likely the detection algorithm would want to make intermediate decisions on the short pulse scenario while the system acquires a high enough N to resolve the long pulse.



Parameter	Value	Units
F_{SAMPLE}	15.36	GSPS
N	512	
M	256	
M × N	131,072	
FFT Bin	117	kHz
Time (NMt$_S$)	8.5	µs
PW	100	ns
Duty	10	%
PRF	1	MHz
PRI	1	µs
Noise Floor	-97	dBFS

Figure 7. A longer FFT of a pulsed Doppler example to resolve spectral lines.



Parameter	Value	Units
F_{SAMPLE}	15.36	GSPS
N	16,384	
M	1536	
M × N	25.2M	
FFT Bin	0.6	kHz
Time (NMt$_S$)	1.6	ms
PW	10	µs
Duty	1	%
PRF	1	kHz
PRI	1	ms
Noise Floor	-120	dBFS

Figure 8. Fast capture of longer pulse, lower PRF pulse train typical of pulsed radar.

The second long pulse FFT example in Figure 9 illustrates how the long PRI (low PRF) results in very close spectral lines, which requires very low FFT bin size or resolution bandwidth. The trade-off is even more time required (FFT N). A benefit is even better sensitivity.

Wideband Digital Receiver RF Front-End Design Using a Cascaded ADC

With dynamic range and sensitivity goals established, an RF front end must be paired with the digital data converter. The optimal RF front end sets the receiver sensitivity (NF) and performs the required spectral signal conditioning with good enough linearity head room to allow the ADC performance to set receiver IP3 and IP2. Front-end RF gain is typically set to be good enough to establish the required cascaded NF, as gain beyond that generally hurts dynamic range and is avoided. It is criminal if the front end bottlenecks dynamic range and ADC capability is thrown out!

A helpful trick is to convert the ADC figures of merit to equivalent RF cascade parameters and treat the ADC like an RF black box. Some rules of thumb:

$$\begin{aligned} ADC\ NF\ \text{dB} &= ADC\ NSD\ (\text{dBm/Hz}) + 174\ (\text{dBm/Hz}) \\ ADC\ IIP2\ \text{dBm} &= 2P_{RF}\ (\text{dBm}) - IMD2\ (\text{dBm}) \\ ADC\ IIP3\ \text{dBm} &= [3P_{RF}\ (\text{dBm}) - IMD3\ (\text{dBm})]/2 \end{aligned} \quad (11)$$

Where PRF (dBm) is the ADC input RF level at which the IMD3 and IMD2 levels are measured.

Note that the cascaded system NF of the combination front end and ADC is broadband noise prior to adjusting for processing gain.

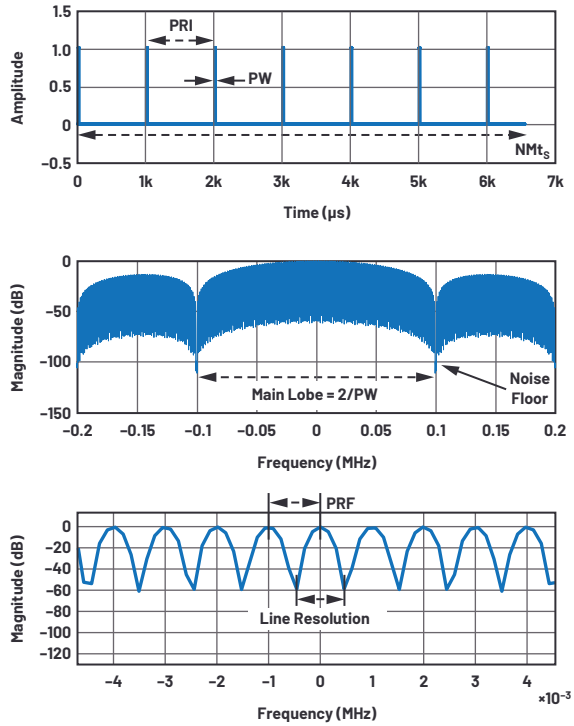
Design Example of Front End to ADC Cascade

An example cascade analysis follows using the front end shown in Figure 10. This chain benefits from the latest ADI releases to the RF catalog, including:

- ADMV8818 wideband programmable high-pass/low-pass tunable filter.
- ADRF5730 wideband RF SOI digital attenuator.
- ADRF5020 wideband RF SOI SPDT.
- ADL8104 ultrahigh IP2 wideband RF amplifier.
- AD9082 MxFE 4× DAC (12 GSPS) + 2× ADC (6 GSPS)

Additionally, the chain features a wideband 200 W RF limiter and small form factor high Q fixed filtering developed at ADI.

An age-old technique to preserve dynamic range is to switch between a high sense mode for lower input signals and bypass mode for higher input signals. As shown in Table 2, the high sense path favors NF performance, and the bypass path concedes higher NF in favor of higher linearity (IP2 and IP3). The performance tables illustrate this benefit.



Parameter	Value	Units
F_{SAMPLE}	15.36	GSPS
N	65,536	
M	1536	
M × N	101M	
FFT Bin	0.153	kHz
Time (NMt$_S$)	6.6	ms
PW	10	µs
Duty	1	%
PRF	1	kHz
PRI	1	ms
Noise Floor	-126	dBFS

Figure 9. A longer FFT of pulsed example to resolve spectral lines.

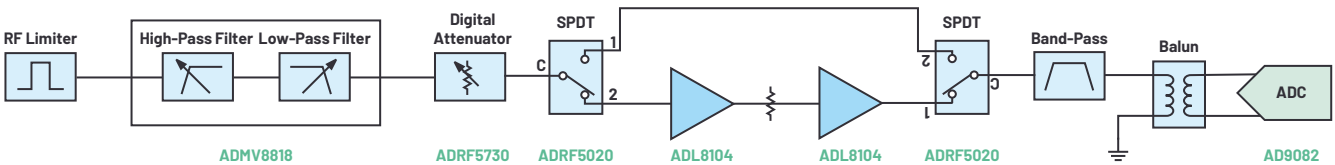


Figure 10. Example RF front end featuring switched high sensitivity and bypass modes.

Table 2. Example RF Front-End Black Box Parameters for the Two Modes

Mode	G (dB)	NF (dB)	IIP2 (dBm)	IIP3 (dBm)	IP1dB (dBm)
High Sense	10	15	31	17	5
Bypass	–14	14	75	40	25

Table 3 compares the front end and ADC black box parameters, and the resulting overall cascade performance.

In the high sense mode, the limiting factor to dynamic range is the noise floor, and so cascaded NF is prioritized. The front-end noise figure depends mostly on the insertion loss of the front-end filtering required for interferer mitigation (this example budgets 6 dB loss). This preselect filtering needs to sit before the amplifier to be effective, as the amplifier will create multisignal IMD products.

In bypass mode, we benefit from the extremely high linearity of the SOI technology. No tricks here as the amplifier limited linearity is simply switched out in favor of higher linearity, lower gain, and higher NF.

Table 3. Example High Sense (top) and Bypass (bottom) Cascaded Performance; the Overall Column Is the Cascaded RF Front End plus ADC All-In Performance

	RF Front End	ADC	Overall	Units
Full Scale		–6.5		dBm
NSD		–148		dBFS/Hz
		–154.5		dBFS/Hz
Gain	10	0		dB
NF	15	19.5	16.1	dB
IIP2	31	35	21.5	dBm
IIP3	17	20	9.2	dBm
Pi	–40	–30		dBm
P_N			–91.2	dBm
	RF Front End	ADC	Overall	Units
Full Scale		–6.5		dBm
NSD		–148		dBFS/Hz
		–154.5		dBFS/Hz
Gain	–14	0		dB
NF	14	19.5	33.5	dB
IIP2	75	35	48.6	dBm
IIP3	40	20	33.0	dBm
Pi	–15	–29		dBm
P_N			–97.8	dBm

Wideband Digital Receiver Design Results and Optimization

The following performance heat maps are sensitivity analyses showing instantaneous spur free dynamic range (DR, dB) for varying:

- Processing bandwidth and RF input level
- RF front-end IIP2 and RF input level
- RF front-end NF and RF input level

Each scenario is run for the high sensitivity and bypass paths. The boxes annotate favorable operating zones. The tables tell you the dynamic range (SFDR), or distance down to the noise floor or highest IMD spur, for a given max input signal level at P_{in}. For any given table, the static variables are set per the previous chain parameters.

As discussed in prior sections, the B_v selected in Figure 11 is dependent upon waveform detection objectives. Lower B_v decreases the noise floor, improving dynamic range at low P_{in}, but at the expense of slower FFT times. Inversely, high B_v values increase the noise floor, and poor sensitivity limits dynamic range. The likely operating zone is at a balance point in between.

DR (dB)		P_{in} (dBm)										
	61	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
B_v (Hz)	1.00E+02	58	68	78	71	61	56	51	46	41	36	31
	1.00E+03	48	58	68	71	61	56	51	46	41	36	31
	1.00E+04	38	48	58	68	61	56	51	46	41	36	31
	1.00E+05	28	38	48	58	61	56	51	46	41	36	31
	1.00E+06	18	28	38	48	58	56	51	46	41	36	31
	1.00E+07	8	18	28	38	48	53	51	46	41	36	31
	1.00E+08	–2	8	18	28	38	43	48	46	41	36	31

DR (dB)		P_{in} (dBm)										
	64	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
B_v (Hz)	1.00E+02	41	51	61	71	81	84	79	74	69	64	59
	1.00E+03	31	41	51	61	71	76	79	74	69	64	59
	1.00E+04	21	31	41	51	61	66	71	74	69	64	59
	1.00E+05	11	21	31	41	51	56	61	66	69	64	59
	1.00E+06	1	11	21	31	41	46	51	56	61	64	59
	1.00E+07	–10	1	11	21	31	36	41	46	51	56	59
	1.00E+08	–20	–10	1	11	21	26	31	36	41	46	51

Figure 11. Instantaneous spur free dynamic range (DR) vs. RF input level (P_{in}) and processing bandwidth (B_v); high sensitivity (top) and bypass mode (bottom).

Figure 12 illustrates that, at low P_{in} levels, IIP2 is irrelevant as the sensitivity sets the dynamic range. The mid-range performance is most sensitive to IIP2. Mid-range input power levels might comprise most use cases, and as P_{in} increases toward the high sense to bypass switch point, amplifier linearity, especially IP2, is critically important. The superior IP2 of ADL8104 stands out over this important mid-range, preserving high dynamic range performance.

The bypass mode higher IIP2 allows the operating zone box to shift down to follow the best dynamic range.

DR (dB)		P_{in} (dBm)										
	61	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
IIP2 (FE, dBm)	20	21	31	41	51	56	51	46	41	36	31	26
	30	21	31	41	51	61	56	51	46	41	36	31
	40	21	31	41	51	61	59	54	49	44	39	34
	50	21	31	41	51	61	60	55	50	45	40	35
	60	21	31	41	51	61	60	55	50	45	40	35
	70	21	31	41	51	61	60	55	50	45	40	35
	80	21	31	41	51	61	60	55	50	45	40	35

DR (dB)		P_{in} (dBm)										
	64	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
IIP2 (FE, dBm)	20	4	14	24	34	44	49	50	45	40	35	30
	30	4	14	24	34	44	49	54	54	49	44	39
	40	4	14	24	34	44	49	54	59	57	52	47
	50	4	14	24	34	44	49	54	59	63	58	53
	60	4	14	24	34	44	49	54	59	64	62	57
	70	4	14	24	34	44	49	54	59	64	63	58
	80	4	14	24	34	44	49	54	59	64	64	59

Figure 12. Instantaneous spur free dynamic range (DR) vs. RF input level (P_{in}) and RF front-end input referenced IP2; high sensitivity (top) and bypass mode (bottom).

Figure 13 shows that for big improvements to NF, which can be very costly to SWaP-C and linearity, there is a diminishing return to dynamic range using a mid-range B_v. For lower NF to pay off, B_v needs to decrease with it and the associated trade-offs tolerated. The high sense mode does well with an NF in the 10 dB to 15 dB range. For the bypass mode, the high NF is shown to be a willing trade-off given the benefit to linearity. Ideally NF can be kept in the 20 dB to 25 dB range for the bypass mode. Better NF in bypass mode doesn't help dynamic range, as we are IMD limited.

DR (dB)		P_{in} (dBm)										
	61	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
NF (dB)	5	27	37	47	57	61	56	51	46	41	36	31
	10	25	35	45	55	61	56	51	46	41	36	31
	15	21	31	41	51	61	56	51	46	41	36	31
	20	17	27	37	47	57	56	51	46	41	36	31
	25	12	22	32	42	52	56	51	46	41	36	31
	30	7	17	27	37	47	52	51	46	41	36	31
	35	2	12	22	32	42	47	51	46	41	36	31

DR (dB)		P_{in} (dBm)										
	64	–80	–70	–60	–50	–40	–35	–30	–25	–20	–15	–10
NF (dB)	5	4	14	24	34	44	49	54	59	64	64	59
	10	4	14	24	34	44	49	54	59	64	64	59
	15	4	14	24	34	44	49	54	59	64	64	59
	20	4	14	24	34	44	49	54	59	64	64	59
	25	3	13	23	33	43	48	53	58	63	64	59
	30	2	12	22	32	42	47	52	57	62	64	59
	35	0	10	20	30	40	45	50	55	60	64	59

Figure 13. Instantaneous spur free dynamic range (DR) vs. RF input level (P_{in}) and RF front-end noise figure (NF); high sensitivity (top) and bypass mode (right).

Summary

Electronic warfare's imminent evolution toward multi-octave, multi-GHz instantaneous bandwidth RF tuners and wideband digital receivers introduce IMD2 effects that challenge dynamic range. Today's consideration of SFDR in terms of IMD3 will broaden to include IMD2, and the designer will use both the SFDR2 and SFDR3 equations. The system noise floor is dynamic because processing bandwidth changes on-the-fly based upon waveform detection and time requirements. When designing the optimal noise floor, decimation M and FFT depth N together define the FFT bin width, yet they each have separate important impacts to consider. Example pulse train FFTs of varying M and N are provided. As ADC performance improves, the front end continues to rely on high linearity wideband RF components with tunable attributes and frequency selectivity. The front end should be designed in cascade with the ADC's RF attributes.

MATLAB® Code

```
clear all; clc; %close all;
% sampling parameters
fs = 15.36e9; %sampling frequency
ts = 1/fs; % time step
N = 2^9; %FFT bins
m= 2^8; %decimation 1536 max
MN=N*m;
fs_dec=fs/m;
bin = fs_dec/N;
capture_time= N*m*ts; % radar waveform
tau = 100e-9; % pulse width
duty = 0.1;
PRI = tau/duty;
PRF = 1/PRI; % Hz
NSD=-148; %dBFs/Hz
floor=NSD+10*log10(2*fs_dec/N);
mainlobe=2/tau;
line_spacing= PRF;
num_cycles = N*m*ts/PRI;
t = 0:ts:(N*m*ts - ts);
d = tau:PRI:(PRI*(num_cycles));
y = pulstran(t,d,@rectpuls,tau); %pulse train
y=awgn(y, 50);
%plot pulse train in time domain
subplot(2,1,1)
plot(t/1e-6,y)
xlabel('Time (us)'); ylabel('Amplitude')
ylim([-0.5,1.5]);
%filter and decimate data stream
ydec=decimate(y,m);
%window
win = blackman(length(ydec)); % blackman window....
   use yup for zero pad
ywin=win'.*ydec;
% FFT
Y = abs(fft(ywin,N));
f = -fs_dec/2:fs_dec/N:(fs_dec/2-fs_dec/N);
%normalize and convert to dB
Y_db = mag2db(Y./max((Y)));
%plot FFT
subplot(2,1,2)
plot(f/1e6,fftshift(Y_db));
xlabel('Frequency (MHz)'); ylabel('Magnitude (dB)');
xlim([-4/tau/1e6 4/tau/1e6])
ylim([-150,0]);
```

References

[1] Peter Delos. "A Review of Wideband RF Receiver Architecture Options." Analog Devices, Inc., February 2017.

[2] Ahmed Ali, Huseyin Dinc, Paritosh Bhoraskar, Scott Bardsley, Chris Dillon, Mohit Kumar, Matthew McShea, Ryan Bunch, Joel Prabhakar, and Scott Puckett. "A 12b 18GS/s RF Sampling ADC with an Integrated Wideband Track-and-Hold Amplifier and Background Calibration." 2020 IEEE International Solid-State Circuits Conference, February 2020.

[3] AD9213 data sheet. Analog Devices, Inc., March 2020.

[4] AD9174 data sheet. Analog Devices, Inc., July 2019.

[5] William F. Egan. *Practical RF System Design*. John Wiley & Sons, April 2003.

[6] James Bao-Yen Tsui. *Microwave Receivers and Related Components*. Peninsula, 1983.

[7] Ian Beavers. "Noise Spectral Density: A New ADC Metric?" Analog Devices, Inc., December 2017.

[8] Travis F. Collins, Robin Getz, Di Pu, and Alexander M. Wyglinski. *Software-Defined Radio for Engineers*. Artech House, 2018.

[9] James Tsui and Chi-Hao Cheng. *Digital Techniques for Wideband Receivers*. SciTech, 2015.

[10] Duty Cycle. *Electronic Warfare and Radar Systems Engineering Handbook*. Naval Air Systems Command, April 1997.

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Gluing the concepts in this article together was a team effort and I got serious help from colleagues. Thanks to Nate Turner, Brad Hall, Wyatt Taylor, Frank Murden, Pete Delos, Ed Woertz, Robin Getz, and Travis Collins. Dr. James Tsui's *Digital Techniques for Wideband Receivers* inspired and informed a good portion of the content and I highly recommend the text to folks interested in getting into the details.

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It's Just a Triangle, or What Does a Symbol Really Mean?

Harry Holt, Staff Applications Engineer and
Mike Skroch, Applications Engineer

Does a symbol help or hinder our thinking about a design?

Symbols are important, but what if the symbol can mean several things?

This can lead to problems, as we shall see. In the analog world, a triangle can represent an op amp, a comparator, or an instrumentation amplifier. You could force one of them to do the function of one of the others, but system performance would not be optimum. Let's look at their differences and what to be cautious of so we can design around them if possible. As we shall see, there are some cases when you don't even want to try to design with the wrong type of part.

Looking at Figure 1, which triangle is the op amp? Which triangle is the comparator? And which triangle is the instrumentation amplifier? The answer is:

They all are!

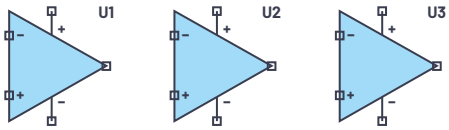

Figure 1. An op amp, an in-amp, and a comparator.

So, what's the difference and why do we care? Looking at Table 1, we can see that there are some big differences in several characteristics, but what do they mean at the circuit and system level?

Table 1. Comparisons of Op Amps, Comparators, and Instrumentation Amplifiers

	Op Amp	Comparator	In-Amp
Feedback	Negative	None/positive	Internal
Open-Loop Gain	5k to 10 million	3k to 50k	Fixed 0.2 to 10k
Closed-Loop Gain	Usually < 10,000		Fixed 0.2 to 10k
Input Caps	Never	Maybe	Good
Output	Analog/linear	Digital	Analog/linear
Important Specs	V_{OS}, GBW/PM	Prop delay	CMRR
Programming	R or C	None	R, SPI, jumpers

Let's see how you can get into trouble …

Feedback

An op amp has a huge gain. We were told in engineering school to start the analysis with the difference between the two inputs equal to zero. But in real life, this can't be true. If the open-loop gain is 1 million, then to get 5 V on the output, you would have to have 5 µV on the input. For a usable circuit, we need to apply feedback, so when the output tries to go too high, a control signal is fed back to the input, counteracting the original stimulus—for example, negative feedback. When used as a comparator, with no feedback, the output will slam against one rail or the other; with positive feedback, it will be driven farther in the same direction. So, op amps need negative feedback. In fact, when some op amps are used as comparators with no feedback, the supply current can be 5 to 10 times higher than the max on the data sheet.[1]

For a comparator, however, positive feedback is exactly what we need. With no feedback, if one input to a comparator slowly crosses the level of the other input, the output will slowly start to change. If there is noise in the system, such as ground bounce, the output may reverse, which is certainly undesirable in a control system. But then it starts changing back, resulting in oscillatory behavior, sometimes called chatter (see Figure 5 in MT-083[2]). The benefits of adding positive feedback, also called hysteresis, are well covered in the article "Curing Comparator Instability with Hysteresis" by Reza Moghimi.[3]

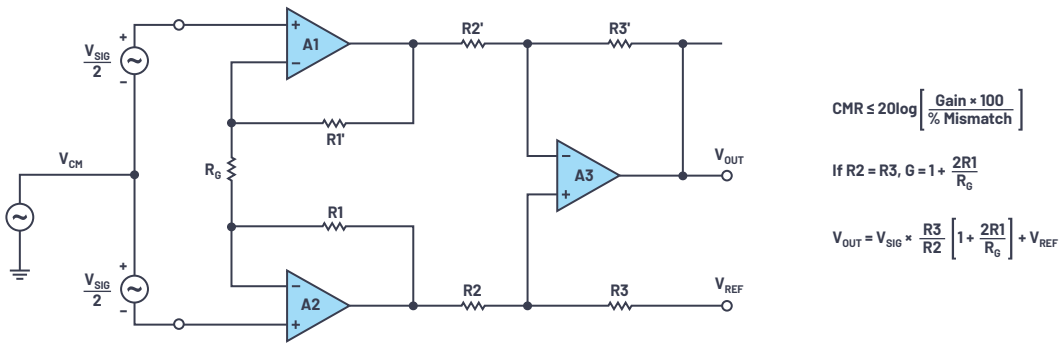

Figure 2. A classic 3-op-amp in-amp.

For an instrumentation amplifier, the feedback is already internal, so adding feedback just produces an inaccurate gain. A typical way to build an instrumentation amplifier with op amps is shown in Figure 2.

Note: there is feedback around each individual op amp. Let's begin by using the standard negative feedback diagram (see Figure 3) with the in-amp being G, with a desired gain of 10, implying a feedback factor of 0.1. Next, choose an in-amp fixed gain of 100. Using Equation 1, the actual closed-loop gain will be 9.09, almost a 10% error. So, using an in-amp triangle as an op amp and putting feedback around it doesn't make sense.

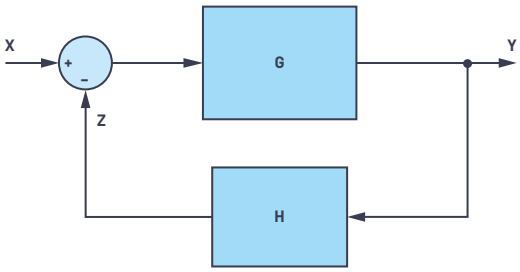

Figure 3. Classic feedback schematic.

$$A_{CL} = \frac{1}{\beta} \times \frac{1}{1 + 1/A_{VOL} \times \beta} \quad (1)$$

For an op amp, we really need negative feedback; for a comparator, we really need positive feedback; and for an in-amp, we don't need any feedback.

Open-Loop and Closed-Loop Gain

For op amps, looking at Equation 1, the higher the open-loop gain (A_{VOL}), the more accurate the closed-loop gain will be. Most op amps have open-loop gain between 100,000 and 10 million, but some of the older high speed op amps might be as low as 3000. As shown earlier, the higher the open-loop gain, the lower the closed-loop gain error.

For a comparator, if the logic swing on the output is 3 V, and you want a 1 mV threshold, then the minimum gain needs to be 3000. Higher gain will give you a smaller window of uncertainty, but if the gain is too high, microvolts of noise will trigger the comparator.

For an instrumentation amplifier, the concept of open-loop gain doesn't really apply.

Input Capacitors

Capacitors are often added to circuits to limit the bandwidth. Looking at Figure 4, at first glance it seems that R1 and C1 form a low-pass filter. This does not work and can lead to oscillations. The feedback factor for an inverting amplifier is R2/R1, but in Figure 4, the feedback factor is R2/(R1 + Xc). As the frequency increases, the feedback factor increases, so the noise gain is going up at +20 dB/decade, while the op amp open-loop gain is going down at –20 dB/decade. They cross at 40 dB, which, according to control system theory, guarantees oscillation. The correct way to restrict the bandwidth of the circuit is to put the capacitor across R2.

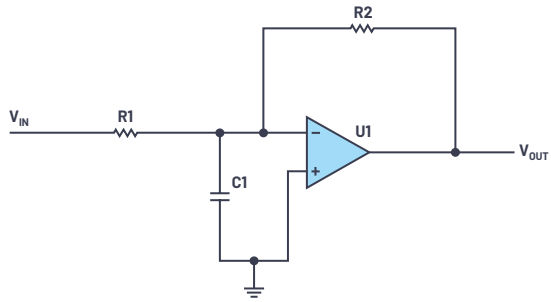

Figure 4. An attempt to reduce op amp bandwidth.

Comparators usually don't have a negative feedback network, so the simple R and C in front of the comparator in Figure 5 forming a low-pass filter works well. R_{HYS} should be much larger than R7, and the two divide the output swing to provide a small amount of positive feedback (hysteresis). If the comparator has built-in hysteresis, such as the LTC6752 or the ADCMP391, then R7 and R_{HYS} are not used.

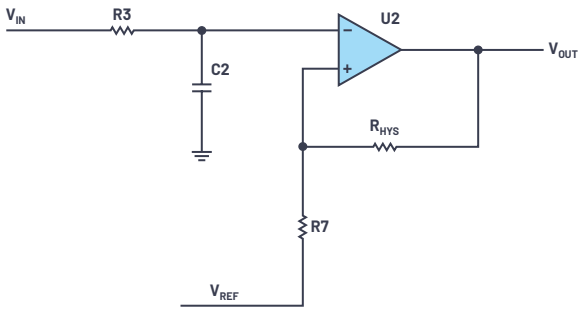

Figure 5. Comparator with LPF and hysteresis.

For instrumentation amplifiers, a cap across the inputs is quite acceptable as shown by C4 in Figure 6. The figure in Chapter 5 of the Analog Devices instrumentation guide[4] shows a good thing to do every time you use an instrumentation amplifier. If you lay out the printed circuit board with the appropriate traces and pads to allow adding the two resistors and three capacitors, you can start with 0 Ω resistors and no capacitors, and measure the system performance. By adjusting the values of the five components, you can set the common-mode roll-off and the normal-mode roll-off independently (see the guide for details).

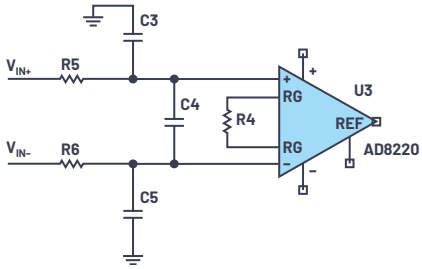

Figure 6. RFI filter before instrumentation amplifier.

Outputs

An op amp or an instrumentation amplifier will have an output that swings from close to one rail and to the other. Depending on whether the output stage uses common emitter or common source configurations, it may get within 25 mV to 200 mV of either rail. This would be considered a rail-to-rail output. If the op amp is powered by +15 V and –15 V, this is inconvenient to interface to digital circuitry. One poor solution that has been tried is to put diode clamps on the output to protect the digital input from damage. Instead, the op amp current goes sky high and the op amp gets damaged. There are more elaborate ways to interface an op amp to digital logic, but why bother? Just use a comparator.

Comparators can have a CMOS totem-pole output, or an NPN or NMOS open-collector or open-drain output. Although the open-collector or open-drain output requires a pull-up resistor, resulting in unequal rise and fall times, it does offer the advantage of operating the comparator on one voltage, say 5 V, and interfacing to logic operating on a different voltage, such as 3.3 V.

Important Specs

For an op amp, we need a gain bandwidth higher than the highest signal frequency to keep the closed-loop error low. Looking at Equation 1, we can see where the rule of gain bandwidth should be 10 to 100 times the highest signal frequency. From Equation 1, as discussed earlier, note that A_{VOL} is a function of frequency and will affect the closed-loop accuracy. Phase margin is also important and will vary with capacitive load, so the spec table should clearly state the test conditions. For dc accuracy, the offset voltage should be low. For a trimmed bipolar op amp, 25 µV to 100 µV is good; for a FET input op amp, 200 µV to 500 µV is good. Auto-zero/chopper/zero-drift op amps are almost always below 20 µV maximum, and this is over temperature. For examples, see some typical op amp data sheets, such as the OP27, AD8610, or ADA4522.

Propagation delay is the key specification for comparators. Contrary to op amps that get slower when overdriven, comparators will get faster when you overdrive them. Spec tables will sometimes have a propagation delay with a small amount of overdrive, say 5 mV, and a different delay with a larger overdrive of 50 mV or even 100 mV.

The number one spec for instrumentation amplifiers is the common-mode rejection ratio (CMRR). You are trying to extract a very small differential signal riding on top of a large common-mode voltage. Like many specs, this varies with frequency and sometimes a dc CMRR or a CMRR at a very low frequency is listed. A graph of CMRR vs. frequency is usually provided. This would be important, for example, if you were trying to sense current in an H-bridge motor drive as shown in Figure 7.

This is probably the most difficult application for an instrumentation amplifier, because the common-mode voltage goes from near one rail to close to the other, and the current reverses quickly. Gain bandwidth and slew rate are both important.

Programming

Programming in this sense doesn't mean writing code; it means configuring the part to meet the requirements of your system (although some in-amps do have traditional software programming features with SPI ports and registers).

For op amps, we configure the part with negative feedback. This can be a purely resistive element, but usually a resistor is used with a capacitor in parallel to

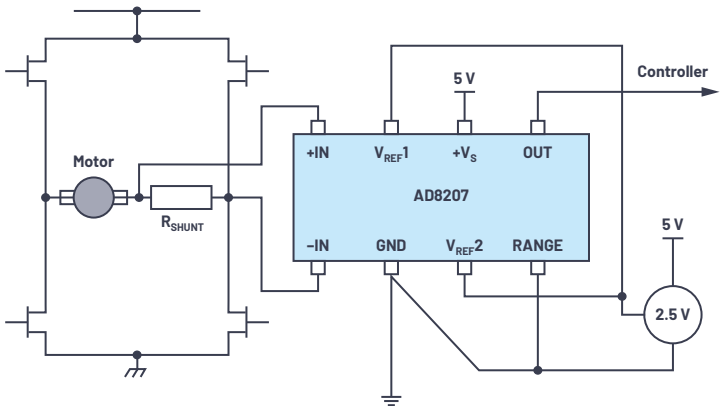

Figure 7. Bidirectional current sensing with high common-mode swing.

restrict the bandwidth. This helps the signal-to-noise ratio because noise will be integrated across the entire range, even if we are only using a part of it. You can also use capacitors by themselves and get an integrator or a differentiator.

Comparators should always have a bit of positive feedback to ensure that once the input forces the output to move, the output reinforces the move (see Figure 4 and Figure 5). Pictures and calculations are included in MT-083. Some comparators do have internal hysteresis, but you can usually add more if desired. Some comparators with internal hysteresis have a pin to add a resistor to slightly change the amount.

It is possible to use an op amp as a comparator, but it's not ideal, and there are several considerations. You must be a good analoger to get away with it in a production environment. Some considerations are in MT-083 and many articles, pro and con, have been written. See the references if you like to live dangerously.

Comparators are almost always programmed with resistors. You can add a high value resistor to give a little bit of positive feedback, and it is also possible to use a capacitor for ac feedback to avoid adding dc hysteresis. Some comparators have built-in hysteresis, but this can be increased, again, by adding a small amount of positive feedback.

Final Considerations

Subtle things happen when trying to use an op amp as a comparator. Quite a few of the low noise bipolar op amps have anti-parallel diodes between the inputs. The input common-mode range for most comparators encompasses 80% of the total range or more. But some low noise, bipolar op amps have one or two diodes in series between the inputs. This is to keep the input stage from Zenering one of the emitter base junctions, which would degrade the noise performance over time.

So a 5 V op amp used as a comparator with a threshold level of 3 V for a power-good indicator in a 3.3 V system would have a problem with 3 V on one input and 0 V on the other, as these diodes limit the maximum differential voltage allowed across the op amp inputs.

Summary

For many applications, the choice of op amp will depend on whether you are focused on dc accuracy, ac accuracy, input offset voltage, gain bandwidth, or supply voltage. In 2020, you have over 700 to choose from. The key parameters for comparators are usually propagation delay and supply voltage. The choice is a little easier, with 122 parts to choose from. The main criterion for instrumentation amplifiers is CMRR as a function of frequency, but near dc, offset voltage, and gain accuracy are also important. Because in-amps are a more specialized part, there are "only" 63 choices.

Choosing the right part will result in a trouble-free, production-worthy design for years to come.

References

[1] Harry Holt. "The Maximum Supply Current that Wasn't." Analog Devices, Inc. November 2011.

[2] MT-083 Tutorial: "Comparators." Analog Devices, Inc. 2009.

[3] Reza Moghimi. "Curing Comparator Instability with Hysteresis." *Analog Dialogue*, Vol. 34, No. 7, November 2000.

[4] A Designer's Guide to Instrumentation Amplifiers, 3rd edition. Analog Devices, Inc. 2006.

About the Author

Harry Holt was a staff applications engineer at Analog Devices (San Jose, CA) for 14 years, finishing up in the Central Applications Group, following 27 years in both field and factory applications at National Semiconductor for a variety of products, including data converters, op amps, references, audio codecs, and FPGAs. He has a B.S.E.E. degree from San Jose State University and is a life member of Tau Beta Pi and a life senior member of the IEEE. Harry retired in August 2017.

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A Practical Method for Separating Common-Mode and Differential-Mode Emissions in Conducted Emissions Testing

Ling Jiang, Applications Engineer, **Frank Wang**, EMI Engineer,
Keith Szolusha, Applications Director, and **Kurk Mathews**, Senior Applications Manager

EMI from switching regulators is broken down into radiated and conducted emissions (CE). This article focuses on conducted emissions, which can be further classified into two categories: common-mode (CM) noise and differential-mode (DM) noise. Why the CM-DM distinction? EMI mitigation techniques that are effective for CM noise are not necessarily effective for DM noise, and vice versa, so identifying the source of conducted emissions can save time and money in suppressing it. This article presents a practical method of separating CM emissions and DM emissions from the total conducted emissions for an LTC7818 controlled switching regulator. Knowing where the CM noise and DM noise appear in the CE spectrum enables power supply designers to effectively apply EMI suppression techniques, which saves design time and BOM costs in the long run.

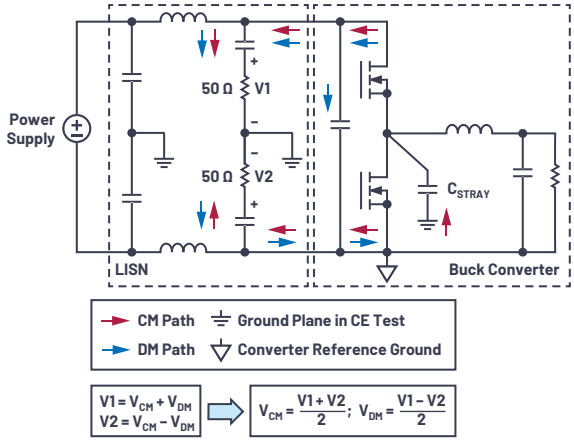


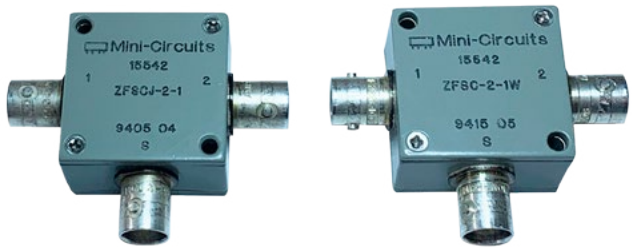
Figure 1. The CM noise path and DM noise path in a buck converter.

Figure 1 shows the CM noise and DM noise paths for a typical buck converter. DM noise is produced between the supply line and the return line, while CM noise is produced between the supply lines and the ground plane (such as a copper test table) via stray capacitance, C_{STRAY}. The LISN for CE measurement is placed between the power supply and buck converter. The LISN itself cannot be used for direct measurement of CM and DM noise, but it does measure supply and return supply line noise—V1 and V2 in Figure 1, respectively. These voltages are measured across 50 Ω resistors. From the definition of CM and DM noise, shown in Figure 1, V1 and V2 can be expressed by the sum and difference of the CM voltage (V_{CM}) and DM voltage (V_{DM}), respectively. This allows us to calculate V_{CM} from the average of V1 and V2, and V_{DM} as half of the difference between V1 and V2.

Measuring CM Noise and DM Noise

A T type power combiner is a passive device that combines two input signals to a single port output. A 0° combiner produces a vector sum of the input signals at the output port and a 180° combiner produces a vector difference of input signals.[1] Therefore, a 0° combiner can be used to produce V_{CM} and a 180° combiner to produce V_{DM}.

The two combiners shown in Figure 2, ZFSC-2-1W+ (0°) and ZFSCJ-2-1+ (180°) from Mini-Circuits, were used to measure V_{CM} and V_{DM} from 1 MHz to 108 MHz. For these devices, measurement error increases for frequencies below 1 MHz. For lower frequency measurements, use different combiners, such as ZMSC-2-1+ (0°) and ZMSCJ-2-2 (180°).



180° Combiner 0° Combiner

Figure 2. 0° and 180° combiners.

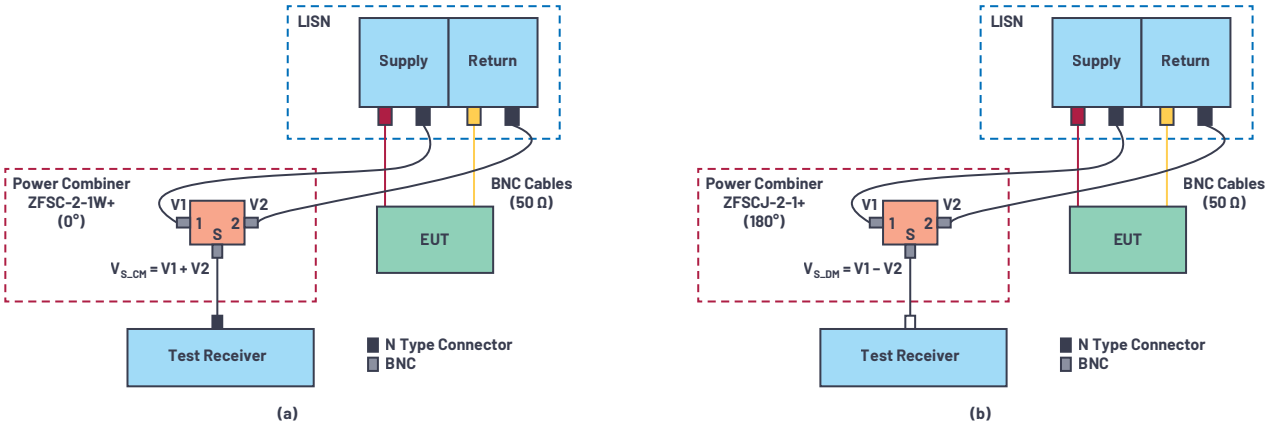


Figure 3. Experimental setup for measuring (a) V_{CM} and (b) V_{DM}.

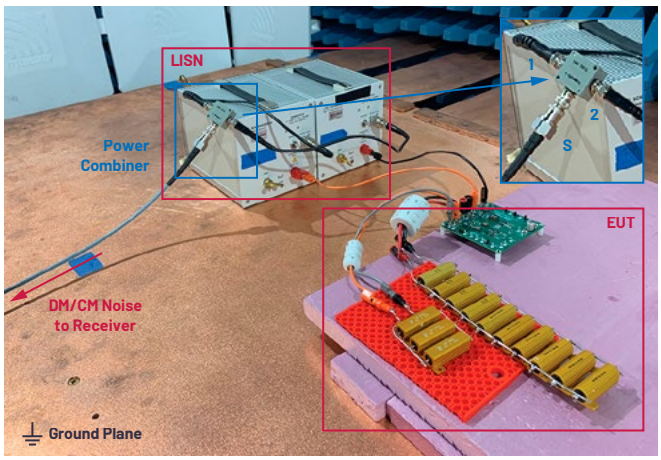


Figure 4. Test setup for measuring CM noise and DM noise.

The diagram of the test setup is shown in Figure 3. The power combiner is added to the standard CE test setup. The outputs of the LISN for the supply line and return line are connected to Input Port 1 and Input Port 2 of the combiner, respectively. For the 0° combiner, the output voltage is V_{S_CM} = V1 + V2; for the 180° combiner, the output voltage is V_{S_DM} = V1 – V2.

The output signals of combiners V_{S_CM} and V_{S_DM} must be processed in the test receiver to produce V_{CM} and V_{DM}. First, the power combiners have specified insertion losses compensated in the receiver. Second, since V_{CM} = 0.5 V_{S_CM} and V_{DM} = 0.5 V_{S_DM}, the test receiver subtracts an additional 6 dBµV from the received signal. After compensating for these two factors, the measured CM noise and DM noise are read in the test receiver.

Experimental Verification of CM Noise and DM Noise Measuring

A standard demo board with dual buck converters is used to verify this method. The switching frequency of the demo board is 2.2 MHz, while V_{IN} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 10 A, V_{OUT2} = 5 V, and I_{OUT2} = 10 A. Figure 4 shows the test setup in the EMI chamber.

Figure 5 and Figure 6 illustrate the test results. In Figure 5, the higher EMI curve shows the total voltage method CE measured with the standard CISPR 25 setup, while the lower emissions curve shows the separated CM noise measured by adding the 0° combiner. In Figure 6, the higher emissions curve shows the total CE, while the lower EMI curve shows the separated DM noise measured by adding the 180° combiner. These test results comply with theoretical analysis, suggesting that DM noise dominates the noise at a lower frequency range, while CM noise dominates at the higher frequency range.

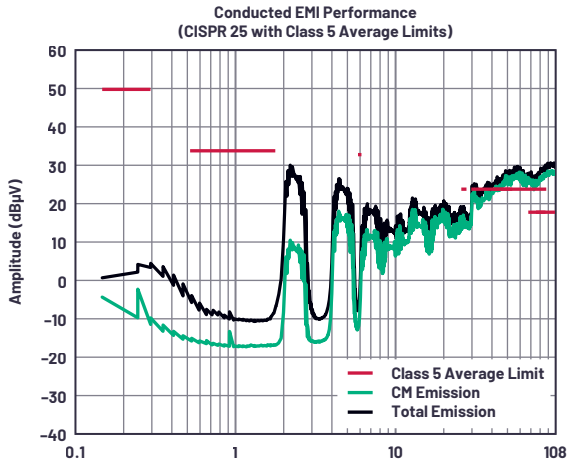


Figure 5. Measured CM noise vs. total noise.

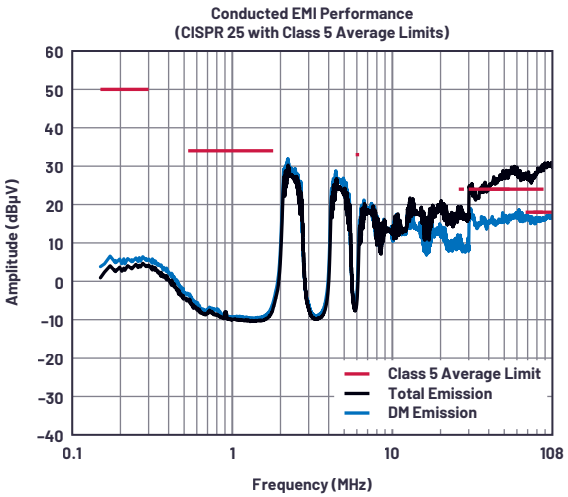


Figure 6. Measured DM noise vs. total noise.

Adjusted Demo Board Passes CISPR 25 Class 5

According to the measured results, the total noise emission exceeds the limit of CISPR 25 Class 5 at the range of 30 MHz to 108 MHz. By separating the CM and DM noise measurements, it appears that the high conducted emissions at this range are caused by CM noise. It makes little sense to add or enhance the DM EMI filter or otherwise reduce the input ripple, as these mitigation techniques would not reduce the problematic CM noise at this range.

Therefore, methods specifically addressing CM noise are implemented on this demo board. One source of CM noise is high dV/dt signals in the switching circuit. Reducing dV/dt by increasing the gate resistance can decrease the noise level. As previously mentioned, CM noise passes through the LISN via the stray capacitance C_{STRAY}. The smaller the C_{STRAY}, the lower the CM noise detected in LISN. To reduce C_{STRAY}, the copper area of the switch node cuts down on this demo board. Furthermore, a CM EMI filter is added at the input of the converter to obtain high CM impedance, therefore reducing the CM noise into the LISN. By implementing these methods, the noise at 30 MHz to 108 MHz is reduced enough for compliance with CISPR 25 Class 5, as shown in Figure 7.

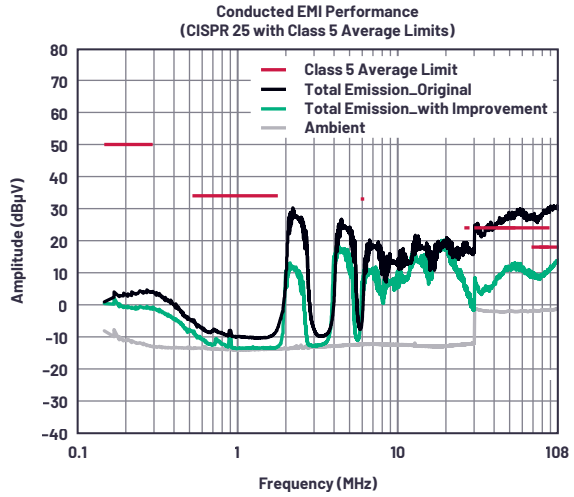


Figure 7. Total noise with improvement.

Conclusion

A practical method for measuring and separating CM noise and DM noise from total conducted emissions is presented in this article and verified with test results. If a designer can separate CM and DM noise, specific CM- or DM-targeted mitigation solutions can be implemented to suppress the noises effectively. Overall, this method helps quickly find the root cause of EMI failure, saving time in EMI design.

References

"AN-10-006: Understanding Power Splitters." Mini-Circuits, April 2015.

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Ling Jiang received a Ph.D. degree in electrical engineering from the University of Tennessee at Knoxville in 2018. After graduating, she joined the Power Products Group at Analog Devices in Santa Clara, California. Ling is an applications engineer supporting controllers and µModule devices for automotive, data center, industrial, and other applications. She can be reached at ling.jiang@analog.com.

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Kurk Mathews is a senior applications manager for the Power Products Group at Analog Devices in California. Kurk joined Linear Technology, now part of Analog Devices, as an applications engineer in 1994, supporting isolated converters and high power products. His group supports power applications and the development of new controllers, monolithic converters, and gate drivers. He enjoys analog circuit design and troubleshooting using a variety of new and old test equipment. Kurk graduated from the University of Arizona with a B.S. in electrical engineering. He can be reached at kurk.mathews@analog.com.

RAQ Issue 185: The Perilous Path from the Transducer to the ADC: What's an Engineer to Do?

Hooman Hashemi, Product Applications Engineer

Question:

Is there a building block that allows me to take a tiny transducer output signal directly to an ADC input voltage?

Answer:

Yes, the latest family of ADI instrumentation amplifiers can reject the CM, gain-up the differential signal, translate the voltage to the ADC input voltage requirements, and protect the ADC against overvoltage in one fell swoop!

One of the most ubiquitous challenges in countless industrial, automotive, instrumentation, and numerous other applications is how to properly connect a minuscule transducer signal to an ADC for digitization and data acquisition. The transducer signal is usually weak, fragile, could be noisy, may look like a very high impedance source, and could ride atop a huge common-mode (CM) voltage. None of these are conducive to what an ADC input likes to see. In this article, I will introduce recent integrated solutions that might once and for all answer the poor engineer's plea for help beyond what is currently available. I will also go through the detailed design steps to configure a complete transducer interfaced instrumentation amplifier (in-amp) driving an ADC input.

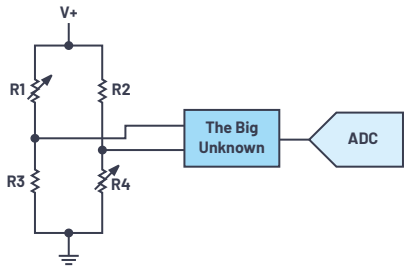

Figure 1. The challenge of getting from the transducer to the ADC.

What Suits the Transducer and Why Is There an Issue?

The short answer to this question is an instrumentation amplifier. That's what a transducer prefers to look into: an in-amp.

In-amps potentially have the precision (low offset) and the low noise to not corrupt the small input signal. They have differential inputs suitable for many transducer signals such as strain gauges, pressure sensors, etc. and will be able to reject any CM present, leaving only the pristine small voltage we are interested in and no unwanted CM. In-amps have a huge input impedance that will not load the transducer, ensuring that the fragile signal is not affected by signal processing. Furthermore, in-amps allow large gains and a large selectable gain range, usually with a single external resistor, for maximum flexibility to adapt the small signal of interest to voltages far above the signal path noise level and fit for ADC analog inputs. Because in-amps are designed for precision, they are internally trimmed and maintain their performance over a wide operating temperature and are immune to variations in supply voltages as well. They also maintain their accuracy by having very low gain error, which limits the measurement or signal error as the swing varies.

What Would the ADC Input Like to See?

An ADC input is not the easiest load to drive. There is charge injection from the internal capacitor, C_{DAC} in Figure 2, switching action at the front end that makes it a challenging task to deliver a highly linear and settled signal for quantization by the ADC. What drives the ADC input must be able to handle these large charge injections and settle quickly before the next conversion cycle. Furthermore, the driver noise and distortion should not be a limiting factor depending on the ADC resolution (number of bits).

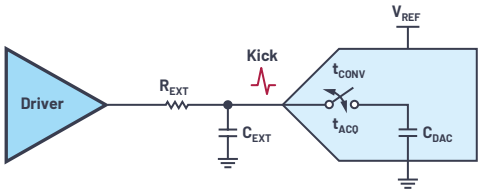

Figure 2. ADC input driving is challenging.

Taken together, these requirements are not trivial tasks, especially with a low power consumption driver. Furthermore, ADC operating supply voltages are shrinking day-by-day as part of the modernization of semiconductor processes. As an unwanted side effect of such a trend, ADC inputs tend to be more susceptible to input overvoltage stress and possible harm or damage. This necessitates that there is external circuitry that protects against such overvoltage. Any such external circuitry should not limit the bandwidth or cause any sort of distortion in addition to not add any measurable noise to the signal. It is also highly desirable that the overall circuit reacts fast and recovers gracefully and quickly from an overvoltage event.

There is also the challenge of shifting the input signal to conform with the ADC analog input voltage range. Any circuit elements added to perform this task is subject to all the constraints listed earlier (that is, low distortion, low noise, sufficient bandwidth, etc.).

The Issue: If Only the In-Amp Could Directly Drive the ADC!

With all that in-amps bring to the table, they have some shortcomings that necessitate more circuit elements to complete the path from the physical world (transducer) to the digital world (ADC). Traditionally, an in-amp would not be the first-choice circuit element chosen to drive the finicky input of an ADC (some ADCs are more finicky than others). There is so much that an in-amp already does that it'd seem unfair to desire that it even do more!

Overcoming the harmonic distortion (HD) of an ADC driver is a difficult challenge. Here is the expression for what kind of distortion an ADC driver would have to meet or exceed as a function of the ADC resolution:

$$SINAD = 6.02 \times ENOB + 1.76 \text{ dB} \quad (1)$$

SINAD: SNR + distortion

ENOB: Effective number of bits

So, for an ENOB of 16 bits, SINAD ≥ 98 dB

The in-amps currently available on the market are usually not meant to drive an ADC input. The most common reason for this is that these devices lack the linearity that a high resolution ADC necessitates. Linearity, or harmonic distortion (also called THD, the total harmonic distortion), is the most likely limiting factor that would prevent an in-amp from being able to drive an ADC directly. When a complex waveform is digitized, once contaminated with distortion terms, the signal becomes indistinguishable from any such contamination and thus the data acquisition is compromised! The driver should also be able to settle quickly from the ADC input charge injection transient explained earlier.

Current Solutions Improved

With the new instrumentation amplifier family, we now have a device family that does all that an in-amp has traditionally done plus it can now drive an ADC directly very well and protect the ADC input as well! The LT6372-1 (for gains from 0 dB to 60 dB) and the LT6372-0.2 (for gains/attenuation from –14 dB to +46 dB) can help fulfill the task of a precision transducer interface that can directly drive an ADC input.

There are obvious advantages to using a high precision, low noise instrumentation amplifier such as the LT6372 family to drive an ADC analog input directly without the need to add another amplification or buffering stage. Some of these benefits are reduced component count, power consumption, cost, and board area, as well as high CMR, excellent dc precision, low 1/f noise, and single component gain selection.

Many high speed op amps selected as ADC drivers may not have the low 1/f noise that the LT6372 family has due to the proprietary process it is built on. Furthermore, additional buffering and gain stages may have to be added to amplify the small transducer signal. With direct in-amp ADC driving, there are no additional noise sources or dc offset terms from amplifier stages or voltage references to contend with either.

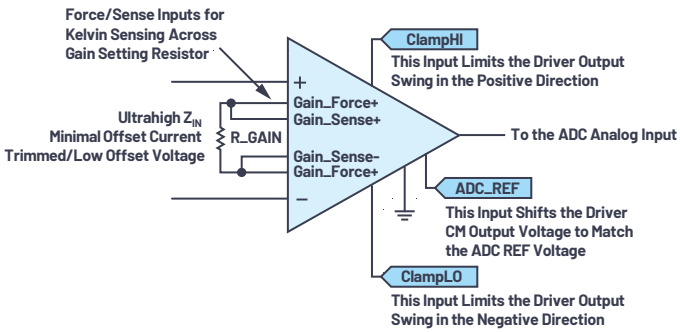

Figure 3. An ideal transducer amplifier/ADC driver visualized.

The LT6372-1 and LT6372-0.2, with their extremely high input impedance, can interface a transducer or similar signal input and provide large gain (LT6372-1) or attenuation (LT6372-0.2) without causing loading, while their low distortion and low noise assure accurate conversion without degradation for 16-bit and lower resolution ADCs at up to 150 kSPS. Figure 4 shows the bandwidth that each device can achieve for a given gain setting.

Refer to Figure 5 for the LT6372-1 distortion vs. frequency to make sure the distortion terms do not significantly dominate the THD performance of the ADC being considered at the highest frequency of interest. For an example of an ADC, LTC2367-16 has a SINAD specification of 94.7 dB. To make sure the driver is not dominant, Figure 5 shows that LT6372-1 would be a suitable choice for frequencies less than ~5 kHz.

The Nitty Gritty of Using LT6372-1 as an ADC Driver

In addition to the advantages previously noted, the split-reference architecture of the LT6372 family (shown in Figure 6 as separate RF1 and RF2 pins) allows an elegant way to shift the signal to within the ADC FS voltage range directly and efficiently, without having to use additional voltage references and other external circuitry to achieve the same, thereby reducing cost and complexity. For most ADCs, REF2 (shown tied to the V_{OCM} dc voltage here) would be tied to the ADC V_{REF} voltage, which would ensure the ADC analog input mid-level to be $V_{REF}/2$.

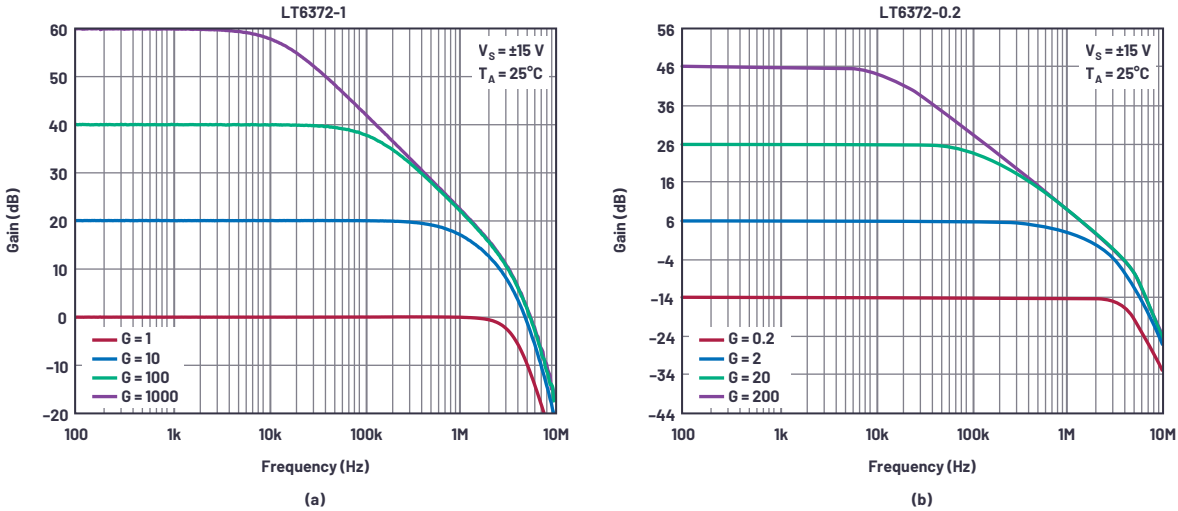

Figure 4. LT6372-1 and LT6372-0.2 frequency response at various gains.

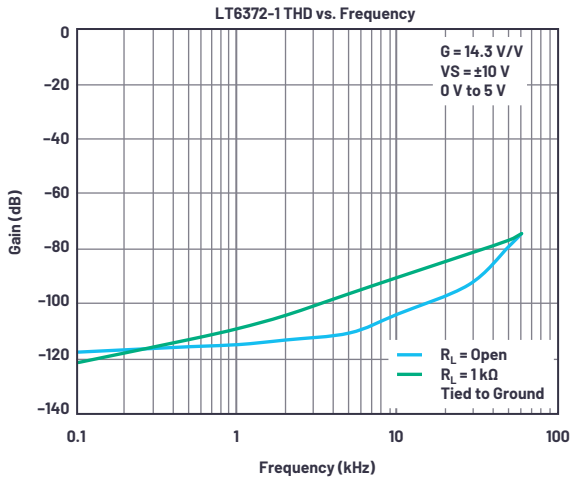

Figure 5. LT6372-1 THD vs. frequency.

The LT6372 family built-in output clamps (CLHI and CLLO) ensure that the sensitive input of the ADC is not violated or possibly harmed from transients in either the positive or negative direction. They allow undistorted output swing right up to the clamp voltage with fast response and recovery to provide ADC protection and quick return to normal operation after a possible transient that could trigger either clamp.

The analog input of some SAR ADCs presents a challenging load for an amplifier to drive. The amplifier needs to be low noise and fast settling, as well as possess high dc precision to keep unwanted signal perturbations to one LSB or less. Higher sampling rates and higher order ADCs place more demand on the amplifier. Figure 7 shows the input of a typical SAR ADC.

The switch positions shown in Figure 7 correspond to the sampling or acquisition mode where the analog input is connected to the sampling cap C_{DAC} before conversion begins on the next phase of operation.

Prior to the start of this phase, switch S2 has discharged C_{DAC} voltage to 0 V or other bias point such as $f_s/2$. At the start of the sampling period when S1 closes and S2 opens, the difference in voltage between VSH and the analog input causes transient current to flow so that C_{DAC} can charge toward analog input voltage. This current can be as large as 50 mA for higher sampling rate ADCs. Capacitor C_{EXT} helps to mitigate the step change in the amplifier output voltage because of this current step, but the amplifier is still subjected to its disturbance and needs to settle in time before the end of the acquisition period. Resistor R_{EXT} isolates the driver from C_{EXT} and also reduces the impact on stability when driving a heavy capacitor. The choice of values for R_{EXT} and C_{EXT} is a trade-off between more isolation from this current injection and degradation of settling time due to the low-pass filter formed this way. This filter can also help reduce the out-of-band noise and to improve SNR, although that is not its main function.

ADC Front-End RC Component Value Design

Many considerations go into the choice of values for R_{EXT} and C_{EXT}. Here is a summary of factors that affect the ADC dynamic response as measured by FFT or other means:

- C_{EXT}: Acts as a charge bucket from the input charge kickback that occurs to minimize the voltage step and thus improve settling time.
  - Too large: It may affect amplifier stability and could lower the LPF roll-off frequency too low to pass the signal.
  - Too small: The charge kickback from the ADC input becomes too large to settle in time.
- R_{EXT}: Provides isolation between the amplifier output and C_{EXT} to ensure stability.
  - Too large: It may make the settling time constant too long. May also cause a THD increase when looking into the ADC input nonlinear impedance.[1] Can increase IR drop error.
  - Too small: Amplifier may become unstable or its forward path settling may be compromised due to C_{EXT}.

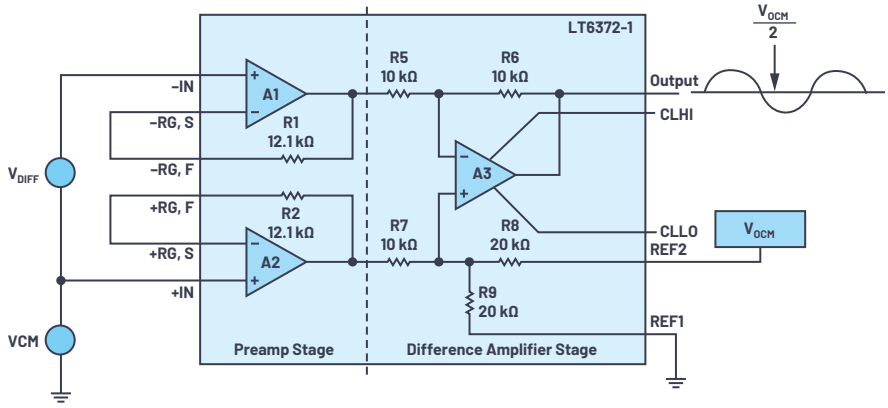

Figure 6. LT6372 split-reference used to shift signal to an ADC analog input.

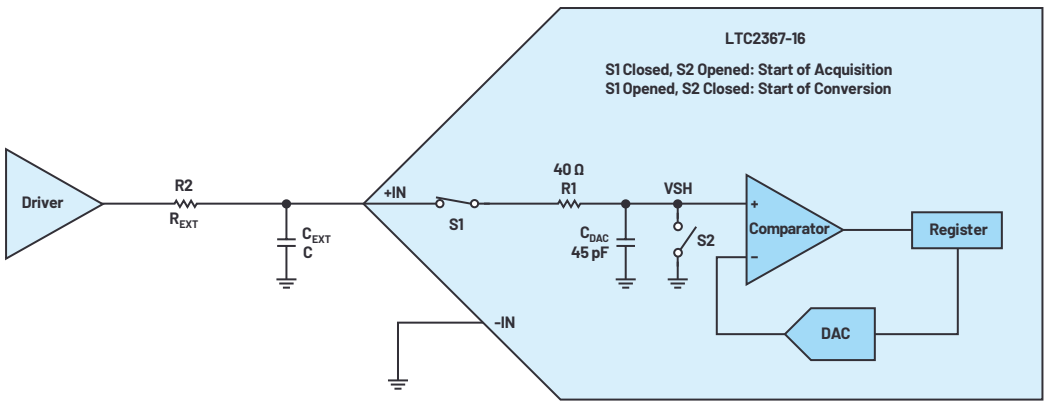

Figure 7. SAR ADC input in acquisition/sampling mode.

Here are a few design steps to design the R_{EXT} and C_{EXT} values using an LT2367-16 ADC, as an example, driven by an LT6372-1 with a 2 kHz max input frequency, f_{IN}, at a sampling rate of 150 kSPS (see Reference 1 for a full derivation of some of the following formulas):

Choose a C_{EXT} large enough to act as a charge bucket to minimize the charge kickback:

$$C_{EXT} > 100 \times C_{DAC} \quad (2)$$

Where:

C_{DAC}: ADC input capacitance = 45 pF (LTC2367-16)

→ C_{EXT} = 10 nF (selected)

Compute the ADC input voltage step V_{STEP} using:

$$V_{STEP} = \frac{V_{REF} \times C_{DAC}}{C_{EXT} + C_{DAC}} \quad (3)$$

Where:

V_{REF} = 5 V (LTC2367-16)

C_{DAC}: ADC input cap = 45 pF (LTC2367-16)

C_{EXT} = 10 nF (from earlier)

→ V_{STEP} = 22 mV (calculated)

Note: This V_{STEP} function assumes that C_{DAC} is discharged to ground at the end of each sample period, as is the case with LTC2367-16. The V_{STEP} formula in Reference 1 has a different assumption in that it is for ADC architectures where C_{DAC} voltage is maintained from sample to sample.

Compute how many input $R_{EXT} \times C_{EXT}$ time constants, N_{TC}, are required to settle, assuming exponential settling of the step input:

$$N_{TC} = \mathrm{LN}\left(\frac{V_{STEP}}{V_{half\ lsb}}\right) \quad (4)$$

Where:

V_{STEP}: ADC input voltage step calculated earlier

V_{HALF_LSB}: LSB/2 size in volts. With 5 V FS and 16 bits, that's 38 µV (= 5 V/2^{17})

→ N_{TC} = 6.4 time constants

Calculate the time constant, τ:

$$\tau \leq \frac{t_{ACQ}}{N_{TC}} \quad (5)$$

Where:

t_{ACQ}: ADC acquisition time; $t_{ACQ} = t_{CYC} - t_{HOLD}$

Assume sampling rate of 150 kSPS:

t_{CYC} = 6.67 µs (= 1/150 kHz)

t_{HOLD} = 0.54 µs (LTC2367-16)

thus: t_{ACQ} = 6.13 µs

→ τ ≤ 0.96 µs

With τ and C_{EXT} known, R_{EXT} can be computed:

$$R_{EXT} \leq \tau / C_{EXT} \quad (6)$$

→ R_{EXT} ≤ 96 Ω

We now have the external RC values that allow proper settling for the chosen ADC. If the computed R_{EXT} is too high, C_{EXT} can be increased and R_{EXT} recalculated to reduce its value, and vice versa. Figure 8 shows the value of R_{EXT} for a chosen value for C_{EXT} to simplify this task when operating under the conditions of this example.

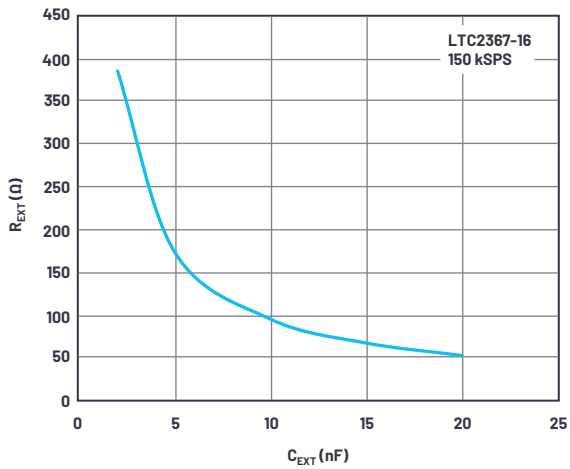

Figure 8. ADC external input RC relationship for proper settling.

Use the previous steps to find suitable R_{EXT} and C_{EXT} starting values. Bench testing and evaluation should be performed and these values optimized as needed while keeping in mind the impact of such changes on performance.

Summary

A new family of instrumentation amplifiers was introduced to help bridge the gap between a transducer and data acquisition. The features of these devices were explored in detail along with a real-world example of how to design the ADC front-end components to ensure that the driver plus ADC combination can deliver the resolution intended.

References

[1] Alan Walsh. "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter." *Analog Dialogue*, December 2012.

About the Author

Hooman Hashemi joined Analog Devices in March 2018, where he works on characterizing new products and developing applications that showcase the products' features and uses. Hooman previously worked for Texas Instruments for 22 years as an applications engineer, concentrating on the high speed portfolio. He graduated from University of Santa Clara with an M.S.E.E. in August 1989 and San Jose State University with a B.S.E.E. in December 1983. He can be reached at hooman.hashemi@analog.com.

DC Energy Metering Applications

Luca Martini, System Engineer

Why Is DC Energy Metering Important?

In the 21st century, world governments are working on action plans to tackle complex and long-term challenges in reducing CO_2 emissions. CO_2 emissions have been proven responsible for the devastating effects of climate change, and the needs of new efficient energy conversion technology and improved battery chemistry are rapidly growing.

Including both renewable and non-renewable energy sources, the world population consumed nearly 18 trillion kWh last year alone and demand keeps growing; in fact more than half of the energy ever generated has been consumed in the last 15 years.

Our electrical grids and power generators are constantly expanding; the need for more efficient and environmentally friendly power has never been greater. Because it was easier to use, early grid developers worked with alternating current (ac) to feed power to the world, but in many areas, direct current (dc) can dramatically improve efficiency.

Driven by the development of efficient and economic power conversion technology based on wide band gap semiconductors, such as GaN and SiC devices, many applications now see benefits in switching to dc energy exchange. As a consequence of that, precision dc energy metering is becoming relevant, especially where energy billing is involved. In this article, opportunities for dc metering in electric vehicle charging stations, renewable energy generation, server farms, microgrids, and peer-to-peer energy sharing will be discussed, and a dc energy meter design will be proposed.

DC Energy Metering Applications

DC Electric Vehicle Charging Stations

The growth rate of plug-in electric vehicles (EVs) is estimated at +70% CAGR as of 2018[1] and projected to grow +25% CAGR year by year from 2017 to 2024.[2] The charging station market will follow at 41.8% CAGR from 2018 to 2023.[3] However, to accelerate the reduction of the CO_2 footprint caused by private transportation, EVs need to become the first choice for the automotive market.

In recent years great effort went into improving the capacity and lifetime of batteries, but a widespread EV charging network is also a fundamental condition to allow long trips without concerns about range or charging time. Many energy providers and private companies are deploying fast chargers up to 150 kW, and there is strong interest in ultrafast chargers with power up to 500 kW per charging pile. Considering ultrafast charging stations with localized charging peak power up to megawatts and associated fast-charge energy premium rates, EV charging will become a massive energy exchange market, with the consequent need of accurate energy billing.

Currently, standard EV chargers are metered on the ac side with the drawback of no measurement of the energy lost in the ac-to-dc conversion and, consequently, billing is inaccurate for the end customer. Since 2019, new EU regulations are forcing energy providers to bill the customer only for the energy transferred to the EV, making the power conversion and distribution losses borne by the energy supplier.

While state-of-the-art SiC EV converters can reach efficiency above 97%, there is a clear need to enable accurate billing on the dc side for fast and ultrafast chargers, where energy is transferred in dc when directly connected to the battery of the vehicle. In addition to public EV charging metering interests, private and residential peer-to-peer EV charging schemes might have even more incentive for precise energy billing on the dc side.

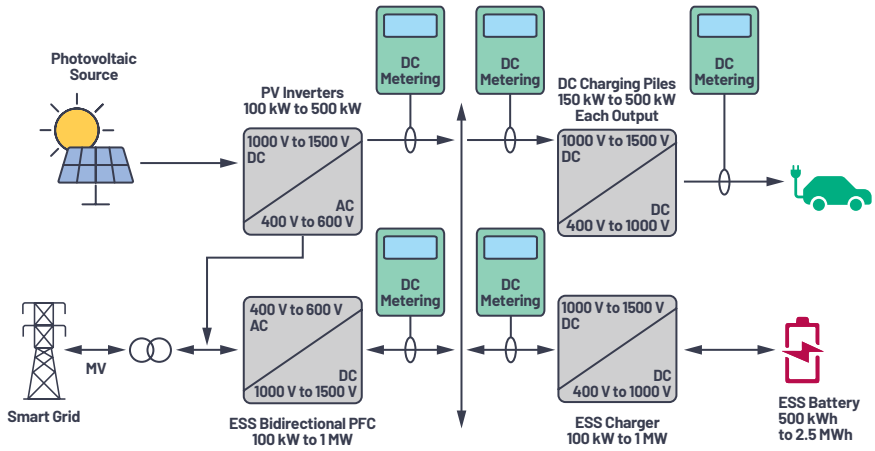

Figure 1. DC energy metering in the EV fuel station of the future.

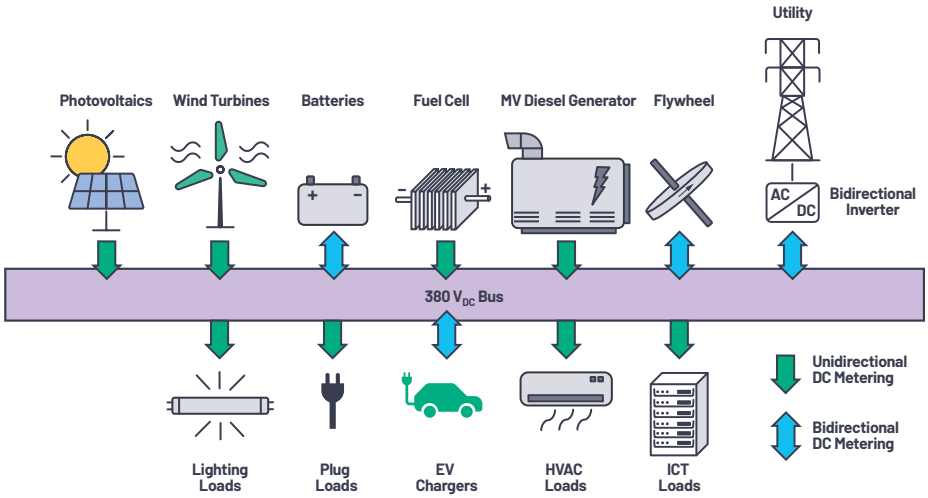

Figure 2. DC energy metering in a sustainable microgrid infrastructure.

DC Distribution—Microgrids

What is a microgrid? In essence, a microgrid is a smaller version of a utility power system. As such, safe, reliable, and efficient power is required. Examples of microgrids can be found in hospitals, on military bases, and even as part of the utility systems where renewable generation, fuel generators, and energy storage are working together to make a reliable energy distribution system.

Other examples of microgrids can be found in buildings. With the wide deployment of renewable energy generators, buildings can even become self-sufficient, with rooftop solar panels and small-scale wind turbines generating as much energy as is used, independent but backed up by the grid.

Moreover, as much as 50% of a building's electric loads run on dc. Currently each electronic device must convert ac to dc power, and up to 20% of energy is lost in the process, with a total savings estimated up to 28% vs. traditional ac distribution.[4]

In a dc building, energy consumption can be decreased by converting ac to dc all at once and feeding dc directly to the appliances that need it, such as LED lights and computers.

Interest in dc microgrids is rapidly growing, as is the need for standardization. IEC 62053-41 is a pending standard that indicates requirements and nominal levels for residential dc systems and enclosed type meters similar to the ac equivalent for dc energy metering.

The dc microgrid segment is valued at around $7 billion as of 2017[5] and will see further growth from the emerging dc distribution trend.

DC Data Center

Data center operators are actively considering different technologies and solutions to improve the power efficiency of their facilities, as power is one of their largest costs.

Data center operators see relevant benefits in dc distribution as the minimum number of conversions required between ac and dc decreases, and the integration with renewable energy is easier and more efficient. The reduction of conversion stages is estimated as:

- 5% to 25% energy savings: increase in transmission and conversion efficiencies, and less heat generation
- 2× reliability and availability
- 33% floor space reduction

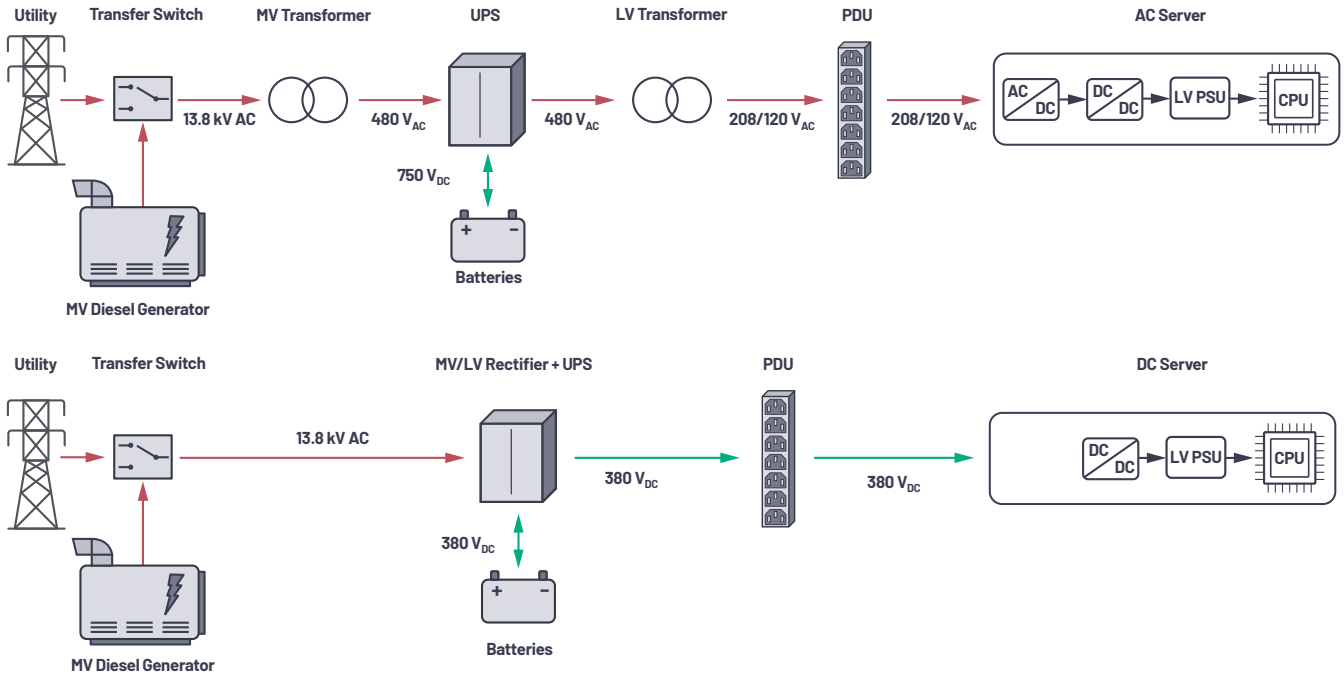

Figure 3. Fewer components are required in a dc supply for data centers, and there are lower losses than with traditional ac distribution.

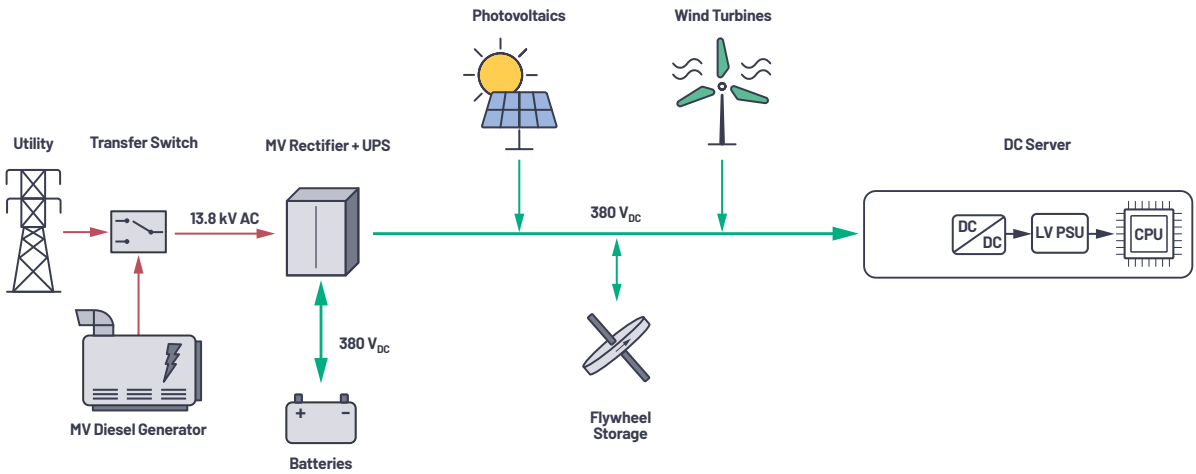

Figure 4. Renewable energy integration in a dc data center.

Distribution bus voltages range up to around 380 V_{DC}, and accurate dc energy metering is gaining interest since many operators are switching to the more measurable approach of charging the colocation customer by power use.

The two most popular ways to charge colocation customers for power usage are:

- Per whip (flat fee for each outlet)
- Consumed energy (metered outlet—power charged for each kWh consumed)

With a view toward encouraging power efficiency, the metered output approach is gaining popularity and customer pricing can be described as:

Recurring cost = space fee + (meter reading for IT equipment × PUE)

- Space fee: fixed, includes security and all the building operational costs
- Meter reading for IT equipment: the number of kWh consumed by the IT equipment multiplied by the cost of energy
- Power usage effectiveness (PUE): takes into account the efficiency of the infrastructure behind IT, such as cooling

A typical modern rack consumes up to 40 kW of dc power. Therefore, currents up to 100 A are required to be monitored with billing-grade dc meters.

Challenges in Precision DC Energy Metering

In the early 1900s traditional ac energy meters were entirely electromechanical. The combination of a voltage and a current coil was used to induce eddy currents in a rotating aluminium disc. The resulting torque on the disc was proportional to the product of the magnetic flux generated by the voltage and current coils. Finally, the addition of a breaking magnet for the disc made the rotational speed directly proportional to real power consumed by the load. At this point, measuring the energy consumed is simply a matter of counting the number of rotations over a period of time.

Modern ac meters are significantly more complex, accurate, and protected from tamperings. Now, a state-of-the-art smart meter can even monitor its absolute accuracy and detect signs of tampering 24/7 while installed in the field. This is the case for the Analog Devices ADE9153B metering IC, enabled with *m*Sure® technology.

Energy meters—either modern, traditional, ac, or dc—are all classified by their impulses per kWh constant and percentage class accuracy. The number of impulses per kWh denotes the energy update rate, or resolution. The class accuracy certifies the maximum measure error of the energy.

Similar to the old mechanical meter, energy in a given time interval is calculated by counting these impulses; the higher the pulse frequency, the higher the instantaneous power, and vice versa.

DC Meter Architecture

The basic architecture of a dc meter is represented in Figure 5. In order to measure the power consumed by the load ($P = V \times I$), at least one current sensor and one voltage sensor are required. When the low side is at earth potential, current flowing through the meter is commonly measured on the high side to minimize the risk of unmetered leakages, but current can also be measured on the low side, or both sides if required by the design architecture. The technique of measuring and comparing currents on both sides of the load is often used to enable the meter with fault and tamper detection capability. However, when the current is measured on both sides, at least one current sensor needs to be isolated in order to deal with the high potential across the conductors.

Voltage Measurement

Voltage is typically measured with a resistive potential divider, where a ladder of resistors is used to proportionally reduce the potential to a level compatible with the system ADC input.

Due to the large amplitude of the input signal, an accurate voltage measurement can be easily achieved with standard components. However, attention must be paid to temperature coefficients and voltage coefficients of the chosen component, in order to guarantee the required accuracy across the entire temperature range.

As previously discussed, dc energy meters for applications such as EV charging stations are sometimes required to bill exclusively for the energy transferred to the vehicle. In order to fulfill the measurement requirement, dc energy meters for EV chargers may be required to have multiple voltage channels, enabling the meter to sense the voltage also at the entry point of the vehicle (4-wire measurement). DC energy metering in a 4-wire configuration ensures that all the resistive losses of the charging pile and the cable are discounted from the total energy bill.

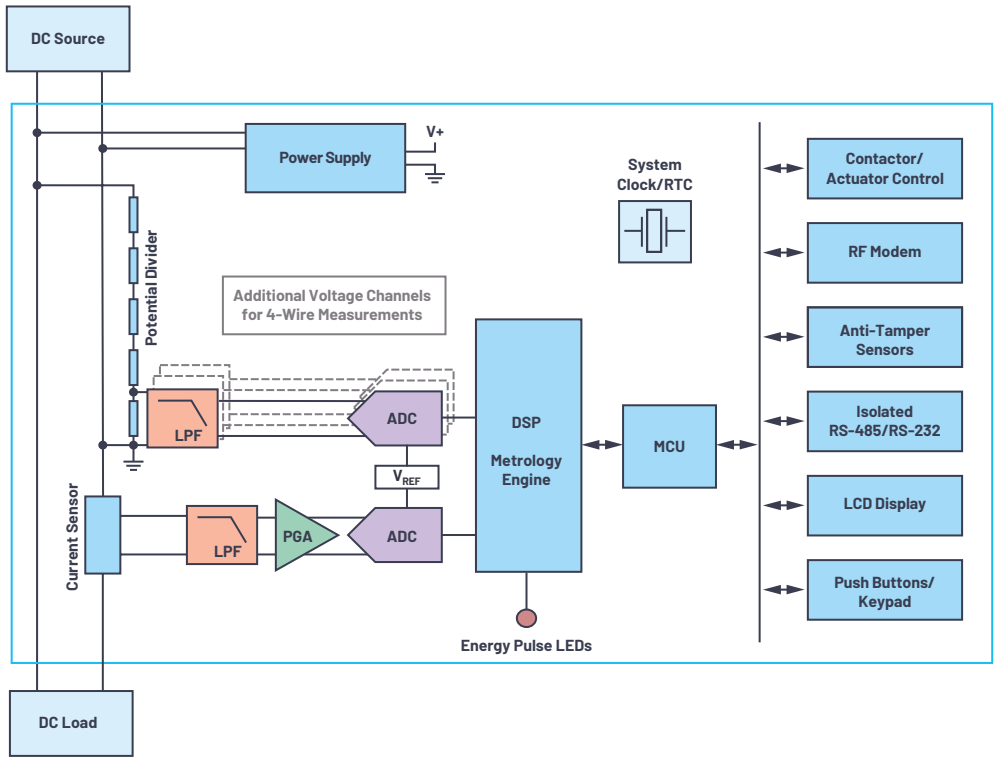

Figure 5. DC energy meter system architecture.

Current Measurement for DC Energy Metering

Electric current can be measured either by direct connection or indirectly, by sensing the magnetic field generated by the flow of the charge carrier. The next section will discuss the most popular sensors for dc current measurement.

Shunt Resistor

Direct connection current sensing is a tried and tested method of measuring ac and dc current. The flow of current is routed through a shunt resistor of known value. The voltage drop across the shunt resistor is directly proportional to the current flowing as described by the well-known Ohm's law ($V = R \times I$), and it can be amplified and digitized, providing an accurate representation of the current flowing in the circuit.

Shunt resistor sensing is a cheap, accurate, and powerful method for measuring current from mA to kA, with theoretically unlimited bandwidth. However, the method suffers from some disadvantages.

When current flows in a resistor, Joule heat is generated proportionally to the square of the current. This will cause not only losses in terms of efficiency, but the self-heating will change the shunt resistive value itself with a consequent accuracy degradation. To limit the self-heating effect, a low value resistance is used. However, when a small resistance is used, the voltage across the sensing element is also small and sometimes comparable with the dc offset of the system. In these conditions, achieving the required accuracy on the low end of the dynamic range may not be a trivial task. State-of-the-art analog front ends, with ultralow dc offset and ultralow temperature drift, can be used to overcome the limitations of small value shunt resistors. However, as operational amplifiers have a constant gain-bandwidth product, a high gain will limit the available bandwidth.

Low value current sensing shunts are usually made from specific metal alloys such as manganese-copper or nickel-chrome, which cancel the opposing temperature drifts of their constituents to result in an overall drift in the order of tens of ppm/°C.

Another error contributor in direct connection dc measurement can be the phenomenon of thermal electromotive force (EMF), also known as the Seebeck effect. The Seebeck effect is a phenomenon in which a temperature difference between at least two dissimilar electrical conductors or semiconductors forming a junction produces a potential difference between the two. The Seebeck effect is a well-known phenomenon, and it is widely used for sensing temperature in thermocouples.

In the case of 4-wire connected current shunts, the Joule heat will form on the center of the resistive alloy element, propagating whilst the copper sensing wires, which may be connected to a PCB (or a different medium), and which may have a different temperature.

The sensing circuit will form a symmetric distribution of different materials; therefore, the potential at the junctions on the negative and positive sensing wires will approximately cancel. However, any difference in thermal capacity, such as a negative sensing wire being connected to a larger copper mass (ground plane), can produce a mismatch in the temperature distribution, resulting in a measure error caused by thermal EMF effect.

For that reason, attention must be reserved to the connection of the shunt and at the distribution of the generated heat.

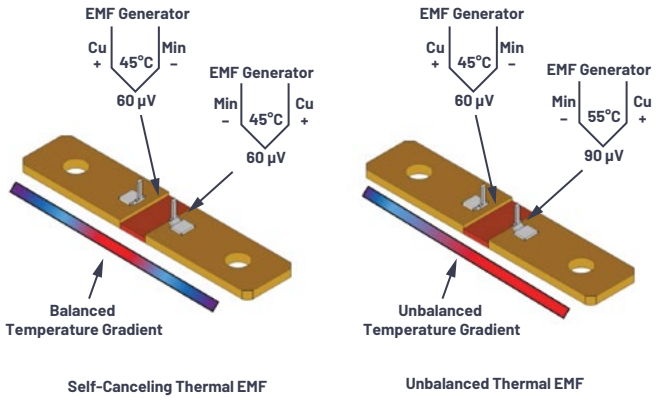

Figure 6. Thermal EMF in shunts caused by temperature gradient.

Magnetic Field Sensing—Indirect Current Measurement

Open-Loop Hall Effect

The sensor is constructed with a high magnetic permeability ring through which the sensed current wire is passed. This concentrates the magnetic field lines surrounding the measured conductor onto a Hall effect sensor, which is inserted within the cross-section area of the magnetic core. The output of this sensor is preconditioned and usually available in different flavors. The most common are: 0 V to 5 V, 4 mA to 20 mA, or digital interface. While providing isolation and high current range for relatively low cost, absolute accuracies typically do not range below 1%.

Closed-Loop Hall Effect

A multiturn secondary winding on the permeable core driven by a current amplifier provides negative feedback to achieve zero total flux condition. By measuring the compensating current, linearity is improved and there is no core hysteresis with overall superior temperature drift and higher accuracy compared to the open-loop solution. Typical error ranges are down to 0.5%, but the additional compensation circuitry make the sensor more expensive and sometimes limited in bandwidth.

Fluxgate

Is a complex open- or closed-loop system where the current is measured by monitoring the magnetic flux variations of an intentionally saturated core. A coil is wound around a high permeability ferromagnetic core that is intentionally saturated by a secondary coil driven by a symmetric square wave voltage. The inductance of the coil collapses every time the core approaches positive or negative saturation, and the rate of change of its current increases. The current waveform of the coil remains symmetrical unless an external magnetic field is additionally applied, in which case the waveform becomes asymmetrical. By measuring the size of this asymmetry, the intensity of the external magnetic field, and consequently the current that generated it, can be estimated. It provides good temperature stability and accuracy down to 0.1%. However, the complex electronics of the sensor makes it an expensive solution with prices 10 times higher than the other isolated solutions.

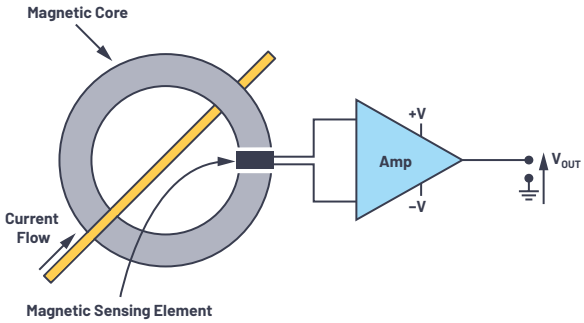

Figure 7. An open-loop current transducer based on a flux concentrator and magnetic sensor.

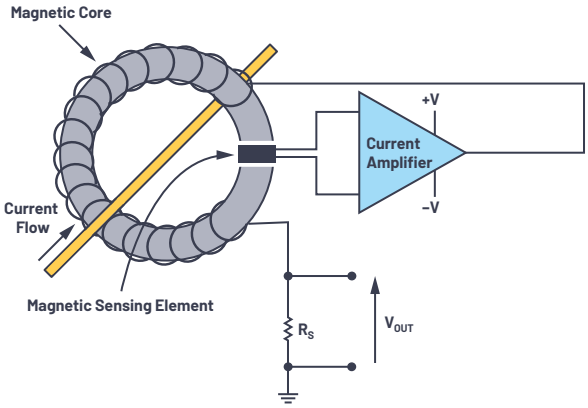

Figure 8. An example of the working principle of closed-loop current transducers.

DC Energy Metering: Requirements and Standardization

While the standardization of dc energy metering may not seem too difficult to achieve compared to the existing ac metering standards ecosystem, industry stakeholders are still debating the requirements for different applications, asking for more time to iron out the exact details of dc metering.

IEC is working on IEC 62053-41 in order to define requirements specific for dc static meters for active energy with accuracy classes of 0.5% and 1%.

The standard proposes a range of nominal voltages and currents, and sets limits on the maximum power consumption of the voltage and current channels of the meter. Moreover, like the ac metering requirement, specific accuracy is defined across the dynamic range, as well as the current threshold for no-load condition.

In the draft, there is no specific requirement for the bandwidth of the system, but a fast load variation test is required to be successfully accomplished, defining implicit requirement on the minimum bandwidth of the system.

DC metering in EV charging applications is sometimes compliant with the German standard VDE-AR-E 2418 or old railway standard EN 50463-2. According to EN 50463-2, accuracies are specified per transducer, and the combined energy error is then a quadrature sum of voltage, current, and calculation error:

$$\epsilon = \sqrt{\epsilon_V^2 + \epsilon_I^2 + \epsilon_{calc}^2} \quad (1)$$

Table 1. Maximum Percentage Current Error per EN 50463-2

Current Range	Class 0.2R	Class 0.5R	Class 1R
1% to 5% I_N	1%	2.5%	5%
5% to 10% I_N	0.4%	1%	1.5%
10% to 120% I_N	0.2%	0.5%	1%

Table 2. Maximum Percentage Voltage Error per EN 50463-2

Voltage Range	Class 0.2R	Class 0.5R	Class 1R
<66% V_N	0.4%	1%	2%
66% to 130% V_N	0.2%	0.5%	1%

Conclusion: A Proof of Concept Standard Compliant DC Meter

Analog Devices is an industry leader in precision sensing technology, offering a complete signal chain for precision current and voltage measurements to meet the restrictive standards requirements. The next section will show a proof of concept for a dc energy meter compliant with the upcoming application-specific standard IEC 62053-41.

Considering the space of billing-grade dc energy metering in microgrids and data centers, we can hypothesize the requirements shown in Table 3.

Table 3. DC Energy Meter Specifications—Proof of Concept

Rating		Nominal	Dynamic Range	Measurement (Max Range)
Voltage		±400 V_{DC}	100:1	±600 V
Current		±80 A	100:1	±240 A
Accuracy	1% to 5% I_{NOM}	1%		
	5% to 120% I_{NOM}	0.5%		
Temperature		–25°C to +55°C		–40°C to +70°C storage
Meter Constant		1000 imp/kWh		
Voltage and Current Bandwidth		2.5 kHz		

Cheap and accurate current sensing can be achieved by using a small value and low EMF shunt (<1 μV_{EMF}/°C). Keeping the shunt resistance small is fundamental to reduce the self-heating effect and keep the power level below the limits required by the standard.

A commercial 75 µΩ shunt will keep the power dissipated below 0.5 W.

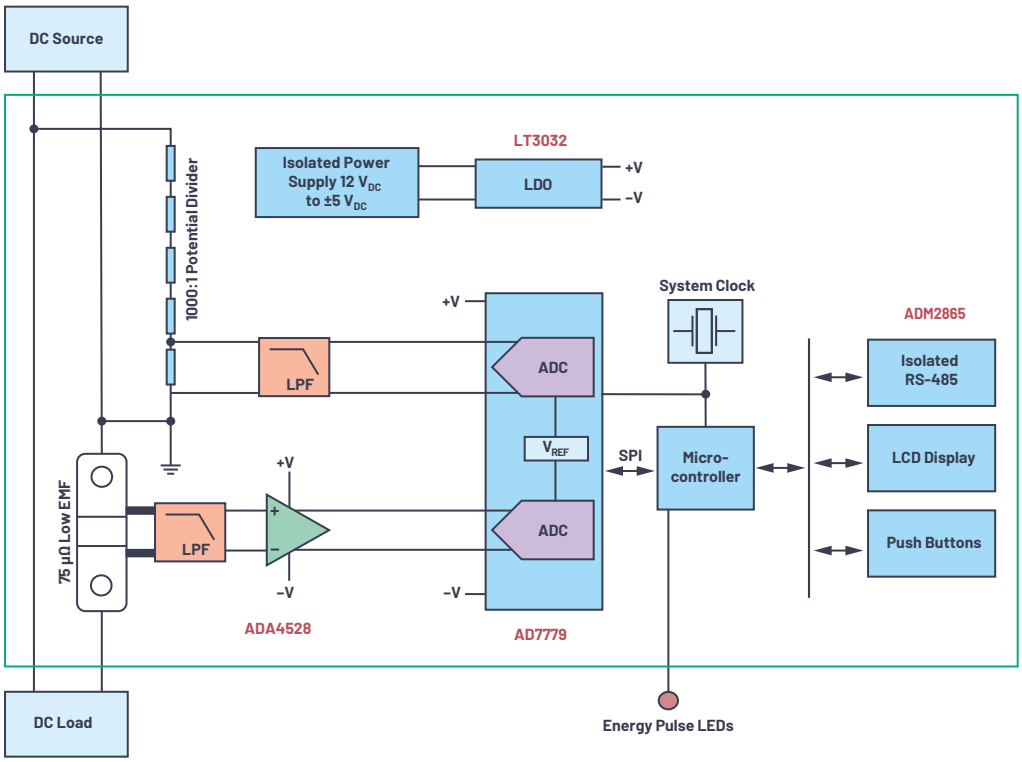

Figure 9. DC meter system architecture.

However, 1% of the 80 A nominal current will generate a small signal of 60 µV on a 75 µΩ shunt, requiring a signal chain in the range of sub-microvolt offset drift performance.

The ADA4528, with a max offset voltage of 2.5 µV and a max offset voltage drift of 0.015 µV/°C, is well suited to provide ultralow drift, 100 V/V amplification for the small shunt signal. Therefore, the simultaneous sampling, 24-bit ADC AD7779 can be directly connected to the amplification stage, with a 5 nV/°C input referred offset drift contribution.

Figure 10. Proof of concept—prototype.

High dc voltage can be accurately measured with a resistive potential divider of 1000:1 ratio directly connected to the AD7779 ADC input.

Finally, a microcontroller implements a simple sample-by-sample, interrupt driven metrology functionality, where for each ADC sample the interrupt routine:

- Reads voltage and current samples
- Calculates instantaneous power (P = I × V)
- Accumulates the instantaneous power in an energy accumulator
- Checks if the energy accumulator exceeds the energy threshold to generate an energy pulse and clears the energy accumulation register

Moreover, in addition to the metrology functionality, the microcontroller enables system-level interfaces such as RS-485, LCD display, and push buttons.

References

[1] Tom Turrentine, Scott Hardman, and Dahlia Garas. "Steering the Electric Vehicle Transition to Sustainability." National Center for Sustainable Transportation, UC Davis, July 2018.

[2] "Global Electric Vehicle Market Report by Type (Battery Electric Vehicle, Hybrid Electric Vehicle, and Plug-In Hybrid Electric Vehicles), by Vehicle Type (Two Wheeler, Passenger Car, and Commercial Vehicles), and by Regions—Industry Trends, Size, Share, Growth, Estimation, and Forecast, 2017-2024." Value Market Research.

[3] *Electric Vehicle Charging Stations Market by Charging Station (AC Charging Station, DC Charging Station), Installation Type (Residential, Commercial), and Region (North America, Europe, Asia Pacific, and Row)—Global Forecast to 2023*. Research and Markets, April 2018.

[4] Venkata Anand Prabhala, Bhanu Prashant Baddipadiga, Poria Fajri, and Mehdi Ferdowsi. "An Overview of Direct Current Distribution System Architectures and Benefits." MDPI, September 2018.

[5] "Global Microgrid Market by Type (AC Microgrid, DC Microgrid, Hybrid), Connectivity (Grid Connected, Remote/Island), Offering (Hardware, Services, Software), Power Source (Natural Gas, Solar, Fuel Cells, Combined Heat and Power, Diesel, and Others), Application (Healthcare, Industrial, Military, Electric Utility, and Educational Institutions), Region (North America, Europe, Asia Pacific, South America, and Middle East and Africa), Global Industry Analysis, Market Size, Share, Growth, Trends, and Forecast, 2018-2025." Researchstore.biz.

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Luca Martini received an M.Eng. degree in electronics and telecommunication engineering for energy from the University of Bologna, Italy, in 2016. As part of his M.Eng. degree, he spent seven months at Fraunhofer IIS, Nuremberg, Germany, developing a precision real-time control system for the characterization of piezoelectric energy harvesters. From 2006 to 2016, Luca worked as a system and hardware developer in the biomedical sector. In 2016, Luca joined the Energy and Industrial System Group at Analog Devices, in Edinburgh, UK. He can be reached at luca.martini@analog.com.

CTSD Precision ADCs—Part 1: How to Improve Your Precision ADC Signal Chain Design Time

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Abstract

Precision signal chain designers are challenged to meet noise performance demands in medium bandwidth applications and often end up making a trade-off between noise performance and accuracy. Achieving faster time to market and getting their design right the first time can add further pressure. Continuous-time sigma-delta (CTSD) ADCs bring out inherent architectural benefits and simplify signal chain design to reduce solution size and help customers achieve faster time to market for their end products. In this series of articles, we will explain the inherent architectural benefits of CTSD ADCs and how they are adapted to a wide range of precision medium bandwidth applications. We will take a deep dive into signal chain design to educate designers on the key advantages of CTSD technology and explore the AD4134 precision ADC's ease of design features.

Introduction

In many digital processing applications and algorithms, the demand to have better resolution and precision for all converter technologies has increased over the last two decades. The limited resolution/precision of ADCs was enhanced by using an external digital controller that would extract and deliver more precise results using software techniques such as averaging and optimized filtering schemes. To reduce extensive postprocessing at the digital microcontroller or DSP, designers could use a high performance precision ADC. This would reduce optimization time at the digital side, and a lower cost microcontroller or DSP could also be considered. The applications and markets for precision ADCs are widespread:

- Industrial instrumentation: vibration analysis, temperature/pressure/strain/flow measurements, dynamic signal analysis, acoustic analysis

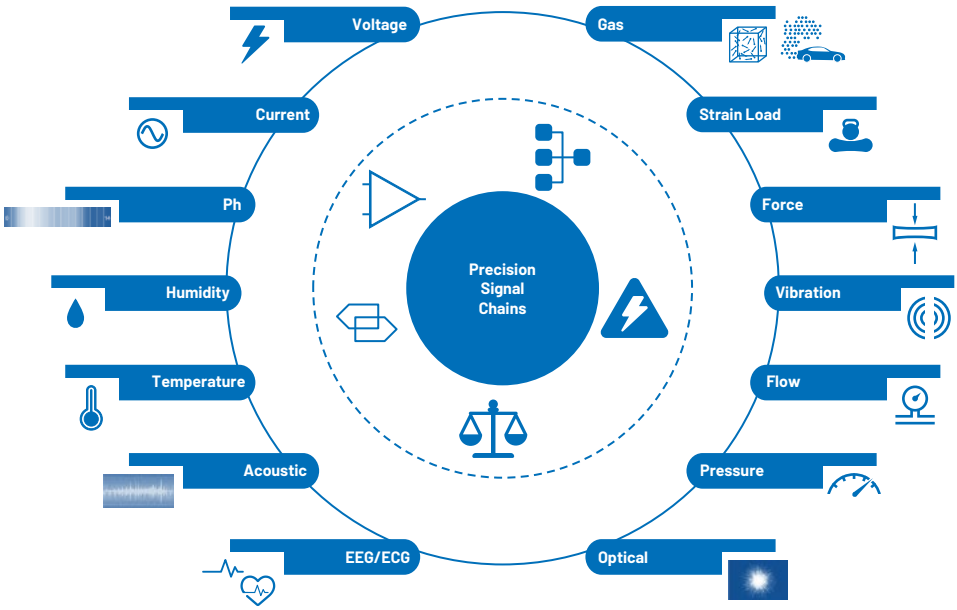

Figure 1. Precision ADC signal chain examples.

- Medical instrumentation: electrophysiology, blood analysis, electrocardiogram (EKG/ECG)
- Defense applications: sonar, telemetry
- Test and measurement: audio test, hardware in loop, power quality analysis

The analog input signal to be processed by an ADC could be a sensor signal with voltage, current output, or a feedback control loop signal with bandwidth ranging from dc to a few hundred kHz. The ADC digital output format and rate are dependent on the application and postprocessing required by the following digital controller. In general, signal chain designers follow the Nyquist sampling theorem and program the ADC's output data rate (ODR) for the digital controller to be at least twice the input frequency. Most ADCs provide the flexibility to tune the output data rate based on the signal frequency band of interest.

For currently available ADCs, there are several signal conditioning stages involved before the ADC can interact with the input signal. Signal conditioning circuits with stringent requirements need to be designed and tailored around specific and individual ADC technologies to ensure that ADC data sheet performance can be achieved. A signal chain designer's job doesn't stop after the selection of the ADC. Considerable time and effort are often required to design and fine tune this surrounding periphery. Analog Devices provides a high level of technical support in the form of design simulation tools and models to overcome most of these inherent design challenges.

A New Approach: Easing the Design Journey with CTSD Architecture

CTSD architecture, which has been predominantly used in audio and high speed ADCs, is being tailored for precision applications to achieve the highest precision while leveraging its unique signal chain simplification properties. The advantages of this architecture remove the burdens involved with designing the periphery. Figure 2 shows a small snippet of how current ADC signal chains can be simplified and shrunk by 68% by using this new solution to enable high channel densities.

To illustrate the simplification that CTSD ADC technology brings to the signal chain, this article highlights some of the key challenges involved in incumbent signal chain design for general applications, as well as shows how CTSD ADCs ease these challenges.

So, let's start with a few design steps involved in incumbent signal chains with the very first task being the selection of the right ADC to best fit the targeted application.

Step 1: Selecting the ADC

When selecting from the wide range of ADCs that are available, important considerations are resolution and accuracy, signal bandwidth, ODR, signal type, and the range to be processed. Generally, in most of the applications, digital controllers require their algorithms to process amplitude, phase, or frequency on the input signal.

To accurately measure any of the previous factors, the errors added in the process of digitization need to be minimal. The major errors and their corresponding measurement terminology are detailed in Table 1 and explained in further detail in the Essential Guide to Data Conversion.

Table 1. ADC Errors and Performance Metrics

ADC Error		Associated Measurements in Data Sheets
1	Thermal and quantization noise	Signal-to-noise ratio (SNR), dynamic range (DR)
2	Distortion	Total harmonic distortion (THD), intermodulation distortion (IMD)
3	Interference	Crosstalk, alias rejection, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR)
4	Magnitude and phase error	Gain error, magnitude, and phase droop at frequency of interest
5	Delay from ADC input to final digital output	Latency, settling time

The performance metrics in Table 1 are related to signal amplitude and frequency, and are generally termed as ac performance parameters.

For dc or near dc applications such as power metering dealing with 50 Hz to 60 Hz input signals, ADC errors such as offset, gain, INL, and flicker noise would have to be accounted for. These dc performance parameters also require a certain level of temperature stability relating to an application's intended use.

ADI provides a wide range of industry-leading high performance ADCs to meet system requirements of several applications, be they precision based, speed based, or based on a restricted power budget. Just comparing one set of ADC specifications to another is not the way to choose an ADC. The overall system performance and design challenges must be considered, and that's where the choice of ADC technology or architecture comes into play. There are two broad classifications of ADC architectures that are traditionally preferred. The most popular is the successive approximation register (SAR) ADC, which follows the simple Nyquist theorem. It states that a signal can be reconstructed if sampled at twice its frequency. The advantages of SAR ADCs are excellent dc performance and small form factors with low latency and power consumption scaling with ODR.

The second technology choice is a discrete-time sigma-delta (DTSD) ADC, which works on the principle that the greater the number of samples, lesser is the information lost. So the sampling frequency is much higher than the stated Nyquist frequency, a scheme referred to as oversampling. An added advantage from this architecture is that the errors added due to sampling are minimized in the frequency band of interest. Because of this, DTSD ADCs have both excellent dc and ac performance but a higher latency.

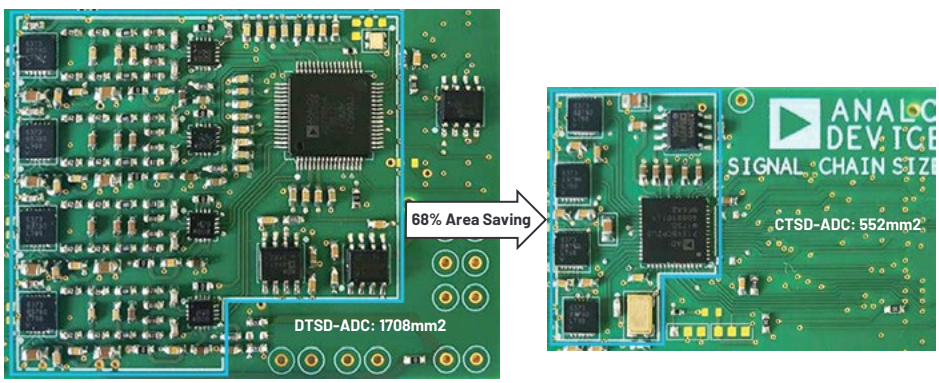

Figure 2. A compact size solution with ADI's new easy to use CTSD ADC.

Figure 3 shows an illustration of the typical analog input bandwidths of both SAR and DTSD ADCs, with some popular product choices at various speeds and resolution. The Precision Quick Search feature can also be referenced to help in your choice of ADC.

Additionally, a new class of precision ADCs are now available. These are based on CTSD ADCs that are on par with the performance of DTSD ADCs but they are unique with regard to simplifying the entire signal chain design process. The challenges highlighted in the next few design steps of an incumbent signal chain can be addressed by this new ADC family.

Step 2: Interfacing the Input to the ADC

Sensors whose outputs are to be processed by the ADC may have very high sensitivity. Designers must have a good understanding of the ADC input structure to which the sensor will be interfaced to ensure ADC errors don't mask or distort the actual sensor signal.

In conventional SAR, DTSD ADCs, the input structure is known as the switched capacitor sample-and-hold circuit, as shown in Figure 4. At every sampling clock edge when the sample switch changes its ON/OFF state, finite current demand needs to be supported to charge or discharge the hold capacitor to a new sampled input value. This current demand needs to be supplied by the input source, which, in our case of discussion, is the sensor. Additionally, the switch itself has some on-chip parasitic capacitors that inject some charge back onto the source, which is called charge injection kickback. This added error source also needs to be absorbed by the sensor to avoid corruption of the sensor signal.

Most of the sensors are incapable of providing such a magnitude of currents, indicating that they fall short of driving switching circuitry directly. In a different scenario, say even if a sensor can support these current demands, the sensor's finite impedance would add an error at the ADC input. The charge injection current is a function of input and this current causes an input dependent voltage drop across the sensor impedance. As shown in Figure 4a, the input of the ADC is then in error. One solution to solve these issues is to place a driving amplifier between the sensor and ADC, as shown in Figure 4b.

Now we need to set the criteria for this amplifier. First and foremost, the amplifier should support the charging current and absorb the charge injection kickback. Next, this amplifier's output needs to be fully settled at the end of the sampling edge so that the ADC samples input without added errors. This means the amplifier should have the capability to provide instantaneous current steps that map to having a high slew rate and provide a fast settling response to these transient events, which maps to having high bandwidth. As the sampling frequency and resolution of the ADC increases, meeting these requirements becomes critical.

The big challenge for designers, especially those who work with medium bandwidth applications, is to identify the right amplifier for the ADC. As indicated earlier, ADI provides a set of simulation models and precision ADC driver tools to ease this step, but for a designer, it is an added design step to achieve the data sheet performance of the ADC. Some of the new age SAR and DTSD ADCs have mitigated this challenge by using novel sampling techniques to completely reduce the transient current demand or by having an integrated amplifier. But either solution limits the range of signal bandwidth or penalizes ADC performance.

The CTSD ADC advantage: CTSD ADCs address this challenge by providing an easy to drive resistive input instead of a switched capacitor input. This shows that there are no hard requirements of high bandwidth, large slew rate amplifiers. If sensors can directly drive this resistive load, they can be directly interfaced to a CTSD ADC; otherwise any low bandwidth, low noise amplifier could be interfaced between a sensor and a CTSD ADC.

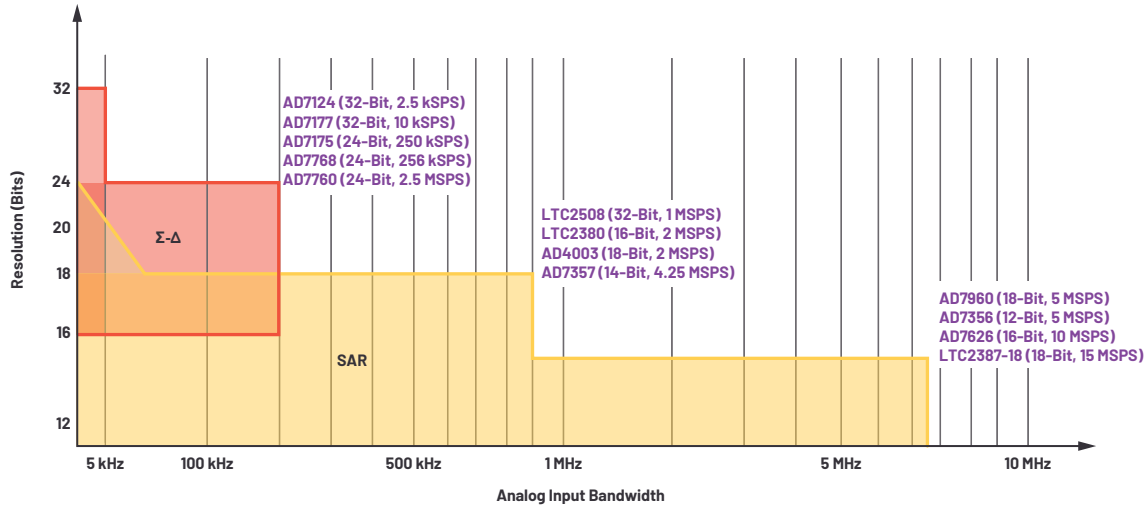

Figure 3. Precision ADC architecture positioning.

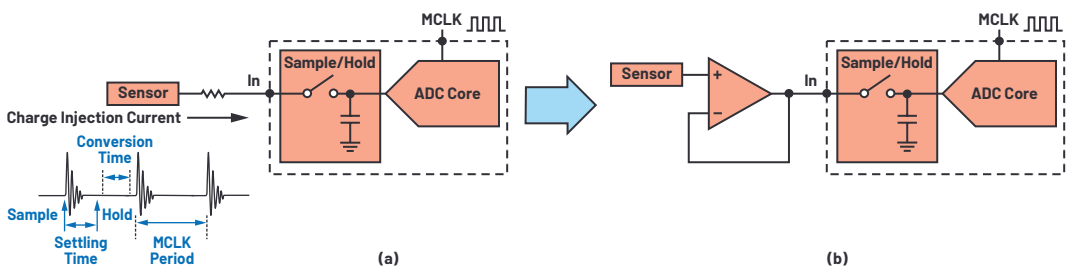

Figure 4. (a) Switched capacitor charge injection kickback into the sensor, and (b) isolating the kickback effect with an input buffer.

Step 3: Interfacing the Reference to the ADC

The challenge involved with interfacing to a reference is similar to input interfacing. The reference input for conventional ADCs is also a switched capacitor. At every sampling clock edge, the reference source needs to charge the internal capacitors, thus demanding large switching current with good settling time.

The reference ICs available cannot support large switching current demand and have limited bandwidth. The second interfacing challenge is that noise from these references is large in comparison to an ADC's noise. To filter this noise, a first-order RC circuit is used. On one hand, we are band-limiting the reference for noise, while on the other hand, we are demanding fast settling time. These are two opposing requirements to satisfy. For this reason, a low noise buffer is used to drive the ADC reference pin, as shown in Figure 5b. Based on the sampling frequency and resolution of an ADC, the slew rate and bandwidth of this buffer is decided.

Again, like with our precision input driver tools, ADI has tools to simulate and select the correct reference buffers for an ADC. And similar to input, some of the new age SAR and DTSD ADCs also have the option of an integrated reference buffer, but they come with performance and bandwidth limitations.

The CTSD ADC advantage: This design step can be completely skipped by using a CTSD ADC as it provides a new, easy option for driving a resistive load that doesn't require such a high bandwidth, large slew rate buffer. The reference IC with low-pass filter can directly be interfaced to the reference pin.

Step 4: Making a Signal Chain Immune to Interference

Sampling and digitizing a continuous signal causes loss of information, which is termed as quantization noise. The sampling frequency and number of bits set the performance limit for an ADC architecture. After addressing the performance and interfacing challenges for the reference and input, the next struggle is to address the issue of high frequency (HF) interferers/noise folding into the low frequency bandwidth of interest. This is termed aliasing or folding back. These reflected images of the HF or out-of-band interferers into the bandwidth of interest cause signal-to-noise ratio (SNR) degradation. Citing the sampling theorem, any tone around the sampling frequency folds back in-band, as illustrated in Figure 6, which causes an unwanted information or error in the frequency band of interest. Further details on aliasing can be found in the tutorial MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design.

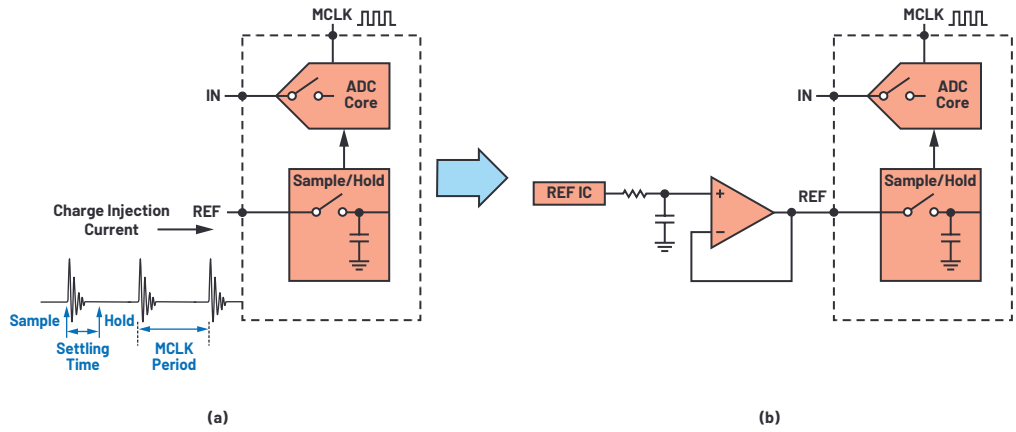

Figure 5. (a) Switched capacitor charge injection kickback into the reference IC and (b) isolating the kickback effect with a reference buffer.

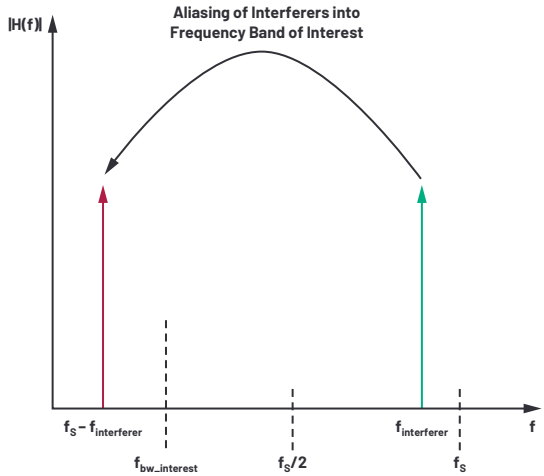

Figure 6. The aliasing/foldback of out-of-band interferers into the frequency band of interest because of sampling.

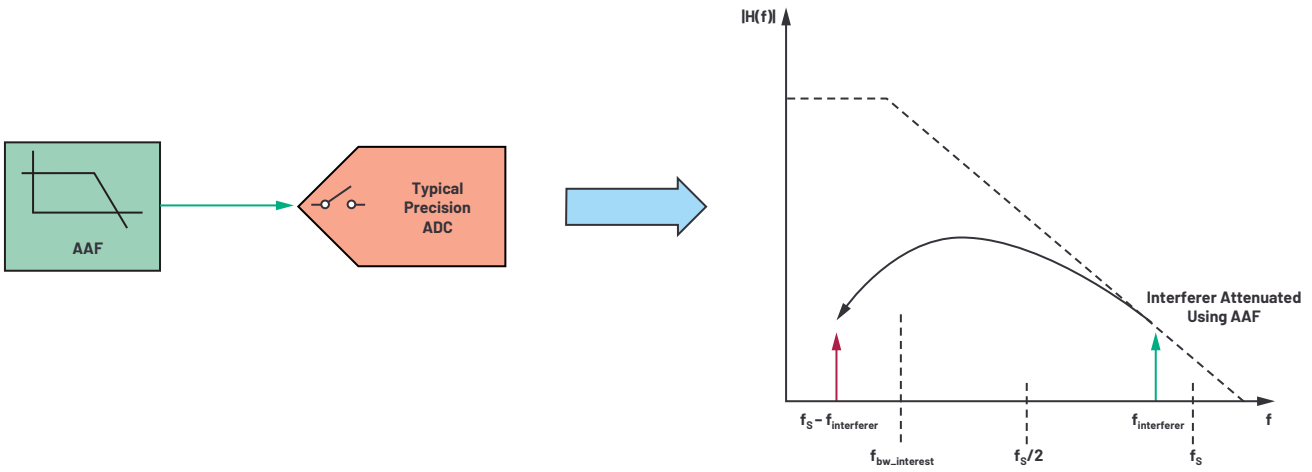

Figure 7. Use of antialiasing filter to mitigate the effect of aliasing on in-band performance.

One solution to mitigate the effect of foldback is to use a type of low-pass filter known as an antialiasing filter (AAF) to attenuate the unwanted interferer's magnitude such that when this attenuated interferer folds back in-band, the desired SNR is maintained. This low-pass filter is generally incorporated with a driver amplifier, as shown in Figure 7.

When designing this amplifier, the biggest challenge is finding a balance between faster settling and the low-pass filtering requirements. An added challenge is that this solution needs to be fine tuned for each application requirement, which limits the adoption of single platform design across various applications. ADI has many antialiasing filter tool designs to help designers overcome this challenge.

The CTSD ADC advantage: This immunity to interference is addressed by the inherent alias rejection property of the CTSD ADC itself, a feature that is unique only to CTSD ADCs. The AAF is not required for ADCs with this technology. So, we would be one step nearer to directly interfacing a CTSD ADC to a sensor without much effort.

Step 5: Selecting the ADC Clock Frequency and the Output Data Rate

Next, let's discuss the clock requirements for the two classes of traditional ADCs we have discussed. The DTSD is an oversampled ADC, which means that the ADC is sampled at a higher than Nyquist sampling rate. But giving ADC oversampled data directly to the external digital controller implies we are overloading it with lot of redundant information. In an oversampled system, the core ADC output is decimated using on-chip digital filters that enable the final ADC digital output at a lower data rate, which is usually twice the signal frequency.

For DTSD ADCs, the designer needs to plan for the provision of the high frequency sampling clock for the core ADC and program the desired output data rate. The ADC will give a final digital output at this desired ODR and the ODR clock. A digital controller uses this ODR clock to clock in the data.

Next, we address the clock requirements of SAR ADCs, which usually follow the Nyquist theorem. Here, the sampling clock of the ADC is provided by a digital controller and the clock also acts as an ODR. But there is less flexibility in the timing of this clock as the sample-and-hold timing needs to be well controlled to get optimum performance from the ADC, which also indicates that the timing of the digital output needs to be well aligned with these requirements.

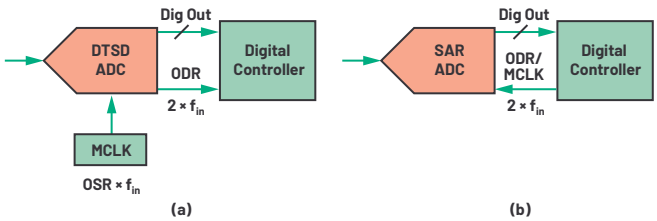

Figure 8. Clocking requirements in (a) a DTSD ADC and (b) a SAR ADC.

In understanding the clock requirements of both these architectures, we see that the ODR is coupled to the sampling clock of the ADC, which is a limitation in many systems where ODR can drift or change dynamically or needs to be tuned to the analog input signal frequency.

The CTSD ADC advantage: The CTSD ADC couples with a novel asynchronous sample rate converter (ASRC) that resamples the core ADC data at any desired ODR. The ASRC also enables designers to granularly set the ODR at any frequency and go beyond the age-old restriction of limiting ODR to a multiple of sampling frequency. The frequency and timing requirements of ODR are now purely a function of the digital interface and completely decoupled from the ADC sampling frequency. This feature eases digital isolation design for signal chain designers.

Step 6: Interfacing with the External Digital Controller

Traditionally, there are two types of data interface modes for ADCs to communicate with the digital controller. One involves the ADC acting as a host, providing the digital/ODR clock, and deciding on the clock's edges for the digital controller to clock-in the ADC data. The other type is hosted mode (receiver mode), in which the digital controller is the host, provides the ODR clock, and decides the clock edges at which the ADC data will be clocked in.

Continuing from Step 5, if a designer selects a DTSD ADC, the ADC acts as host for the following digital controller since the ADC provides the ODR clock. If a SAR ADC is selected, the digital controller needs to provide the ODR clock implying SAR ADCs are always configured as hosted peripheral. So, the obvious limitation is that, once an ADC architecture is chosen, the digital interface is restricted to being in host mode or hosted mode. Currently, there is no flexibility in choosing the interface regardless of ADC architecture.

The CTSD ADC advantage: The novel ASRC that has been coupled with a CTSD ADC enables designers to independently configure the ADC data interface mode. This opens up a whole new opportunity for applications where high performing ADCs can be configured in any mode suitable for the digital controller of the application irrespective of ADC architecture.

Putting It All Together

Figure 9 shows the building blocks of a traditional signal chain with an analog front end (AFE) comprising an ADC input driver, an alias rejection filter, and a reference buffer that can be drastically simplified by a CTSD ADC. Figure 10a illustrates an example signal chain with a DTSD ADC that requires significant design effort to fine tune and derive the data sheet performance of the ADC. To ease the customer journey, ADI has reference designs that can be reused or retweaked for various applications for these ADCs.

Figure 10b shows a signal chain with a CTSD ADC with its simplified analog input front end (AFE) because its ADC core does not have a switch capacitor sampler at the input and reference. The switch sampler is moved to a later stage of the ADC core, making the signal input and reference input purely resistive. This results in an almost nonsampling ADC, making a class of its own. Also, the signal transfer function of this class of ADCs mimics the antialiasing filter response, which means it inherently attenuates noise interferers. With CTSD technology, the ADC is reduced to an easy plug and play component.

In summary, CTSD ADCs simplify signal chain design while achieving a system solution with the same performance level as a traditional ADC signal chain, along with offering the following advantages:

- Provides alias free, low latency signal chain with excellent channel-to-channel phase matching
- Simplifies the analog front end with no added step of selection and fine tuning of high bandwidth input and reference driver buffers, enabling higher channel density
- Breaks barrier of ODR being a function of the sampling clock
- Gives independent control of interface to external digital controller
- Improves the signal chain reliability rating, which is a direct result of periphery component reduction
- Reduces size and has a 68% reduction in BOM, leading to faster time to market for customers

The next few articles in this series will explain the concepts of CTSD ADCs and ASRCs in greater detail, highlight the signal chain advantages, and will conclude with leveraging the features of the new AD4134. Keep a look out to learn more about the breakthrough CTSD and ASRC technologies that can simplify your designs!

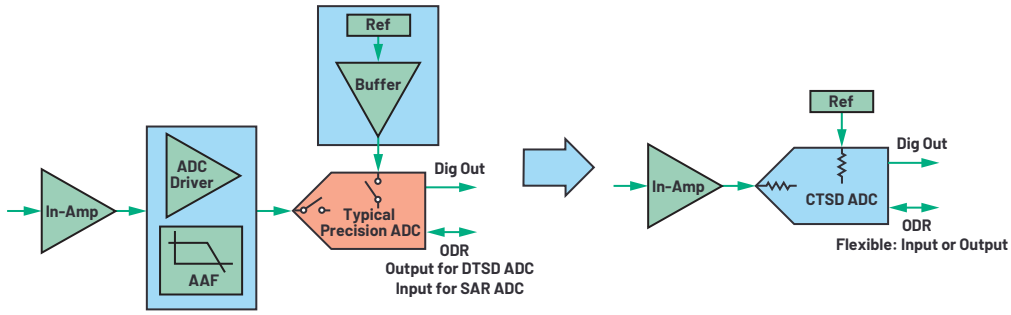

Figure 9. The building blocks of a signal chain with a traditional precision ADC vs. a CTSD ADC.

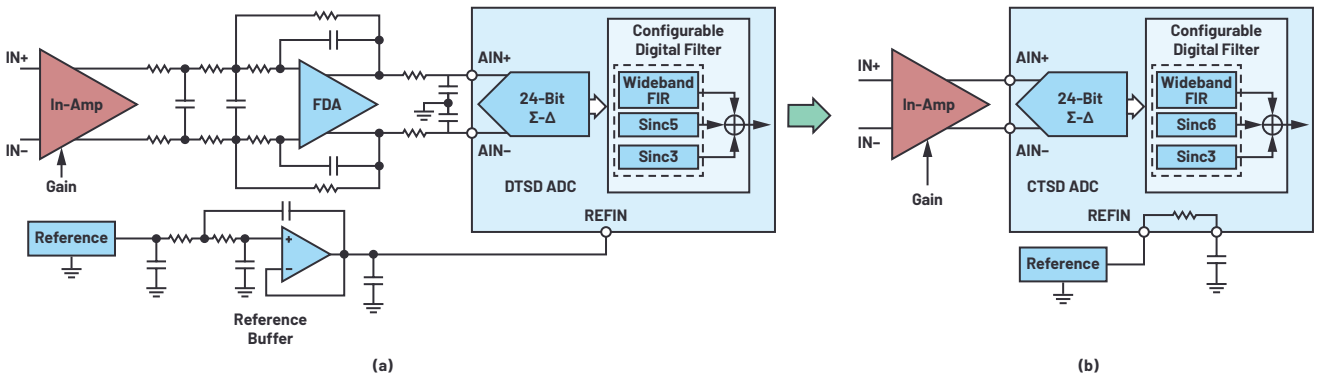

Figure 10. An example signal chain using (a) DTSD technology vs. (b) CTSD technology.

Acknowledgements

The authors would like to thank product applications engineer Ren Naiqian and product marketing engineer Mark Murphy for their useful insights in writing this article.

References

"Application Note AN-282: Fundamentals of Sampled Data Systems." Analog Devices, Inc.

Driving Precision Converters: Selecting Voltage References and Amplifiers. Analog Devices, Inc.

Kester, Walt. "MT-021 Tutorial: ADC Architectures II: Successive Approximation ADCs." Analog Devices, Inc., 2009.

Sigma-Delta ADC Tutorial. Analog Devices, Inc.

Shaikh, Wasim and Srikanth Nittala. "AC and DC Data Acquisition Signal Chains Made Easy." *Analog Dialogue*, Vol. 54, No. 3, August 2020.

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Improving Power Supply Design Using Semi-Automation—Five Steps to Quick and Efficient Design

Frederik Dostal, Senior Staff Field Applications Engineer, Power Management

Introduction

Designing the correct power source is essential and complex, since there is no one typical application. While total automation of power supply design is yet to be achieved, a comprehensive range of semi-automated tools are available today. This article details the use of semi-automated design tools through five critical steps of the power supply design process. These tools can be valuable to both the novice and expert power supply design engineer.

Power Supply Design Step 1: Creating the Power Supply Architecture

Creating a suitable power supply architecture is a decisive step in power supply design. This step becomes more complex by increasing the number of needed voltage rails. At this point, the decision is made as to whether and how many intermediate circuit voltages need to be created. Figure 1 shows a typical block diagram of a power supply. The 24 V supply voltage of an industrial application is shown on the left. This voltage must be converted now into 5 V, 3.3 V, 1.8 V, 1.2 V, and 0.9 V with corresponding currents. What is the best method for generating the individual voltages? Selecting a classic step-down switching (buck) converter makes the most sense for converting from 24 V to 5 V. However, how do you generate the other voltages? Does it make sense to generate the 3.3 V from the 5 V already created, or should we convert to 3.3 V directly from 24 V? Answering these questions requires further analysis. Since an important property of a power supply is the conversion efficiency, keeping the efficiency as high as possible is important when selecting the architecture.

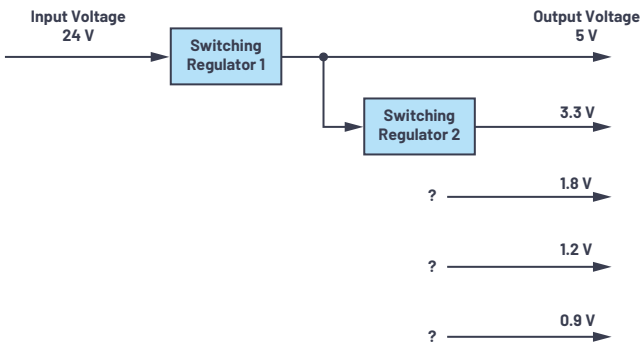

Figure 1. Creating a power supply architecture.

If intermediate voltages, such as 5 V in the example shown in Figure 1, are used to generate additional voltages, the energy used for the 3.3 V must already pass through two conversion stages. Each conversion stage has only limited efficiency. If, for example, a conversion efficiency of 90% is assumed for each conversion stage, the energy for 3.3 V, which has already passed through two conversion stages, only has an efficiency of 81% (0.9 × 0.9 = 0.81). Can this rather low efficiency be tolerated in a system or not? This depends on the current required from this 3.3 V rail. If current of only a few mA is needed, the low efficiency might not be a problem at all. For higher currents, however, this lower efficiency might have a greater effect on the overall system efficiency and consequently represent a big disadvantage.

From the considerations just mentioned, however, you cannot draw the general conclusion that it is always better to convert directly from a higher supply voltage to the lower output voltage in one step. Voltage converters that can handle a higher input voltage are usually more expensive and have a reduced efficiency when there is a greater difference between the input voltage and the output voltage.

In power supply design, the solution to finding the best architecture is to use an architecture tool such as LTpowerPlanner®. It is available free of charge from Analog Devices and is part of the LTpowerCAD® development environment, which can be installed locally on your computer. LTpowerPlanner is a tool that makes evaluating different architectures quick and easy.

Finalizing the Specification

Finalizing the specification is extremely important in power supply design. All additional development steps depend on the specification. Frequently, the precise requirements of the power supply are unknown until the rest of the electronic system has been completely designed. This usually results in increasing time constraints on power supply design development. It also often happens that the specification is changed in a later development stage. For example, if in its final programming, an FPGA requires additional power, the voltage for a DSP must be reduced to save energy, or the originally intended switching frequency of 1 MHz must be avoided because it is coupled into the signal path. Such changes can have very serious effects on the architecture and, in particular, on the circuit design of the power supply.

A specification is usually adopted at an early stage. This specification should be designed to be as flexible as possible so that it is relatively easy to implement any changes. In this effort, selecting versatile integrated circuits is helpful. Working with development tools is particularly valuable. This allows the power supply to be recalculated within a short time. In this way, specification changes can be implemented more easily and, above all, more quickly.

The specification includes the available energy, the input voltage, the maximum input current, and the voltages and currents to be generated. Other considerations include size, financial budget, thermal dissipation, EMC

requirements (including both conducted and radiated behaviors), expected load transients, changes in the supply voltage, and safety.

LTpowerPlanner as an Optimization Aid

LTpowerPlanner provides all the necessary functions for creating a power supply system architecture. It is very simple to operate, allowing for rapid concept development.

An input energy source is defined and then individual loads, or electrical consumers, are added. This is followed by adding individual dc-to-dc converter blocks. These could be switching regulators or low dropout (LDO) linear regulators. All components can be assigned their own name. An expected conversion efficiency is stored for efficiency calculations.

Using LTpowerPlanner has two great benefits. First, a simple architecture calculation can identify the configuration of the individual conversion stages most beneficial for overall efficiency. Figure 2 shows two different architectures for the same voltage rails. The architecture at the bottom has an overall efficiency that is somewhat higher than that of the architecture at the top. This property is not evident without a detailed calculation. When using LTpowerPlanner, this difference is immediately revealed.

The second benefit of LTpowerPlanner is that it provides well-organized documentation. The graphical user interface provides a neat sketch of the architecture, a visual aid that can be invaluable in discussions with coworkers and in documenting the development effort. Documentation can be stored either as a paper hard copy or a digital file.

Power Supply Design Step 2: Selecting Integrated Circuits for Each DC-to-DC Converter

When designing power supplies today, an integrated circuit is used rather than a discrete circuit with many separate components. There are a multitude of different switching regulator ICs and linear regulators available in the market. All of them are optimized for one specific property. Interestingly, all integrated circuits are different and can be interchanged only in the rarest of cases. Selecting the integrated circuit thus becomes a very important step. Once an integrated circuit has been selected, the properties of that circuit are fixed for the rest of the design process. Later, if it turns out that a different IC is better suited, the effort to incorporate a new IC begins again. This development effort can be very time consuming but can be easily mitigated with the use of design tools.

Using a tool is critical for effectively selecting the integrated circuit. The parametric search on analog.com is suitable for this. Searching for components within LTpowerCAD can be even more productive. Figure 3 shows the search window.

To use the search tool, only a few specifications need to be entered. For example, you may enter the input voltage, output voltage, and required load current. Based on these specifications, LTpowerCAD generates a list of recommended solutions. Additional criteria can be entered to further narrow down the search. For example, in the **Features** category you can select from features such as an enable pin or galvanic isolation to find an appropriate dc-to-dc converter.

Power Supply Design Step 3: Circuit Design of the Individual DC-to-DC Converters

Step 3 is the circuit design. The external, passive components need to be selected for the chosen switching regulator IC. The circuit is optimized in this step. Usually, this requires studying a data sheet thoroughly and performing all the required calculations. This step in power supply design can be drastically simplified by the comprehensive design tool, LTpowerCAD, and the results can be optimized further.

LTpowerCAD as a Powerful Calculation Tool

LTpowerCAD was developed by Analog Devices to greatly simplify circuit design. It is not a simulation tool, but rather a calculation tool. It recommends, in a very short time, the optimized external components based on the specification entered. The conversion efficiency can be optimized. The transfer function of the control loop is also calculated. This makes it easy to implement the best control bandwidth and stability.

After opening a switching regulator IC in LTpowerCAD, the main screen displays the typical circuit with all the necessary external components. Figure 4 shows this screen for the LTC3310S as an example. This is a step-down switching regulator with an output current of up to 10 A and a switching frequency of up to 5 MHz.

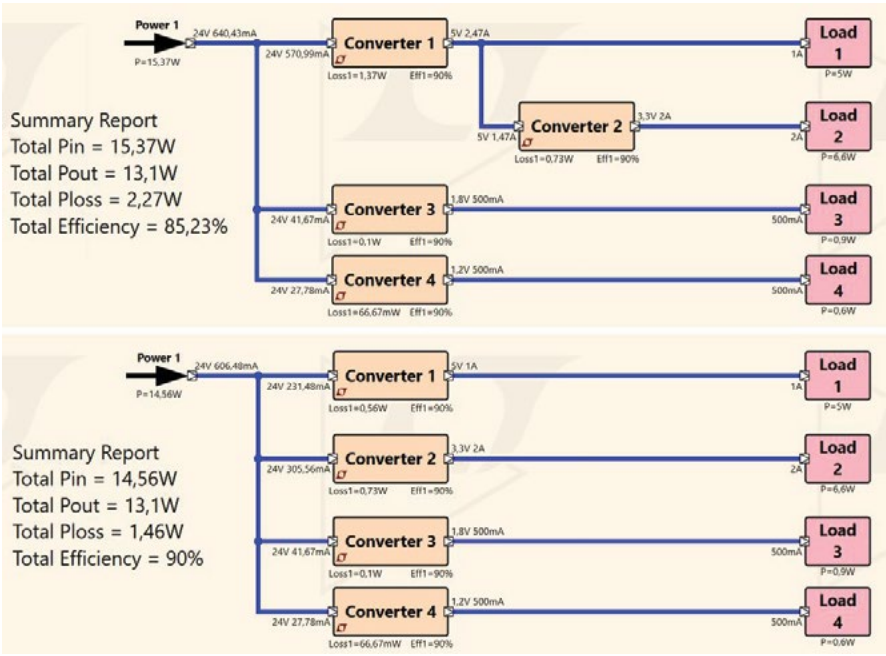

Figure 2. Two competing architectures with the efficiency calculation for each.

The yellow fields on the screen show the calculated or specified values. The user can configure settings using the blue fields.

Selecting the External Components

LTpowerCAD reliably simulates the behaviors of a real circuit as calculations are based on detailed models of external components, not just ideal values. LTpowerCAD includes a large database of integrated circuit models from several manufacturers. For instance, the equivalent series resistance (ESR) of a capacitor and the core losses of a coil are taken into consideration. To select external components, click on a blue external component as shown in Figure 4. A new window will open, showing a long list of possible components. As an example, Figure 5 shows a list of recommended output capacitors. This example shows a selection of 88 different capacitors from various manufacturers. You can also exit the list of recommended components and select the **Show All** option to choose from a variety of more than 4660 capacitors.

This list is continuously expanded and updated. While LTpowerCAD is an offline tool and does not require internet access, regular software updates (using the update function) will ensure that the integrated switching regulator ICs and the database of external components remain up to date.

Checking the Conversion Efficiency

Once the optimal external components have been selected, the conversion efficiency of the switching regulator is checked using the **Loss Estimate & Break Down** button.

A precise diagram of the efficiency and losses is then displayed. In addition, the junction temperature reached in the IC can be calculated based on the thermal resistance of the housing. Figure 6 shows the page of calculations for the conversion efficiency and thermal behavior.

Once you are satisfied with the circuit response, you can move to the next set of calculations. If the efficiency is not satisfactory, the switching frequency of the switching regulator can be changed (see left side of Figure 6), or the selection

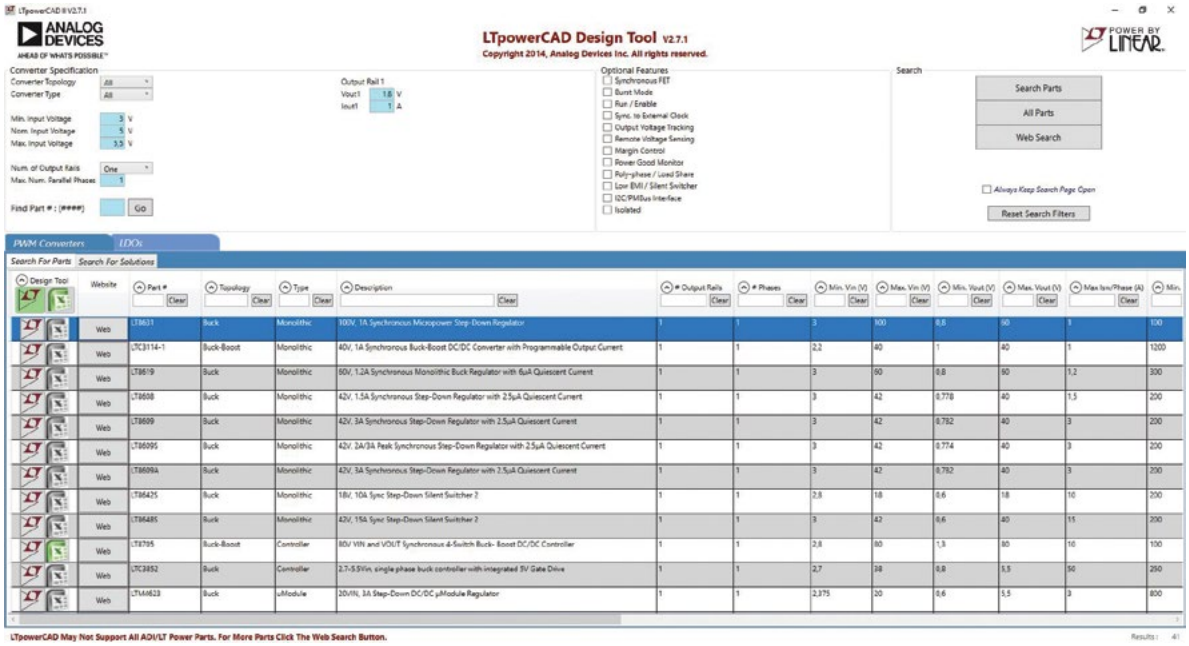

Figure 3. Searching for suitable switching regulator ICs with LTpowerCAD.

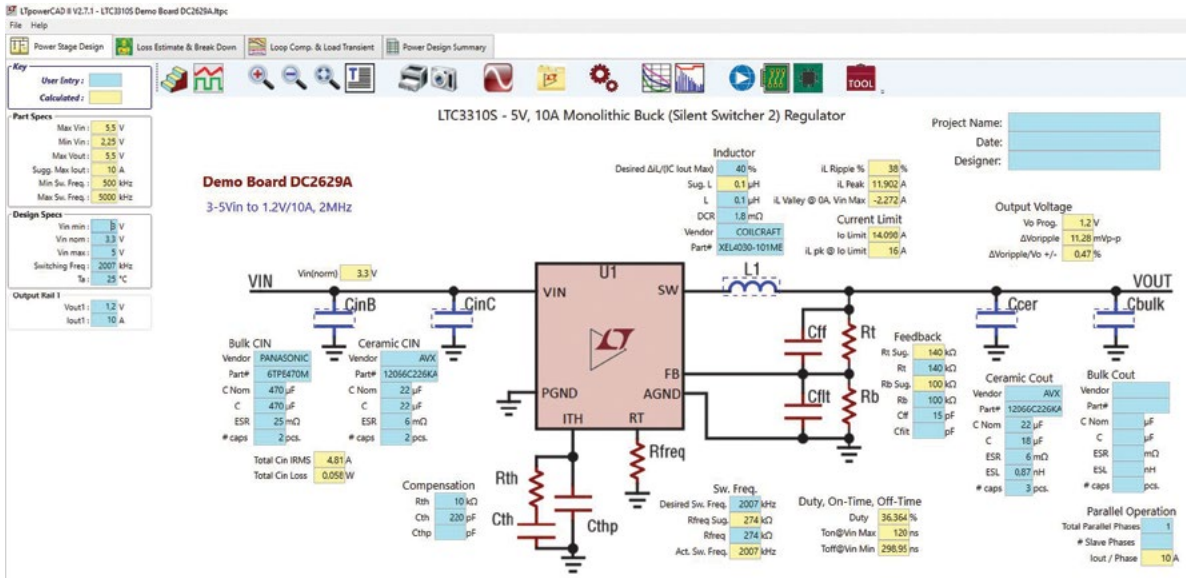

Figure 4. LTpowerCAD calculating tool for a power supply.

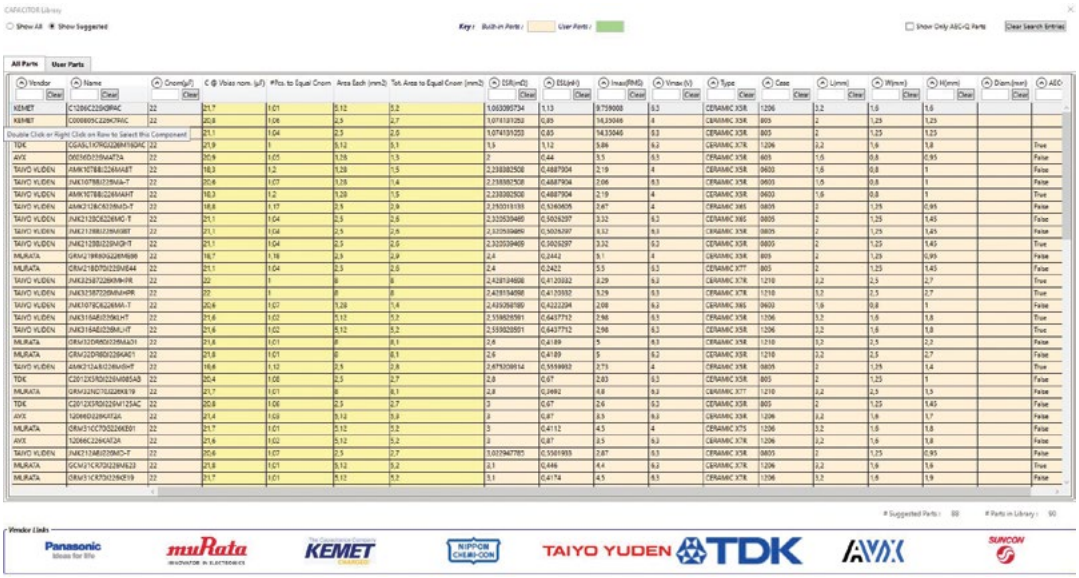

Figure 5. List box for different output capacitors for the LTC3310S.

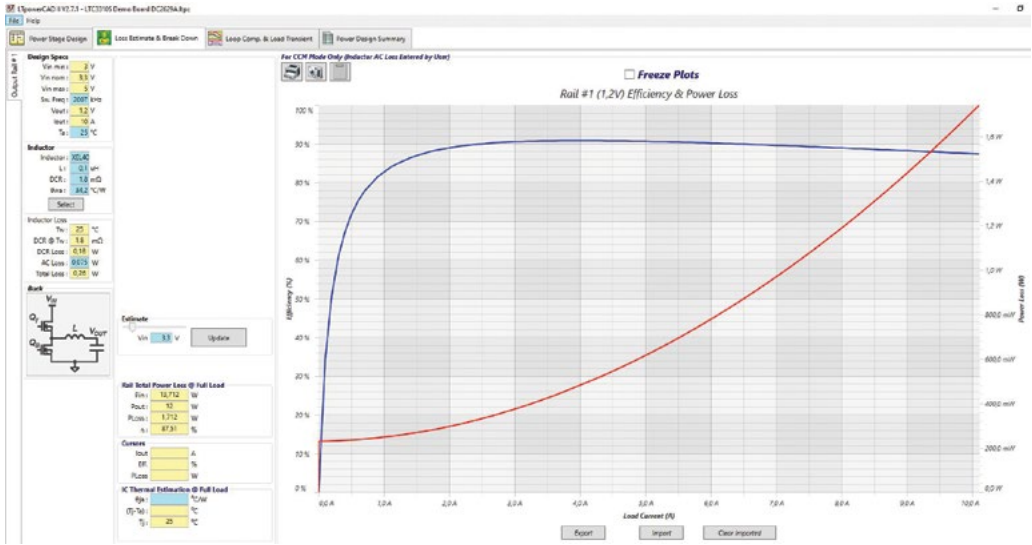

Figure 6. Efficiency calculation and thermal response of the circuit.

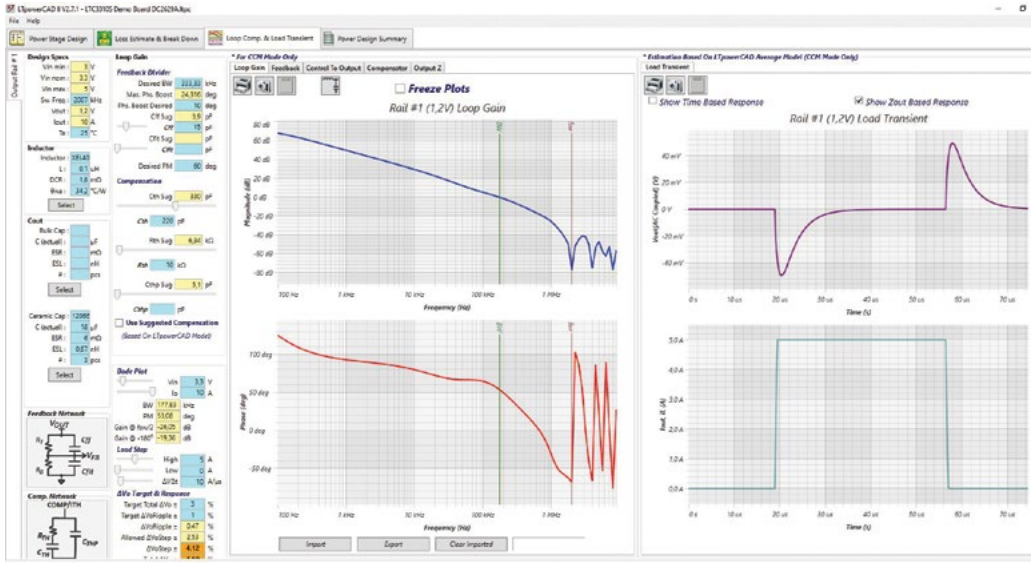

Figure 7. Setting the control loop with LTpowerCAD.

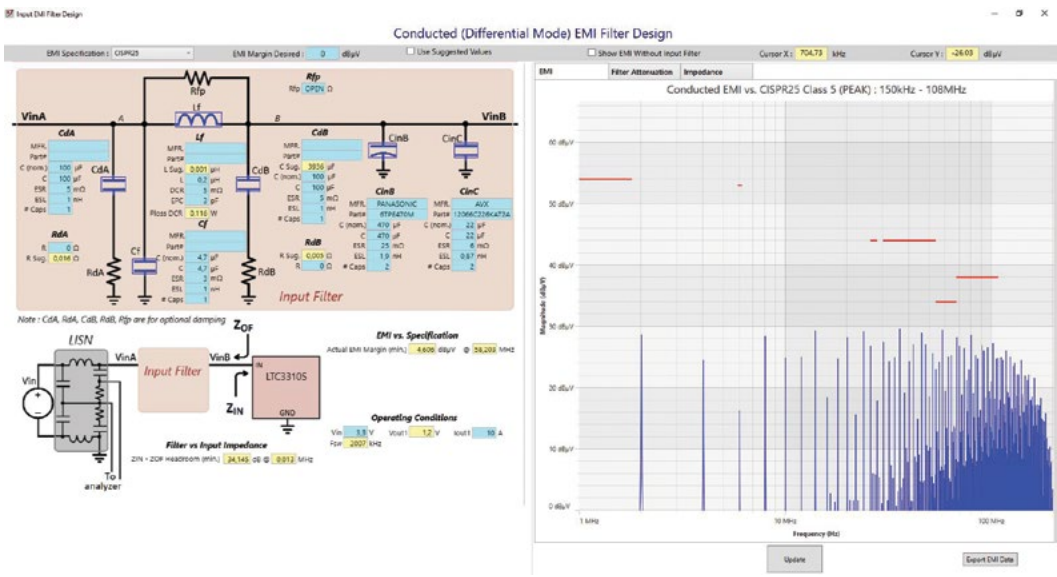

Figure 8. The filter designer in LTpowerCAD for minimizing conducted interference at the input of a switching regulator.

of the external coil can be changed. The efficiency is then recalculated until a satisfactory result is achieved.

Optimizing the Control Bandwidth and Checking the Stability

After selecting the external components and calculating the efficiency, the control loop is optimized. The loop must be set so that the circuit is reliably stable, not prone to oscillations or even instability while providing a high bandwidth—that is, the ability to respond to changes of the input voltage and, in particular, to load transients. The stability considerations in LTpowerCAD can be found in the **Loop Comp. & Load Transient** tab. In addition to a Bode plot and curves on the response of the output voltage following load transients, there are many setting options.

The **Use Suggested Compensation** button is the most important. In this case, the optimized compensation is used, and the user need not dive deeply into control engineering to adjust any parameters. Figure 7 shows the LTpowerCAD screen when setting the control loop.

The stability calculations performed in LTpowerCAD are a highlight of its architecture. The calculations are performed in the frequency domain and are very fast, much faster than simulations in the time domain. As a result, parameters can be changed on a trial basis and an updated Bode plot is provided in a few seconds. For a simulation in the time domain, this would take many minutes or even hours.

Checking the EMC Response and Adding Filters

Depending on the specification, additional filters may be necessary at the input or output of the switching regulator. This is where less experienced power supply developers, in particular, face large challenges. The following questions arise: How must the filter components be selected to ensure a certain voltage ripple at the output? Is an input filter necessary and, if so, how must this filter be designed to keep conducted emissions below certain EMC limits? In this respect, interaction between the filter and the switching regulator must not result in instability under any circumstances.

Figure 8 shows the Input EMI Filter Design, which is a sub-tool in LTpowerCAD. This can be accessed from the first page where the external, passive components are optimized. Starting the filter designer brings up a filter design using passive ICs and an EMC graph. This graph plots the conducted interference with or without an input filter and within appropriate limits from various EMC specifications such as CISPR 25, CISPR 22, or MIL-STD-461G.

The filter characteristic in the frequency domain and the filter impedance can also be displayed graphically beside the illustration of the input conducted EMC response. This is important to ensure that a filter does not have total harmonic distortion that is too high, and that the filter impedance matches the impedance of the switching regulator. Problems with the impedance match can lead to instabilities between the filter and the voltage converter.

Such detailed considerations can be accounted for in LTpowerCAD and do not require in-depth knowledge. With the **Use Suggested Values** button, the filter design is automated.

Of course, LTpowerCAD also supports the use of a filter on the output of the switching regulator. This filter is often used for applications where the output voltage is only allowed to have a very low output voltage ripple. To add a filter in the output voltage path, click the LC filter icon on the **Loop Comp. & Load Transient** page. Once this icon is clicked, a filter appears in a new window, as shown in Figure 9. The parameters of the filter can be easily selected here. The feedback loop can either be connected in front of this additional filter or behind it. Here, a stable response of the circuit can be ensured in all operating modes despite very good dc precision of the output voltage.

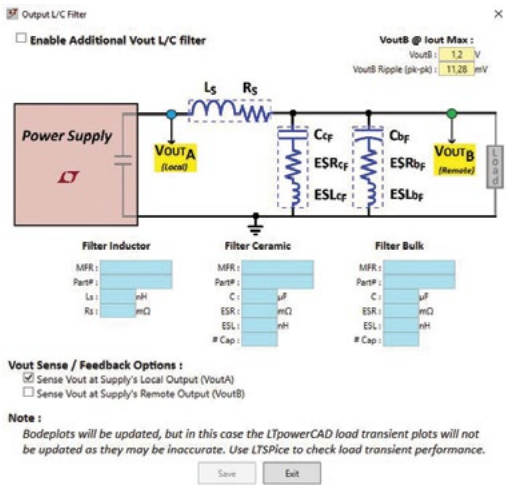

Figure 9. Selecting an LC filter at the output of a switching controller to reduce voltage ripple.

Power Supply Design Step 4: Simulation of the Circuit in the Time Domain

Once you have completely designed a circuit using LTpowerCAD, simulating it is the crowning achievement. Simulations are usually run in the time domain. Individual signals are checked against time. The interaction of different circuits can also be tested on a printed circuit board. It is also possible to integrate parasitic effects into the simulation. With this, the result of the simulation becomes very accurate, but the simulation times are longer.

Generally, a simulation is suitable for collecting additional information prior to implementing real hardware. It is important to know the potential and the limits of circuit simulation. Finding the optimal circuit might not be possible using simulation only. During simulation, one can modify parameters and restart the simulation. However, if the user is not an expert in designing circuits, it can be difficult to determine the right parameters and then to optimize them. As a result, it is not always clear to the user of a simulation whether the circuit has already achieved the optimal state. A computing tool such as LTpowerCAD is better suited for this purpose.

Simulating the Power Supply Using LTspice

LTspice®, from Analog Devices, is a powerful simulation program for electric circuits. It is very widely used by hardware developers globally, due to its ease of use, extended network of user support, optimization options, and high quality, reliable simulation results. Additionally, LTspice is free of charge and can easily be installed on a personal computer.

LTspice is based on the SPICE program, which originated from the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. The acronym SPICE stands for simulation program with integrated circuit emphasis. Many commercial versions of this program are available. Although originally based on Berkeley's SPICE, LTspice offers considerable improvements in the convergence of circuits and simulation speed. Additional features of LTspice include a circuit diagram editor and waveform viewer. Both are intuitive to operate, even for a beginner. These features also provide a great deal of flexibility for the experienced user.

LTspice is designed to be simple and easy to use. The program, available for download at analog.com, includes a very large database containing simulation models of nearly all power ICs from Analog Devices along with external passive components. As mentioned, once installed, LTspice can operate offline. However, regular updates will ensure that the newest models of switching regulators and external components are loaded.

To start an initial simulation, choose an LTspice circuit in the product folder of a power product on analog.com (for example, the LT8650S evaluation board). These are usually the suitable circuits of the available evaluation boards. By double-clicking the related LTspice link in a specific product folder on analog.com, LTspice will launch the complete circuit locally on your PC. It includes all external components and presets necessary to run a simulation. Then, click on the runner icon, pictured in Figure 10, to start simulation.

Following a simulation, all the voltages and currents of a circuit can be accessed using the waveform viewer. Figure 11 shows a typical illustration of the output voltage and the input voltage as the circuit ramps up.

A SPICE simulation is primarily suited for getting to know a power supply circuit in detail so that there are no unwanted surprises when building the hardware. A circuit can also be changed and optimized using LTspice. In addition, the interaction of the switching regulator with the other parts of the circuit on the printed circuit board can be simulated. This is particularly helpful in uncovering interdependencies. For example, several switching regulators can be simulated at the same time in one run. This extends the simulation time, but certain interactions can be checked in this case.

Finally, LTspice is an extremely powerful and reliable tool used by IC developers today. Many ICs from Analog Devices have been developed with the help of this tool.

Power Supply Design Step 5: Testing the Hardware

While automation tools have a valuable purpose in power supply design, the next step is to perform a basic hardware evaluation. The switching regulator operates with currents switched at a very high rate. Due to the parasitic effects of the circuit—particularly of the printed circuit board layout—these switched currents cause voltage offset, which generates radiation. Such effects can be simulated using LTspice. To do this, however, you need precise information about the parasitic properties. Most of the time this information is not available. You would have to make many assumptions, and these reduce the value of the simulation result. Consequently, a thorough hardware evaluation must be completed.

Printed Circuit Board Layout—An Important Component

The printed circuit board layout is usually known as a component. It is so critical that, for example, it is not possible to operate a switching regulator for test purposes using jumper wires, as it is with a breadboard. Mainly, the parasitic inductance in the paths where the currents are switched leads to a voltage offset that makes operation impossible. Some circuits could also be destroyed due to excessive voltage.

There is support available for creating an optimal printed circuit board layout. The corresponding data sheets for the switching regulator ICs usually provide information about a reference printed circuit board layout. For most applications, this suggested layout can be used.

Evaluating the Hardware Within the Specified Temperature Range

During the power supply design process, conversion efficiency is considered to determine whether the switching regulator IC operates within the permissible temperature range. However, testing the hardware at its intended temperature limits is important. The switching regulator IC and even the external components vary their rated values over the permissible temperature range. These temperature effects can easily be taken into consideration during the simulation using LTspice. However, such a simulation is only as good as the given parameters. If these parameters are available with realistic values, LTspice can perform a Monte Carlo analysis that leads to the desired result. In many cases, evaluating the hardware through physical testing is still more practical.

EMI and EMC Considerations

In late stages of system design, hardware must pass electromagnetic interference and compatibility (EMI and EMC) tests. While these tests must be passed with real hardware, simulation and calculation tools can be extremely useful in gathering insights. Different scenarios can be evaluated prior to hardware testing. Certainly, there are some parasitics involved that are usually not modeled in simulation, but general performance trends related to these test parameters can be obtained. Additionally, the data obtained from such simulations can provide the insights necessary to apply modifications to the hardware quickly, in case an initial EMC test was not passed. Since EMC tests are costly and time intensive, utilizing software such as LTspice or LTpowerCAD in early design stages can help achieve more accurate results prior to testing, thus speeding up the overall power supply design process and reducing costs.

Summary

The tools available for power supply design have become very sophisticated and powerful enough to meet the demands of complex systems. LTpowerCAD and LTspice are high performance tools with simple to use interfaces. As a result, these tools can be invaluable to a designer with any level of expertise. Anyone from the experienced developer to the less experienced can use these programs to develop power supplies on a day-to-day basis.

It is astounding how much simulation capabilities have evolved. Using the proper tools can help you build a reliable, sophisticated power supply more quickly than ever before.

The Free Power Tools from ADI

Follow these links:

- Optimization help LTpowerPlanner
- Calculation tool LTpowerCAD
- Simulation tool LTspice

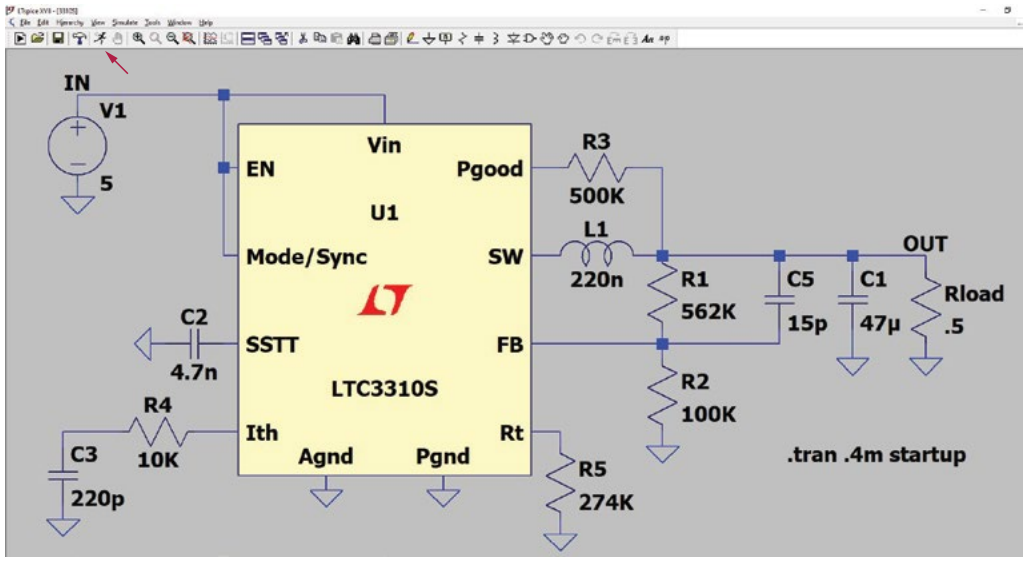

Figure 10. Simulation circuit of an LTC3310S using LTspice.

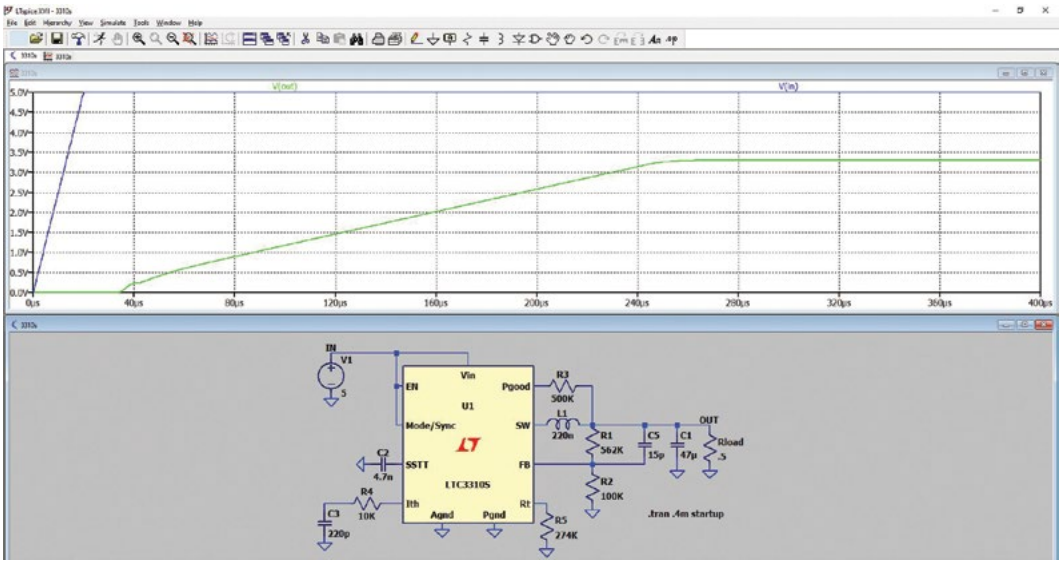

Figure 11. Simulation result of an LTC3310S circuit using LTspice.

About the Author

Frederik Dostal studied microelectronics at the University of Erlangen in Germany. Starting work in the power management business in 2001, he has been active in various applications positions including four years in Phoenix, Arizona, where he worked on switch-mode power supplies. He joined Analog Devices in 2009 and works as a field applications engineer for power management at Analog Devices in München. He can be reached at frederik.dostal@analog.com.

RAQ Issue 186: Adding a Flexible Current Limit

Frederik Dostal, Field Applications Engineer

Question:

Could I easily and precisely limit a current to my load?

Answer:

There are current limiting ICs available.

In some power management applications, precise current limiting is required. This is necessary either to protect the energy source, for example, if an intermediate circuit voltage requires overload protection so that it can reliably supply other system parts with energy, or to protect a load that can cause damage due to overcurrent in a fault condition.

In the search for a suitable dc-to-dc point of load regulator to meet this requirement, very few voltage converters with adjustable current limit are found on the market. While adjustable current limit is more often found on controller designs with external power switches, all integrated solutions seldomly offer such function. Also, adjustable current limits often do not have very high accuracy. In addition, the current limiters in dc-to-dc converter ICs usually only limit the inductor current and not the input or output current of the power supply. Such an integrated current limit is designed to protect "just" the switching regulator itself from destruction in a fault condition. The current limit lies above the nominally specified maximum output current and sometimes has a relatively low accuracy. This is adequate for protecting the switching regulator, but often not adequate for use as an adjustable current limiter.

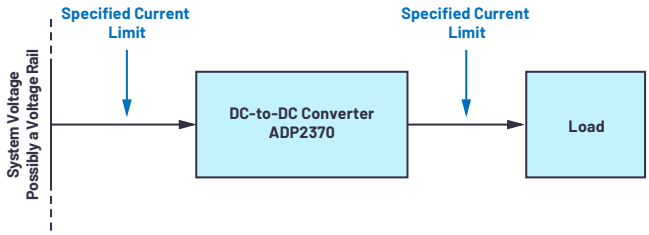

Figure 1. System in which the current flow to or from a switching regulator needs to be limited.

A flexible solution to this problem is to add an adjustable current limit via an additional component such as the LTC7003. Depending on the application, accuracies of approximately 15% can be achieved. The LTC7003 is a high-side N-channel MOSFET static switch driver. Through its adjustable current limit and its current monitoring function, it is ideal for adding current limiting to common dc-to-dc converters. Figure 2 shows the use of the LTC7003 current limiter for monitoring the output current of an ADP2370. The ADP2370 is a step-down dc-to-dc converter.

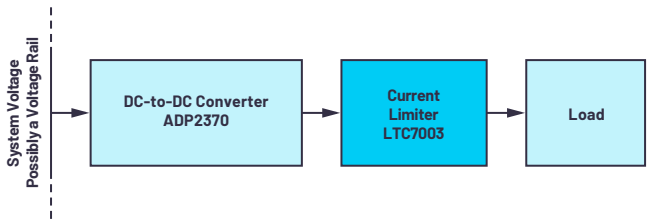

Figure 2. Current limiting added via an LTC7003 driver component.

In general, high-side current sense amplifiers can also be used for measuring a small voltage drop via a current sense resistor in the power path. They can measure currents with a very high accuracy. However, with the majority of them, the permissible voltage difference between the two current-sensing connections is very small. When such a general current sense amplifier is used in a power supply in which short circuits can occur due to the load, the voltage across the sense resistor can quickly go outside the permissible range. In this case, a solution such as the LTC7003, which is permitted for use in a power supply, is better. Here, the LTC7003 is designed in such a way that a large voltage difference is permitted at the SENS inputs. The LTC7003 also offers the

possibility of interrupting the power path through the optional N-channel MOSFET Q1 if the set current threshold is reached. Figure 3 shows an LTC7003 solution with an external N-channel MOSFET to interrupt the power path when a set current threshold is reached.

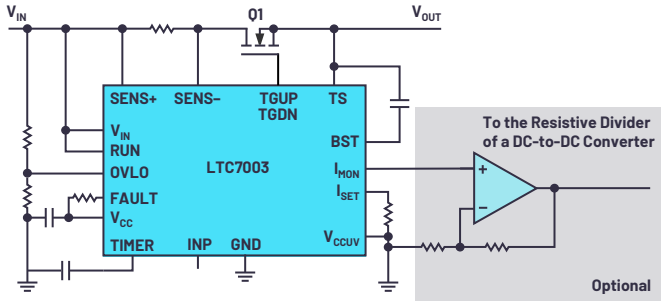

Figure 3. Circuit with the LTC7003 for limiting current.

Through the I_{MON} output, a voltage that is proportional to the current flow through the sense resistor is provided. This voltage is in respect to the system ground and corresponds to the voltage across the sense resistor multiplied by a factor of 20. The voltage lies between 0 V and 1.5 V. This voltage can be used with an additional external op amp to feed into the feedback circuit of a switching regulator. In this way, the output voltage of the dc-to-dc converter can be reduced in proportion to the current level sensed by the LTC7003. This option is shown in Figure 3 in a grayed-out circuit.

With its interesting functions, the LTC7003 is suitable for monitoring, limiting, and disconnecting supply lines in numerous different systems.

About the Author

Frederik Dostal studied microelectronics at the University of Erlangen in Germany. Starting work in the power management business in 2001, he has been active in various applications positions including four years in Phoenix, Arizona, where he worked on switch-mode power supplies. He joined Analog Devices in 2009 and works as a field applications engineer for power management at Analog Devices in München. He can be reached at frederik.dostal@analog.com.

Adding Hysteresis for Smooth Undervoltage and Overvoltage Lockout

Pinkesh Sachdev, Senior Applications Engineer

Resistive dividers attenuate high voltages down to a level that low voltage circuits can accommodate without getting overdriven or damaged. In power path control circuits, resistive dividers help set up power supply undervoltage and overvoltage lockout thresholds. Such supply voltage qualification circuits are found in automotive systems, battery-powered portable instruments, and data processing and communication boards.

Undervoltage lockout (UVLO) prevents the downstream electronic system from operating with abnormally low power supply voltages, which could cause system malfunction. For example, digital systems can behave erratically or even freeze up when their supply voltage is below specification. When the power supply is a rechargeable battery, undervoltage lockout prevents battery damage due to deep discharge. Overvoltage lockout (OVLO) protects the system from damagingly high supply voltages. Since undervoltage and overvoltage thresholds depend on the system's valid operating range, resistive dividers are used to set up custom thresholds with the same control circuit. Threshold hysteresis is needed to obtain a smooth and chatter-free lockout function even in the presence of supply noise or resistance. After discussing a simple UVLO/OVLO circuit, this article will present some simple methods for adding threshold hysteresis, which is necessary when the default value is insufficient.

Undervoltage and Overvoltage Lockout Circuit

Figure 1 shows an undervoltage lockout circuit (without hysteresis for now). It has a comparator with a positive reference voltage (V_T) at its negative input. The comparator controls a power switch that opens or closes the path between the power supply input and the downstream electronic system. The comparator's positive input connects to a resistive divider from the input. If the supply is turned on and starts rising from 0 V, the comparator output is initially low, keeping the power switch off. The comparator output trips when its positive input reaches V_T. At this moment, the current in the bottom resistor is V_T/R_B. The same current flows in R_T if the comparator has no input bias current. Therefore, the supply voltage when the comparator trips is $V_T + R_T \times V_T/R_B = V_T \times (R_B + R_T)/R_B$. This is the supply UVLO threshold set up by the resistive divider. For example, a V_T of 1 V and $R_T = 10 \times R_B$ yields a UVLO threshold of 11 V. Below this threshold, the comparator output is low, opening the power switch; above this UVLO threshold, the switch is closed and the supply flows through to power up the system. The threshold can be easily adjusted by changing the ratio of R_B and R_T. The absolute resistor value is set by the amount of bias current budgeted for the divider (more on this later). To set up an OVLO threshold, just swap the two inputs of the comparator (for example, see the lower comparator in Figure 2) such that a high going input forces the comparator output low and opens the switch.

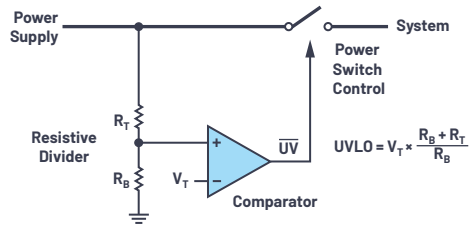

Figure 1. Power supply undervoltage lockout using a resistive divider, comparator, and power switch.

While not the focus of this article, the switch can be implemented with an N-channel or a P-channel power MOSFET. The previous discussion assumes an N-channel MOSFET switch that opens (high resistance) when its gate voltage is low (for example, 0 V). To completely close (low resistance) an N-channel MOSFET, the gate voltage must be higher than the supply by at least the MOSFET threshold voltage, requiring a charge pump. Protection controllers such as LTC4365, LTC4367, and LTC4368 integrate comparators and charge pumps to drive N-channel MOSFETs while still consuming low quiescent current. P-channel MOSFETs don't require a charge pump but the gate voltage polarity is reversed; that is, a low voltage closes whereas a high voltage opens a P-channel MOSFET switch.

Getting back to resistive dividers: a 3-resistor string sets up both undervoltage and overvoltage lockout thresholds (Figure 2), saving one divider's bias current vs. using two separate 2-resistor strings. The UVLO threshold is $V_T \times (R_B + R_M + R_T)/(R_B + R_M)$ while the OVLO threshold is $V_T \times (R_B + R_M + R_T)/R_B$. An AND gate combines the output of the two comparators before sending it to the power switch. Therefore, the power switch closes to power the system when the input voltage is between the undervoltage and overvoltage thresholds; otherwise, the switch is open, disconnecting the supply from the system. If divider current consumption is not a concern, separate undervoltage and overvoltage dividers provide more flexibility in adjusting each threshold independently of the other.

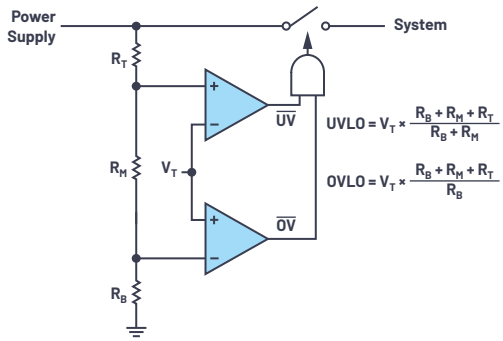

Figure 2. Undervoltage and overvoltage lockout using a single resistive divider.

Undervoltage and Overvoltage Lockout with Hysteresis

In Figure 1, if the power supply rises slowly and has noise or if the supply has inherent resistance (as in a battery) that causes the voltage to drop with load current, the output of the comparator will switch high and low repeatedly as the input crosses its UVLO threshold. This is because the comparator's positive input repeatedly goes above and below the V_T threshold due to the input noise or the drop due to load current through the supply resistance. For battery-powered circuits, this can be a never-ending oscillation. Using a comparator with hysteresis eliminates this chatter, making the switch transition smoother. As illustrated in Figure 3, a hysteretic comparator presents different thresholds for a rising (for example, V_T + 100 mV) vs. a falling input (for example, V_T – 100 mV). The hysteresis at the comparator level is scaled up by R_B and R_T to 200 mV × $(R_B + R_T)/R_B$ at the supply level. If the noise or the drop at the supply input is below this hysteresis, the chatter is eliminated. There are ways to add or increase hysteresis if that provided by the comparator is either absent or insufficient. All these methods use positive feedback at the divider tap—for example, a rising comparator input jumps higher when the comparator trips. For simplicity, the following equations assume no intrinsic hysteresis in the comparator.

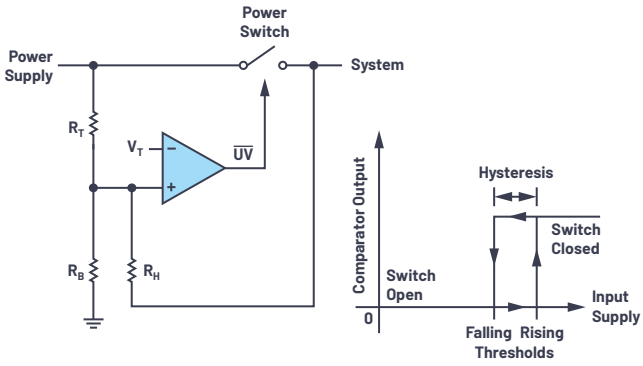

Figure 3. Adding undervoltage lockout threshold hysteresis with a resistor from the divider tap to the power switch output.

Resistor from Divider to Output (Figure 3):

Add a resistor (R_H) from the divider tap (the comparator's positive input) to the power switch output. When the supply starts rising from 0 V, the comparator's positive input is below V_T and the comparator output is low, keeping the power switch off. Assume that the switch output is at 0 V due to the system load. Hence, R_H is in parallel with R_B for input threshold calculation. The rising input undervoltage threshold is $V_T \times ((R_B \parallel R_H) + R_T)/(R_B \parallel R_H)$, where $R_B \parallel R_H = R_B \times R_H/(R_B + R_H)$. The switch turns on above this threshold, connecting the supply to the system. To calculate the falling input undervoltage threshold, R_H is in parallel with R_T since the switch is closed, giving the falling input undervoltage threshold as: $V_T \times (R_B + (R_T \parallel R_H))/R_B$, where $R_T \parallel R_H = R_T \times R_H/(R_T + R_H)$. If the comparator itself had some hysteresis, substitute V_T with the rising or falling comparator threshold in the previous equations. Recall the Figure 1 example, with V_T = 1 V and $R_T = 10 \times R_B$, where both the rising and falling thresholds are 11 V in the absence of comparator hysteresis or R_H. Adding an $R_H = 100 \times R_B$, as in Figure 3, gives a rising input threshold of 11.1 V and a falling threshold of 10.09 V; that is, a hysteresis of 1.01 V. This method does not work for OVLO because a rising input turns off the power switch, causing R_H to pull the comparator input lower (which turns on the switch again) instead of higher.

Switching in a Resistor (Figure 4):

Another method of adding hysteresis is to switch in a resistor that changes the effective value of the bottom resistor. The switched resistor can be in parallel (Figure 4a) or in series (Figure 4b). Consider Figure 4a: when V_{IN} is low—say, 0 V—the comparator's output (UV or $\overline{OV}$ node) is high, turning on the N-channel MOSFET M1 and connecting R_H in parallel with R_B. Assume that M1's on-resistance is either negligible compared to R_H or is included in R_H's value. The rising input threshold is the same as in Figure 3: $V_T \times ((R_B \parallel R_H) + R_T)/(R_B \parallel R_H)$. Once V_{IN} is above this threshold, the comparator output is low, turning off M1 and disconnecting R_H from the divider. Therefore, the falling input threshold is the same as in Figure 1: $V_T \times (R_B + R_T)/R_B$. Continuing our example with V_T = 1 V, $R_T = 10 \times R_B$, and $R_H = 100 \times R_B$, the rising input threshold is 11.1 V and the falling threshold is 11 V; that is, R_H yields a hysteresis of 100 mV. This and the following methods can be used for either undervoltage or overvoltage lockout as their purpose depends on how the comparator output turns on the power switch (not shown).

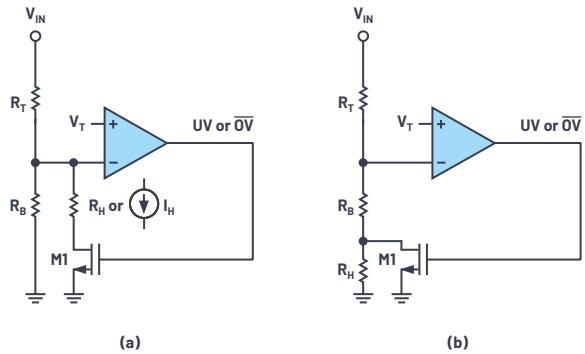

Figure 4. Adding undervoltage or overvoltage lockout threshold hysteresis with a switched (a) shunt resistor or current and (b) a series resistor.

The configuration of Figure 4b gives the rising input threshold as $V_T \times (R_B + R_T)/R_B$ and the falling input threshold as $V_T \times (R_B + R_H + R_T)/(R_B + R_H)$. $R_H = R_B/10$ in Figure 4, giving 11 V as the rising input threshold and 10.091 V as the falling threshold—that is, 909 mV of hysteresis. This shows that the Figure 4b configuration needs a much smaller R_H to yield a much larger hysteresis.

Switching in a Current (Figure 4a):

The resistor R_H of Figure 4a can be replaced by a current source I_H. This method is used in the LTC4417 and LTC4418 prioritized controllers. When V_{IN} is low, the comparator's high output enables I_H. At the rising input threshold, the negative input of the comparator is at V_T. Therefore, the current in R_T is $I_H + V_T/R_B$, yielding the rising threshold as $V_T + (I_H + V_T/R_B) \times R_T = V_T \times (R_B + R_T)/R_B + I_H \times R_T$. Once V_{IN} is above this threshold, I_H is turned off by the comparator's low output. Therefore, the falling threshold is the same as in Figure 1: $V_T \times (R_B + R_T)/R_B$, and the input threshold hysteresis is $I_H \times R_T$.

Resistive Divider Bias Current

The previous equations have assumed that the input bias current of the comparator input is zero while the examples have only considered resistor ratios instead of absolute values. Comparator inputs have both input offset voltage (V_{OS}), reference inaccuracy (which can be clubbed with V_{OS}), and input bias or leakage current (I_{LK}). The zero leakage assumption works out if the divider bias current, V_T/R_B at Figure 1's trip point, is much larger than the input leakage. For instance, a divider current that is 100 times the input leakage current keeps leakage-caused input threshold error below 1%. Another method is to compare the leakage induced threshold error to that from the offset voltage. The comparator nonidealities change the Figure 1 input undervoltage threshold equation to be: $(V_T \pm V_{OS}) \times (R_B + R_T)/R_B \pm I_{LK} \times R_T$ (similar to the previous hysteretic current equation), which can be rewritten as $(V_T \pm V_{OS} \pm I_{LK} \times R_B \times R_T/(R_B + R_T)) \times (R_B + R_T)/R_B$. The input leakage shows up as an error in the comparator's threshold voltage and this error can be minimized in relation to the offset voltage—that is, $I_{LK} \times (R_B \parallel R_T) < V_{OS}$, by proper resistor selection.

As an example, the LTC4367 undervoltage and overvoltage protection controller has ±10 nA maximum leakage for the UV and OV pins while the UV/OV pin comparator's 500 mV threshold offset voltage is ±7.5 mV (±1.5% of 500 mV). Budgeting a ±3 mV (±0.6% of 500 mV, or less than half of the 7.5 mV offset) leakage caused threshold error gives $R_B \parallel R_T < 3$ mV/10 nA = 300 kΩ. To set up an 11 V input undervoltage threshold with a 0.5 V comparator threshold requires $R_T = R_B \times 10.5$ V/0.5 V = 21 × R_B. Therefore, $R_B \parallel R_T = 21 \times R_B/22 < 300$ kΩ, giving $R_B < 315.7$ kΩ. The nearest 1% standard value for R_B is 309 kΩ, yielding R_T to be 6.49 MΩ. The divider bias current at the trip point is 0.5 V/309 kΩ = 1.62 µA, which is 162 times the 10 nA leakage current. This kind of analysis is important when minimizing the divider current without increasing the threshold error due to the comparator's input leakage current.

Conclusion

Resistive dividers enable easy adjustment of power supply undervoltage and overvoltage lockout thresholds with the same comparator-based control circuit. Supply noise or resistance requires threshold hysteresis to prevent power switch on and off chattering as the supply crosses the threshold. A few different methods for implementing undervoltage and overvoltage lockout hysteresis have been shown. The essential principle is to have some positive feedback at the divider tap when the comparator trips. When adding or increasing hysteresis of protection controller ICs, some methods depend on the availability of the comparator output or a similar signal at the IC output pins. While picking resistor values, care should be taken that the comparator's input leakage doesn't become a dominant source of threshold error. A comprehensive set of related equations, including those in this article, have been implemented in a spreadsheet that's available to download.

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CTSD Precision ADCs—Part 2: CTSD Architecture Explained for Signal Chain Designers

Abhilasha Kawle, Analog Design Manager

This article will explain continuous-time sigma-delta (CTSD) ADC technology in a less traditional approach, enabling signal chain designers to envision a new class of easy to use precision ADC technology as a simple system that interconnects a few well-known components. In Part 1, we highlighted the key challenges of incumbent signal chain designs that can be simplified significantly with a precision CTSD ADC, as it maintains continuous-time signal integrity while achieving the highest precision. Now, the question is what's behind the CTSD architecture that enables it to achieve these advantages?

The traditional approach of explaining the concept of CTSD technology is by first understanding the basics of a discrete-time sigma-delta (DTSD) modulator loop and then substituting the discrete-time loop elements with equivalent continuous-time elements. While this method gives an in-depth understanding of sigma-delta functionality, we aim to provide a more intuitive understanding behind the inherent advantages of precision CTSD ADCs. To begin, we will outline a step-by-step approach to building a CTSD modulator loop starting with the widely known closed-loop inverting amplifier configuration and combining it with an ADC and a DAC. Finally, we will evaluate the basic sigma-delta functionality from the circuit we build.

Step 1: Revisiting the Closed-Loop Inverting Amplifier Configuration

One of the key advantages of the CTSD ADC is that it offers an easy to drive continuous resistive input rather than a traditional switched capacitor sampler upfront. One of the circuits that has a similar input impedance concept is the inverting amplifier, which we will use as a starting block toward building a CTSD modulator loop.

A closed-loop op amp configuration has always been the go-to option for replicating an analog input with high fidelity, and Figure 1 shows one of the most popular op amp configurations, which is called an inverting amplifier configuration.[1] One of the measures of the fidelity is the output to input gain, also known as, in sigma-delta nomenclature, the signal transfer function (STF). Determining the parameters that affect the STF requires analyzing the circuit.

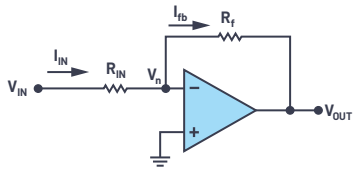


Figure 1. A closed-loop op amp in inverting amplifier configuration.

To refresh our mathematical skills, let's revisit the derivation of famous V_{OUT}/V_{IN}. In the first step, the open-loop gain of the op amp A is assumed to be infinite. This assumption directly leads to making negative input of op amp, V_n at potential ground. The application of Kirchhoff's laws at this node gives

$$I_{IN} = \frac{V_{IN}}{R_{IN}},\ I_{fb} = -\frac{V_{OUT}}{R_f} \tag{1}$$

Mapping this to V_{OUT} and V_{IN}, we get the gain or STF as

$$STF = \frac{V_{OUT}}{V_{IN}} = -\frac{R_f}{R_{IN}} \tag{2}$$

Next let's go beyond the impractical assumption of infinite gain and rederive the STF with the finite gain of A for the op amp. The STF now looks like

$$STF = -\frac{R_f}{R_{IN}} \times \left(\frac{A}{\left(1 + \frac{R_f}{R_{IN}}\right) + A} \right) \tag{3}$$

From here, textbooks generally describe the sensitivity toward each of the parameters R_{IN}, R_f, and A. For our case, lets proceed toward building the CTSD loop.

Step 2: Introducing Discretization into the Amplifier

The requirement for our ADC signal chain is a digitized version of V_{IN}. In our next step, we introduce the digitization in this circuit. Rather than use the traditional way of putting a sampling ADC directly at the input signal, we will try a different approach and put a representative ADC that follows the amplifier output to get the digitized data. But the output of the ADC cannot be used as feedback directly, as it is required to be an analog voltage. So then, we need to follow up the ADC with a voltage digital-to-analog converter (DAC) as shown in Figure 2.

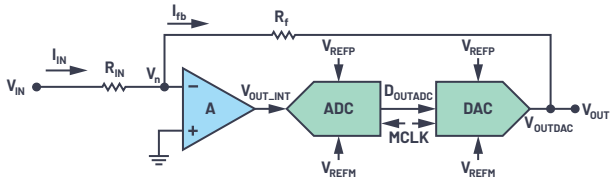


Figure 2. Introducing an ADC and DAC in an inverting amplifier configuration.

Because of the ADC and DAC, V_{OUT} is still a representation of V_{IN} but with quantization error due to the digitization added. So, nothing has changed in the signal flow from V_{IN} to V_{OUT}. One point of note here, to keep the functionality of loop symmetric about 0 V and ease our mathematical derivation, the references of ADC and DAC are chosen to be

$$V_{REFP} = V_{REF}/2, \text{ and } V_{REFM} = -V_{REF}/2 \quad (4)$$

Step 3: Introducing the Analog Accumulator–The Integrator

Is the closed-loop configuration in Figure 2 stable? Both the ADC and DAC are discretization elements working on a sampling clock, MCLK. It has been an unachievable dream of converter specialists to design a delay free ADC or DAC. Since these loop elements are clocked, the input is generally sampled on one edge and processed on the other clock edge. So, the output of the ADC and DAC combination V_{OUT}, which is the feedback in Figure 2, is available only after 1 clock cycle delay.

Does this delay in feedback have any implication on stability? Let's trace how V_{IN} transfers along. For simplification let's assume V_{IN} = 1, R_{IN} = 1, R_f = 1, and the gain of op amp A is 100. At the first clock cycle, the input voltage is 1 and the DAC output feedback, V_{OUT} or V_{OUTDAC}, is 0 and is not available until the next clock edge. As we trace the error between the input and feedback to the output of the amplifier and ADC, we can see the output keeps growing exponentially and this is technically termed as the runaway problem.

Table 1. Clock Edge Samples

	V_{IN}	V_{OUT} = V_{OUTDAC}	V_n = $(V_{OUT} + V_{IN})/2$	V_{OUT_INT} = $-A \times (V_n)$	D_{OUTADC}
First Sample Edge	1	0	0.5	–50	–50
Second Sample Edge	1	–50	~–25	~2500	2500
Third Sample Edge	1	2500	~1250	~–12,500	–12,500

This happened because the ADC input works on instantaneous error gained up by the amplifier; that is, the ADC decides even before the feedback is available, which was not required. If the ADC works on an accumulated, averaged error data so that the error due to 1 clock delay of feedback is averaged out, then the output of system would be bounded.

The integrator is one such analog equivalent of an averaging accumulator. The gain of the loop is still high but only at low frequencies or, in other words, in the frequency bandwidth of interest. This ensures that the ADC is not presented with any instantaneous errors that can lead to a runaway situation. So, the loop is now amplifier modified as an integrator followed by the ADC and DAC, as shown in Figure 3a.

Step 4: Simplifying the Feedback Resistor

Our element of interest is D_{OUTADC}, so let's rearrange the loop elements to highlight D_{OUTADC} as the output of the system, as shown in Figure 3b. Next, let's visit the simplification of the DAC and R_f path. And for that let's dig into the DAC's details. The purpose of the DAC is to convert a digital code, D_{IN}, to an equivalent analog current or voltage in proportion to the reference. To further extend the advantages of continuity to reference, what we have considered here is a general DAC architecture based on a resistor ladder that has no switching load on reference. Let's review a thermometric resistor DAC,[2] which converts D_{IN} to the DAC current, with relation to Equation 5.

$$I_{DAC} = \frac{V_{REF}}{R_f} \times \frac{D_{IN}}{2^N} \quad (5)$$

Where $V_{REF} = V_{REFP} - V_{REFM}$, the total reference voltage across the DAC.

- D_{IN} = Digital input in the thermometric code
- R_f = Feedback resistor; split as each unit element
- N = Number of bits

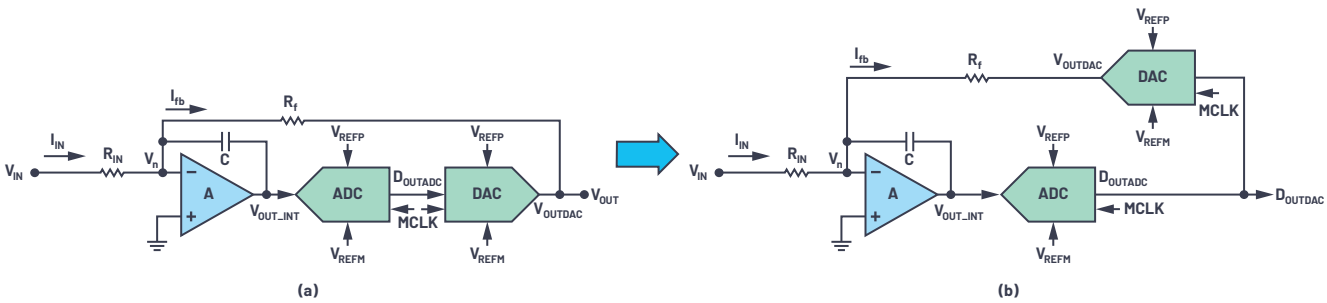


Figure 3. (a) Introducing the integrator into the loop. (b) Rearranging the loop to highlight D_{OUTADC} as output.

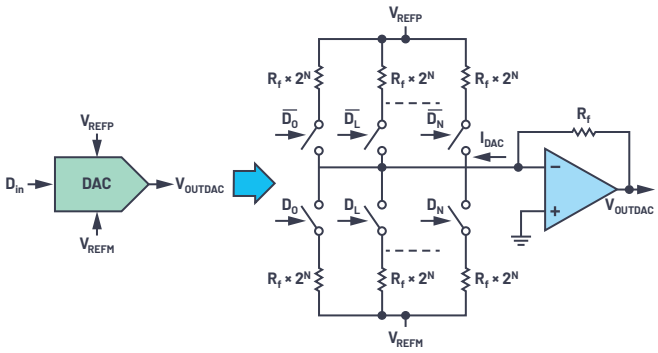


Figure 4. A general thermometric resistive DAC.

To get the voltage output, an *I* to *V* conversion follows by using an op amp in a transimpedance configuration,[3] as shown in Figure 4. So,

$$V_{OUTDAC} = I_{DAC} \times R_f \quad (6)$$

Going back to our discretized loop of Figure 3b, this V_{OUTDAC} is again converted back to current, I_{fb}, through the feedback resistor of the inverting amplifier, implying the signal flow is $I_{DAC} \rightarrow V_{OUTDAC} \rightarrow I_{fb}$. Mathematically,

$$I_{fb} = \frac{V_{OUTDAC}}{R_f} = I_{DAC} \quad (7)$$

From the above signal flow and formula, we see that converting V_{OUTDAC} to I_{fb} is a redundant step that can be bypassed. Removing the redundant elements and, for simplicity, representing (V_{REFP} – V_{REFM}) as V_{REF}, let's redraw our loop, as shown in Figure 5.

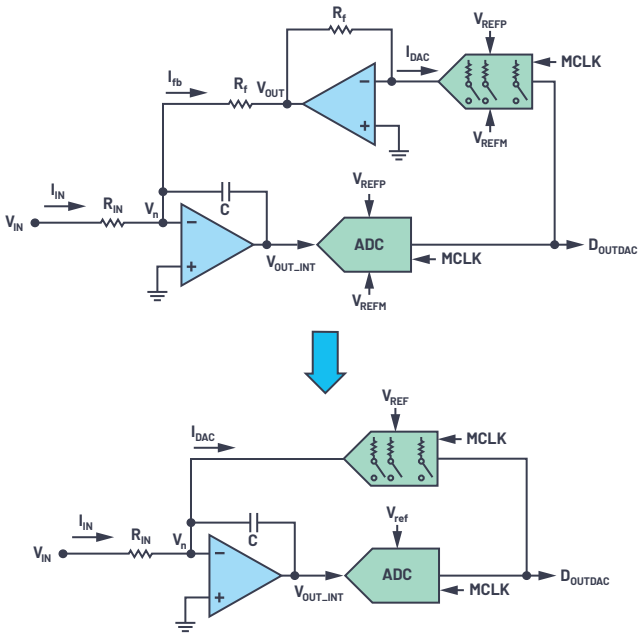


Figure 5. Removing redundant I to V and the feedback resistor.

And voila! We have built a first-order sigma-delta loop! And all by stitching together well-known elements—an inverting amplifier, an ADC, and a DAC.

Step 5: Understanding Oversampling

We have up to now grasped the construction of a CTSD loop, but we have yet to appreciate the particularities offered by this fanciful loop. The first step toward that is understanding oversampling. ADC data is useful only if there are enough sampled and digitized data points to extract or interpret the analog signal information. The Nyquist theorem advises that, for faithful reconstruction of an input signal, the sampling frequency of the ADC should be at least twice the frequency of the signal. If we keep adding more data points over this minimum requirement, the error in interpretation would be further reduced. Following this line of thought, in sigma-delta the sampling frequency is selected to be much higher than the suggested Nyquist frequency and this is known as oversampling. Oversampling[4] helps reduce the quantization noise in the frequency band of interest by spreading the total noise over much higher frequency, as shown in Figure 6.

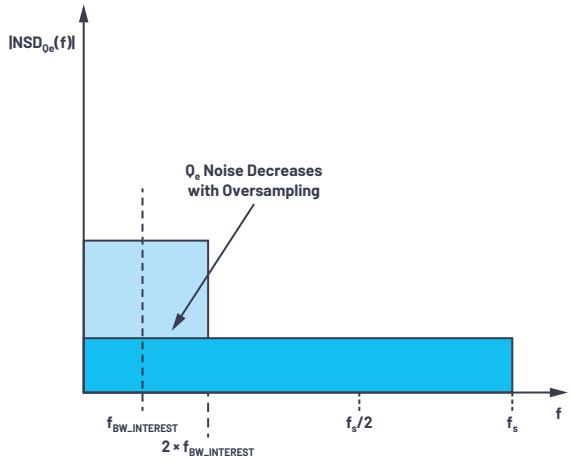


Figure 6. A noise spectral density comparison between Nyquist sampling and oversampling.

Step 6: Understanding Noise Shaping

Signal chain designers shouldn't feel lost when sigma-delta experts use terms like noise transfer function (NTF) or noise shaping,[4] and our next step will help them get an intuitive understanding of these terms as they are unique to sigma-delta converter nomenclature. Let's revisit our simple inverting amplifier configuration and introduce the error 0_e at the output of the amplifier, as shown in Figure 7.

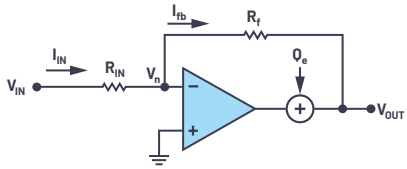


Figure 7. The introduction of an error in an inverting amplifier configuration.

The contribution of this error at the output is quantified as

$$V_{OUT} = \frac{Q_e}{\left(1 + \frac{A}{\left(1 + \frac{R_f}{R_{IN}}\right)}\right)} \quad (8)$$

The mathematical formula translates that the error Q_e is attenuated by the open-loop gain of the amplifier, which is just reiterating the advantage of a closed loop.

This understanding of the closed-loop advantage can be extended to quantization error Q_e of the ADC in CTSD loop, which is the error introduced due to digitization of the continuous signal at the output of the integrator, as shown in Figure 8.

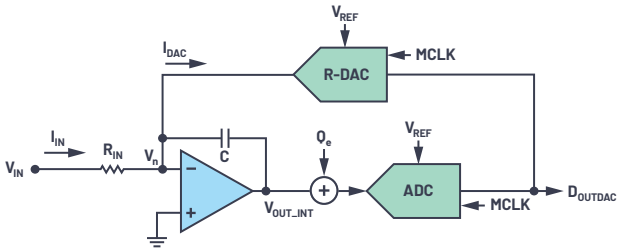


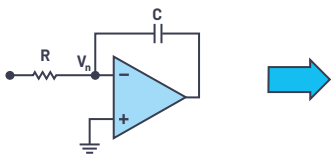
Figure 8. The introduction of quantization error Q_e in a sigma-delta loop.

We can now intuitively conclude that this Q_e would be attenuated by the integrator. The integrator TF is $|H_{INTEG}(f)| = 1/|s \times RC| = 1/2\pi fRC$ and its corresponding frequency domain representation is shown in Figure 9. Its profile is equivalent to a low-pass filter profile with high gain at low frequencies, and the gain reduces linearly as frequency increases. Correspondingly, the attenuation for Q_e would then look like a high-pass filter.

The mathematical representation of this attenuation factor is the noise transfer function. For an interim, let's ignore the sampler in the ADC and the switches in the DAC. The NTF, V_{OUTADC}/Q_e, can be evaluated by following the same exercise as we did for the inverting amplifier configuration, which in the frequency domain looks like a high-pass filter profile, as shown in Figure 10.

$$NTF\_int = \frac{V_{OUTADC}}{Q_e} = \frac{sR_fC}{(1 + sR_fC)} \quad (9)$$

In the frequency band of interest, the quantization noise is completely attenuated and pushed to "not to our concern" high frequencies. This is what is called noise shaping.



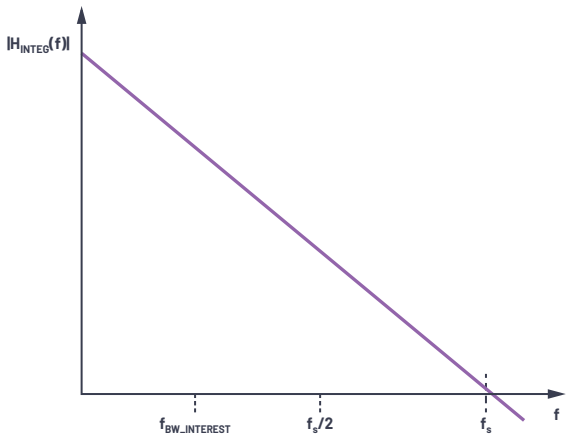


Figure 9. Integrator transfer function.

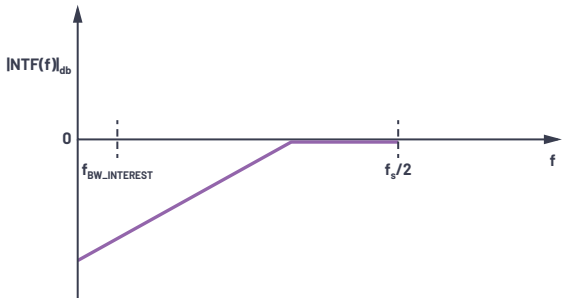


Figure 10. Noise transfer function without the sampler—has a high-pass filter profile.

With the sampler in loop, the quantization noise shaping analogy remains the same. The difference being the NTF frequency response would have replicated images at every multiple of f_S, as shown in Figure 10, thus creating notches at every integer multiple of the sampling frequency.

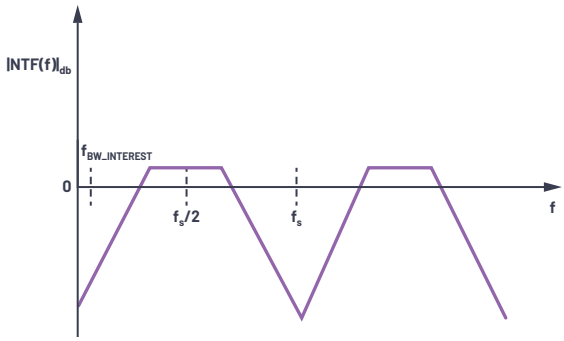


Figure 11. The noise transfer function of a CTSD ADC.

The uniqueness of sigma-delta architecture lies in the fact that putting an integrator and a DAC loop around a crude ADC—for example, a 4-bit ADC—and applying the concept of oversampling and noise shaping reduces the quantization noise significantly in the frequency bandwidth of interest and masks this crude ADC to a 16- to 24-bit precision ADC.

These basics of the first-order CTSD ADC can now be extended to any order of modulator loop. The sampling frequency, the crude ADC specifications, and the order of loop are top-level design decisions driven by the performance requirements of the ADC.

Step 7: Completing the CTSD Modulator with a Digital Filter

Generally, in an ADC signal chain, the digitized data is postprocessed by an external digital controller for any signal information extraction. In sigma-delta architecture, as we know now, the signal is oversampled. If this oversampled digital data is directly given to the external controller, then there is a lot of redundant data that needs to be processed. This causes excess power and real estate cost overheads in the digital controller design. So, before data is presented to the digital controller, the data samples are dropped in an efficient way without affecting the performance. This process is called decimation and is done by digital decimation filters. Figure 11 shows a typical CTSD modulator with on-chip digital decimation filters.

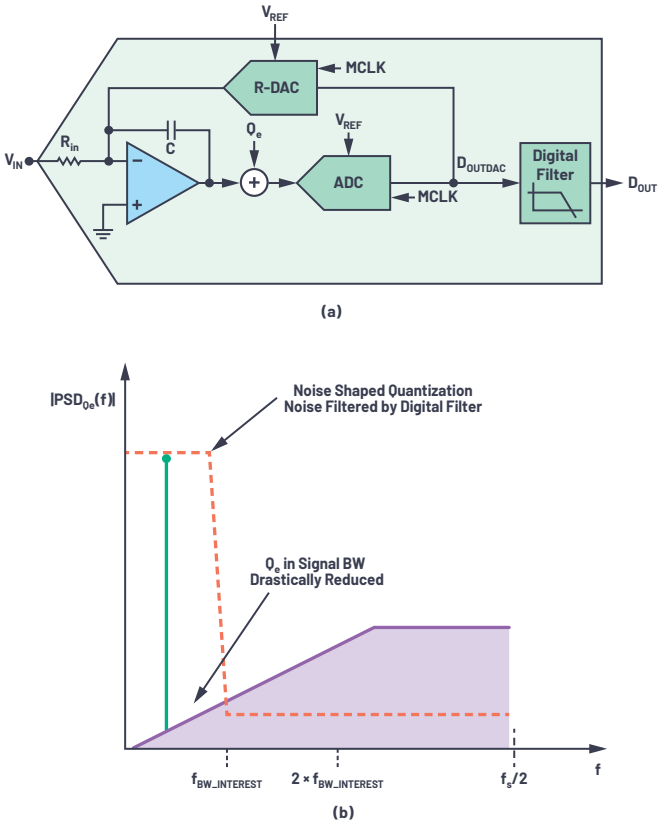


Figure 12. (a) A block diagram of a CTSD ADC modulator loop from an analog input to a digital output. (b) A frequency spectrum representation of an input signal at the output of a modulator and the output of a digital filter.

Figure 12b shows frequency response for an in-band analog input signal. At the output of the modulator we observe the noise shaping of the quantization noise, drastically reducing it in frequency band of interest. The digital filter helps attenuating the shaped noise beyond this frequency bandwidth of interest so that at the final digital output, D_{OUT}, is at the Nyquist sampling rate.

Step 8: Understanding the Clock Sensitivity of CTSD ADCs

So far, we have understood how CTSD ADCs keep the continuous integrity of the input signal, which significantly simplifies signal chain design. There are also a few limitations with this architecture, mainly dealing with the sampling clock, MCLK. The CTSD modulator loop works on the concept of integrating the error current between I_{IN} and I_{DAC}. Any error in this integrated value would cause the ADC in loop to sample the error and would reflect this in the output. For our first-order integrator loop, the integrated value over the sampling time period of T_s for constant I_{IN} and I_{DAC} is given by

$$\delta Vout_{integ} = \frac{T_S}{RC} \times (I_{IN} - I_{DAC}) \quad (10)$$

For an input of 0, the parameters that would affect this integration error are

- MCLK frequency: As indicated by Equation 10, if the MCLK frequency scales, then the RC coefficient that controls the slope of integration also needs to be retuned to get back the same integrated value. This implies that a CTSD modulator is tuned for a fixed MCLK clock frequency and cannot support varying MCLK.
- MCLK jitter: The DAC code and, hence, I_{DAC} change every clock time period T_s. If the I_{DAC} time period randomly changes, then the average integrated value keeps changing, as shown in Figure 13. So, any error in the sampling clock time period in the form of jitter would affect the performance of the modulator loop.

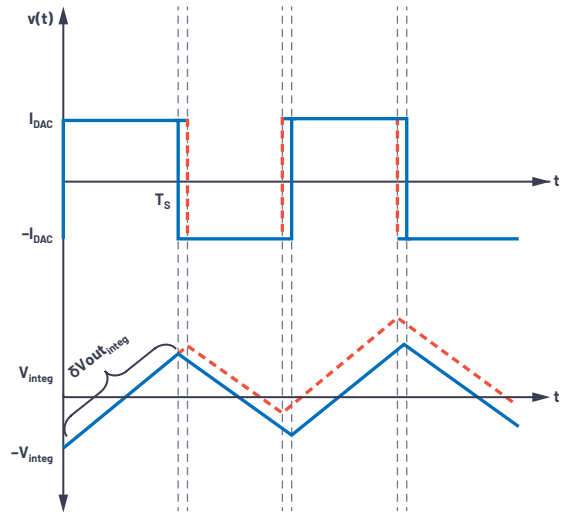


Figure 13. The clock sensitivity of a CTSD modulator.

CTSD ADCs are sensitive to the frequency and jitter of an MCLK because of the above reasons.[5] But ADI has identified solutions to work around these fallacies. For example, the challenges of generating and routing accurate, low jitter MCLK along the system to the ADC can be addressed using a local, low cost crystal and oscillator near the ADC. The fallacy around the fixed sampling frequency has been addressed by using innovative asynchronous sample rate conversion (ASRC) that enables a variable and independent digital output data rate for the digital controller irrespective of the fixed sampling MCLK. More information about this will be detailed later in this series.

Step 9: Voila! All Set to Explain the CTSD Concept to Your Buddies!

Part 1 highlighted certain signal chain advantages of a CTSD ADC, while Part 2 focused on the insights of the modulator loop built from Step 1 to Step 6 using the concept of a closed-loop op amp configuration. Figure 11a also helped us visualize these advantages.

The input impedance of a CTSD ADC is equivalent to the input impedance of the inverting amplifier, which is resistive and easy to drive. Using innovative techniques, the reference used by the modulator loop's DAC has also been made resistive. The sampler of the ADC is after the integrator and not directly at the input, which enables inherent alias rejection for interferers outside the frequency band of interest. We will deep dive into each of these advantages and their corresponding impact in a signal chain in the next few articles of this series. In the next article, we'll begin with the most unique advantage: inherent alias rejection. Keep an eye out for Part 3 to catch up on inherent alias rejection and to learn more about its quantification using a new set of measurements and performance parameters introduced for the first time with the AD4134, which is based on the CTSD architecture.

Acknowledgements

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References

[1] Hank Zumbahlen. "Mini Tutorial MT-213: Inverting Amplifier." Analog Devices, Inc., February 2013.

[2] Walt Kester. "MT-014 Tutorial: Basic DAC Architectures I: String DACs and Thermometer (Fully Decoded) DACs." Analog Devices, Inc., 2009.

[3] Luis Orozco. "Programmable-Gain Transimpedance Amplifiers Maximize Dynamic Range in Spectroscopy Systems." *Analog Dialogue*, Vol. 47, No. 2, May 2013.

[4] Walt Kester. "MT-022 Tutorial: ADC Architectures III: Sigma-Delta ADC Basics." Analog Devices, Inc., 2009.

[5] Pawel Czapor. "Sigma-Delta ADC Clocking—More Than Jitter." *Analog Dialogue*, Vol. 53, No. 3, April 2019.

Pavan, Shanthi, Richard Schreier, and Gabor C. Temes. *Understanding Delta-Sigma Data Converters*, 2nd edition. Wiley, January 2017.

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Optimizing Power Systems for the Signal Chain—Part 1: How Much Power Supply Noise Is Tolerable?

Patrick Errgy Pasaquian, Senior Applications Engineer, and
Pablo Perez, Jr., Senior Applications Engineer

Introduction

The increasing volume of data collected, communicated, and stored in everything from 5G to industrial applications has expanded the performance limits of analog signal processing devices, some into the gigasamples per second. As the pace of innovation never slows, the next generation of electronics solutions will lead to further shrinking in solution volumes, increasing power efficiency, and greater demand for better noise performance.

One might assume that the noise produced in the various power domains—analog, digital, serial digital, and digital input-output (I/O)—should be simply minimized or isolated to achieve optimum dynamic performance, but chasing the absolute minimum in noise can be a study in diminishing returns. How does a designer know when noise performance of a supply or supplies is sufficient? A good start is to quantify the sensitivity of devices so that the power supply spectral output can be matched to the domain. Knowledge is power: it can greatly help in design by, namely, avoiding over-engineering and thus saving in design time.

This article gives an overview of how to quantify the power supply noise sensitivity of the loads in signal processing chain, and how to calculate the maximum acceptable power supply noise. Measurement setups are also discussed. We finish by touching on some strategies to meet power domain sensitivity with realistic power supply noise requirements. Subsequent articles in this series will dive deeper into the details of optimizing power distribution networks (PDNs) for ADCs, DACs, and RF transceivers.

Understanding and Quantifying Signal Processing Load Sensitivity to Power Supply Noise

The first step in power supply optimization is to investigate the true sensitivity of analog signal processing devices to power supply noise. This includes understanding the effects of power supply noise to key dynamic performance specifications, and characterization of power supply noise sensitivity—namely, the power supply modulation ratio (PSMR) and power supply rejection ratio (PSRR).

PSMR and PSRR are good supply rejection characteristics, but alone they are insufficient to determine how low the ripple should be. This article demonstrates how to establish a ripple tolerance threshold or maximum allowable power supply noise using PSMR and PSRR. Matching this threshold to the power supply spectral output is the basis in designing an optimized power system design. An *optimized* power supply will not degrade the dynamic performance of each analog signal processing device if power supply noise remains below its maximum specification.

Effects of Power Supply Noise on Analog Signal Processing Devices

The effects of power supply noise on signal processing devices should be understood. These effects can be quantified by three measured parameters:

- Spurious-free dynamic range (SFDR)
- Signal-to-noise ratio (SNR)
- Phase noise (PN)

Understanding the effects of power supply noise on these parameters is the first step to optimizing the power supply noise specification.

Spurious-Free Dynamic Range (SFDR)

Power supply noise can be coupled into the carrier signal of any analog signal processing system. The effect of power supply noise depends on its strength relative to that of the carrier signal in the frequency domain. One measure is SFDR, which represents the smallest signal that can be distinguished from a large interfering signal—specifically, the ratio of the amplitude of the carrier signal to the amplitude of the highest spurious signal, regardless of where it falls in the frequency spectrum, such that:

$$SFDR = 20 \times log \left[\frac{Carrier\ Signal}{Spurious\ Signal} \right] \quad (1)$$

SFDR = spurious-free dynamic range (dB)

Carrier signal = rms value of the carrier signal amplitude (peak or full scale)

Spurious signal = rms value of the highest spur amplitude in the frequency spectrum

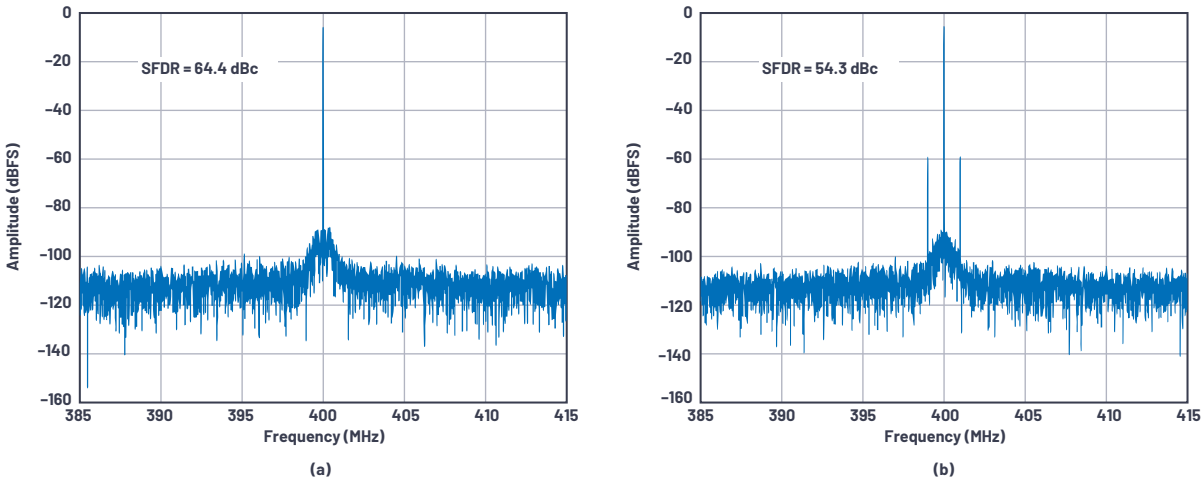

Figure 1. An AD9208 high speed ADC's SFDR using (a) a clean power supply and (b) a noisy power supply.

SFDR can be specified with respect to full scale (dBFS) or with respect to the carrier signal (dBc). Power supply ripple can produce unwanted spurs by coupling into the carrier signal, which degrades SFDR. Figure 1 compares the SFDR performance of the AD9208 high speed ADC when powered by a clean vs. a noisy power supply. In this case, power supply noise degrades the SFDR about 10 dB when a 1 MHz power supply ripple appears as modulated spurs beside the carrier frequency in the fast Fourier transform (FFT) spectrum output of the ADC.

Signal-to-Noise Ratio (SNR)

While SFDR depends on the highest spur in the frequency spectrum, the SNR depends on the total noise within the spectrum. SNR limits the capability of an analog signal processing system to see low amplitude signals and is theoretically limited by a converter's resolution in the system. SNR is mathematically defined as the ratio of the carrier signal level to the sum of all noise spectral components, except the first five harmonics and dc where:

$$SNR = 20 \times log \left[\frac{Carrier\ Signal}{Spectral\ Noise} \right] \quad (2)$$

SNR = signal-to-noise ratio (dB)

Carrier signal = rms value of the carrier signal (peak or full scale)

Spectral noise = rms sum of all noise spectral components excluding the first five harmonics

A noisy power supply can contribute to the decrease of SNR by coupling at the carrier signal and adding noise spectral components in the output spectrum. As shown in Figure 2, the SNR of the AD9208 high speed ADC decreases from 56.8 dBFS to 51.7 dBFS when a 1 MHz power supply ripple produces spectral noise components in the FFT output spectrum.

Phase Noise (PN)

Phase noise is a measure of the frequency stability of a signal. Ideally, an oscillator should be able to produce a specific set of stable frequencies over a specific time period. However, in the real world, there are always small, unwanted amplitude and phase fluctuations present on the signal. These phase fluctuations, or jitter, can be seen spreading out on either side of the signal in the frequency spectrum.

Phase noise can be defined in several ways. For the purposes of this article, phase noise is defined as single sideband (SSB) phase noise, a commonly used definition, which uses the ratio of the power density of an offset frequency from the carrier signal to the total power of the carrier signal where:

$$SSB\ PN = 10 \times log \left[\frac{Sideband\ Power\ Density}{Carrier\ Power} \right] \quad (3)$$

SSB PN = single sideband phase noise (dBc/Hz)

Sideband power density = noise power per 1 Hz bandwidth at an offset frequency from the carrier signal (W/Hz)

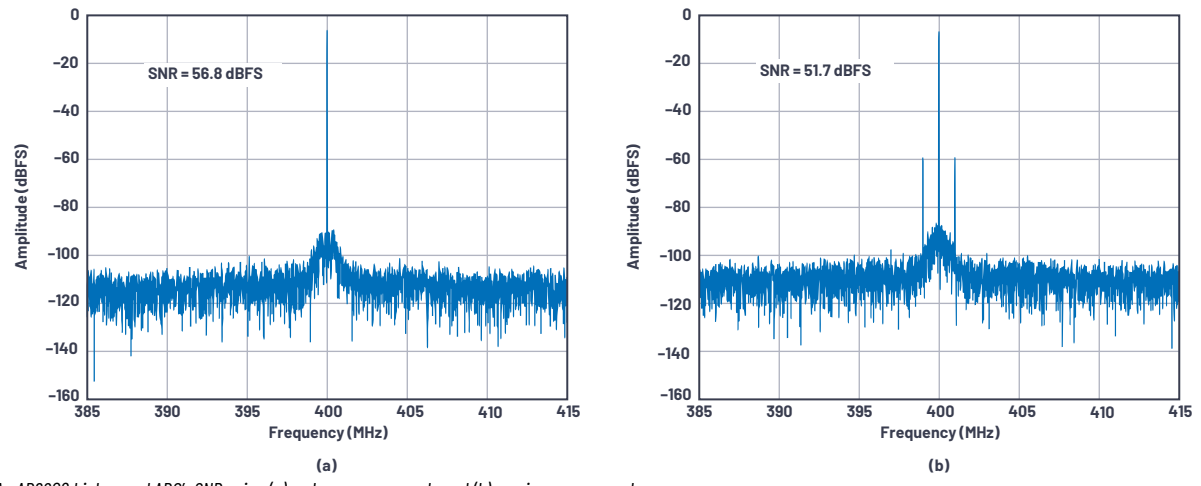

Figure 2. An AD9208 high speed ADC's SNR using (a) a clean power supply and (b) a noisy power supply.

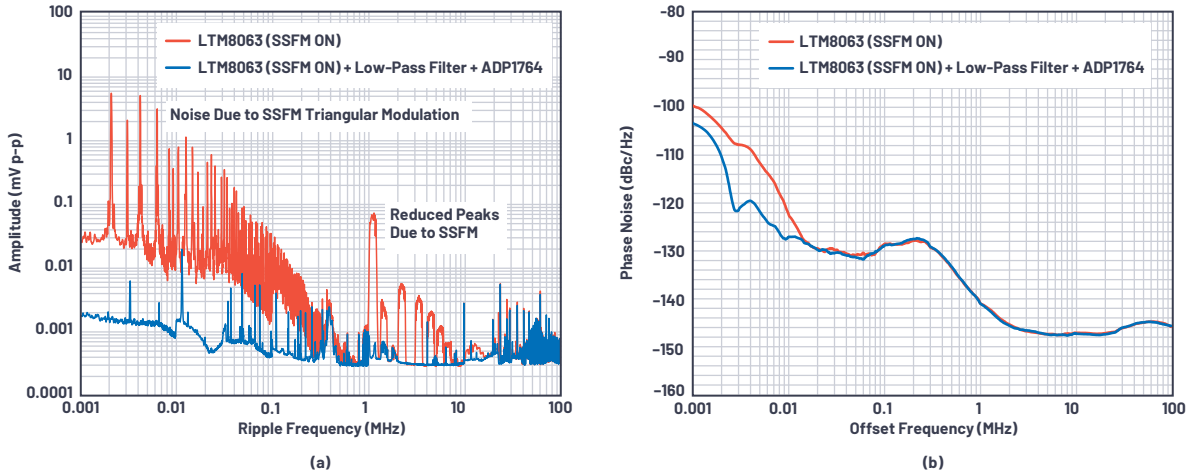

Figure 3. (a) Two different power supplies with significant differences in output noise content. (b) The resulting phase noise performance of the ADRV9009 when powered by those two supplies, respectively.

Carrier power = total carrier power (W)

In the case of analog signal processing devices, voltage noise coupled to the device clock through the clock supply voltage produces phase noise, which in turn affects the frequency stability of the internal local oscillator (LO). This widens the scope of LO frequency in the frequency spectrum, increasing the power density at the corresponding offset frequency from the carrier, in turn increasing phase noise.

Figure 3 shows the comparative phase noise performance of the ADRV9009 transceiver when powered by two different power supplies. Figure 3a shows the noise spectra of the two supplies, and Figure 3b shows the resulting phase noise. Both power supplies are based on the LTM8063 µModule® regulator with spread spectrum frequency modulation (SSFM) on. The advantage of SSFM is that it improves noise performance at the converter's fundamental switching frequency and its harmonics by spreading the fundamental over a range of frequencies. This can be seen in Figure 3a—note the relatively wide noise peaks at 1 MHz and its harmonics. The trade-off is that the frequency of SSFM's triangular wave modulation produces noise below 100 kHz—note the peaks starting around 2 kHz.

The alternate power supply adds a low-pass filter to suppress noise above 1 MHz, and an ADP1764 low dropout (LDO) postregulator to reduce the overall noise floor, particularly below 10 kHz (mostly SSFM-induced noise). The overall improvement in power supply noise due to the additional filtering results in enhanced phase noise performance below the 10 kHz offset frequency, as seen in Figure 3b.

Power Supply Noise Sensitivity of Analog Signal Processing Devices

The sensitivity of the load to power supply ripple can be quantified by two parameters:

- Power supply rejection ratio (PSRR)
- Power supply modulation ratio (PSMR)

Power Supply Rejection Ratio (PSRR)

PSRR represents the ability of the device to attenuate the noise on the power supply pin over a range of frequencies. In general, there are two types of PSRR: static (dc) PSRR and dynamic (ac) PSRR. DC PSRR is used as a measure of change in the output offset caused by the variation in the dc power supply voltage. This is a minimal concern, as power supply systems should provide a well-regulated dc voltage to the load. AC PSRR, on the other hand, represents the ability of a device to reject ac signals in the dc power supply over a range of frequencies.

AC PSRR is determined by injecting a sine wave signal at the power supply pin of the device and observing the error spur that appears on the noise floor of the data converter/transceiver output spectrum at the injection frequency (Figure 4). AC PSRR is defined as the ratio of the measured amplitude of the injected signal to the corresponding amplitude of the error spur on the output spectrum where:

$$AC_{PSRR}(dB) = 20\ log\left[\frac{Injected\ Ripple}{Error\ Spur}\right] \quad (4)$$

Error spur = spur amplitude seen in the output spectrum due to the injected ripple

Injected ripple = sine wave amplitude coupled and measured at the input supply pin

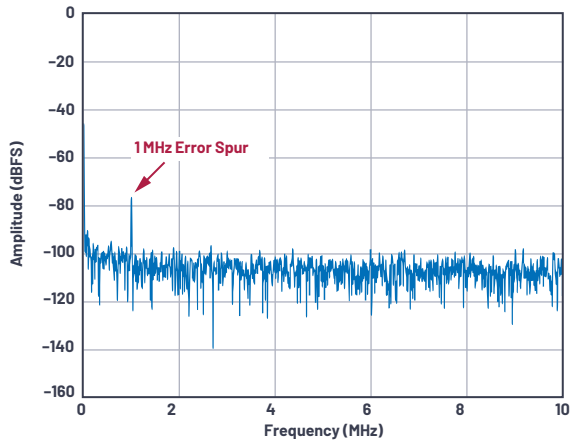

Figure 4. Error spur at the output spectrum of analog signal processing devices due to power supply ripple.

Figure 5 shows the block diagram of a typical PSRR setup. Using the AD9213 10 GSPS high speed ADC as an example, a 1 MHz, 13.3 mV p-p sine wave is actively coupled at the 1.0 V analog supply rail. A corresponding 1 MHz digitized spur appears above the –108 dBFS FFT spectrum noise floor of the ADC. The 1 MHz digitized spur is –81 dBFS, corresponding to a peak-to-peak voltage of 124.8 µV in reference to the analog input full-scale range of 1.4 V p-p. Calculating the ac PSRR at 1 MHz using Equation 4 yields an ac PSRR of 40.5 dB at 1 MHz. Figure 6 shows the ac PSRR of AD9213 for the 1.0 V AVDD rail.

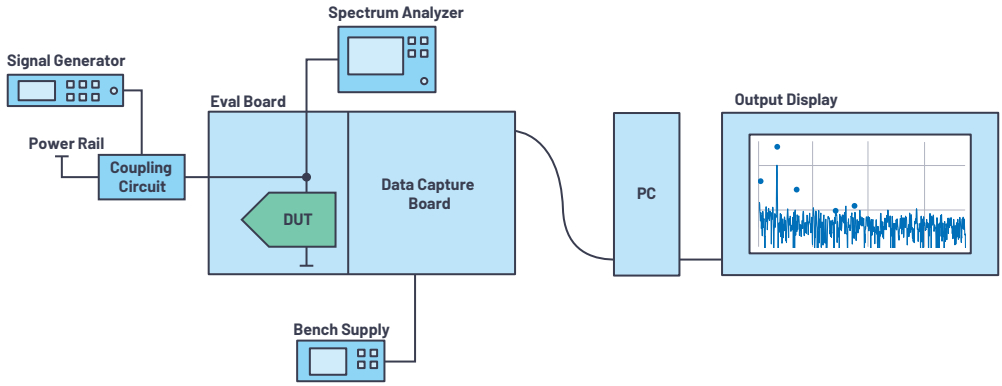

Figure 5. Simplified block diagram of a PSRR/PSMR test setup.

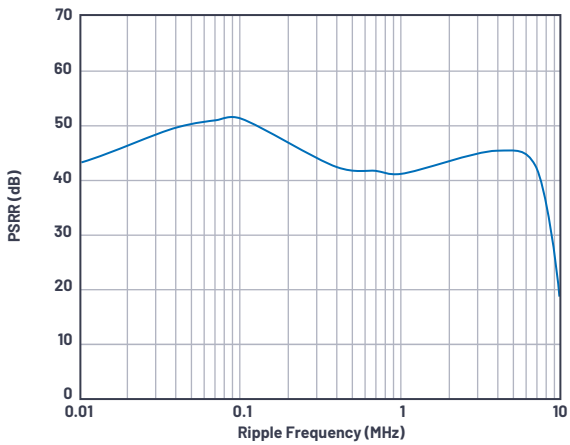

Figure 6. AD9213 high speed ADC ac PSRR for a 1.0 V AVDD rail.

Power Supply Modulation Ratio (PSMR)

PSMR affects analog signal processing devices differently than PSRR. PSMR shows the sensitivity of a device to power supply noise when it modulates with an RF carrier signal. The effect can be seen as a modulated spur around the carrier frequency applied to the device and appears as the carrier sideband.

Power supply modulation is achieved by combining the input ripple signal with a clean dc voltage using a line injector/coupling circuit. Supply ripple is injected as a sine wave signal from the signal generator to the power supply pin. The sine wave modulated into the RF carrier creates sideband spurs with offset frequency equal to the sine wave frequency. The level of the spurs is affected by both the sine wave amplitude and the sensitivity of the device. A simplified PSMR test setup is the same as that of PSRR as shown in Figure 5, but the output display is focused on the carrier frequency and its sideband spurs as shown in Figure 7. PSMR is defined as the ratio of the injected ripple amplitude of the power supply to the modulated sideband spur amplitude around the carrier where:

$$PSMR(dB) = 20 \log \left[\frac{Injected\ Ripple}{Modulated\ Spur} \right] \quad (5)$$

Modulated spur = spur amplitude at the sideband of the carrier frequency due to the injected ripple

Injected ripple = sine wave amplitude coupled and measured at the input supply pin

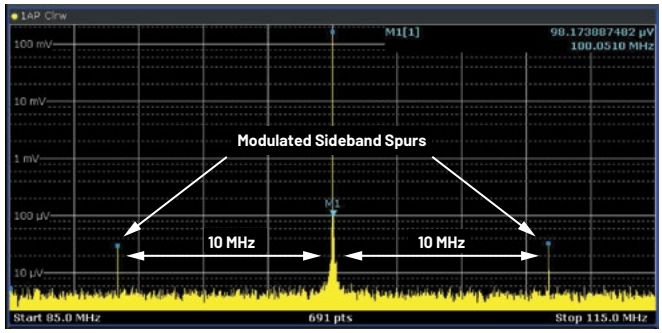

Figure 7. Modulated sideband spurs in the carrier signal due to power supply ripple.

Consider the AD9175 12.6 GSPS high speed DAC operating with a 100 MHz carrier, and a 10 MHz supply ripple of about 3.05 mV p-p actively coupled at the 1.0 V AVDD rail. A corresponding 24.6 µV p-p modulated spur appears in the sideband of the carrier signal with offset equal to the frequency of the supply ripple of about 10 MHz. Calculating the PSMR at 10 MHz using Equation 5 yields 41.9 dB. Figure 8 shows the AD9175 1.0V AVDD rail PSMR for channel DAC0 at various carrier frequencies.

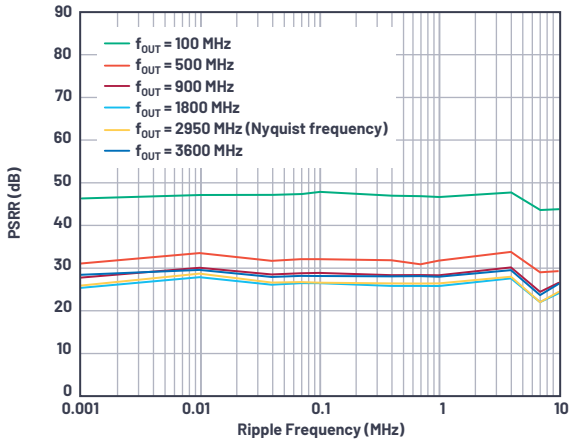

Figure 8. AD9175 high speed DAC PSMR for a 1.0 V AVDD rail (Channel DAC0).

Determining Maximum Allowable Power Supply Ripple

PSMR can be combined with a powered device's reference threshold to determine the maximum allowable voltage ripple on each of the power supply domains of an analog signal processing device. The reference threshold itself can be one of several values representing the allowable spur level (as caused by power supply ripple) that the device can tolerate without significantly affecting its dynamic performance. This spur level can be the spurious-free dynamic range (SFDR), a percentage of least significant bit (LSB) or output spectrum noise floor. Equation 6 shows the maximum allowable input ripple (V_{R_MAX}) as a function of PSMR and the measured noise floor of each device where:

$$V_{R\_MAX} = \left[10^{\frac{PSMR}{20}} \right] \times Threshold \quad (6)$$

V_{R_MAX} = the maximum allowable voltage ripple on each of the power supply rails before producing spur in the output spectrum noise floor

PSMR = the noise sensitivity of the power supply rail of interest (in dB)

Threshold = a predefined reference threshold (for the purposes of this article, the output spectrum noise floor)

For example, the output spectrum noise floor of AD9175 is about 1 µV p-p. The PSMR at 10 MHz ripple for the 1800 MHz carrier is about 20.9 dB. Using Equation 6, the maximum allowable ripple in the device supply pin that it can tolerate without degrading its dynamic performance is 11.1 µV p-p.

Figure 9 shows the combined results of the spectral output of the LT8650S step-down Silent Switcher® regulator (with and without an output LC filter) and the maximum allowable ripple of AD9175 for the 1.0 V AVDD rail. The regulator spectral output contains spurs at the fundamental switching frequency and its harmonics. The LT8650S directly powering the AD9175 produces a fundamental exceeding the maximum allowable threshold, resulting in modulated sideband spurs in the output spectrum, as shown in Figure 10. Simply adding an LC filter reduces the switching spurs below the maximum allowable ripple, as shown in Figure 11.

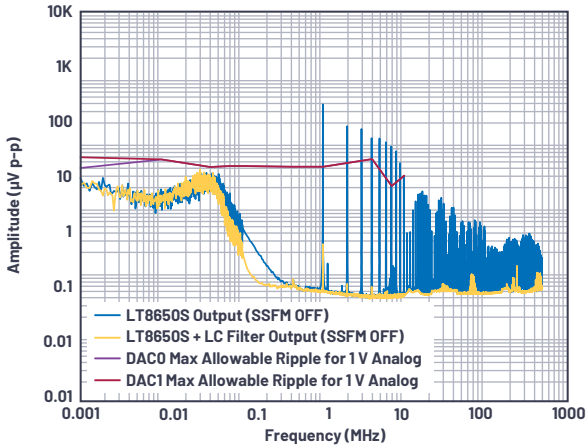

Figure 9. LT8650S power supply spectral output vs. the maximum allowable voltage ripple at the 1.0 V AVDD rail.

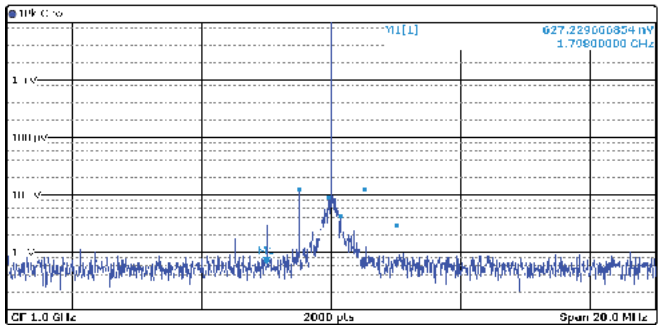

Figure 10. AD9175 DAC0 output spectrum at 1800 MHz carrier frequency using the LT8650S dc-to-dc Silent Switcher converter output directly to the AVDD rail.

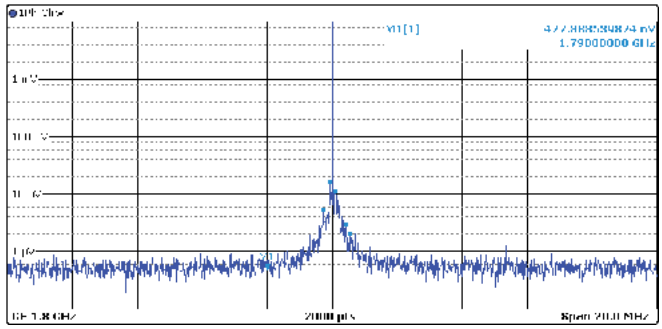

Figure 11. AD9175 DAC0 output spectrum at 1800 MHz carrier frequency using an LT8650S with LC filter power supply.

Conclusion

The superior dynamic performance of high speed analog signal processing devices can easily be undercut by power supply noise. A thorough understanding of the sensitivity of the signal chain to power supply noise is necessary to avoid performance degradation of the system. This can be determined by establishing a maximum allowable ripple—vital to designing the power distribution network (PDN). When the maximum allowable ripple threshold is known, various approaches in designing an optimized power supply can be applied. A good margin from the maximum allowable ripple is an indication that the PDN will not degrade the dynamic performance of high speed analog signal processing devices.

References

Delos, Peter. "Power Supply Modulation Ratio Demystified: How Does PSMR Differ from PSRR?" Analog Devices, Inc., December 2018.

Delos, Peter and Jarrett Liner. "Improved DAC Phase Noise Measurements Enable Ultralow Phase Noise DDS Applications." *Analog Dialogue*, Vol. 51, No. 3, August 2017.

"The Essential Guide to Data Conversion." Analog Devices, Inc.

Jayamohan, Umesh. "Powering GSPS or RF Sampling ADCs: Switcher vs. LDO." Analog Devices, Inc., November 2015.

Limjoco, Aldrick, Patrick Errgy Pasaquian, and Jefferson Eco. "Silent Switcher µModule Regulators Quietly Power GSPS Sampling ADCs in Half the Space." Analog Devices, Inc., October 2018.

Naeem, Naveed and Samantha Fontaine. "Characterizing the PSRR of Data Acquisition µModule Devices with Internal Bypass Capacitors." *Analog Dialogue*, Vol. 54, No. 3, July 2020.

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Patrick Errgy Pasaquian has been at Analog Devices for seven years. He joined ADI in 2014 and works as a senior applications engineer focusing on aerospace and defense (ADEF) power systems. He has handled various engineering roles in applications development, design evaluation, power attached to ADEF signal chains, and customer support through EngineerZone and Who's Who. He has authored and showcased several papers and projects at the ADI General Technical Conference (GTC), Asia Technical Symposium (ATS), and ADI Philippines Technical Symposium (ADTS). He received his bachelor's degree in electronics engineering at Central Philippine University in Iloilo City, Philippines. He can be reached at patrick.pasaquian@analog.com.

RAQ Issue 187: How to Choose the Right Protection for Your Circuit

Diarmúid Carey, Applications Engineer

Question:

What active circuit protection solutions can replace TVS diodes and fuses?

Answer:

Go with a surge stopper.

Abstract

Manufacturers in all industries constantly push cutting-edge performance, while trying to balance such innovation against tried-and-true robust solutions. Designers are faced with the difficult task of balancing design complexity, reliability, and cost. One subsystem in particular, electronics protection, rebuffs moves to innovate due to its nature. These systems protect sensitive and expensive downstream electronic devices (FPGAs, ASICs, and microprocessors), requiring a zero failure rate.

Many traditional and historically proven protection methodologies—such as diodes, fuses, and TVS devices—retain their go-to status, but these are often inefficient, bulky, and require maintenance. To address these deficiencies, active, intelligent protection ICs have proven they can match the protection requirements of traditional methods but in many ways are more robust. Because of the wide range of devices available, the most difficult problem for the designer is simply choosing appropriate solutions.

To help designers narrow their choices, this article compares traditional protection methods to the ADI protection portfolio, presenting the features of these products and suggested applications.

Introduction

The increase in the amount of electronics used in all industries, and the expansion of functions handled by expensive FPGAs and processors, has elevated the need to protect these devices from the harsh environments in which they operate. Layer on top of this a need for small form factors, high reliability, and fast response to overvoltage and overcurrent surge events. This article discusses the challenges faced in many applications and why protection is needed. Traditional protection methodologies are discussed and compared to newer, alternative solutions, which offer better accuracy, reliability, and design flexibility.

Why Consider Voltage and Current Protection Devices?

Automotive, industrial, communications, and aviation electronic systems must operate through a range of power supply surges, such as those shown in Figure 1. In each of these markets, transient events are defined in a number of industry specifications. For example, automotive transients are covered by the ISO 7637-2 and ISO 16750-2 specifications, which outline both the details of expected transients and test procedures to ensure these are consistently validated.

The types of surge events and their energy content can vary depending on the area in which the electronic device is used; circuitry can be exposed to overvoltage, overcurrent, reverse voltage, and reverse current conditions. Ultimately, many electronic circuits would not survive, let alone operate, if directly facing the transient conditions shown in Figure 1, so the designer must consider all of the input events and implement protection mechanisms that protect the circuit from these voltage and current surges.

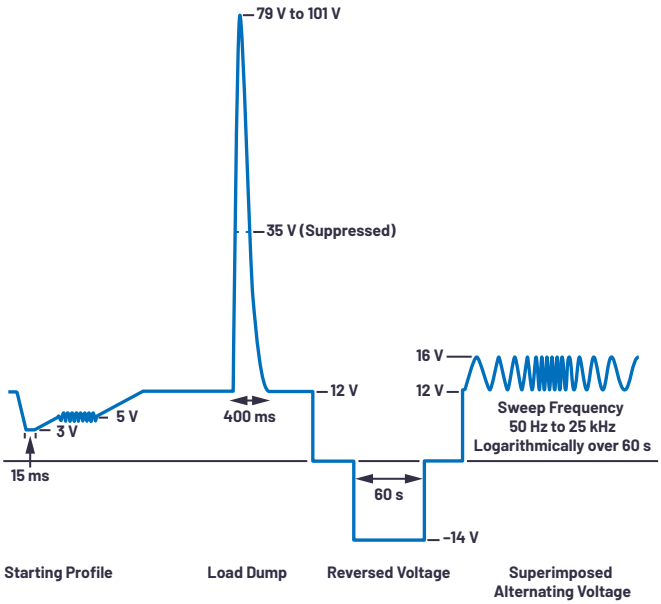
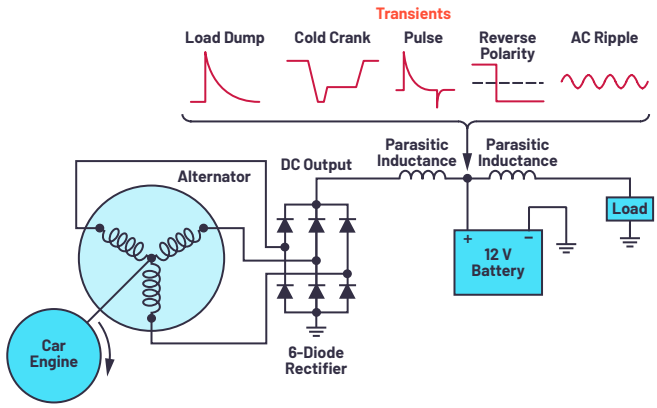


Figure 1. Overview of some of the tougher ISO 16750-2 tests.



Design Challenges

There are many different causes of transient voltage and current surges in electronic systems, but some electronic environments are more prone to transient events than others. Applications in automotive-, industrial-, and communications-based environments notoriously experience potentially harmful events, wreaking havoc on downstream electronic devices, but surge events are not limited to these environments. Other possible candidates for surge protection circuitry include any application that requires high voltage or high current supplies, or those that feature supply connections that are hot plugged, or systems that have motors or that may be exposed to potential lightning induced transients. High voltage events can occur over a wide range of time bases, from microseconds to hundreds of milliseconds, so a flexible and reliable protection mechanism is imperative to ensure the longevity of costly downstream electronic devices.

For instance, automotive load dump can occur when the alternator (charging the battery) is momentarily disconnected from the battery. As a result of this disconnect, the full charge current from the alternator is placed on the power rail, which raises the rail voltage to very high (>100 V) levels for hundreds of milliseconds.

Communications applications can have a number of possible surge causes, ranging from hot swapping communication cards to outdoor installations that can be exposed to lightning strikes. Inductive voltage spikes are also possible with long cables used in large facilities.

Ultimately, the environment in which the device must operate must be understood along with meeting published specifications. This helps the designer to put together an optimal protection mechanism that is both robust and unobtrusive, but allows downstream electronics to operate within safe voltage levels with minimal interruption.

Traditional Protection Circuitry

With so many different types of electrical events to consider, what should be in an electronics engineer's arsenal to protect the sensitive downstream electronics?

A traditional protection implementation relies on several devices rather than just one—for example, a transient voltage suppressor (TVS) for overvoltage protection, an in-line fuse for overcurrent protection, a series diode for reverse battery/supply protection, and a mix of capacitors and inductors to filter out lower energy spikes. While discrete setups can meet published specs—protecting downstream circuits—they result in complex implementations, requiring multiple selection iterations to correctly size the filtering.

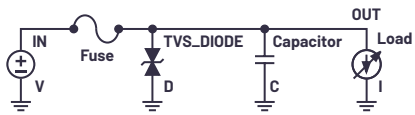


Figure 2. Traditional protection devices.

Let us take a closer look at each of these devices, touching on the advantages and disadvantages of this implementation.

TVS—Transient Voltage Suppressor

This is a relatively simple device that helps to protect downstream circuitry from high voltage spikes on the power supply. It can be broken into several different types, which have a wide range of characteristics (Table 1 is in order of response time, smallest to largest).

Table 1. Response Time for Different Transient Voltage Suppressor Devices

Transient Voltage Suppressor Device	Response Time
TVS Diodes	~1 ps
Metal-Oxide Varistor (MOV)	~1 ns
Avalanche Diode/Zener Diode	<1 µs
Gas Discharge Tube (GDT)	<5 µs

Although these feature a range of constructions and characteristics, they all operate in a similar manner: shunting the excess current when the voltage exceeds the device threshold. A TVS clamps the voltage at the output to the rated level within a very short period of time. A TVS diode, for example, can respond in as low as picoseconds' time, while a GDT can take a few microseconds to respond but can handle much larger surges.

Figure 3 shows the simple implementation of a TVS diode to protect a downstream circuit. Under normal operating conditions, the TVS is high impedance and the input voltage simply passes to the output. When an overvoltage condition occurs at the input, the TVS becomes conductive and responds by shunting the excess energy to ground (GND), clamping the voltage seen by the downstream load. The rail voltage rises above the typical operation value but is clamped to a value at a safe level for any downstream circuitry.

Although TVS devices are effective in suppressing very high voltage excursions, they are not immune to damage when faced with sustained overvoltage events, resulting in a requirement for regular device monitoring or replacement. Another concern is that a TVS can fail short and thus crowbar the input supply. Also, depending on the energy involved, they can be physically large to match with margin, increasing the solution size. Even when a TVS has been correctly sized, the downstream circuitry must be capable of handling the clamped voltage, resulting in increased voltage rating requirements downstream.

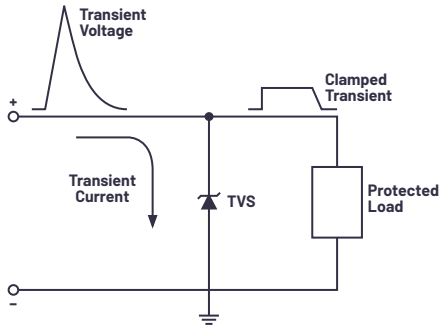


Figure 3. Protecting against voltage surges with a traditional TVS solution.

In-Line Fuse

Overcurrent protection can be implemented using the ubiquitous in-line fuse with a fuse blow rating at some margin above nominal—for example, 20% higher than the max rated current (the percentage will depend on the type of circuit as well as the typical operational loads expected). The biggest problem with fuses, of course, is that they must be replaced once blown. Time and cost savings resulting from fuses' simple design can be incurred later because of relatively complex maintenance, especially if the application is physically hard to reach. Maintenance requirements can be reduced with alternate fuses, such as resettable fuses, which utilize a positive temperature coefficient to open the circuit when a larger than normal current passes through the device (the increased current level increases the temperature, resulting in a sharp increase in resistance).

Maintenance issues aside, one of the biggest problems with fuses is their reaction time, which can vary widely depending on the type of fuse selected. Fast blow fuses are available, but clearing time (time to open the circuit) can still range from hundreds of microseconds to milliseconds, so the circuit designer must consider the energy released over these extended times to ensure that downstream electronics can survive.

Series Diode

In some environments, circuits are exposed to supply disconnection and reconnection—for example, in a battery-operated environment. In such instances, correct polarity is not guaranteed in reconnection of the supply. Polarity protection can be achieved by adding a series diode on the positive supply line of the circuit. While this simple addition is effective in protecting against reverse polarity, the voltage drop of the series diode results in commensurate power dissipation. In relatively low current circuits, the trade-off is minimal, but for many modern high current rails, an alternative solution is required. Figure 4 shows an update to Figure 3, showing both the TVS and the added series diode to protect against the reverse polarity connection.

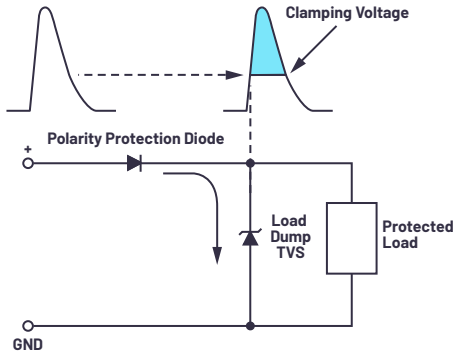


Figure 4. Adding a series diode protects against reverse polarity, but the voltage drop of the diode can be a problem in high current systems.

Filters Using Inductors and Capacitors

The passive solutions discussed so far all limit the amplitude of the events passed through but generally capture larger events while leaving some smaller spikes to pass. These smaller transients can still cause damage to downstream circuitry, so additional passive filters are required to clean the line. This is achievable using discrete inductors and capacitors, which must be sized to attenuate the voltage at the unwanted frequencies. Filter design requires test and measurement before design to ascertain the size and frequency before the filter can be correctly sized. The drawbacks of this path are the cost of BOM and real estate requirements—the board area and cost of the components required to achieve the level of filtering—as well as the need for overdesign—rating the component tolerances to compensate for changes over time and temperature.

Active Protection Using a Surge Stopper

One way to overcome the challenges and disadvantages of the passive protection solutions described is to instead utilize a surge stopper IC. A surge stopper eliminates the need for bulky shunt circuitry (TVS devices, fuses, inductors, and capacitors) with an easy to use controller IC and a series N-channel MOSFET. Surge stopper controllers can greatly simplify system design since there are few components to size and qualify.

A surge stopper continuously monitors the input voltage and current. Under nominal operating conditions, the controller drives the gate of an N-channel MOSFET pass device fully on, providing a low resistance path from the input to the output. When an overvoltage or surge condition occurs—with a threshold dictated by a feedback network at the output—the IC regulates the gate of the N-channel MOSFET to clamp the output voltage of the MOSFET at the level set by the resistor divider.

Figure 5 shows a simplified schematic of a surge stopper implementation, along with the results of a 100 V input surge on a nominal 12 V rail. The output of the surge stopper circuit is clamped to 27 V for the duration of the surge event. Some surge stoppers also monitor for overcurrent conditions using a series sense resistor (the circuit breaker in Figure 5), and adjust the gate of the N-channel MOSFET to limit the current presented to the output load.

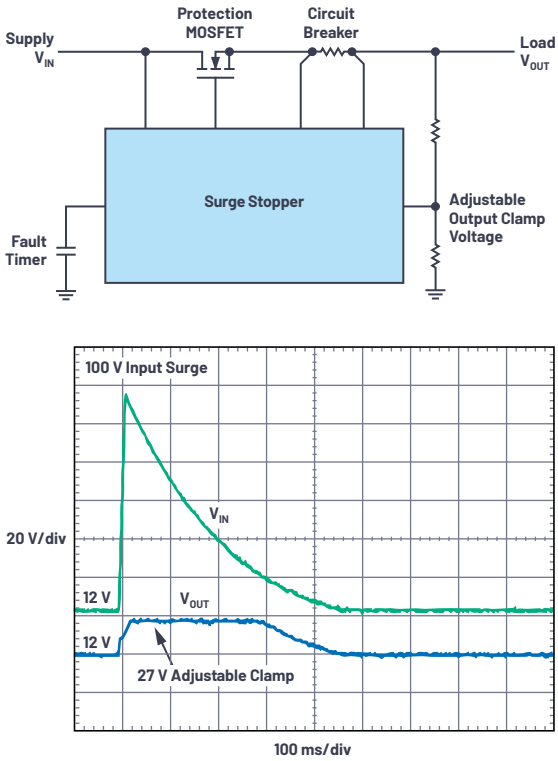


Figure 5. A high level diagram of a surge stopper implementation.

There are four broad types of surge stopper, classified by their response to an overvoltage event:

- Linear surge stopper
- Gate clamp
- Switching surge stopper
- Output disconnect protection controller

The choice of surge stopper depends on the application, so let's compare their operation and advantages.

Surge Stopper Type: Linear

A linear surge stopper drives the series MOSFET much like a linear regulator would, limiting the output voltage to the pre-programmed safe value, dissipating excess energy in the MOSFET. To help protect the MOSFET, the device limits the time spent in the high dissipation region by implementing a capacitive fault timer.

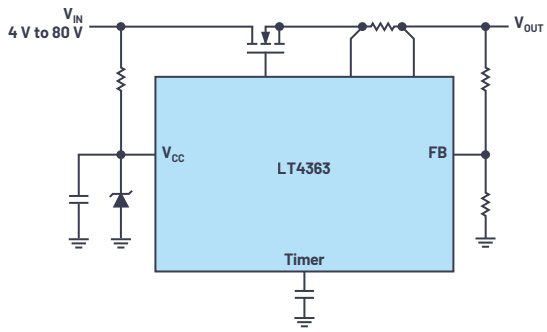


Figure 6. The LT4363, a linear surge stopper.

Surge Stopper Type: Gate Clamp

The gate clamp surge stopper operates by utilizing either an internal or external clamp (31.5 V or 50 V internal, for example, or an adjustable external clamp) to limit the gate pin to this voltage. The threshold voltage of the MOSFET then determines the output voltage limit. For example, with an internal 31.5 V gate clamp and a MOSFET threshold voltage of 5 V, the output voltage is limited to 26.5 V. Alternately, an external gate clamp allows a much wider range of voltages to be selected. An example of a gate clamp surge stopper is shown in Figure 7.

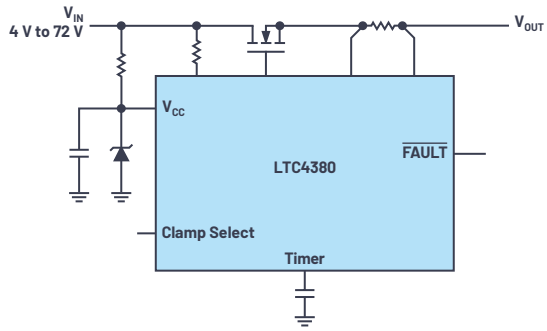


Figure 7. The LTC4380, a gate clamp surge stopper.

Surge Stopper Type: Switching

For higher power applications, a switching surge stopper is a good choice. Like linear and gate clamp surge stoppers, a switching surge stopper fully enhances the pass FET under normal operation to provide a low resistance path between the input and output (minimizing power dissipation). The main difference between a switching surge stopper and a linear or gate clamp surge stopper appears when a surge event is detected. In the event of a surge, the output of a switching surge stopper is regulated to the clamp voltage by switching the external MOSFET much like a switching dc-to-dc converter.

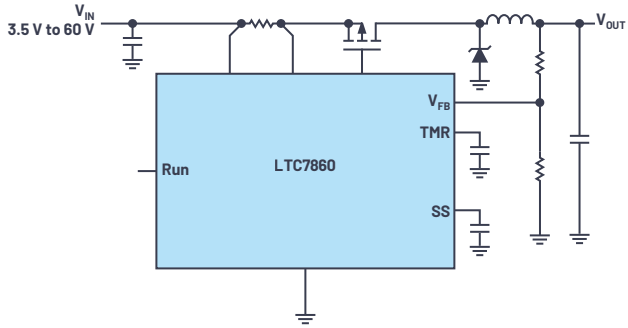


Figure 8. The LTC7860, a switching surge stopper.

Protection Controller: Output Disconnect

A protection controller is not officially a surge stopper, but it does stop surges. Like a surge stopper, a protection controller monitors for overvoltage and overcurrent conditions, but instead of clamping or regulating the output, the protection controller disconnects the output immediately to protect downstream electronics. This simple protection circuit can have a very compact footprint, suitable for battery-operated, portable applications. The LTC4368 protection controller is shown in a simplified schematic in Figure 9, along with its response to an overvoltage event. Protection controllers are available in a number of variants.

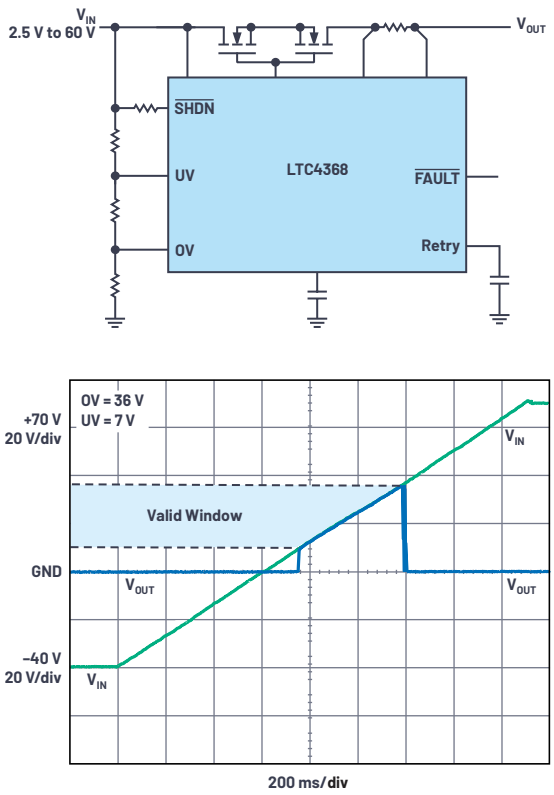


Figure 9. The LTC4368, a protection controller.

A protection controller operates by monitoring the input voltage to ensure that it remains within a voltage window configured by the resistor divider on the OV/UV pins, disconnecting the output via back-to-back MOSFETs when the input is outside this window, as shown in Figure 9. The back-to-back MOSFETs can also protect against a reversed input. The sense resistor at the output enables overcurrent protection capability by continually monitoring the forward current, but without a timer-based ride-through operation.

Surge Stopper Features

In order to select the most suitable surge stopper for your application you will need to know what features are available and what challenge they are helping to solve. The devices can be found at the parametric table.

Disconnect vs. Ride-Through

Some applications require disconnecting the output from the input when a surge event is detected. In this instance, overvoltage disconnect would be required. If you needed the output to remain operational in the face of surge events, thus minimizing the downtime of downstream electronics, you would require the surge stopper to ride through the surge event. In this case, a linear or a switching surge stopper can achieve this functionality (provided the power levels were reasonable for the topology and FET selected).

Fault Timer

Ride-through operation requires some protection for the MOSFET against persistent surges. To remain within the safe operating area (SOA) of the FET, a timer can be implemented. The timer is essentially a capacitor to ground. When an overvoltage condition occurs, an internal current source starts to charge this external capacitor. Once the capacitor reaches a certain threshold voltage, a digital fault pin pulls low to indicate the pass transistor will soon turn off due to the extended overvoltage condition. If the timer pin voltage continues to rise to a secondary threshold, the GATE pin pulls low to turn off the MOSFET.

The rate of change of the timer voltage varies with the voltage across the MOSFET—that is, a shorter timer for larger voltages and a longer timer for smaller voltages. This useful feature enables the device to ride through short overvoltage events, allowing downstream components to remain operational while protecting the MOSFET from damage by longer-lasting overvoltage events. Some devices feature a retry function, enabling the device to turn on the output again after a cool down period.

Overcurrent Protection

Many surge stoppers have the ability to monitor current and protect against overcurrent events. This is achieved by monitoring the voltage drop across a series sense resistor and responding appropriately. Inrush current can also be monitored and controlled to protect the MOSFET. The response can be similar to an overvoltage condition, as it either disconnects by latching off or riding through the event if the circuitry can handle the power levels.

Reverse Input Protection

Reverse input protection is possible due to the wide operating capabilities of the surge stopper devices (capable of withstanding up to 60 V below ground potential on some devices). Figure 10 shows a back-to-back MOSFET implementation of reverse current protection. During normal operation, Q2 and Q1 are turned on by the GATE pin, and Q3 doesn't have any impact. However, when a reverse voltage condition exists, Q3 turns on, pulling Q2's gate down to the negative input and isolating Q1, protecting the output.

Reverse output voltage protection is also achieved with robust device pin protection, with up to 20 V below ground potential possible, depending on the device selected.

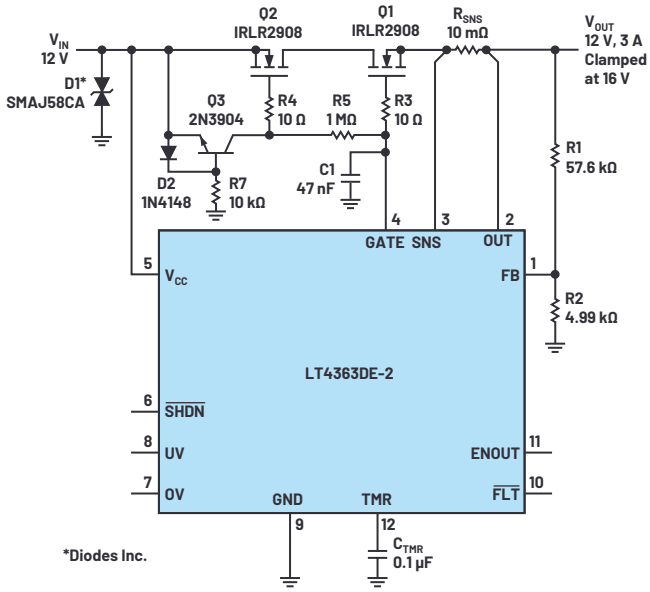


Figure 10. LT4363 reverse input protection circuit.

For applications that require wide input voltage ranges, a floating topology surge stopper can be used. When a surge event occurs, the full surge voltage is seen by the surge stopper IC so the internal transistor technology limits the voltage range of the IC. With a floating surge stopper such as the LTC4366, the IC floats just below the output voltage, giving it a much wider operating voltage range. A resistor is placed in the return line (V_{SS}), which allows the IC to float up with the supply voltage. The result is an input voltage limitation set by the voltage capability of the external components and MOSFETs. Figure 11 shows an application circuit capable of operating from a very high dc supply while protecting the downstream load.

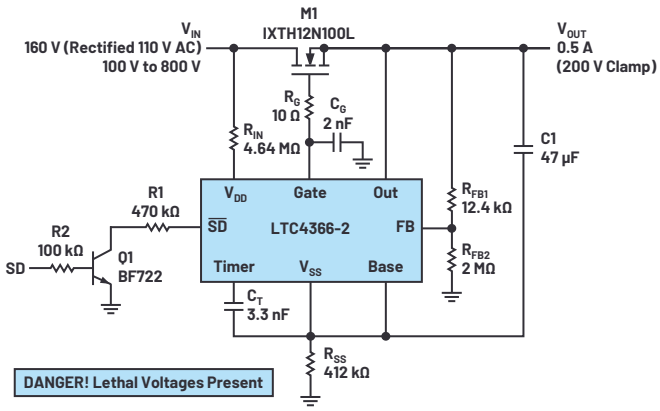


Figure 11. LTC4366 high voltage floating topology.

Choosing the Right Device for My Application

In many ways, because of their inherently robust design, using a surge stopper simplifies protection circuit design. Data sheets can help greatly with sizing components, with many possible applications already shown. The hardest part might be choosing the most appropriate device. Follow these few steps to narrow the field:

- Go to ADI's protection family parametric table.
- Choose input voltage range.
- Choose the number of channels.
- Filter on features to narrow the possible options.

As with all product selection, it is important to understand your system requirements before looking for the correct device. Some important considerations are the expected supply voltage and the voltage tolerance of downstream electronics (important for deciding the clamp voltage), as well as any particular features that are important for the design.

Some example filtered parametric tables are shown below for reference. These can further be modified on the website to include some other parameters.

- The high voltage surge stopper devices can be found here.
- Protection controllers with the 0V disconnect feature can be found here.

Conclusion

Regardless of the surge stopper type implemented, active, IC-based surge stopper designs eliminate the need for bulky TVS diodes or large profile inductors and capacitors for filtering. This results in an overall smaller area and a lower profile solution. The output voltage clamp is more accurate than a TVS with 1% to 2% accuracy possible. This prevents overdesign and allows for downstream devices with tighter tolerances to be selected.

The system protection family of devices available from Analog Devices enables designers to implement reliable, flexible, and small form factor protection for downstream devices—especially those facing harsh overvoltage and overcurrent events, which can occur in many industrial-, automotive-, aerospace-, and communications-based designs.

References

"AN-9768: Transient Suppression Devices and Principles." Littelfuse, January 1998.

"Fuseology." Automotive Passenger Car Solutions Catalog, Littelfuse, 2014.

Kalb, Jim. "Total Clearing Time" Technical Bulletin, OptiFuse, January 2010.

Megaw, David. "Protecting and Powering Automotive Electronics Systems with No Switching Noise and 99.9% Efficiency." *Analog Dialogue*, Vol. 54, No. 1, February 2020.

Wu, Bin and Zhongming Ye. "Comprehensive Power Supply System Designs for Harsh Automotive Environments Consume Minimal Space, Preserve Battery Charge, Feature Low EMI." *Analog Dialogue*, Vol. 53, No. 3, August 2019.

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