**RISC-V Microprocessor & DSP Element**

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# Project Overview

This report details the design and implement of a microprocessor based on the RISC-V instruction set architecture, along with an integrated digital signal processing (DSP) coprocessor. The processor features a Harvard architecture for efficient single-cycle data access. The processor includes memory mapped I/O for interfacing with peripherals such as LEDs, switches, buttons, and the DSP coprocessor. The DSP coprocessor performs efficient image processing tasks, while interfacing with a VGA driver to allow images to be displayed to a monitor. Application software, automation scripts, and verification environments were developed to verify and support device operation. Finally, a memory-aware design approach was implemented for full utilization for fast on-chip Block SRAM when mapping to an Altera DE-1 FPGA. By combining the RISC-V CPU core with a DSP coprocessor, this project demonstrates the strengths of a hardware-focused design in multimedia applications that involve processing and displaying images.

# RISC-V CPU

## Overview

A single-core pipelined RISC-V Base 32-I architecture was implemented with a Harvard-style memory model, 32x32b Register File supporting Register file bypassing, a Byte-Addressable data memory supporting Byte, Halfword, and word accesses, and a memory-mapped I/O interface. The following section details the top-level pipeline architecture, data & control hazard solutions, memory mapped I/O architecture, and finally, verification efforts.

## Pipeline Architecture

*Figure 1* below depicts a detailed data and control flow for the pipelined RISC-V processor.

## Memory-Mapped I/O Architecture

## Dedicated LWCP Instruction

## Verification & Validation

# DSP Accelerator

## Overview

## Image Buffer

## Direct Memory Access (DMA) Convention

## Processing Element

## Video Driver & Video Memory

## Verification & Validation

# UART Bootloader

## Bootloader Protocol & Architecture

## Verification & Validation

# Synthesis Report

# Implementation & Application Software

# Project Final Demo

# Discussion

## Performance Results

## Challenges

## Societal Implications

## Engineering Standards Employed