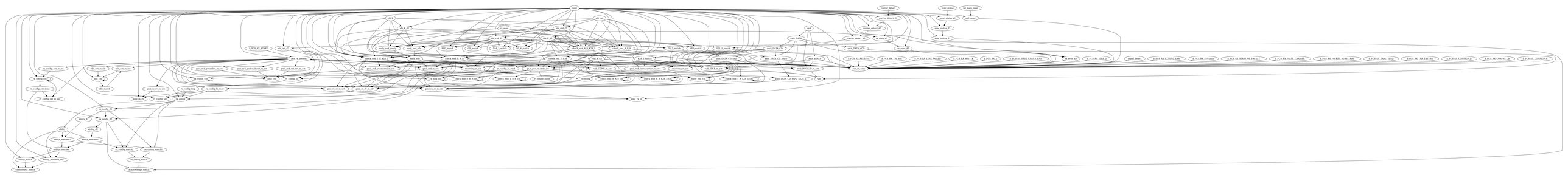

S_PCS_RX_START

pcs_rx_present

gmii_rxd_trr_extend_m_set

gmii_rx_er_m_clr

gmii_rxd_m_set receiving_m_clr pcs_rx_next

gmii_rx_er_m_set gmii_rx_dv_m_clr

rx_config_cnt_m_rst ge_x_pcs_rx_stats_inc gmii_rxd_false_carrier_m_set rudi_IDLE_m_set rudi_INVALID_m_set

rx_config_hi_read

idle_cnt_m_inc

gmii_rx_dv_m_set

gmii_rxd_preamble_m_set gmii_rxd_packet_burst_m_set gmii_rxd_ext_err_m_set rx_config_lo_read

rx_config_cnt_m_inc

idle_cnt_m_clr rudi_CONF_m_set receiving_m_set

idle_cnt

idle_match

early_end

gmii_rxd

gmii_rx_er

receiving

gmii_rx_dv

rx_frame_cnt rx_data_cnt check_end_R_R_R_cnt check_end_T_R_R_cnt rx_frame_pulse check_end_R_R_S_cnt check_end_R_R_K28_5_cnt early_end_cnt check_end_T_R_K28_5_cnt

S_PCS_RX_IDLE_D

SPD_match

xmit_DATA_CD_SPD xmit_DATA_CD_nSPD

xmit_DATA_CD_nSPD_nK28_5 rudi

signal_detect S_PCS_RX_EXTEND_ERR

ebi_rxd

early_end_config early_end_idle

check_end_T_R_K28_5 check_end_T_R_R

check_end_R_R_K28_5

ebi_rxd_d1

check_end_R_R_R

check_end_R_R_S

ebi_rxd_d2

D2_2_match

ability_matched_reg

consistency_match

S_PCS_RX_INVALID

rx_config_cnt

rx_config_cnt_done

rx_config_lo

rx_config_tmp

rx_config_set rx_config

S_PCS_RX_START_OF_PACKET

ability

rx_config_match2 rx_config_match1

rx_config_d1

rx_config_d2

carrier_detect_d1

carrier_detect_d2

carrier_detect_d3

xmit_DATA_CD xmit_DATA_nCD

ability_match

S_PCS_RX_FALSE_CARRIER

D21_5_match

ability_matched1 ability_matched2

ability_matched

xmit_nDATA S_PCS_RX_PACKET_BURST_RRS

rx_config_match

ability_d1

soft_reset

carrier_detect

ability_d2

acknowledge_match

rx_even_d2

rx_even_d3

rx_even_d1

rx_even

ebi_K_d3 S_PCS_RX_EARLY_END

ebi_K_d2

EPD_match CE_match

K28_5_match

D16_2_match D5_6_match

ebi_K_d1

S_PCS_RX_TRR_EXTEND

ebi_rxd_d3

sync_status

sync_status_d1

sync_status_d2

xmit_DATA

S_PCS_RX_CONFIG_CD S_PCS_RX_CONFIG_CB S_PCS_RX_CONFIG_CC

reset

sync_status_d3

S_PCS_RX_RECEIVE S_PCS_RX_TRI_RRI

xmit

mr_main_reset

ebi_K

S_PCS_RX_LINK_FAILED S_PCS_RX_WAIT_K S_PCS_RX_K S_PCS_RX_EPD2_CHECK_END