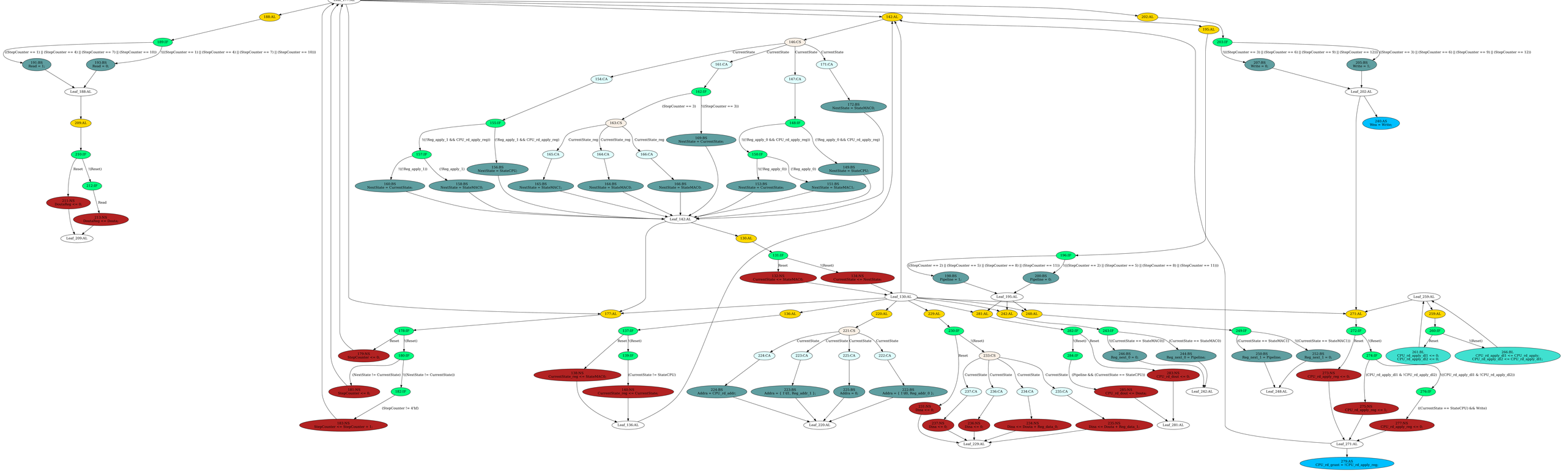
Leaf_177:AL
188:AL
189:IF
((StepCounter == 1) || (StepCounter == 4) || (StepCounter == 7) || (StepCounter == 10))
!((StepCounter == 1) || (StepCounter == 4) || (StepCounter == 7) || (StepCounter == 10))
191:BS
Read = 1;
193:BS
Read = 0;
Leaf_188:AL
209:AL
210:IF
Reset
!(Reset)
212:IF
Read
!(Read)
211:NS
DoutaReg <= 0;
213:NS
DoutaReg <= Douta;
Leaf_209:AL
142:AL
202:AL
195:AL
166:CS
CurrentState
154:CA
161:CA
147:CA
171:CA
162:IF
(StepCounter == 3)
!((StepCounter == 3))
172:BS
NextState = StateMAC0;
163:CS
149:IF
!(!Reg_apply_1 && CPU_rd_apply_reg)
!(Reg_apply_1 && CPU_rd_apply_reg)
CurrentState_reg
169:BS
NextState = CurrentState;
!(!Reg_apply_0 && CPU_rd_apply_reg)
(!Reg_apply_0 && CPU_rd_apply_reg)
135:IF
157:IF
165:CA
164:CA
166:CA
150:IF
!(!Reg_apply_1)
(!Reg_apply_1)
!(!Reg_apply_0)
(!Reg_apply_0)
156:BS
NextState = StateCPU;
149:BS
NextState = StateCPU;
160:BS
NextState = CurrentState;
158:BS
NextState = StateMAC0;
165:BS
NextState = StateMAC1;
164:BS
NextState = StateMAC0;
166:BS
NextState = StateMAC0;
153:BS
NextState = CurrentState;
151:BS
NextState = StateMAC1;
Leaf_142:AL
130:AL
131:IF
Reset
!(Reset)
114:NS
CurrentState <= StateMAC0;
134:NS
CurrentState <= NextState;
Leaf_130:AL
196:IF
((StepCounter == 2) || (StepCounter == 5) || (StepCounter == 8) || (StepCounter == 11))
!((StepCounter == 2) || (StepCounter == 5) || (StepCounter == 8) || (StepCounter == 11))
198:BS
Pipeline = 1;
200:BS
Pipeline = 0;
Leaf_195:AL
103:IF
!((StepCounter == 3) || (StepCounter == 6) || (StepCounter == 9) || (StepCounter == 12))
((StepCounter == 3) || (StepCounter == 6) || (StepCounter == 9) || (StepCounter == 12))
207:BS
Write = 0;
205:BS
Write = 1;
Leaf_202:AL
249:AS
Wsa = Write;
Leaf_259:AL
177:AL
136:AL
220:AL
229:AL
281:AL
242:AL
248:AL
271:AL
259:AL
178:IF
137:IF
221:CS
230:IF
282:IF
243:IF
249:IF
272:IF
260:IF
Reset
!(Reset)
179:NS
StopCounter <= 0;
180:IF
139:IF
224:CA
223:CA
225:CA
222:CA
233:CS
!(Reset)
Reset
!(Reset)
!(!CurrentState == StateMAC0)
(CurrentState == StateMAC0)
(CurrentState == StateMAC1)
!(!CurrentState == StateMAC1)
(Pipeline && (CurrentState == StateCPU))
246:BS
Reg_next_0 = 0;
244:BS
Reg_next_0 = Pipeline;
250:BS
Reg_next_1 = Pipeline;
252:BS
Reg_next_1 = 0;
261:BL
CPU_rd_apply_dl1 <= 0;
CPU_rd_apply_dl2 <= 0;
266:BL
CPU_rd_apply_dl1 <= CPU_rd_apply ;
CPU_rd_apply_dl2 <= CPU_rd_apply_dl1 ;
(NextState != CurrentState)
!(NextState != CurrentState))
138:NS
CurrentState_reg <= StateMAC0;
140:NS
CurrentState_reg <= CurrentState;
224:BS
Addra = CPU_rd_addr;
223:BS
Addra = { 1'd1, Reg_addr_1 };
225:BS
Addra = 0;
222:BS
Addra = { 1'd0, Reg_addr_0 };
237:CA
236:CA
234:CA
235:CA
284:IF
283:NS
CPU_rd_dout <= 0;
282:NS
CPU_rd_dout <= Douta;
Leaf_242:AL
(CPU_rd_apply_dl1 & !CPU_rd_apply_dl2)
((CPU_rd_apply_dl1 & !CPU_rd_apply_dl2))
274:IF
276:IF
181:NS
StopCounter <= 0;
182:IF
(StopCounter != 4'hf)
183:NS
StopCounter <= StopCounter + 1;
231:NS
Dsa <= 0;
232:NS
Dsa <= 0;
233:NS
Dsa <= Douta + Reg_data_0;
234:NS
Dsa <= Douta + Reg_data_1;
Leaf_248:AL
273:NS
CPU_rd_apply_reg <= 0;
275:NS
CPU_rd_apply_reg <= 1;
277:NS
CPU_rd_apply_reg <= 0;
(!(CurrentState == StateCPU) && Write)
Leaf_220:AL
Leaf_229:AL
Leaf_281:AL
Leaf_136:AL
Leaf_271:AL
278:AS
CPU_rd_grant = !CPU_rd_apply_reg;