

102:AL

103:BL

104:IF

rst

!(rst)

160:IF

104:BL

```
fpu_op_1 <= 0;
fpu_op_final <= 0;
fpu_op_2 <= 0;
fpu_op_3 <= 0;
fpuf_2 <= 0;
fpuf_3 <= 0;
fpuf_4 <= 0;
fpuf_5 <= 0;
fpuf_6 <= 0;
fpuf_7 <= 0;
fpuf_8 <= 0;
fpuf_9 <= 0;
fpuf_10 <= 0;
fpuf_11 <= 0;
fpuf_12 <= 0;
fpuf_13 <= 0;
fpuf_14 <= 0;
fpuf_15 <= 0;
fpuf_16 <= 0;
fpuf_17 <= 0;
fpuf_18 <= 0;
fpuf_19 <= 0;
fpuf_20 <= 0;
fpuf_21 <= 0;
rm_1 <= 0;
rm_2 <= 0;
rm_3 <= 0;
rm_4 <= 0;
rm_5 <= 0;
rm_6 <= 0;
rm_7 <= 0;
rm_8 <= 0;
rm_9 <= 0;
rm_10 <= 0;
rm_11 <= 0;
rm_12 <= 0;
rm_13 <= 0;
rm_14 <= 0;
rm_15 <= 0;
rm_16 <= 0;
sign_a <= 0;
sign_a2 <= 0;
sign_b2 <= 0;
sign_a3 <= 0;
sign_b3 <= 0;
exponent_a <= 0;
exponent_b <= 0;
expa_2 <= 0;
expa_3 <= 0;
expb_2 <= 0;
expb_3 <= 0;
mantissa_a <= 0;
mantissa_b <= 0;
mana_2 <= 0;
mana_3 <= 0;
manb_2 <= 0;
manb_3 <= 0;
expa_et_inf <= 0;
expb_et_inf <= 0;
input_is_inf <= 0;
in_inf2 <= 0;
in_inf3 <= 0;
in_inf4 <= 0;
in_inf5 <= 0;
in_inf6 <= 0;
in_inf7 <= 0;
in_inf8 <= 0;
in_inf9 <= 0;
in_inf10 <= 0;
in_inf11 <= 0;
in_inf12 <= 0;
in_inf13 <= 0;
in_inf14 <= 0;
in_inf15 <= 0;
in_inf16 <= 0;
in_inf17 <= 0;
in_inf18 <= 0;
in_inf19 <= 0;
in_inf20 <= 0;
in_inf21 <= 0;
expa_gt_expb <= 0;
expa_et_expb <= 0;
mana_gtet_manb <= 0;
a_gtet_b <= 0;
sign_2 <= 0;
sign_3 <= 0;
sign_4 <= 0;
sign_5 <= 0;
sign_6 <= 0;
sign_7 <= 0;
sign_8 <= 0;
sign_9 <= 0;
sign_10 <= 0;
sign_11 <= 0;
sign_12 <= 0;
sign_13 <= 0;
sign_14 <= 0;
sign_15 <= 0;
sign_16 <= 0;
sign_17 <= 0;
sign_18 <= 0;
sign_19 <= 0;
exponent_small <= 0;
exponent_large <= 0;
expl_2 <= 0;
expl_3 <= 0;
expl_4 <= 0;
expl_5 <= 0;
expl_6 <= 0;
expl_7 <= 0;
expl_8 <= 0;
expl_9 <= 0;
expl_10 <= 0;
expl_11 <= 0;
exp_small_et0 <= 0;
exp_large_et0 <= 0;
exp_small_et0_2 <= 0;
exp_large_et0_2 <= 0;
mantissa_small <= 0;
mantissa_large <= 0;
mantissa_small_2 <= 0;
mantissa_large_2 <= 0;
mantissa_small_3 <= 0;
mantissa_large_3 <= 0;
exponent_diff <= 0;
exponent_diff_2 <= 0;
exponent_diff_3 <= 0;
bits_shifted_out <= 0;
bits_shifted_out_2 <= 0;
bits_shifted <= 0;
large_add <= 0;
large_add_2 <= 0;
large_add_3 <= 0;
large_add_4 <= 0;
large_add_5 <= 0;
small_add <= 0;
small_shift <= 0;
small_shift_2 <= 0;
small_shift_3 <= 0;
small_shift_4 <= 0;
small_shift_nonzero <= 0;
small_is_nonzero_2 <= 0;
small_is_nonzero_3 <= 0;
small_is_nonzero_4 <= 0;
small_fraction_enable <= 0;
sum <= 0;
sum_2 <= 0;
sum_overflow <= 0;
sum_3 <= 0;
sum_4 <= 0;
sum_5 <= 0;
sum_6 <= 0;
sum_7 <= 0;
sum_8 <= 0;
sum_9 <= 0;
sum_10 <= 0;
sum_11 <= 0;
sumround_overflow <= 0;
sum_lsb <= 0;
sum_lsb_2 <= 0;
exponent_add <= 0;
exp_add_2 <= 0;
exp_add_3 <= 0;
exp_add_4 <= 0;
exp_add_5 <= 0;
exp_add_6 <= 0;
exp_add_7 <= 0;
exp_add_8 <= 0;
exp_add_9 <= 0;
diff_shift_2 <= 0;
diff <= 0;
diffshift_gt_exponent <= 0;
diffshift_et_55 <= 0;
diff_2 <= 0;
diff_3 <= 0;
diff_4 <= 0;
diff_5 <= 0;
diff_6 <= 0;
diff_7 <= 0;
diff_8 <= 0;
diff_9 <= 0;
diff_10 <= 0;
diff_11 <= 0;
diffround_overflow <= 0;
exponent_sub <= 0;
exp_sub_2 <= 0;
exp_sub_3 <= 0;
exp_sub_4 <= 0;
exp_sub_5 <= 0;
exp_sub_6 <= 0;
exp_sub_7 <= 0;
exp_sub_8 <= 0;
outfp <= 0;
round_nearest_mode <= 0;
round_posinf_mode <= 0;
round_neginf_mode <= 0;
round_nearest_trigger <= 0;
round_nearest_exception <= 0;
round_nearest_enable <= 0;
round_posinf_trigger <= 0;
round_posinf_enable <= 0;
round_neginf_trigger <= 0;
round_neginf_enable <= 0;
round_enable <= 0;
```

enable

160:BL

```
fpu_op_1 <= fpu_op;
fpu_op_final <= fpu_op_1 ^ (sign_a ^ sign_b);
fpu_op_2 <= fpu_op_final;
fpuf_2 <= fpuf_2;
fpuf_3 <= fpuf_2;
fpuf_4 <= fpuf_3;
fpuf_5 <= fpuf_4;
fpuf_6 <= fpuf_5;
fpuf_7 <= fpuf_6;
fpuf_8 <= fpuf_7;
fpuf_9 <= fpuf_8;
fpuf_10 <= fpuf_9;
fpuf_11 <= fpuf_10;
fpuf_12 <= fpuf_11;
fpuf_13 <= fpuf_12;
fpuf_14 <= fpuf_13;
fpuf_15 <= fpuf_14;
fpuf_16 <= fpuf_15;
fpuf_17 <= fpuf_16;
fpuf_18 <= fpuf_17;
fpuf_19 <= fpuf_18;
fpuf_20 <= fpuf_19;
fpuf_21 <= fpuf_20;
fpu_op_2 <= fpu_op_1;
fpu_op_3 <= fpu_op_2;
rm_1 <= rmode;
rm_2 <= rm_1;
rm_3 <= rm_2;
rm_4 <= rm_3;
rm_5 <= rm_4;
rm_6 <= rm_5;
rm_7 <= rm_6;
rm_8 <= rm_7;
rm_9 <= rm_8;
rm_10 <= rm_9;
rm_11 <= rm_10;
rm_12 <= rm_11;
rm_13 <= rm_12;
rm_14 <= rm_13;
rm_15 <= rm_14;
rm_16 <= rm_15;
sign_a <= opb[63];
sign_b <= opb[63];
sign_a2 <= sign_a;
sign_b2 <= sign_b;
sign_a3 <= sign_a2;
sign_b3 <= sign_b2;
exponent_a <= opa[62:52];
expa_2 <= exponent_a;
expa_3 <= expa_2;
exponent_b <= opb[62:52];
expb_2 <= exponent_b;
expb_3 <= expb_2;
mantissa_a <= opa[51:0];
mana_2 <= mantissa_a;
mana_3 <= mana_2;
mantissa_b <= opb[51:0];
manb_2 <= mantissa_b;
manb_3 <= manb_2;
expa_et_inf <= exponent_a == 2047;
expb_et_inf <= exponent_b == 2047;
input_is_inf <= expa_et_inf | expb_et_inf;
in_inf2 <= input_is_inf;
in_inf3 <= in_inf2;
in_inf4 <= in_inf3;
in_inf5 <= in_inf4;
in_inf6 <= in_inf5;
in_inf7 <= in_inf6;
in_inf8 <= in_inf7;
in_inf9 <= in_inf8;
in_inf10 <= in_inf9;
in_inf11 <= in_inf10;
in_inf12 <= in_inf11;
in_inf13 <= in_inf12;
in_inf14 <= in_inf13;
in_inf15 <= in_inf14;
in_inf16 <= in_inf15;
in_inf17 <= in_inf16;
in_inf18 <= in_inf17;
in_inf19 <= in_inf18;
in_inf20 <= in_inf19;
in_inf21 <= in_inf20;
expa_gt_expb <= (exponent_a > exponent_b);
expb_et_expb <= exponent_a == exponent_b;
mana_gtet_manb <= (mantissa_a > mantissa_b);
a_gtet_b <= (expa_gt_expb | expa_et_expb | mana_gtet_manb);
sign <= (a_gtet_b)? sign_a3 : sign_b3 ^ (fpu_op_3 == 0);
sign_2 <= sign;
sign_3 <= sign_2;
sign_4 <= sign_3;
sign_5 <= sign_4;
sign_6 <= sign_5;
sign_7 <= sign_6;
sign_8 <= sign_7;
sign_9 <= sign_8;
sign_10 <= sign_9;
sign_11 <= sign_10;
sign_12 <= sign_11;
sign_13 <= sign_12;
sign_14 <= sign_13;
sign_15 <= sign_14;
sign_16 <= sign_15;
sign_17 <= sign_16;
sign_18 <= sign_17;
sign_19 <= sign_18;
exponent_small <= (a_gtet_b)? expb_3 : expa_3;
exponent_large <= (a_gtet_b)? expa_3 : expb_3;
expl_2 <= exponent_large;
expl_3 <= expl_2;
expl_4 <= expl_3;
expl_5 <= expl_4;
expl_6 <= expl_5;
expl_7 <= expl_6;
expl_8 <= expl_7;
expl_9 <= expl_8;
expl_10 <= expl_9;
expl_11 <= expl_10;
exp_small_et0 <= exponent_small == 0;
exp_large_et0 <= exponent_large == 0;
exp_small_et0_2 <= exp_small_et0;
exp_large_et0_2 <= exp_large_et0;
mantissa_small <= (a_gtet_b)? manb_3 : mana_3;
mantissa_large <= (a_gtet_b)? mana_3 : manb_3;
mantissa_small_2 <= mantissa_small;
mantissa_large_2 <= mantissa_large;
mantissa_small_3 <= (exp_small_et0)? 0 : mantissa_small_2;
mantissa_large_3 <= (exp_large_et0)? 0 : mantissa_large_2;
exponent_diff <= exponent_large - exponent_small;
exponent_diff_2 <= exponent_diff;
exponent_diff_3 <= exponent_diff_2;
bits_shifted_out <= (exp_small_et0)? 108'b0 : { 1'b1, mantissa_small_2, 55'b0 };
bits_shifted_out_2 <= bits_shifted_out >> exponent_diff_3;
bits_shifted <= |bits_shifted_out_2[52:0];
large_add <= { 1'b0, exp_large_et0_2, mantissa_large_3, 2'b0 };
large_add_2 <= large_add;
large_add_3 <= large_add_2;
large_add_4 <= large_add_3;
large_add_5 <= large_add_4;
small_add <= { 1'b0, exp_small_et0_2, mantissa_small_3, 2'b0 };
small_shift <= (small_add <> exponent_diff_3);
small_fraction_enable <= small_is_nonzero_3 & !small_shift_nonzero;
small_shift_4 <= (small_fraction_enable)? small_shift_LSB : small_shift_3;
small_shift_nonzero <= !small_shift[54:0];
small_is_nonzero <= !exp_small_et0_2;
small_is_nonzero_2 <= small_is_nonzero;
small_is_nonzero_3 <= small_is_nonzero_2;
sum <= large_add_5 + small_shift_4;
sum_overflow <= sum[55];
sum_2 <= sum;
sum_lsb <= sum[0];
sum_3 <= (sum_overflow)? sum_2 >> 1 : sum_2;
sum_lsb_2 <= sum_lsb;
sum_4 <= { sum_3[55:1], sum_lsb_2 | sum_3[0] };
sum_5 <= sum_4;
sum_6 <= sum_5;
sum_7 <= sum_6;
sum_8 <= sum_7;
exponent_add <= (sum_overflow)? exp_10 + 1 : expl_10;
exp_add_2 <= exponent_add;
diff_shift_2 <= diff_shift;
diff <= large_add_5 - small_shift_4;
diff_2 <= diff;
diff_3 <= diff_2;
diffshift_gt_exponent <= diff_shift > expl_10;
diffshift_et_55 <= diff_shift_2 == 55;
diff_4 <= (diffshift_gt_exponent)? diff_3 << expl_11 : diff_3 << diff_shift_2;
diff_5 <= diff_4;
diff_6 <= diff_5;
diff_7 <= diff_6;
diff_8 <= diff_7;
exponent_sub <= (diffshift_gt_exponent)? 0 : expl_11 - diff_shift_2;
exp_sub_2 <= (diffshift_et_55)? 0 : exponent_sub;
round_nearest_mode <= rm_16 == 2'b00;
round_posinf_mode <= rm_16 == 2'b10;
round_neginf_mode <= rm_16 == 2'b11;
round_nearest_trigger <= (fpuf_15)? diff_5[1]? diff_5[1] : sum_5[0] & !sum_5[2];
round_nearest_exception <= round_nearest_mode & round_nearest_trigger;
round_posinf_trigger <= (fpuf_15)? diff_5[1:0] & !sign_13 : sum_5[1:0] & !sign_13;
round_posinf_enable <= round_posinf_mode & round_posinf_trigger;
round_neginf_trigger <= (fpuf_15)? diff_5[1:0] & sign_13 : sum_5[1:0] & sign_13;
round_neginf_enable <= round_neginf_mode & round_neginf_trigger;
round_enable <= round_posinf_enable | round_neginf_enable | round_nearest_enable;
sum_9 <= (round_enable)? sum_8 + 4 : sum_8;
sumround_overflow <= sum_9[55];
sum_10 <= sum_9;
sum_11 <= (sumround_overflow)? sum_10 >> 1 : sum_10;
diff_9 <= (round_enable)? diff_8 + 4 : diff_8;
diffround_overflow <= diff_9[55];
diff_10 <= diff_9;
diff_11 <= (diffround_overflow)? exp_add_8 + 1 : exp_add_8;
exp_add_3 <= exp_add_2;
exp_add_4 <= exp_add_3;
exp_add_5 <= exp_add_4;
exp_add_6 <= exp_add_5;
exp_add_7 <= exp_add_6;
exp_add_8 <= exp_add_7;
exp_add_9 <= (sumround_overflow)? exp_add_8 + 1 : exp_add_8;
exp_sub_3 <= exp_sub_2;
exp_sub_4 <= exp_sub_3;
exp_sub_5 <= exp_sub_4;
exp_sub_6 <= exp_sub_5;
exp_sub_7 <= exp_sub_6;
exp_sub_8 <= (diffround_overflow)? exp_sub_7 + 1 : exp_sub_7;
outfp <= (fpuf_21)? { sign_19, exp_sub_8, diff_11[53:2] } : { sign_19, exp_add_9, sum_11[53:2] };
```

Leaf 102:AL