191:BS
NextState = StatePktRange;
Leaf_172:AL
Leaf_128:AL
114:AL
166:AL
140:AL
128:AL
115:IF
167:IF
141:IF
129:IF
Reset
!(Reset)
116:BL
Pkt_type_rmon_dl1 <= 0;
Pkt_length_rmon_dl1 <= 0;
Pkt_err_type_rmon_dl1 <= 0;
122:BL
Pkt_type_rmon_dl1 <= Pkt_type_rmon;
Pkt_length_rmon_dl1 <= Pkt_length_rmon;
Pkt_err_type_rmon_dl1 <= Pkt_err_type_rmon;
!(Reset)
Reset
170:NS
CurrentState <= NextState;
168:NS
CurrentState <= StateIdle;
(Apply_rmon_dl1 & !Apply_rmon_dl2)
!((Apply_rmon_dl1 & !Apply_rmon_dl2))
142:BS
Apply_rmon_pulse = 1;
144:BS
Apply_rmon_pulse = 0;
!(Reset)
Reset
135:BL
Apply_rmon_dl1 <= Apply_rmon;
Apply_rmon_dl2 <= Apply_rmon_dl1;
130:BL
Apply_rmon_dl1 <= 0;
Apply_rmon_dl2 <= 0;
Reg_next
Leaf_114:AL
Leaf_166:AL
Leaf_140:AL
148:AL
207:AL
282:AL
172:AL
149:IF
208:IF
283:IF
173:CS
!(Reset)
Reset
((CurrentState == StatePktLength) || (CurrentState == StatePktNumber) || (CurrentState == StatePktType) || (CurrentState == StatePktRange))
!(((CurrentState == StatePktLength) || (CurrentState == StatePktNumber) || (CurrentState == StatePktType) || (CurrentState == StatePktRange)))
!(Reset)
Reset
CurrentState
CurrentState
CurrentState
CurrentState
CurrentState
CurrentState
155:IF
210:BS
Reg_apply = 1;
212:BS
Reg_apply = 0;
285:IF
179:CA
199:CA
194:CA
174:CA
189:CA
184:CA
150:BL
PktTypeReg <= 0;
PktLengthReg <= 0;
PktErrTypeReg <= 0;
(Apply_rmon_pulse && (CurrentState == StateIdle))
((CurrentState != StateIdle) && Apply_rmon_pulse)
!(((CurrentState != StateIdle) && Apply_rmon_pulse))
284:NS
Reg_drop_apply <= 0;
156:BL
PktTypeReg <= Pkt_type_rmon_dl1;
PktLengthReg <= Pkt_length_rmon_dl1;
PktErrTypeReg <= Pkt_err_type_rmon_dl1;
Leaf_207:AL
286:NS
Reg_drop_apply <= 1;
288:NS
Reg_drop_apply <= 0;
180:IF
200:BS
NextState = StateIdle;
195:IF
175:IF
190:IF
185:IF
!(Reg_next)
Reg_next
Reg_next
!(Reg_next)
!(Apply_rmon_pulse)
Apply_rmon_pulse
!(Reg_next)
!(Reg_next)
Reg_next
Leaf_148:AL
Leaf_282:AL
183:BS
NextState = CurrentState;
181:BS
NextState = StatePktNumber;
196:BS
NextState = StateIdle;
198:BS
NextState = CurrentState;
178:BS
NextState = StateIdle;
176:BS
NextState = StatePktLength;
193:BS
NextState = CurrentState;
188:BS
NextState = CurrentState;
186:BS
NextState = StatePktType;
215:AL
267:AL
216:IF
268:CS
Reset
!(Reset)
CurrentState
CurrentState
CurrentState
CurrentState
CurrentState
218:CS
271:CA
277:CA
269:CA
273:CA
275:CA
217:NS
Reg_addr <= 0;
CurrentState
CurrentState
CurrentState
CurrentState
CurrentState
272:BS
Reg_data = 1;
278:BS
Reg_data = 0;
270:BS
Reg_data = PktLengthReg;
274:BS
Reg_data = 1;
276:BS
Reg_data = 1;
234:CA
221:CA
223:CA
219:CA
262:CA
Leaf_267:AL
235:CS
263:NS
Reg_addr <= 5'd05;
222:NS
Reg_addr <= 5'd01;
PktErrTypeReg
PktErrTypeReg
PktErrTypeReg
PktErrTypeReg
PktErrTypeReg
236:CA
240:CA
242:CA
259:CA
238:CA
220:NS
Reg_addr <= 5'd00;
243:IF
237:NS
Reg_addr <= 5'd05;
260:NS
Reg_addr <= 5'd05;
(PktLengthReg < 64)
!((PktLengthReg < 64))
239:NS
Reg_addr <= 5'd06;
245:IF
241:NS
Reg_addr <= 5'd07;
244:NS
Reg_addr <= 5'd08;
!((PktLengthReg == 64))
(PktLengthReg == 64)
247:IF
246:NS
Reg_addr <= 5'd09;
!((PktLengthReg < 128))
(PktLengthReg < 128)
249:IF
248:NS
Reg_addr <= 5'd10;
(PktLengthReg < 256)
!((PktLengthReg < 256))
251:IF
250:NS
Reg_addr <= 5'd11;
!((PktLengthReg < 512))
(PktLengthReg < 512)
224:CS
253:IF
252:NS
Reg_addr <= 5'd12;
PktTypeReg
PktTypeReg
PktTypeReg
PktTypeReg
(PktLengthReg < 1024)
!((PktLengthReg < 1024))
227:CA
231:CA
229:CA
225:CA
255:IF
254:NS
Reg_addr <= 5'd13;
!((PktLengthReg < 1519))
(PktLengthReg < 1519)
228:NS
Reg_addr <= 5'd03;
232:NS
Reg_addr <= 5'd04;
230:NS
Reg_addr <= 5'd16;
226:NS
Reg_addr <= 5'd02;
258:NS
Reg_addr <= 5'd15;
256:NS
Reg_addr <= 5'd14;
Leaf_215:AL