ECE 485/585 **Dr. Faust**

Fall 2019 **Achraf Dayoub**

Homework 2

1. [60] Use an on-line article index from the PSU library, Google scholar, or another library of your choice to obtain and read a copy of the article by David A. Patterson, "Latency Lags Bandwidth", Communications of the ACM, 47:10, October 2004, 71- 75. Hint: there's a link to the article on the course syllabus!

a) [5] Patterson examines performance milestones for bandwidth and latency for

what four technological areas?

Performance milestones in bandwidth and latency for

- Disks
- Processors
- local area networks
- memory modules

b) [5] What does he conclude about the improvement in latency in the time it takes

for bandwidth to double?

He concludes about the improvement in latency in the time it takes for bandwidth to double "The relative improvements in latency over that shorter time are still similar to the latency improvements over the longer time"

c) [5] What three techniques have been developed to cope with this imbalance?

- Caching: Leveraging capacity to help latency
- Prediction: Leveraging bandwidth to again help latency
- Replication: Leveraging capacity to again help latency

d) [5] Rank the following three from most to least important criteria for memory

and disk drives by placing the numbers 1 through 3 next to each.

o Capacity

o Latency

o Bandwidth

1. Capacity
2. Bandwidth
3. Latency

e) [5] What does he assert is the annual capacity improvement for performance oriented (e.g. SCSI) disk drives?

Performance-oriented versions of memory and storage, capacity improves more rapidly than bandwidth.

f) [5] Using only the Seagate ST373453 and the ST4000VN000 (introduced in 2013) do you think this rate of improvement has held true the decade? Why or why not? You can easily find information on the ST4000VN000 on the web.

Yes, the capacity of ST4000VN000 is 4TB which much higher than ST373453 73.4 GB

g) [5] What does he assert is the annual latency improvement for disk drives?

He asserts is the annual latency improvement for disk drives "Annual Latency hasn't improved by no more than a factor of 1.09."

h) [5] Do you think this has held true for the decade 2003-2013? Why or why not?

Yes, I think this has held true for the decade 2003-2013 because the looking at the tables that the author provided it we can see that we that the improvement factor did not have a big change and it maintain the same for the newer disk drives it was increasing in almost the same rate year after year.

i) [5] What does he assert is the annual bandwidth improvement for disk drives?

He asserts is the annual bandwidth improvement for disk drives is 1.28

j) [5] Do you think this has held true for the decade? Why or why not?

Yes, I think this has held true for the decade because looking at the table that the author provided, we can look at the years between 1983-1993 we can see that the number hold true for a decade.

k) [5] When released the ST4000VN000 cost approximately $200. What was the approximate cost/GB for the ST4000VN000?

Cost/GB = 200 dollars & 4TB = 4000 Gigabytes

⇨ 200/4000 = 0.05 $/GB

l) [5] At its recent introduction several years ago, the Seagate 10TB BarraCuda Pro was the largest consumer hard disk drive. At current prices, what is the approximate cost/GB for the Seagate 14TB BarraCuda Pro?

Cost/GB = 579.99 dollars & 14TB = 14000 Gigabytes

⇨ 579.99 /14000 = 0.04142 $/GB

2. [70] The Motorola 68000 was a popular microprocessor. It and its successors, the 68020 and 68030, have been used in everything from early workstations and computers (Tandy TRS-80, Sun Microsystems SUN-1, Apple Lisa and Macintosh) to video game consoles (Sega) to embedded systems (HP LaserJet, TI graphing calculators). Its architecture is still in use. A simpler version of its architecture is employed in Freescale's ColdFire series of microprocessors and microcontrollers. Research the architecture of the 68000 (you'll find many of the documents on-line).
Freescale (successor to Motorola's Semiconductor Products Sector) is now responsible for the 68000 family.

a) [10] Does the 68000-architecture use memory-mapped, direct I/O or both?
Memory-mapped I/O

b) [10] Aside from I/O interrupts, give two examples of exceptions.

1. Trace exceptions (higher priority than the interrupt)
2. Reset exceptions

c) [10] Aside from these, is there an instruction that can be used to explicitly invoke the interrupt mechanism? If so, what is it? If not, why not?

Yes, address error, and bus error are considered exceptions from group 0 while interrupts error is considered exceptions from group 1.
Exceptions from group 0 always override an active exception from group 1 or group 2

d) [10] How is the address of the interrupt service procedure obtained? Be specific but brief.

It will reserve an area of read/write memory (Stack) typically used by a microcomputer during subroutine calls or occurrence of an interrupt. The microcomputer saves in the stack the contents of the program counter before executing the subroutine or program counter contents and other status information before executing the interrupt service routine. Thus, the microcomputer can return to the main program after execution of the subroutine or the interrupt service routine The technique used to find the starting address of the service routine (commonly known as the interrupt address vector) varies from one processor to another. With some microprocessors, the manufacturers define the fixed starting address for each interrupt. Other manufacturers use an indirect approach by defining fixed locations where the interrupt address vector is stored.

e) [10] What registers (if any) are saved by the processor prior to beginning execution of the interrupt service procedure? What information is contained? Be specific but brief.

1. Eight 32-bit general-purpose data registers (D0-D7)
2. Eight address registers (A0-A7).
3. The last address register is the stack pointer, and assemblers accept the label SP as equivalent to A7.

f) [10] What instruction is used to return from the interrupt and how is the return address provided? What restrictions are there on the use of this instruction? How are they enforced?

Interrupt service routines should be terminated with an IRET (interrupt return) instruction. An IRET (Interrupt Return) is used as return instruction at the end of a service routine for both hardware and software interrupts.
NT (nested task) controls the IRET operation. If NT = 0, a usual return from interrupt is taken by the Pentium by popping EFLAGS, CS, and EIP from the stack. If NT = 1, the Pentium returns from an interrupt via task switching.

g) [10] Cite your references by author, document title, and (if accessed on-line)
URL.

Mohamed Rafiquzzaman, “Microprocessor Theory and Applications with 68000/68020 and Pentium.”

3. [40] Consider the following 8086 assembly language code that uses an 8255.

```
PORTA EQU   0A8H
PORTB EQU   0AAH
CNTRL EQU   0AEH
```

```
PROG SEGMENT
ASSUME CS:  PROG
            MOV AL, 99H
            OUT CNTRL, AL
BEGIN:      IN AL, PORTA
            AND AL, 0C0H
            JPE LEDON
            MOV AL, 00H
            OUT PORTB, AL
            JMP BEGIN
LEDON:      MOV AL, 04H
            OUT PORTB, AL
            JMP BEGIN
            PROG ENDS
            END
```

a) [5] Does this code use memory-mapped or direct I/O? How can you tell?

We can say the code is using direct I/O because the addresses of ports and control registers are represented by 8-bit values.
Since direct I/O uses 8-bit addresses, and memory-mapped I/O uses 16-bit addresses. We can conclude that it is using direct I/O.

b) [5] What is the address of the 8255's control register?

The code has CNTRL EQU 0AEH
=> The address of the control register of 8255 is hex 0x0AE.

c) [5] What is the address of the 8255's A port?

The code has PORTA EQU 0A8H
=> The address of the control register of 8255 is hex 0x0A8.

d) [5] What is the address of the 8255's B port?

The code has PORTB EQU 0AAH
=> The address of the control register of 8255 is hex 0x0AA.

e) [5] What is the address of the 8255's C port?

The address of the PORT C of 8255 will be hex 0x0AC. It can be found from part (f).

f) [5] Which bits of the address are connected to pins A1 and A0 respectively of the 8255?

	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS
PORT A	1	0	1	0	1	0	0	0	0A8H
PORT B	1	0	1	0	1	0	1	0	0AAH
PORT C	1	0	1	0	1	1	0	0	0ACH
CONTROL REGISTER	1	0	1	0	1	1	1	0	0AEH

From the table, it can be seen that address bits A_1 and A_2 are controlling the selection of PORT of the register. A. So, address bits A_1 and A_2 are connected to the A1 and A0 pins of 8255.

g) [5] How is the 8255 being configured? Be specific and comprehensive.

Address bits A3 to A7 are used to generate the CS bit of 8255 and A1 and A2 are connected to the A1 and A0 pins of 8255. And other corresponding pins are connected to 8086.

h) [5] What does this program do? Be specific.

By moving 99H in control register, I/O mode is selected, PORT A is declared as an input port and PORT B is declared as an output port.
A subroutine LEDON is called and the third pin of PORT B is being made ON (04H = 0000 0100) and it is being made OFF by passing 00H on PORT B. And this process is being repeated by instruction JMP BEGIN by jumping to the start again.

4. [10] In the diagram below ETA is the enable signal for the transmitter's drive logic. When enabled, it drives data on the bus. The transmitter then signals that there is valid data on the bus by asserting Req. The receiving, upon seeing Req, samples the data from the bus and asserts Ack to

acknowledge receipt. The transmitter then disables its driver and de-asserts Req (not shown). In response, the receiver de-asserts Ack (not shown).

What kind of interface is this?

Fully Interlocked