Migration Note

Eon Flash

	P/N	Datasheet Version
From	EN25F16	Rev. H
To	EN25QH16	Rev. D

1. INTRODUCTION

The migration note introduces how to implement a system design from Eon flash EN25F16 to EN25QH16.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table highlights the major features of these two devices.

Features	EN25QH16	EN25F16
Process	90nm	130nm
Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Pin to Pin[1.]	Yes	Yes
SPI Mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI Frequency	104MHz (standard mode) 80MHz @ dual & quad mode	100MHz (standard mode)
Sector Architecture	Uniform ● 512 sectors of 4Kbyte ● 32 blocks of 64Kbyte ● Any sector or block can be erased individually.	Uniform ● 512 sectors of 4Kbyte ● 32 blocks of 64Kbyte ● Any sector or block can be erased individually.
Lockable OTP Security Sector	512 Bytes	128 Bytes
HOLD# Pin	Yes	Yes
Page Programming	Yes	Yes
EQPI Mode	Yes	No
Software Reset	Yes	No
SFDP Signature	Yes	No
Minimum Endurance Cycle	100K	100K
Package[1.]	✓ 8 pins SOP 150mil body width ✓ 8 pins SOP 200mil body width ✓ 8 contact VDFN (5x6mm) ✓ 8 pins PDIP 24 balls BGA (6x8mm) ● All Pb-free packages are RoHS compliant	✓ 8 pins SOP 150mil body width ✓ 8 pins SOP 200mil body width ✓ 8 contact VDFN (5x6mm) ✓ 8 pins PDIP ● All Pb-free packages are RoHS compliant

Note:

1. Please refer to the datasheet in detail.

3. HARDWARE CONSIDERATIONS

3.1. I_{CC} Comparison

Current	EN25QH16	EN25F16	Unit
	Max (@ Single 104MHz)	Max (@ Single 100MHz)	
Read I_{CC3}	25	25	mA
Page Program (PP) I_{CC4}	28	28	mA
Sector Erase (SE) I_{CC6}	25	25	mA
Standby I_{CC1}	20	20	µA

3.2. Pins Description

EN25QH16		EN25F16	
Pin Name	Function	Pin Name	Function
CLK	Serial Clock Input	CLK	Serial Clock Input
DI (DQ0)	Serial Data Input (Data Input Output 0) *1	DI	Serial Data Input
DO (DQ1)	Serial Data Output (Data Input Output 1) *1	DO	Serial Data Output
CS#	Chip Enable	CS#	Chip Enable
WP# (DQ2)	Write Protect (Data Input Output 2) *2	WP#	Write Protect
HOLD#(DQ3)	HOLD# pin (Data Input Output 3) *2, *3	HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)	Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground	Vss	Ground

Note:

1. DQ0 and DQ1 are used for Dual and Quad instructions.
2. DQ0 ~ DQ3 are used for Quad instructions.
3. The HOLD# function is disabled from Quad SPI operation.

* Users must take care of the different pin definition!

4. SOFTWARE CONSIDERATIONS

4.1. Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, ID15~ID8: memory type, ID7~ID0: memory density) comparison.

4.1.1. For **EN25QH16**：MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	7015h	

4.1.2. For **EN25F16**：MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	3115h	

4.2. Instruction Set Comparison

4.2.1. For **EN25QH16 and EN25F16**：Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQPI	38h						
RSTQIO(2) / Release Quad I/O or Fast Read Enhanced Mode	FFh						
RSTEN	66h						
RST(1)	99h						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)(3)					continuous(4)
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
Enter OTP mode	3Ah						
Read SFDP mode	5Ah	A23-A16	A15-A8	A7-A0	dummy	(ID7-ID0)	(Next Byte) continuous

Notes:

1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
4. The Status Register contents will repeat continuously until CS# terminates the instruction.
5. The Device ID will repeat continuously until CS# terminates the instruction.
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.

Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) (1)	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8(2)	A7-A0, dummy (2)	(D7-D0, ...) (1)			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy (4)	(dummy, D7-D0) (5)	(D7-D0, ...) (3)			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data

DQ_0 = (D6, D4, D2, D0)

DQ_1 = (D7, D5, D3, D1)

2. Dual Input Address

DQ0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0

DQ1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1

3. Quad Data

DQ0 = (D4, D0, …….)

DQ1 = (D5, D1, …….)

DQ2 = (D6, D2, …….)

DQ3 = (D7, D3, …….)

4. Quad Input Address

DQ0 = A20, A16, A12, A8, A4, A0, dummy 4, dummy 0

DQ1 = A21, A17, A13, A9, A5, A1, dummy 5, dummy 1

DQ2 = A22, A18, A14, A10, A6, A2, dummy 6, dummy 2

DQ3 = A23, A19, A15, A11, A7, A3, dummy 7, dummy 3

5. Quad I/O Fast Read Data

DQ0 = (dummy 12, dummy 8, dummy 4, dummy 0, D4, D0)

DQ1 = (dummy 13, dummy 9, dummy 5, dummy 1, D5, D1)

DQ2 = (dummy 14, dummy 10, dummy 6, dummy 2, D6, D2)

DQ3 = (dummy 15, dummy 11, dummy 7, dummy 3, D7, D3)

Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.

2. Users must modify the appropriate codes for EN25QH16!

4.3. Different Block Protection Area

* The definitions of Block Protection Area are different!

4.3.1. For **EN25QH16**：

Protected Area Sizes Sector Organization Table

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 31	1F0000h-1FFFFFh	64KB	Upper 1/32
0	0	1	0	Block 30 to 31	1E0000h-1FFFFFh	128KB	Upper 2/32
0	0	1	1	Block 28 to 31	1C0000h-1FFFFFh	256KB	Upper 4/32
0	1	0	0	Block 24 to 31	180000h-1FFFFFh	512KB	Upper 8/32
0	1	0	1	Block 16 to 31	100000h-1FFFFFh	1024KB	Upper 16/32
0	1	1	0	All	000000h-1FFFFFh	2048KB	All
0	1	1	1	All	000000h-1FFFFFh	2048KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 0	000000h-00FFFFh	64KB	Lower 1/32
1	0	1	0	Block 0 to 1	000000h-01FFFFh	128KB	Lower 2/32
1	0	1	1	Block 0 to 3	000000h-03FFFFh	256KB	Lower 4/32
1	1	0	0	Block 0 to 7	000000h-07FFFFh	512KB	Lower 8/32
1	1	0	1	Block 0 to 15	000000h-0FFFFFh	1024KB	Lower 16/32
1	1	1	0	All	000000h-1FFFFFh	2048KB	All
1	1	1	1	All	000000h-1FFFFFh	2048KB	All

4.3.2. For **EN25F16**：

Protected Area Sizes Sector Organization Table

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Block 0 to 30	000000h-1EFFFFh	1984KB	Lower 31/32
0	1	0	Block 0 to 29	000000h-1DFFFFh	1920KB	Lower 30/32
0	1	1	Block 0 to 27	000000h-1BFFFFh	1792KB	Lower 28/32
1	0	0	Block 0 to 23	000000h-17FFFFh	1536KB	Lower 24/32
1	0	1	Block 0 to 15	000000h-0FFFFFh	1024KB	Lower 16/32
1	1	0	All	000000h-1FFFFFh	2048KB	All
1	1	1	All	000000h-1FFFFFh	2048KB	All

4.4. Different RDSR Bits Definition

* The definition of RDSR bits [S6:S5] are different!

4.4.1. For **EN25QH16**：

Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	QE (Quad Enable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = Quad enable 0 = not Quad enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table “Protected Area Sizes Sector Organization”.

4.4.2. For **EN25F16**：

Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table “Protected Area Sizes Sector Organization”.

4.5. Different One Time Programming Definition

* The definitions of OTP are different!

4.5.1. For **EN25QH16**：

OTP Sector Address

Sector	Sector Size	Address Range
511	512 Bytes	1FF000h – 1FF1FFh

Note: The OTP sector is mapping to sector 511

4.5.2. For **EN25F16**：

OTP Sector Address

Sector	Sector Size	Address Range
511	128 Bytes	1FF000h – 1FF07Fh

Note: The OTP sector is mapping to sector 511

4.6. Serial Flash Discoverable Parameters (SFDP) Mode

Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode. Writing the SFDP Query command “5Ah”, the system can read SFDP information at the address given. A reset command is required to exit SFDP mode and go back to read array mode. The system can write the SFDP Query command only when the device is in read mode.

4.6.1. For **EN25QH16**：YES

4.6.2. For **EN25F16**：NO

5. PERFORMANCE DIFFERENCES

5.1. KEY AC PARAMETER PERFORMANCE

Parameter		EN25QH16	EN25F16
t_{CH} (serial clock high time)		Min @ 4ns	Min @ 4ns
t_{CL} (serial clock low time)		Min @ 4ns	Min @ 4ns
t_{CLCH}(serial clock rise time)		Min @ 0.1V / ns	Min @ 0.1V / ns
t_{CLCL}(serial clock fall time)		Min @ 0.1V / ns	Min @ 0.1V / ns
t_{CHSH}(CS# active setup / hold time)		Min@ 5ns	Min@ 5ns
t_{SHSL}	(CS# high time for read) (CS# high time for program/erase)	Min @ 15ns Min @ 50ns	Min @ 100ns
t_{DSU}(Data in setup time)		Min @ 2ns	Min @ 2ns
t_{DH}(Data in hold time)		Min @ 5ns	Min @ 5ns

5.2. Power-On Timings

Parameter	Description	EN25QH16	EN25F16
t_{VSL}	V_{CC}(min) to CS# low	10µs	10µs
t_{PUW}	Time delay to Write instruction	10ms	10ms

5.3. ERASE AND PROGRAM PERFORMANCE

The ERASE and PROGRAM Performance Comparison

Parameter	EN25QH16		EN25F16		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	1.3	5	ms
Sector Erase Time	0.06	0.3	0.09	0.3	sec
Block Erase Time	0.4	2	0.4	2	sec
Chip Erase Time	12	30	7	35	sec

Revisions List

Revision No	Description	Date
A	Initial Release	2011/2/24