

MICROPROCESSORS AND INTERFACING

DESIGN ASSIGNMENT

IC TESTER

LIST OF TEAM MEMBERS

SERIAL NUMBER	NAME	BITS ID
1	KSHITIJ CHHABRA	2017A8PS0691G
2	SHIRIN KAUSHIK	2017AAPS0229G
3	HARSHWARDHAN SHIRODKAR	2017AAPS0169G
4	ACHYUTH E M	2017AAPS0235G
5	PRANAY MATHUR	2017A8PS0487G

ASSUMPTIONS

1. The first key pressed is always a digit (backspace is never pressed in the beginning).
2. Enter is pressed after the IC number.
3. Test key is pressed only after the enter key.
4. 5V supply is available from SMPS.

PROBLEM STATEMENT

Design a Microprocessor based Tester to test the logical functioning of the following chips:

1. 7400
2. 7408
3. 7432
4. 7486
5. 747266

The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard.

The keyboard has keys 0-9, backspace, enter and test.

The user places the IC in a ZIF socket, closes it, then enters the IC number, followed by enter key.

The IC number is displayed on the 7 segment display.

The testing will start once the user presses the test key.

After Test, the result PASS/FAIL must be displayed on the 7 segment display.

COMPONENTS USED

SERIAL NO.	NAME OF COMPONENT	QUANTITY
1	8086 Microprocessor	1
2	8255A (Programmable Peripheral Interface with 24 I/O lines)	3
3	74LS138 (3:8 Decoder)	1
4	74LS373 (Octal D-type transparent latches with 3 state outputs)	2
5	6116 (4K (2K*2) Static RAM)	2
6	2732 (8K (4K*2) EPROM)	2
7	7-Segment Anode Display	6
8	74LS245 (Octal Bus Transceivers with 3 state outputs)	3
9	OR Gates (2 Input)	5
10	NOT Gate	3
11	SW-SPDT (Interactive SPDT switch (Momentary Action))	1
12	7400	1
13	7408	1
14	7432	1
15	7486	1
16	747266	1

PIN OUTS OF COMPONENTS USED

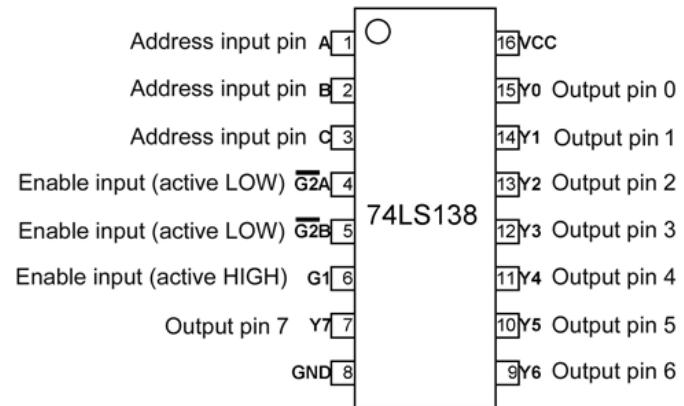
8086

		8086	MAX MODE	MIN MODE
Vss (GND)	1		40 Vcc (5P)	
AD14	2		39 AD15	
AD13	3		38 A16/S3	
AD12	4		37 A17/S4	
AD11	5		36 A18/S5	
AD10	6		35 A19/S6	
AD9	7		34 BHE/S7	
AD8	8		33 MN/MX	
AD7	9		32 RD	
AD6	10		31 RQ/GT0	HOLD
AD5	11		30 RQ/GT1	HLDA
AD4	12		29 LOCK	WR
AD3	13		28 S2	M/I/O
AD2	14		27 S1	DT/R
AD1	15		26 S0	DEN
AD0	16		25 QS0	ALE
NMI	17		24 QS1	INTA
INTR	18		23 TEST	
CLK	19		22 READY	
Vss (GND)	20		21 RESET	

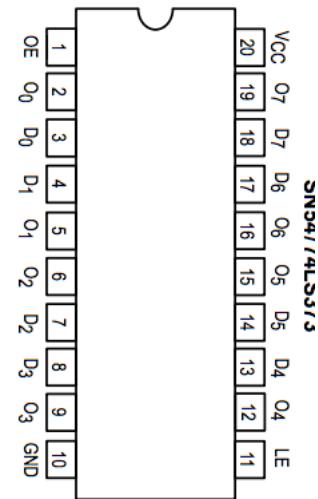
8255A

PA ₃	1	8255A	40 PA ₄
PA ₂	2		39 PA ₅
PA ₁	3		38 PA ₆
PA ₀	4		37 PA ₇
RD	5		36 WR
CS	6		35 RESET
GND	7		34 D ₀
A ₁	8		33 D ₁
A ₀	9		32 D ₂
PC ₇	10		31 D ₃
PC ₆	11		30 D ₄
PC ₅	12		29 D ₅
PC ₄	13		28 D ₆
PC ₀	14		27 D ₇
PC ₁	15		26 V _{CC} (+5V)
PC ₂	16		25 PB ₇
PC ₃	17		24 PB ₆
PB ₀	18		23 PB ₅
PB ₁	19		22 PB ₄
PB ₂	20		21 PB ₃

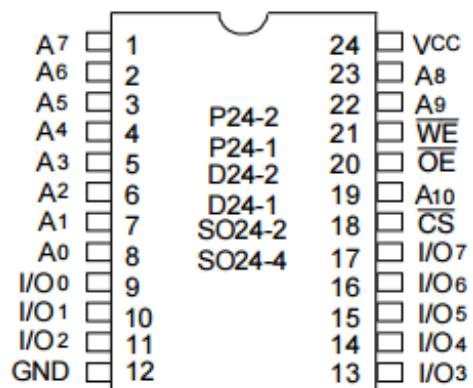
74LS138



74LS373

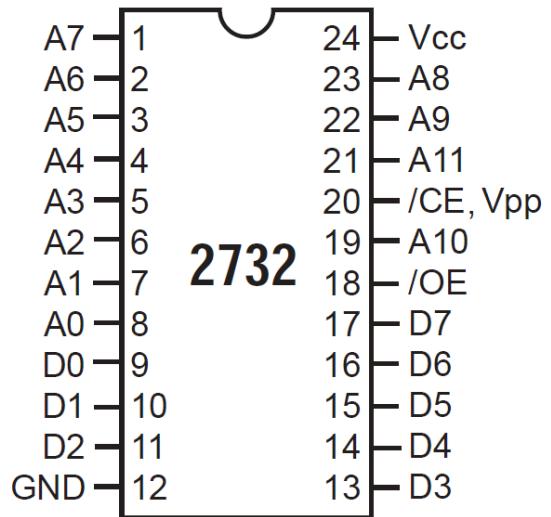


6116 (RAM)

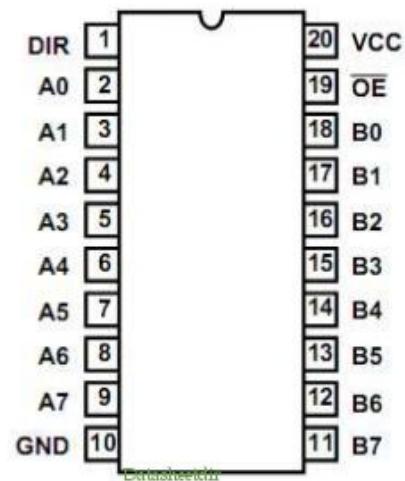


3089 drw 02

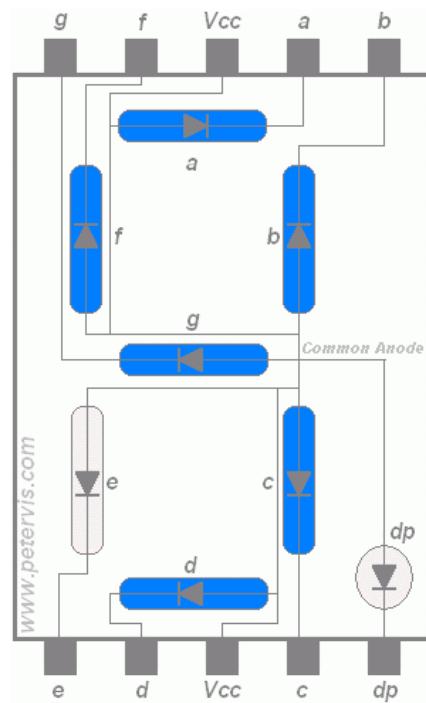
2732 (ROM)



74LS245

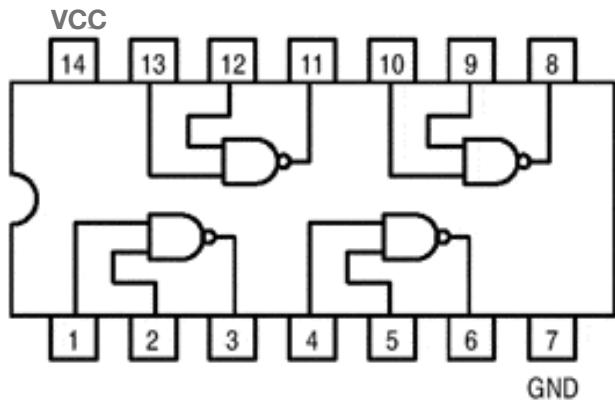


7 SEGMENT DISPLAY

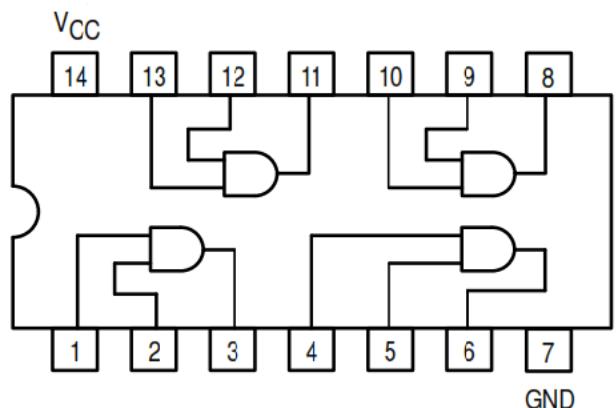


ICS TO BE TESTED

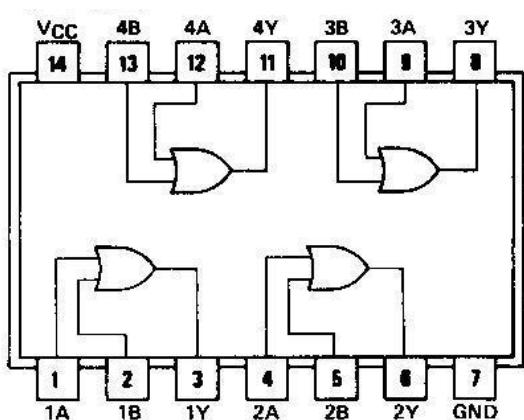
7400



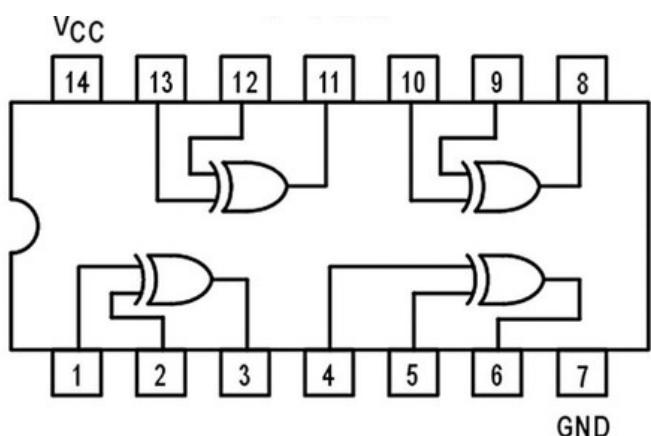
7408



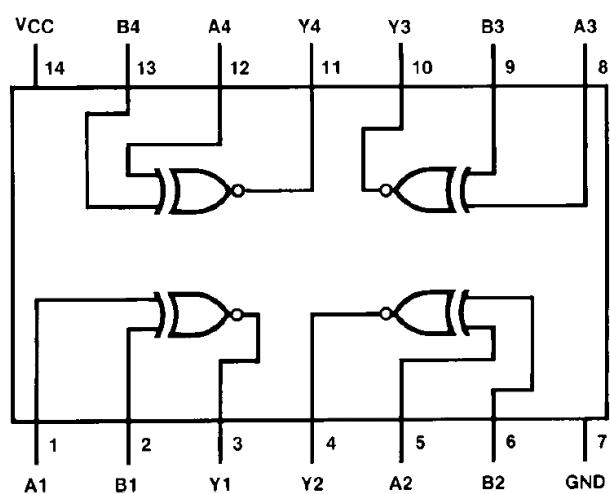
7432



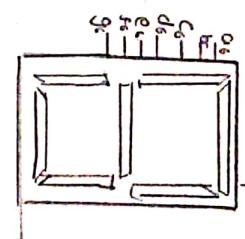
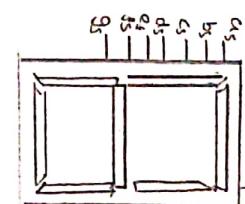
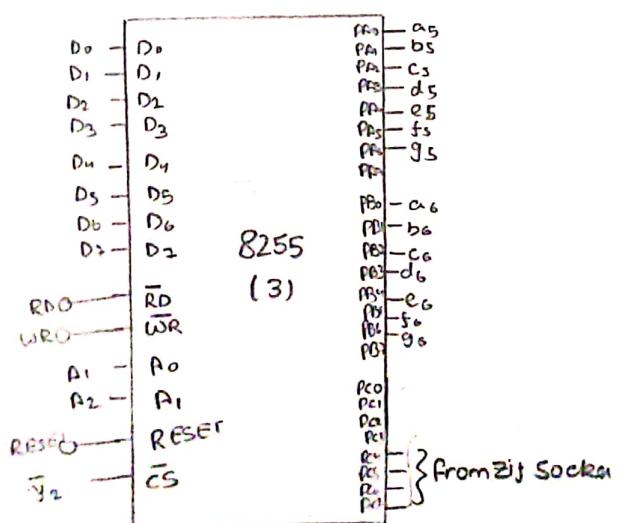
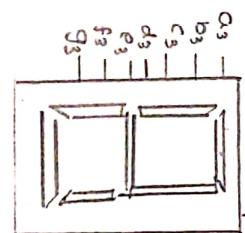
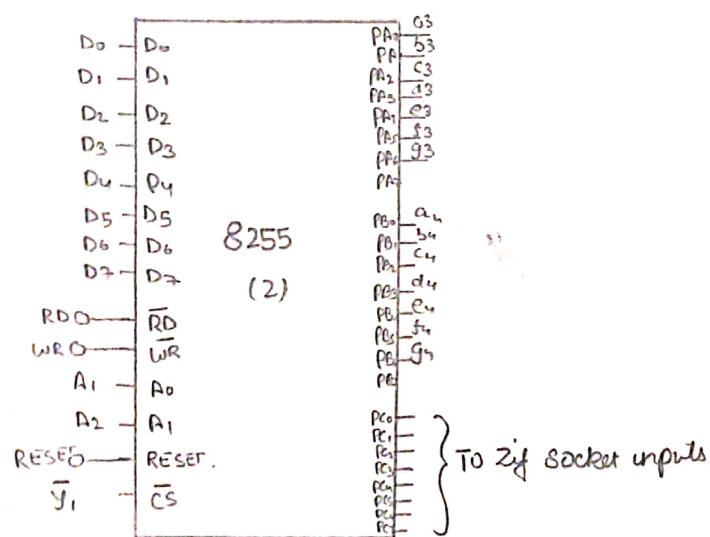
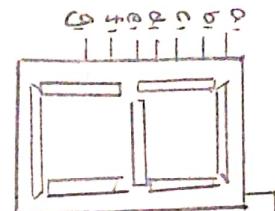
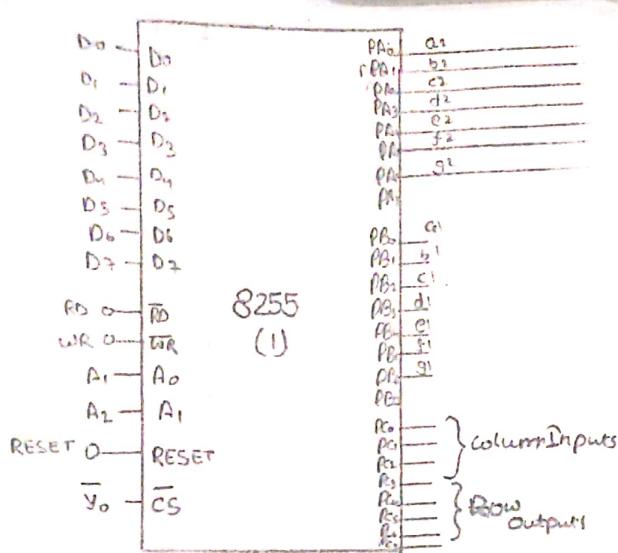
7486



747266

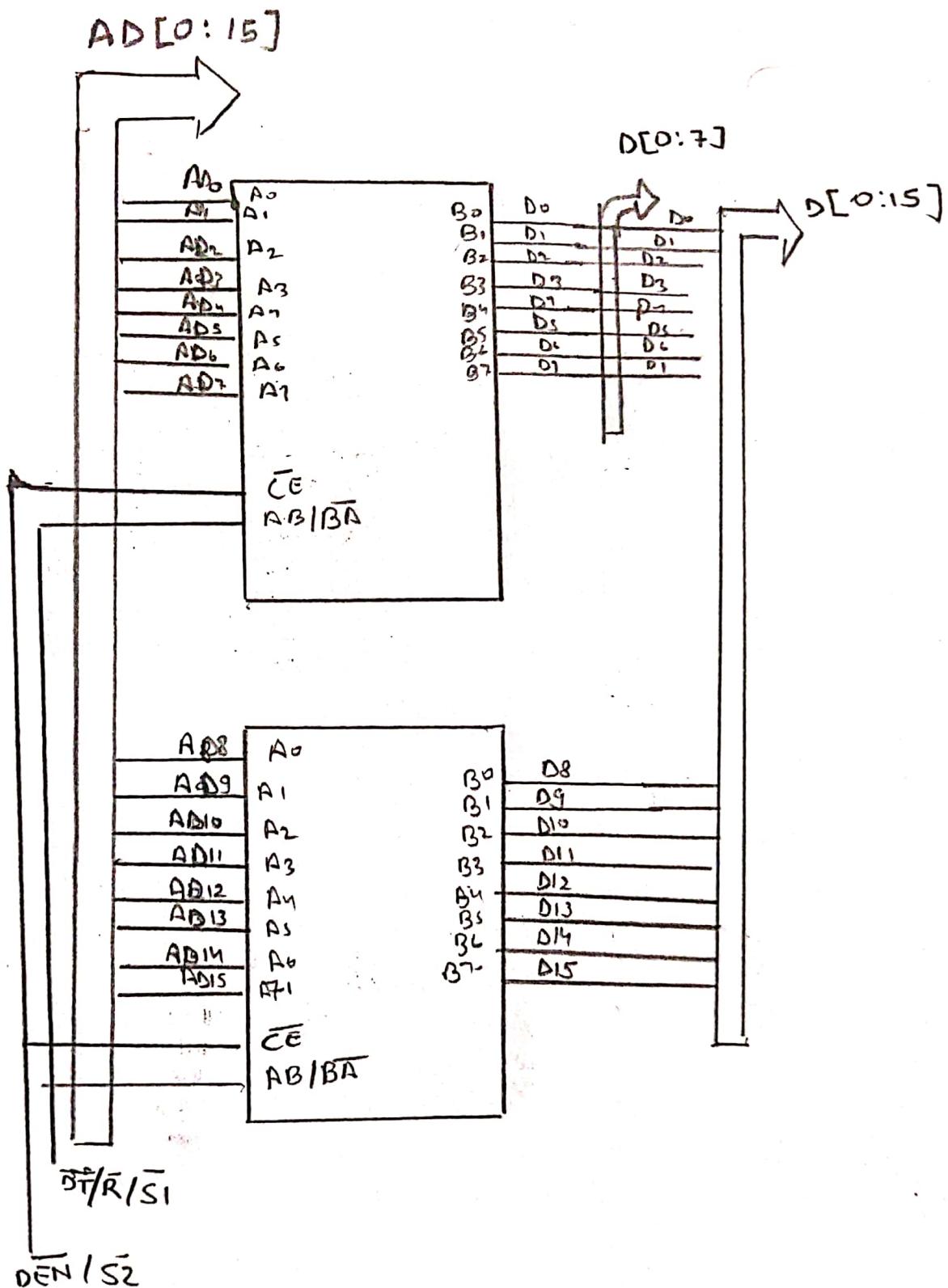


Interfacing 8255 with displays

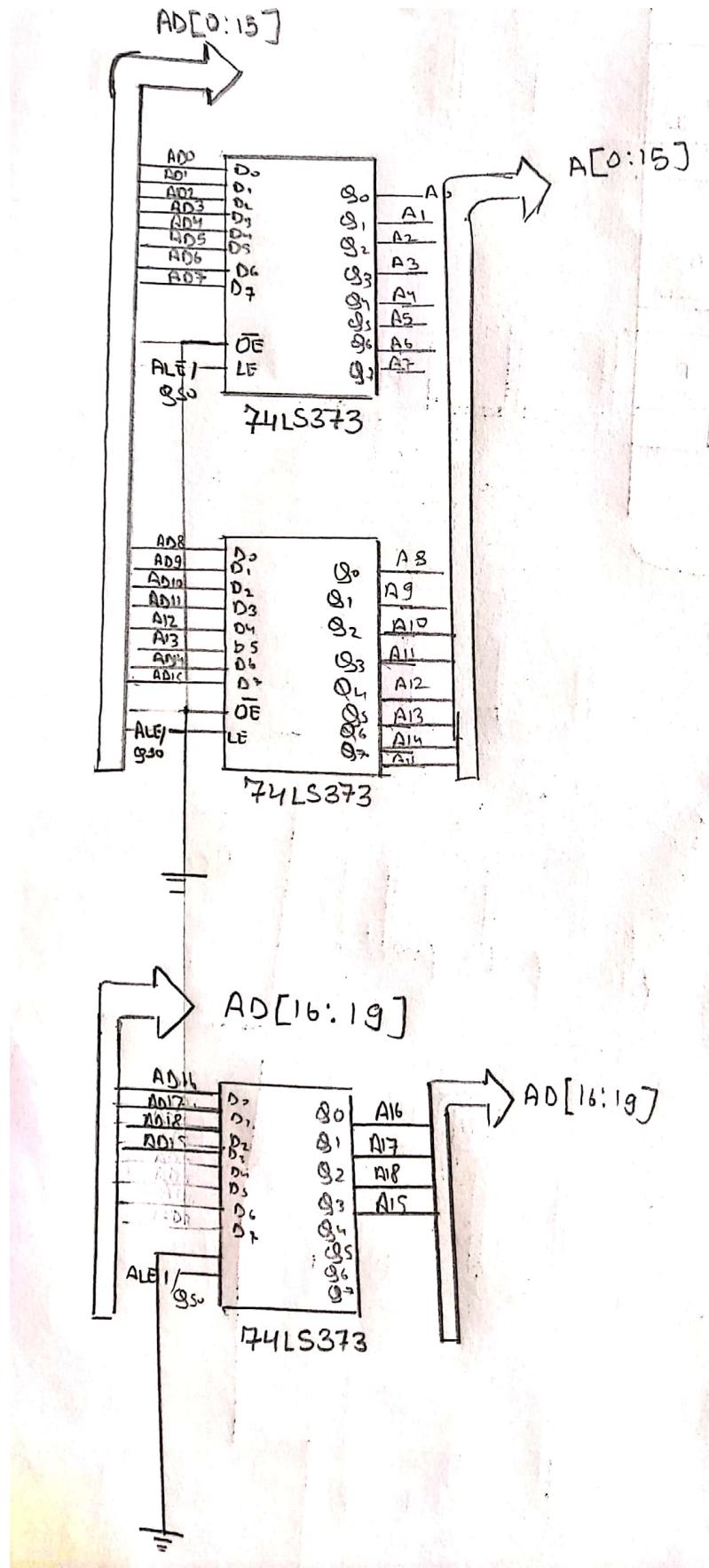


51

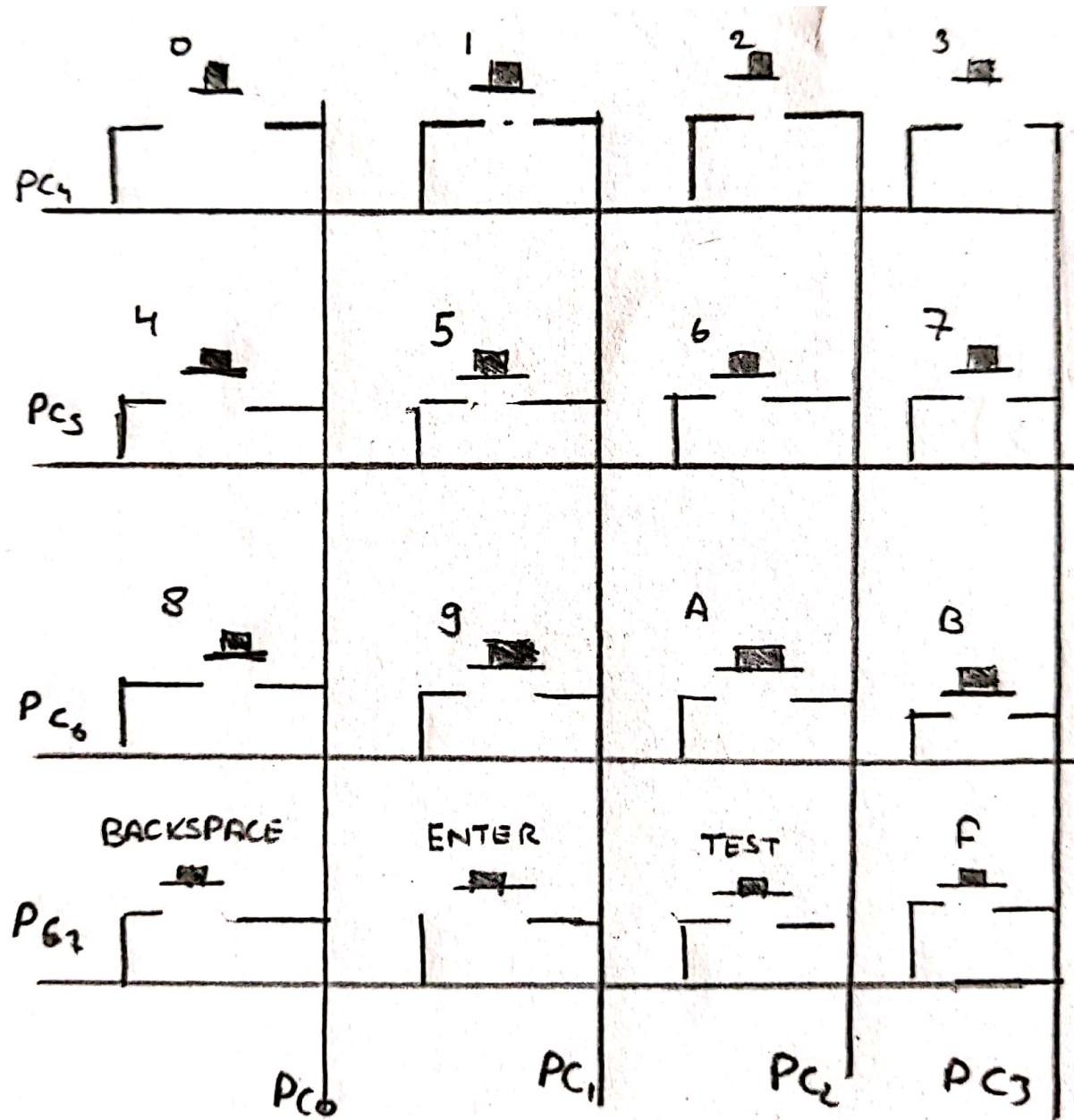
System Bus of 8086(Data)



System Bus of 8086(Address)



Interfacing with keyboard



Memory Interfacing

- * Memory Requirements:

4K RAM starting at 00000_H

8K ROM starting at $FE000_H$.

- * No of chips:

2732 ROM ($\text{C size of ROM} = 32/8 = 4k \times 2$)

6116 RAM ($\text{C size of RAM} = 16/8 = 2k \times 2$)

- * Memory allocation:

RAMIE - $00000_H, 00002_H, 00004_H, \dots, 00FFE_H$

RAMIO - $00001_H, 00003_H, 00005_H, \dots, 00FFF_H$

ROMIE - $FE000_H, FE002_H, FE004_H, \dots, FFFFE_H$

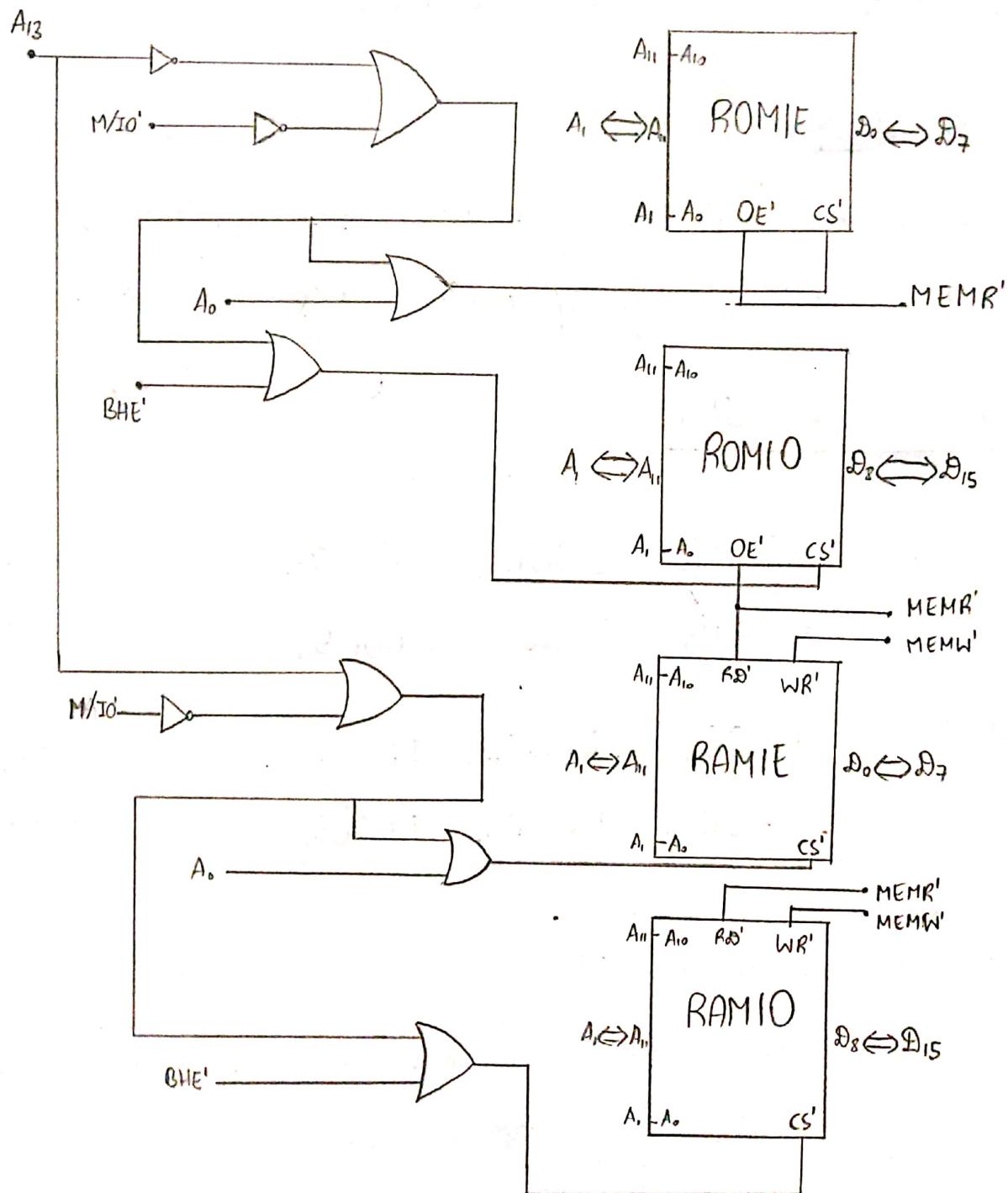
ROMIO - $FE001_H, FE003_H, FE005_H, \dots, FFFFF_H$

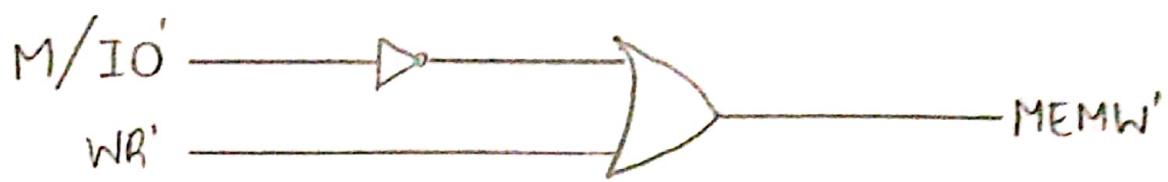
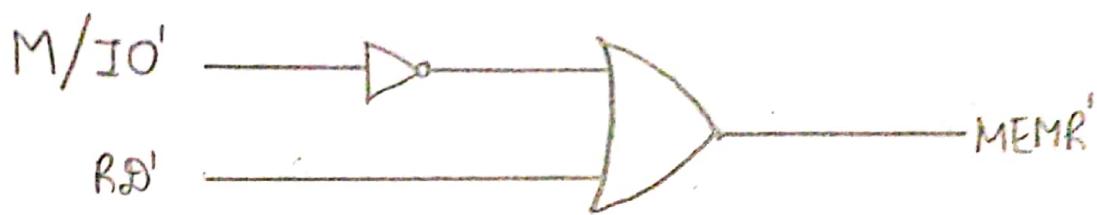
RAMI: $00000_H - 00FFF_H$

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

ROM1 - FE000_H - FFFFF_H

A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1





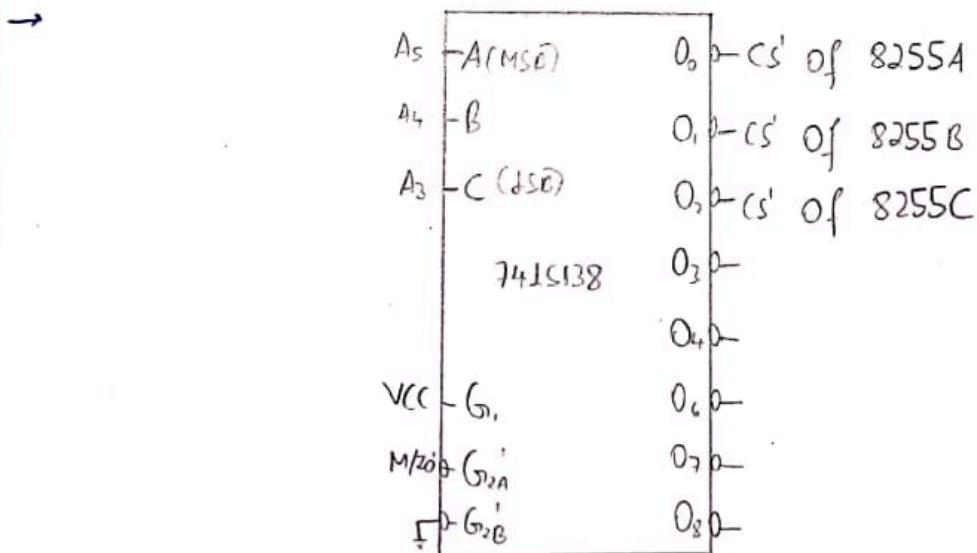
I/O Interfacing

→ 8255A ⇒ 00H - 0FH

8255B ⇒ 08H - 0EH

8255C ⇒ 10H - 16H

A ₂	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁ , A ₀	
0	0	0	0	0	0	0 0 0	} 8255A
0	0	0	0	0	1	1 0	
0	0	0	0	1	0	0 0	} 8255B
0	0	0	0	1	1	1 0	
0	0	0	01	0	0	0 0	} 8255C
0	0	0	1	0	1	1 0	



Algorithm

