Digital Design and Computer Organization Laboratory

UE19CS206

3rd Semester, Academic Year 2020-21

Date:

Name : Achyut Jagini	SRN : PES2UG19CS013	Section : A

Experiment Number: 7 Week #: 7

Title of the Program:

16 Bit Microprocessor Control Logic

Aim of the Program:

To Design and Implement the Microprocessor Control logic, which is essentially a finite state machine

Code (mproc.v)

Users > achyutjagini > Desktop > ddco lab > Week7 > mproc.v > ...

```
module ir (input wire clk, reset, load, input wire [15:0] din, output wire [15:0] dout);

dfrl dfrl_0 (clk,reset,load,din[0],dout[0]);

dfrl dfrl_1 (clk,reset,load,din[1],dout[1]);

dfrl dfrl_2 (clk,reset,load,din[2],dout[2]);

dfrl dfrl_3 (clk,reset,load,din[3],dout[3]);

dfrl dfrl_4 (clk,reset,load,din[4],dout[4]);

dfrl dfrl_5 (clk,reset,load,din[5],dout[5]);

dfrl dfrl_6 (clk,reset,load,din[6],dout[6]);

dfrl dfrl_7 (clk,reset,load,din[7],dout[7]);

dfrl dfrl_8 (clk,reset,load,din[8],dout[8]);

dfrl dfrl_9 (clk,reset,load,din[9],dout[9]);

dfrl dfrl_a (clk,reset,load,din[10],dout[10]);

dfrl dfrl_b (clk,reset,load,din[11],dout[11]);


dfrl dfrl_c (clk,reset,load,din[12],dout[12]);


dfrl dfrl_d (clk,reset,load,din[13],dout[13]);

dfrl dfrl_e (clk,reset,load,din[14],dout[14]);

```

```
34
35
36  dfrl dfrl_f (clk,reset,load,din[15],dout[15]);
37
38
39  endmodule
40
41
42  module nor5 (input wire [0:4] i, output wire o);
43    wire t;
44    or3 or3_0 (i[0], i[1], i[2], t);
45    nor3 nor3_0 (t, i[3], i[4], o);
46  endmodule
47
48
49  module control_logic (input wire clk, reset, input wire [15:0] cur_ins, output wire [2:0] rd_addr_a, rd_addr_b, wr_addr, o
50
51  wire t, alu_ins;
52
53  //assignment 3 logic here
54  dfsl fetch (clk,reset,1'b1,wr_reg,pc_inc);
55
56  assign load_ir=pc_inc;
57
58  dfrl dec_exec (clk,reset,1'b1,load_ir,t);
59
60  nor5 nor5_0 (cur_ins [15:11] ,alu_ins);
61
62
63  and2 and2_0 (t,alu_ins,wr_reg);
64
65  assign rd_addr_a=cur_ins[2:0];
66
```

```
67  assign rd_addr_b =cur_ins[5:5];
68
69   assign wr_addr =cur_ins[8:6];
70
71  assign op =cur_ins[10:9];
72
73  endmodule
74
75
76
77  module mproc (input wire clk, reset, input wire [15:0] ins, output wire [15:0] addr);
78    wire pc_inc, cout;
79  wire [2:0] rd_addr_a, rd_addr_b, wr_addr;
80  wire [1:0] op;
81  wire [15:0] cur_ins, d_out_a, d_out_b;
82
83
84  pc pc_0 (clk,reset,pc_inc,1'b0,1'b0,16'b0,addr);
85
86  ir ir_0 (clk,reset,load_ir,ins,cur_ins);
87
88  control_logic control_logic_0 (clk,reset,cur_ins,rd_addr_a,rd_addr_b,wr_addr,op,pc_inc,load_ir,wr_reg);
89
90  reg_alu reg_alu_0 (clk,reset,1'b1,wr_reg,op,rd_addr_a,rd_addr_b,wr_addr,16'b0,d_out_a,d_out_b,cout);
91
92  endmodule
93
```

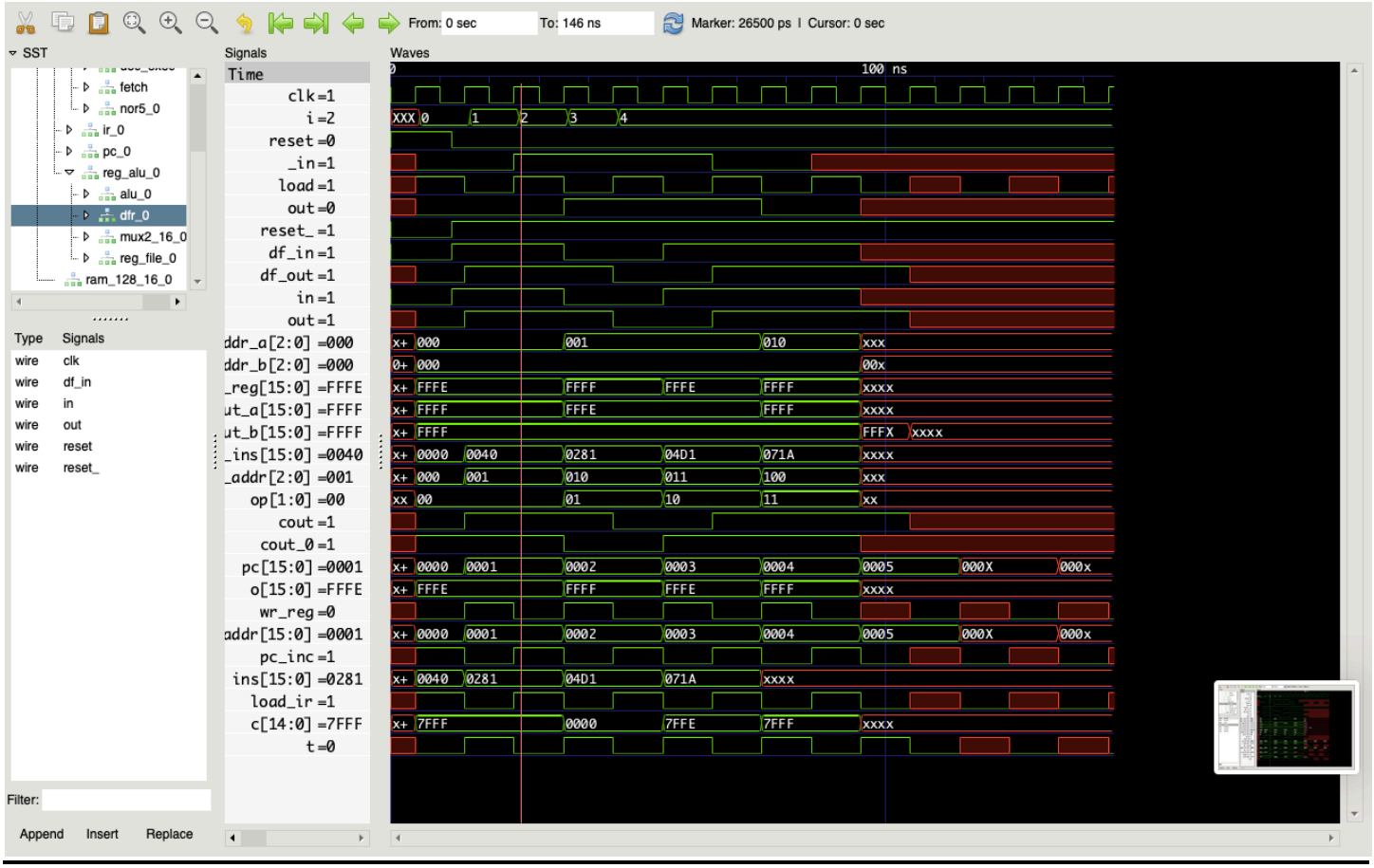
TABLE

cur_ins [15:0]	ram	Octal Value Of cur_ins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0040 (Hex)	ram [0]	16‘o 000100;	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	d_out_a+ d_out_b= FFFF+FFFF =FFFE with carry =1
0281 (Hex)	ram [1]	16'o 001100;	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	d_out_a- d_out_b= FFFE-FFFF =FFFF with borrow=1
04D1 (Hex)	ram [2]	16'o 002100	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	1	d_out_a AND d_out_b= FFFE AND FFFF=FFFE
071A (Hex)	ram [3]	16'o 003100;	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0	d_out_a OR d_out_b= FFFF OR FFFE=FFFF

Output waveform

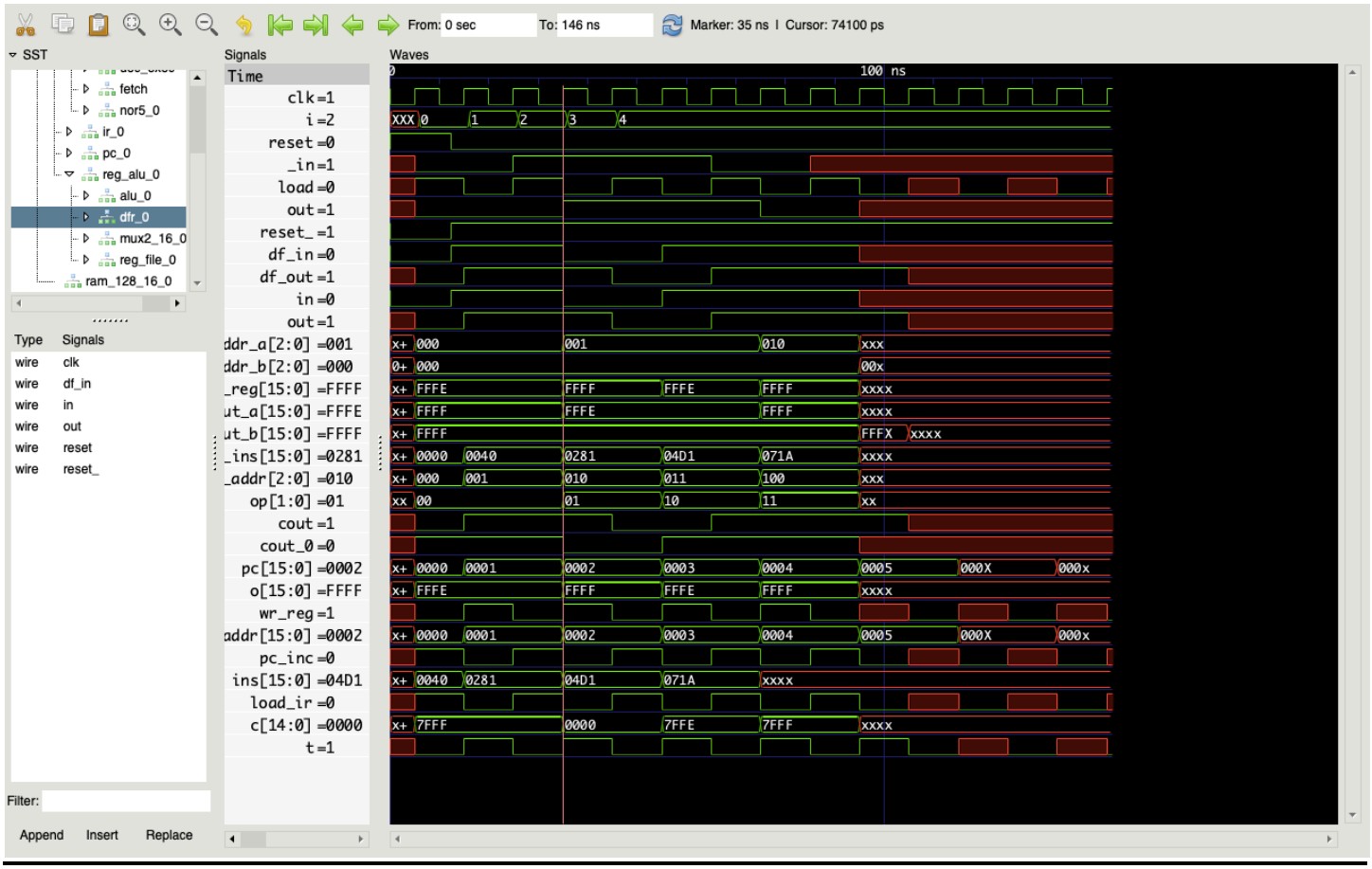
SCREENSHOT1(ADD Instruction)

cur_ins [15:0]	ram	Octal Value Of cur_ins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0040 (Hex)	ram [0]	16'o 000100;	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	d_out_a+ d_out_b= FFFF+FFFF =FFFE with carry =1



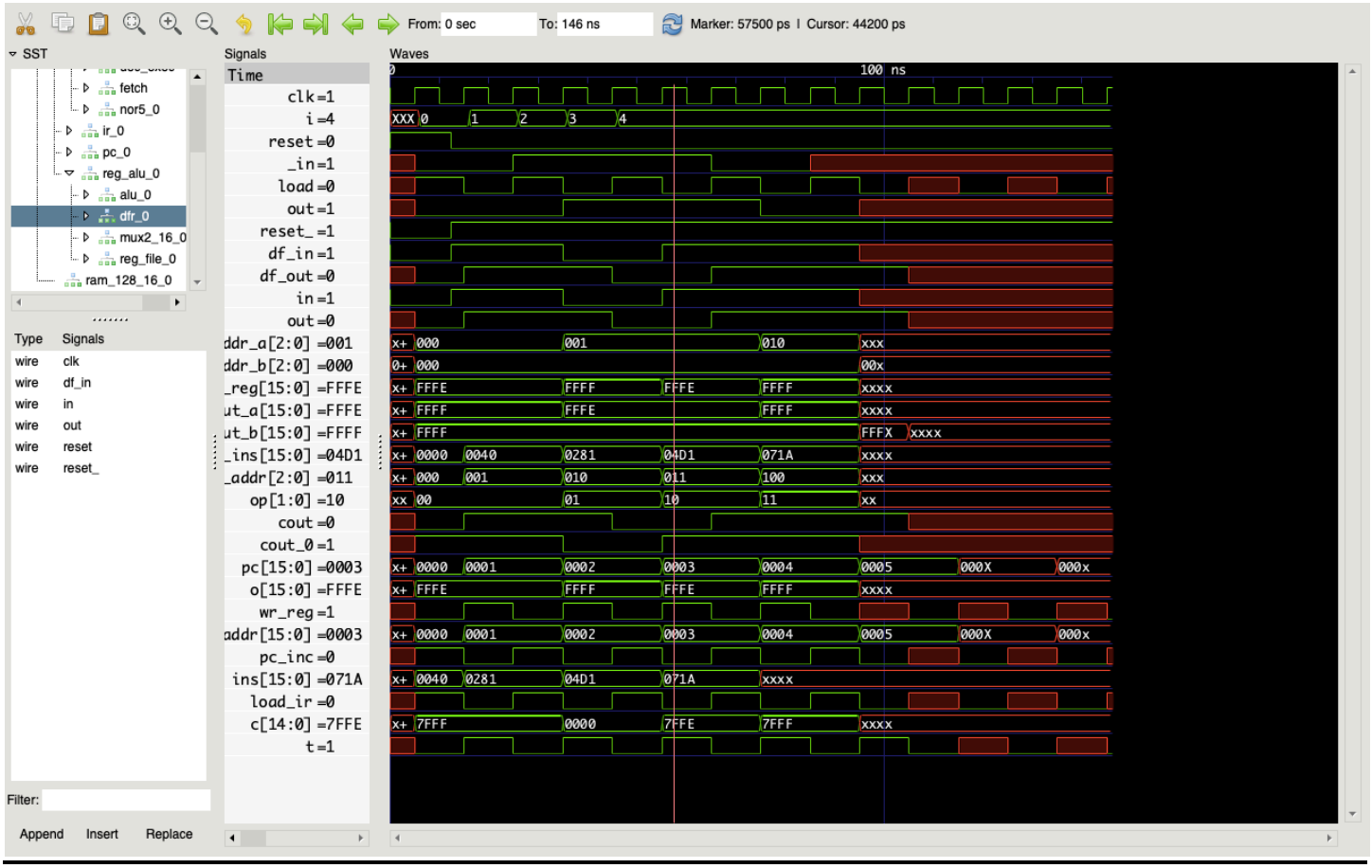
SCREENSHOT2(SUBTRACT Instruction)

cur_ins [15:0]	ram	Octal Value Of cur_ins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0281 (Hex)	ram [1]	16'o 001100;	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	d_out_a- d_out_b= FFFE-FFFF =FFFF with borrow=1



SCREENSHOT 3(AND Instruction)

cur_ins [15:0]	ram	Octal Value Of cur_ins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
04D1 (Hex)	ram [2]	16'o 002100	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	1	d_out_a AND d_out_b= FFFE AND FFFF=FFFE



SCREENSHOT 4 (OR Instruction)

cur_ins [15:0]	ram	Octal Value of cur_ins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
071A (Hex)	ram [3]	16'o 003100;	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0	d_out_a OR d_out_b= FFFF OR FFFE=FFFF