Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

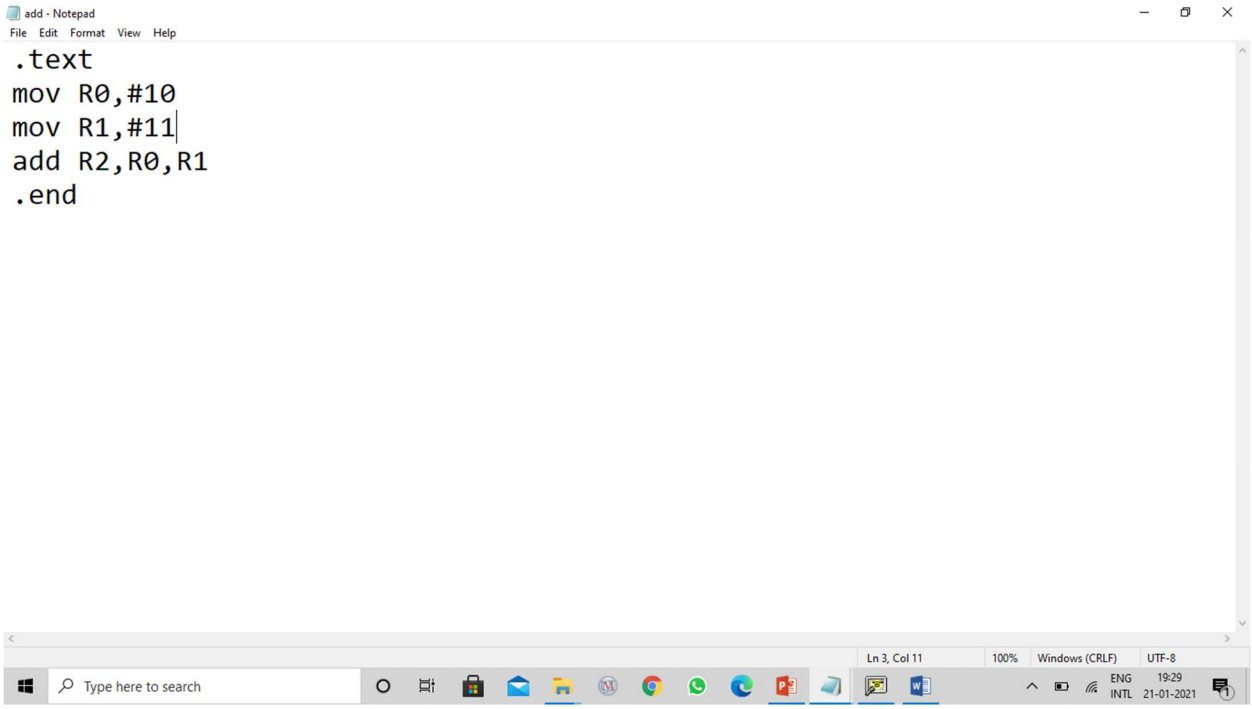
Name: Achyut Jagini	SRN:PES2UG19CS013	Section A

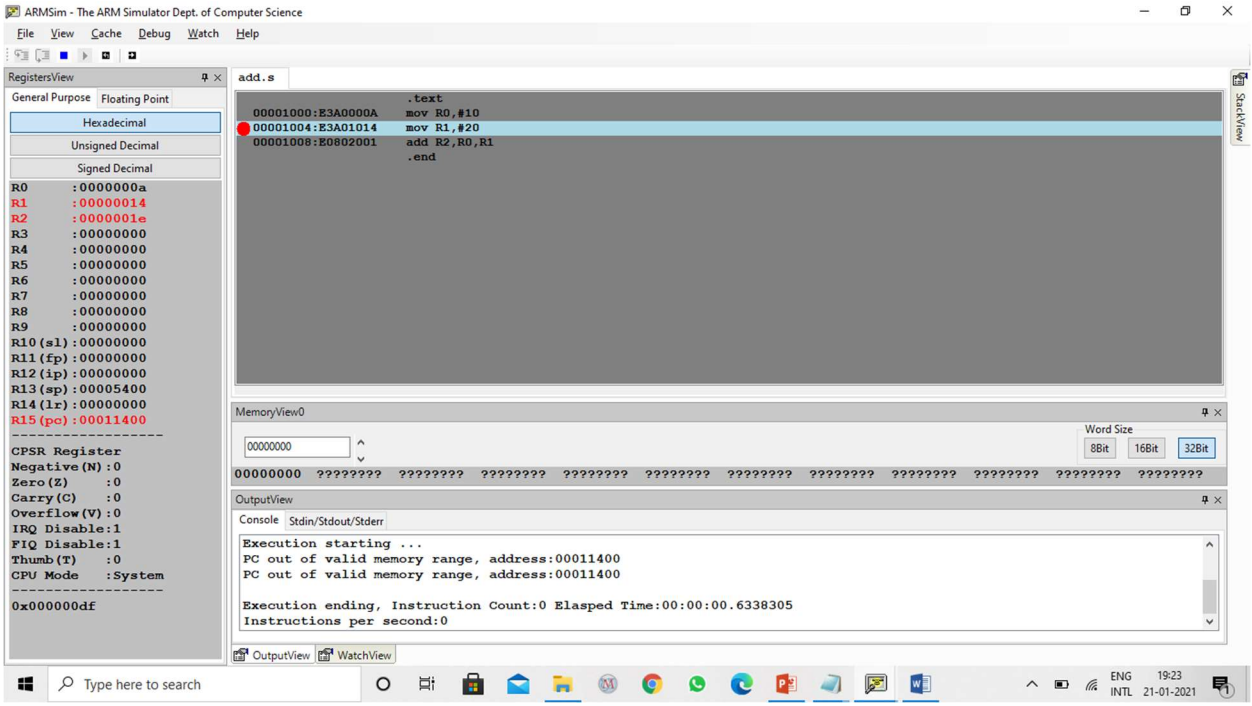
Week#____1_____ Program Number: ____1___

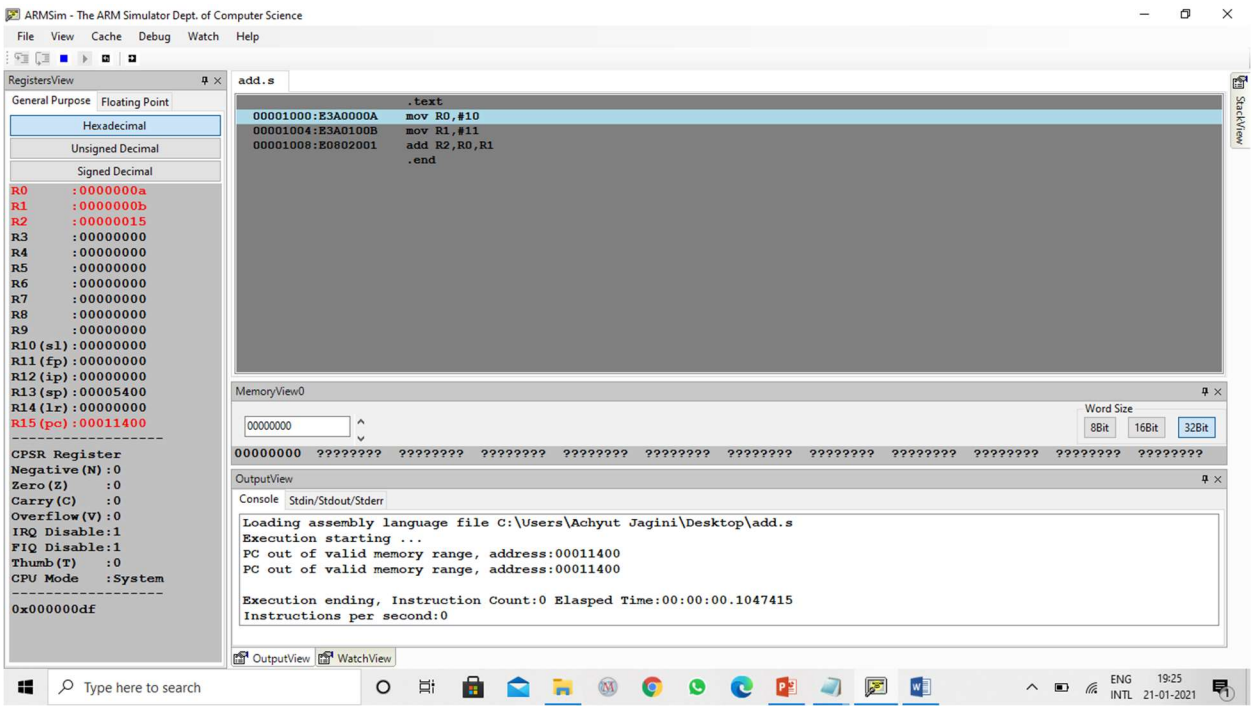
Title of the Program

Write an ALP using ARM instruction set to add and subtract two 32 bit numbers .Both numbers are in registers.

I. ARM Assembly code






ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :0000000a
R1 :0000000b
R2 :00000015
R3 :00000000
R4 :00000000
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00011400
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
add.s
.text
00001000:E3A0000A mov R0,#10
00001004:E3A0100B mov R1,#11
00001008:E0802001 add R2,R0,R1
.end
MemoryView0
00000000
Word Size
8Bit 16Bit 32Bit
00000000 ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ????????
OutputView
Console Stdin/Stdout/Stderr
Loading assembly language file C:\Users\Achyut Jagini\Desktop\add.s
Execution starting ...
PC out of valid memory range, address:00011400
PC out of valid memory range, address:00011400
Execution ending, Instruction Count:0 Elasped Time:00:00:00.1047415
Instructions per second:0
OutputView WatchView
Type here to search
ENG INTL 19:25 21-01-2021

2.subtract

sub - Notepad

File Edit Format View Help

```
.text
mov R0,#10
mov R1,#20
sub R2,R1,R0
.end
```

Ln 6, Col 1 | 100% | Windows (CRLF) | UTF-8

Type here to search

ENG INTL 19:33 21-01-2021

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :10
R1      :20
R2      :10
R3      :0
R4      :0
R5      :0
R6      :0
R7      :0
R8      :0
R9      :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):70656
------------------
CPSR Register
Negative(N):0
Zero(Z)    :0
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
------------------
0x000000df
```

sub.s

```
                    .text
  00001000:E3A0000A mov R0,#10
  00001004:E3A01014 mov R1,#20
  00001008:E0412000 sub R2,R1,R0
                    .end
```

StackView

MemoryView0

00000000 | Word Size: 8Bit 16Bit 32Bit

```
00000000 ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ???????? ????????
```

OutputView

Console | Stdin/Stdout/Stderr

```
Loading assembly language file C:\Users\Achyut Jagini\Desktop\sub.s
Execution starting ...
PC out of valid memory range, address:00011400
PC out of valid memory range, address:00011400

Execution ending, Instruction Count:0 Elasped Time:00:00:00.0988475
Instructions per second:0
```

OutputView | WatchView

Type here to search

ENG INTL 19:37 21-01-2021

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

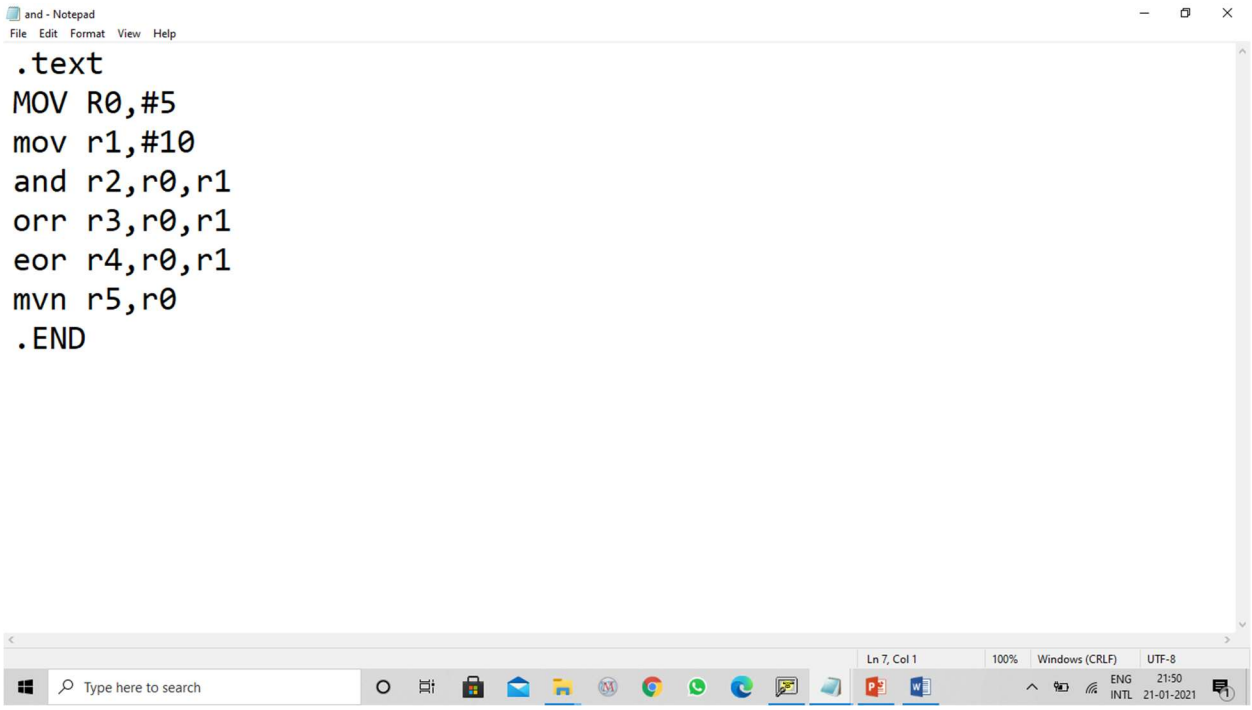
Date:

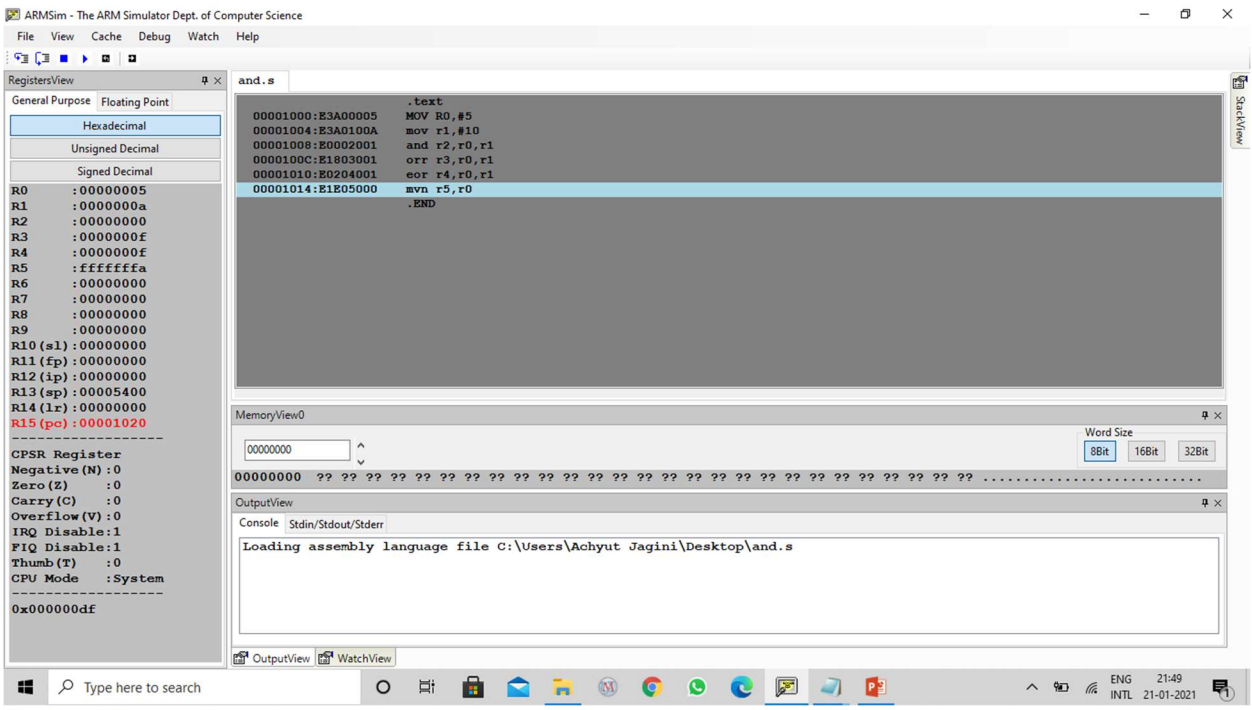
Name: Achyut Jagini	SRN:PES2UG19CS013	Section A

Week#____1_____ Program Number: ____2___

Title of the Program

Write an ALP to demonstrate logical operations. All operands are in registers.


and - Notepad
File Edit Format View Help
.text
MOV R0,#5
mov r1,#10
and r2,r0,r1
orr r3,r0,r1
eor r4,r0,r1
mvn r5,r0
.END
Ln 7, Col 1
100%
Windows (CRLF)
UTF-8
Type here to search
ENG
INTL
21:50
21-01-2021


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000005
R1 :0000000a
R2 :00000000
R3 :0000000f
R4 :0000000f
R5 :fffffffa
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001020
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
and.s
.text
00001000:E3A00005 MOV R0,#5
00001004:E3A0100A mov r1,#10
00001008:E0002001 and r2,r0,r1
0000100C:E1803001 orr r3,r0,r1
00001010:E0204001 eor r4,r0,r1
00001014:E1E05000 mvn r5,r0
.END
MemoryView0
00000000
Word Size
8Bit 16Bit 32Bit
00000000 ?? ?? ??

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

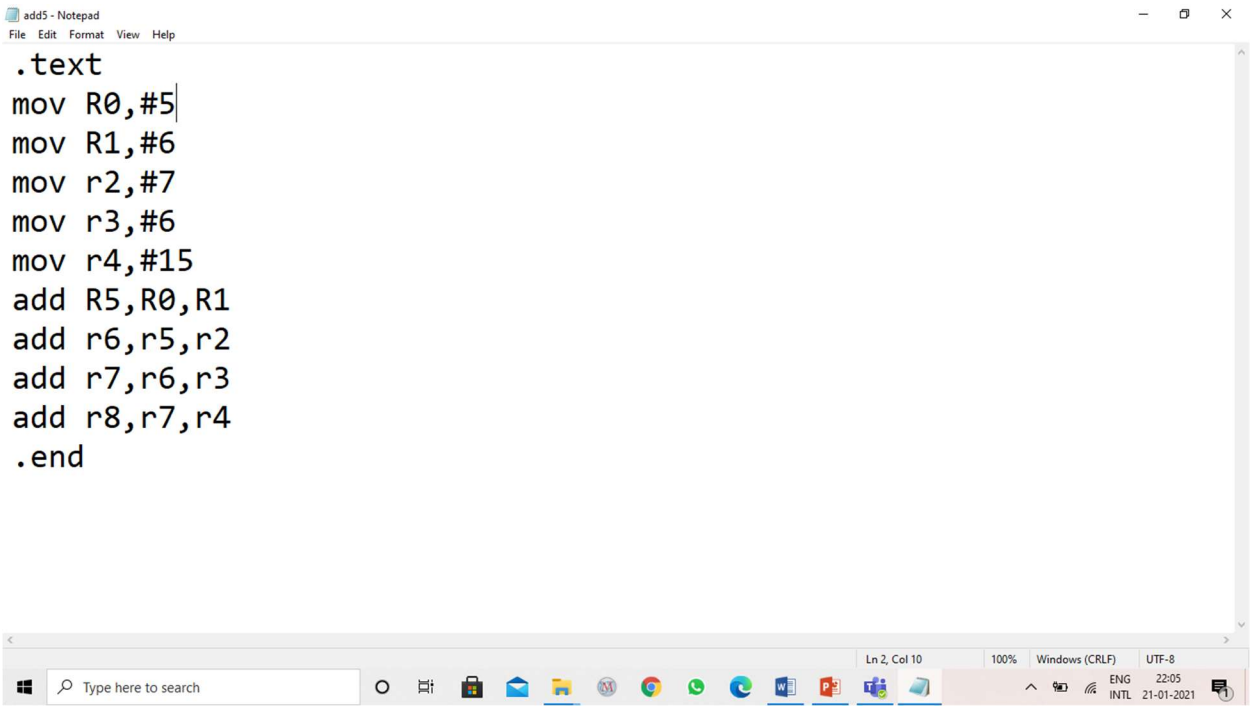
Date:

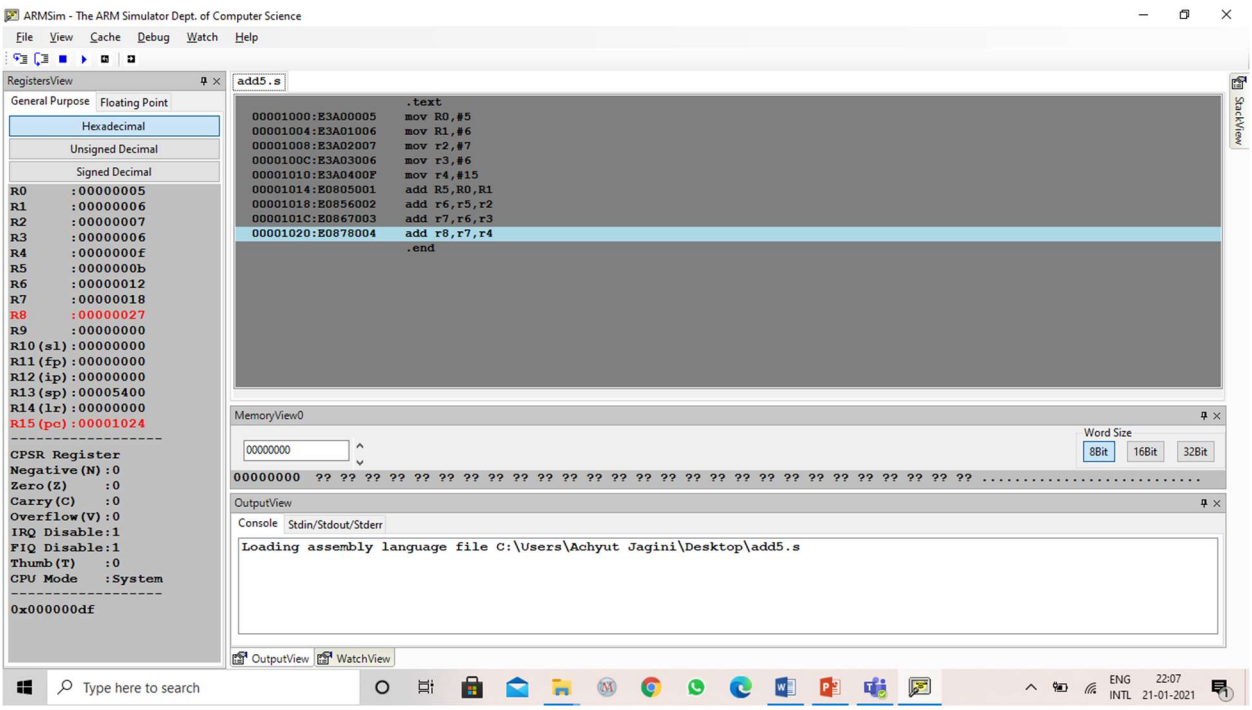
Name: Achyut Jagini	SRN:PES2UG19CS013	Section A

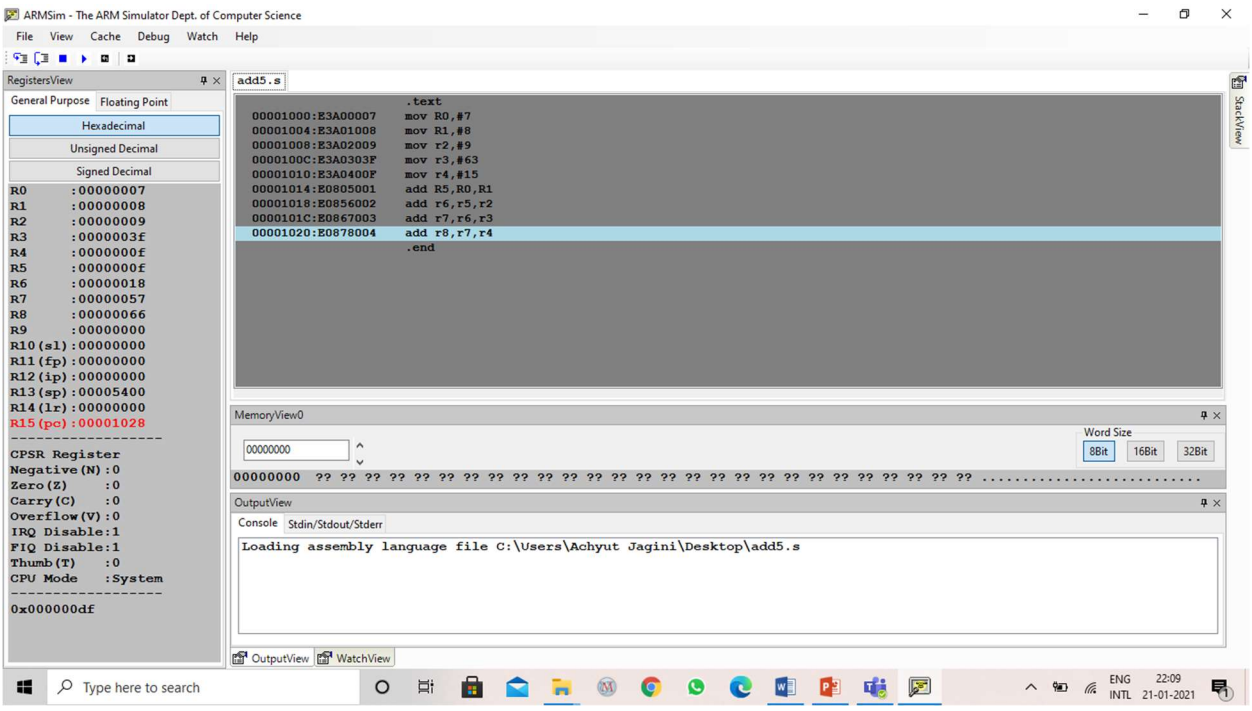
Week#____1_____ Program Number: ____3___

Title of the Program

Write an ALP to add 5 numbers where values are present in registers.




ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose
Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000005
R1 :00000006
R2 :00000007
R3 :00000006
R4 :0000000f
R5 :0000000b
R6 :00000012
R7 :00000018
R8 :00000027
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001024
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
add5.s
.text
00001000:E3A00005 mov R0,#5
00001004:E3A01006 mov R1,#6
00001008:E3A02007 mov r2,#7
0000100C:E3A03006 mov r3,#6
00001010:E3A0400F mov r4,#15
00001014:E0805001 add R5,R0,R1
00001018:E0856002 add r6,r5,r2
0000101C:E0867003 add r7,r6,r3
00001020:E0878004 add r8,r7,r4
.end
StackView
MemoryView0
00000000
Word Size
8Bit
16Bit
32Bit
00000000 ?? ?? ??


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000007
R1 :00000008
R2 :00000009
R3 :0000003f
R4 :0000000f
R5 :0000000f
R6 :00000018
R7 :00000057
R8 :00000066
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001028
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
add5.s
.text
00001000:E3A00007 mov R0,#7
00001004:E3A01008 mov R1,#8
00001008:E3A02009 mov r2,#9
0000100C:E3A0303F mov r3,#63
00001010:E3A0400F mov r4,#15
00001014:E0805001 add R5,R0,R1
00001018:E0856002 add r6,r5,r2
0000101C:E0867003 add r7,r6,r3
00001020:E0878004 add r8,r7,r4
.end
StackView
MemoryView0
00000000
Word Size
8Bit 16Bit 32Bit
00000000 ?? ?? ??

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: Achyut Jagini	SRN:PES2UG19CS013	Section A

Week#____1_____ Program Number: ____4___

Title of the Program

Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

4 - Notepad

File Edit Format View Help

```
.text
mov r1,#6
ands r2,r1,#1
BEQ condition
          MOV r0,#0xFF
            B exit
        condition:
                MOV r0,#00
exit:
.end
```

Ln 3, Col 14 | 100% | Windows (CRLF) | UTF-8

Type here to search

ENG INTL 15:09 22-01-2021

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :00000000
R1      :00000006
R2      :00000000
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001014
----------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
----------------
0x400000df
```

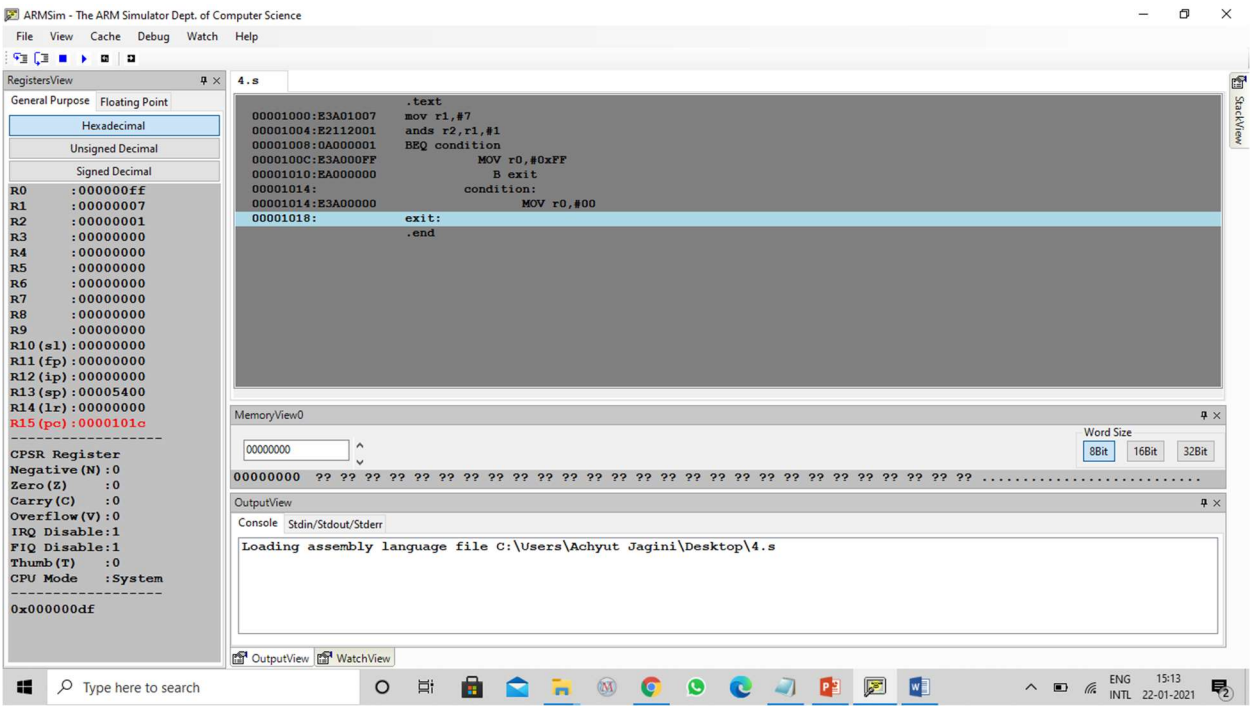
4.s

```
00001000:E3A01006    mov r1,#6
00001004:E2112001    ands r2,r1,#1
00001008:0A000001    BEQ condition
0000100C:E3A000FF            MOV r0,#0xFF
00001010:EA000000              B exit
00001014:                  condition:
00001014:E3A00000                  MOV r0,#00
00001018:            exit:
                     .end
```

MemoryView0

00000000 | Word Size: 8Bit 16Bit 32Bit

```
00000000  ?? ?? ??
```


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :000000ff
R1 :00000007
R2 :00000001
R3 :00000000
R4 :00000000
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):0000101c
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
4.s
.text
00001000:E3A01007 mov r1,#7
00001004:E2112001 ands r2,r1,#1
00001008:0A000001 BEQ condition
0000100C:E3A000FF MOV r0,#0xFF
00001010:EA000000 B exit
00001014: condition:
00001014:E3A00000 MOV r0,#00
00001018: exit:
.end
StackView
MemoryView0
00000000
Word Size
8Bit 16Bit 32Bit
00000000 ?? ?? ??

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:achyut
Name:Achyut Jagini
SRN:PES2UG19CS013
Section: A
Date:21/01/21