Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:3-4-2020

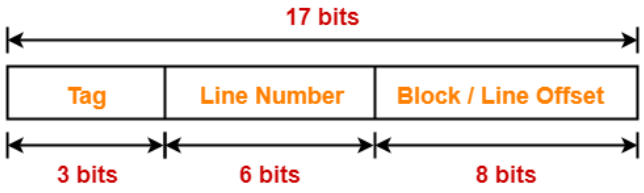
Name: Achyut Jagini	SRN:PES2UG19CS013	Section:A

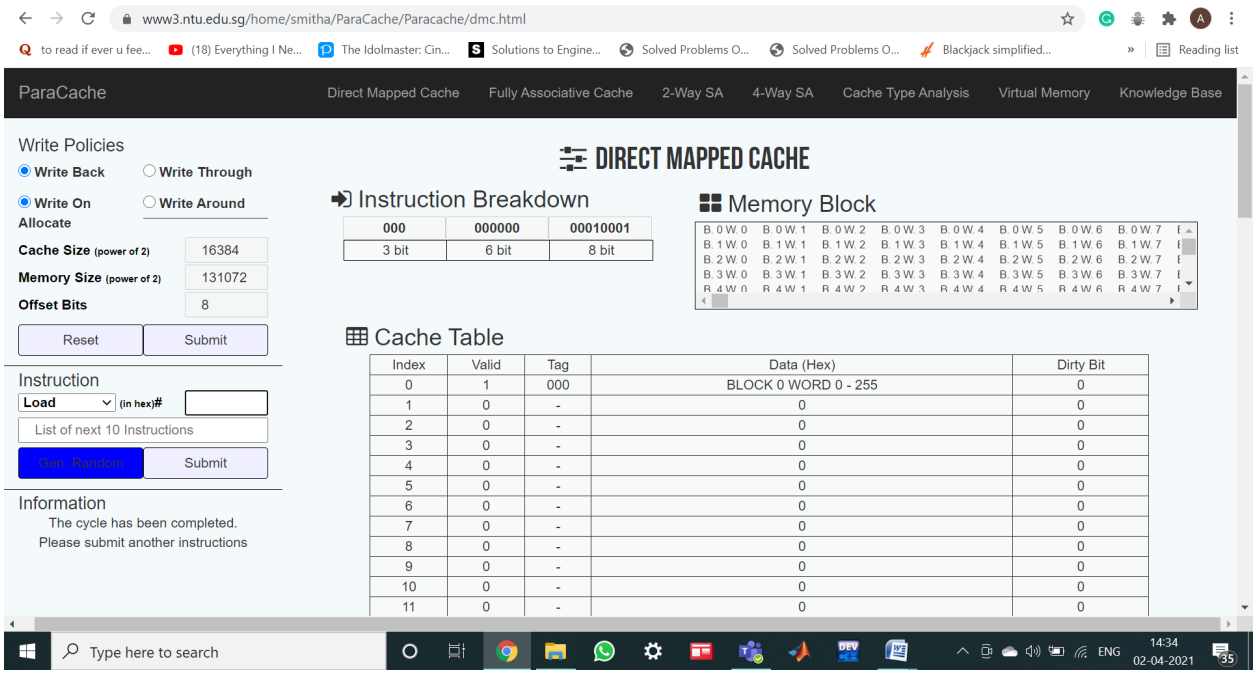
Week#____9_____Program Number: __1____

Title of the Program

1. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

   Solution:
   Given-
   Cache memory size = 16 KB
   Block size = Frame size = Line size = 256 bytes
   Main memory size = 128 KB = 2^17




www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html
ParaCache
Direct Mapped Cache
Fully Associative Cache
2-Way SA
4-Way SA
Cache Type Analysis
Virtual Memory
Knowledge Base
Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2) 16384
Memory Size (power of 2) 131072
Offset Bits 8
Reset
Submit
Instruction
Load
(in hex)#
List of next 10 Instructions
Gen. Random
Submit
Information
The cycle has been completed.
Please submit another instructions
DIRECT MAPPED CACHE
Instruction Breakdown
000 | 000000 | 00010001
3 bit | 6 bit | 8 bit
Memory Block
Cache Table
Index | Valid | Tag | Data (Hex) | Dirty Bit
0 | 1 | 000 | BLOCK 0 WORD 0 - 255 | 0
1 | 0 | - | 0 | 0
2 | 0 | - | 0 | 0
3 | 0 | - | 0 | 0
4 | 0 | - | 0 | 0
5 | 0 | - | 0 | 0
6 | 0 | - | 0 | 0
7 | 0 | - | 0 | 0
8 | 0 | - | 0 | 0
9 | 0 | - | 0 | 0
10 | 0 | - | 0 | 0
11 | 0 | - | 0 | 0
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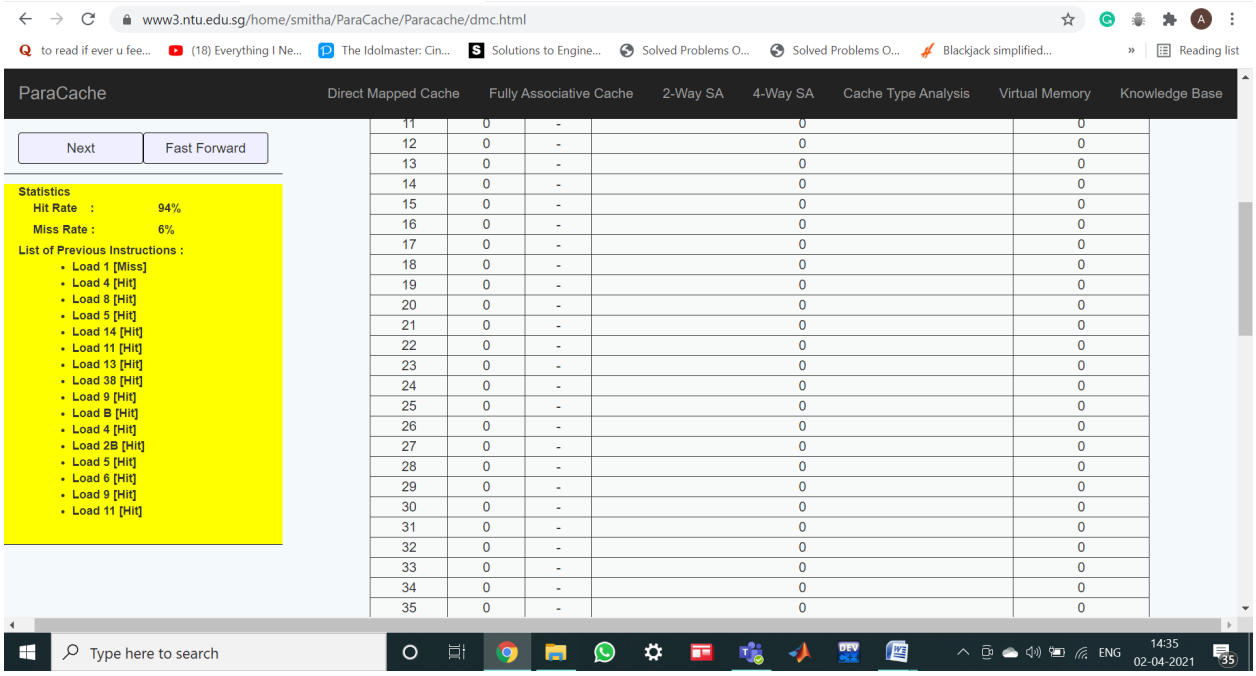
ENG
14:34
02-04-2021


www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html
ParaCache
Direct Mapped Cache
Fully Associative Cache
2-Way SA
4-Way SA
Cache Type Analysis
Virtual Memory
Knowledge Base
Next
Fast Forward
Statistics
Hit Rate : 94%
Miss Rate : 6%
List of Previous Instructions :
Load 1 [Miss]
Load 4 [Hit]
Load 8 [Hit]
Load 5 [Hit]
Load 14 [Hit]
Load 11 [Hit]
Load 13 [Hit]
Load 38 [Hit]
Load 9 [Hit]
Load B [Hit]
Load 4 [Hit]
Load 2B [Hit]
Load 5 [Hit]
Load 6 [Hit]
Load 9 [Hit]
Load 11 [Hit]
11 | 0 | - | 0 | 0
12 | 0 | - | 0 | 0
13 | 0 | - | 0 | 0
14 | 0 | - | 0 | 0
15 | 0 | - | 0 | 0
16 | 0 | - | 0 | 0
17 | 0 | - | 0 | 0
18 | 0 | - | 0 | 0
19 | 0 | - | 0 | 0
20 | 0 | - | 0 | 0
21 | 0 | - | 0 | 0
22 | 0 | - | 0 | 0
23 | 0 | - | 0 | 0
24 | 0 | - | 0 | 0
25 | 0 | - | 0 | 0
26 | 0 | - | 0 | 0
27 | 0 | - | 0 | 0
28 | 0 | - | 0 | 0
29 | 0 | - | 0 | 0
30 | 0 | - | 0 | 0
31 | 0 | - | 0 | 0
32 | 0 | - | 0 | 0
33 | 0 | - | 0 | 0
34 | 0 | - | 0 | 0
35 | 0 | - | 0 | 0
Type here to search
ENG
14:35
02-04-2021

Name:	SRN:	Section:

Week#____9_____Program Number: __2____

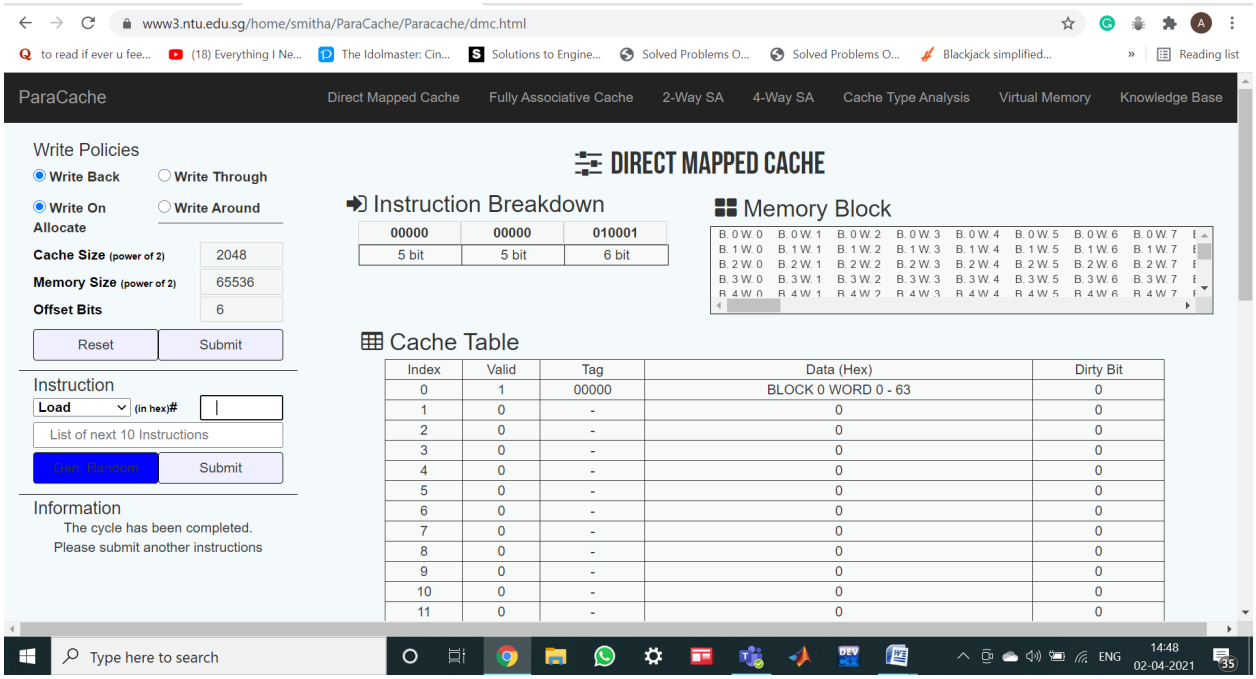
2.computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

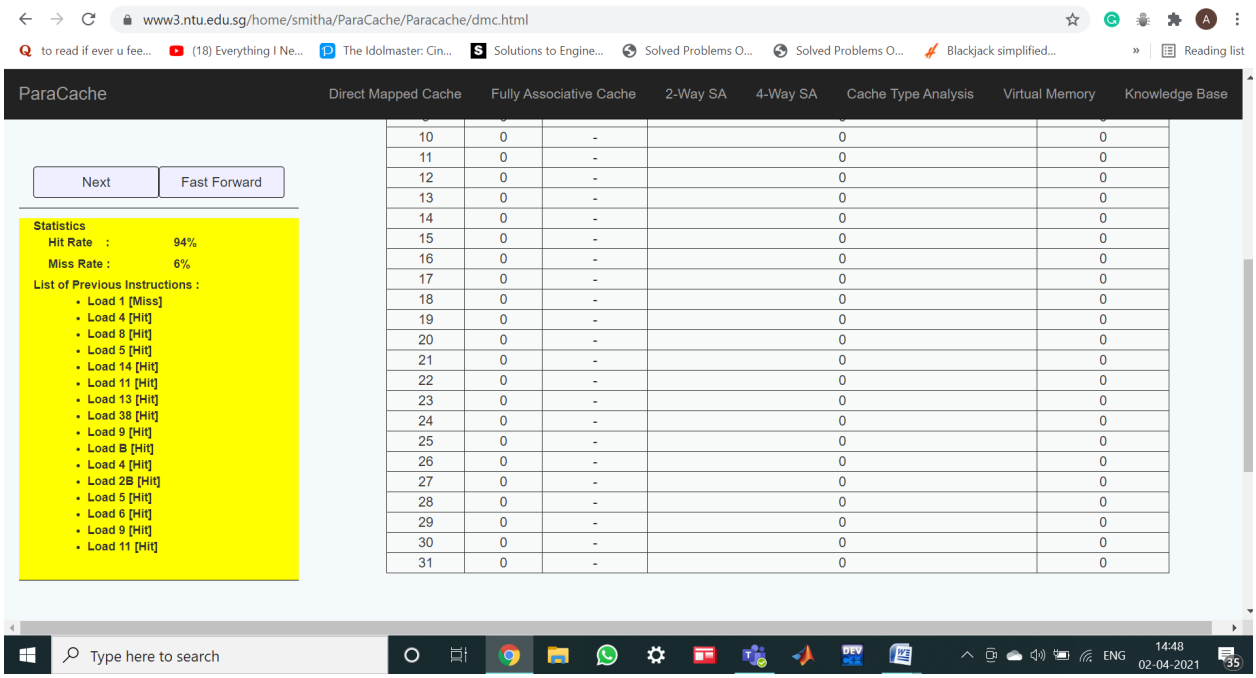
a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

(b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

A) Tag = 5, *Block* = 5, *Word* = 6





10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Name:	SRN:	Section:

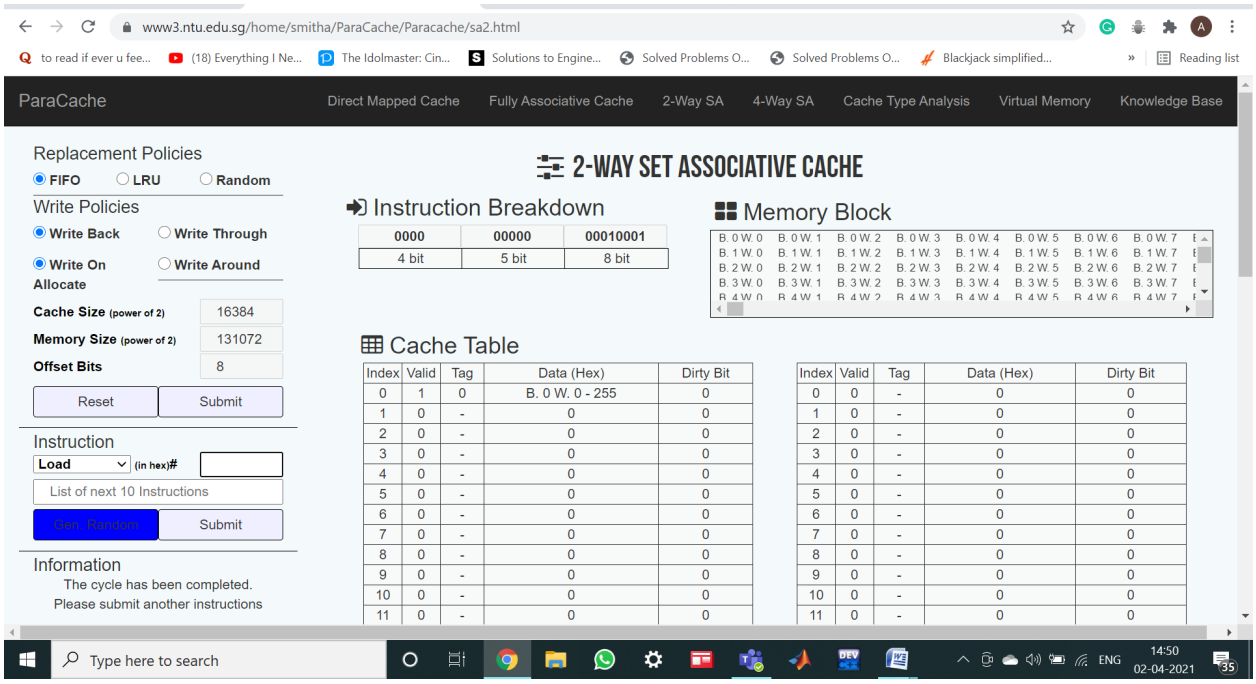
Week#____9_____Program Number: __3____

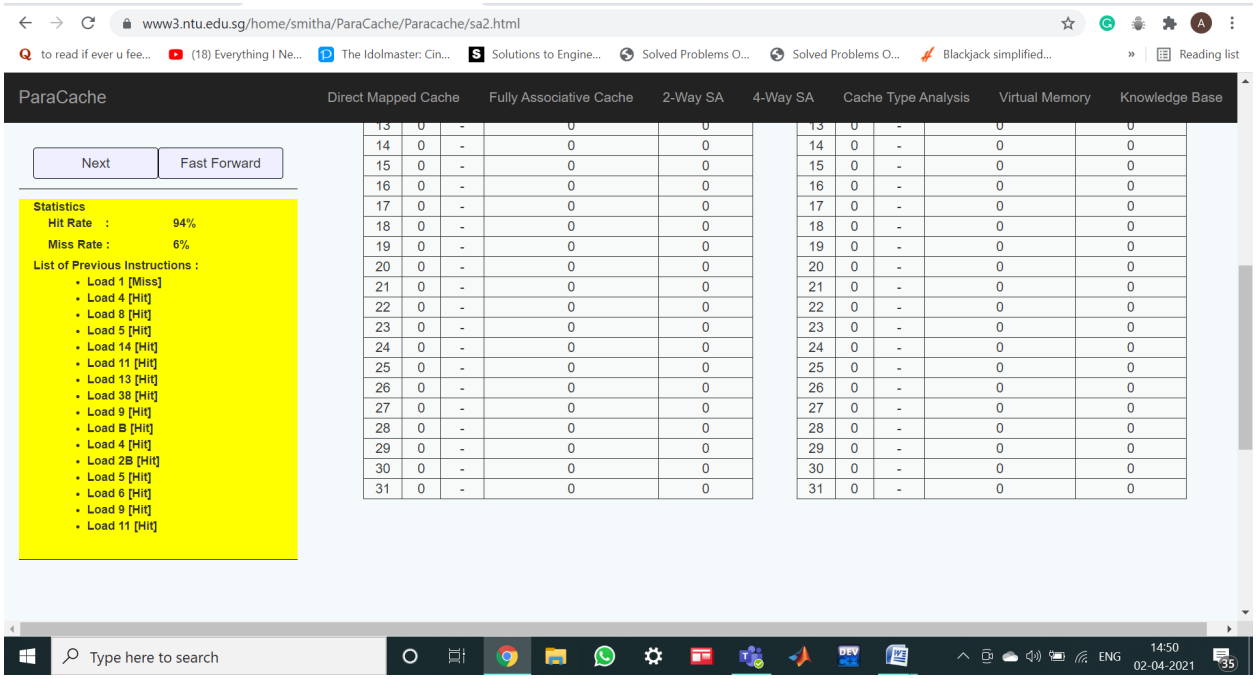
3.Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Randomly generate 10 addresses and find hit rate and miss rate.

Solution:

Given- •Cache memory size = 16 KB
•Block size = Frame size = Line size = 256 bytes
•Main memory size = 128 KB = 217 bytes
Thus, Number of bits in physical address = 17 bits




www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa2.html
ParaCache
Direct Mapped Cache
Fully Associative Cache
2-Way SA
4-Way SA
Cache Type Analysis
Virtual Memory
Knowledge Base
Next
Fast Forward
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Hit Rate : 94%
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List of Previous Instructions :
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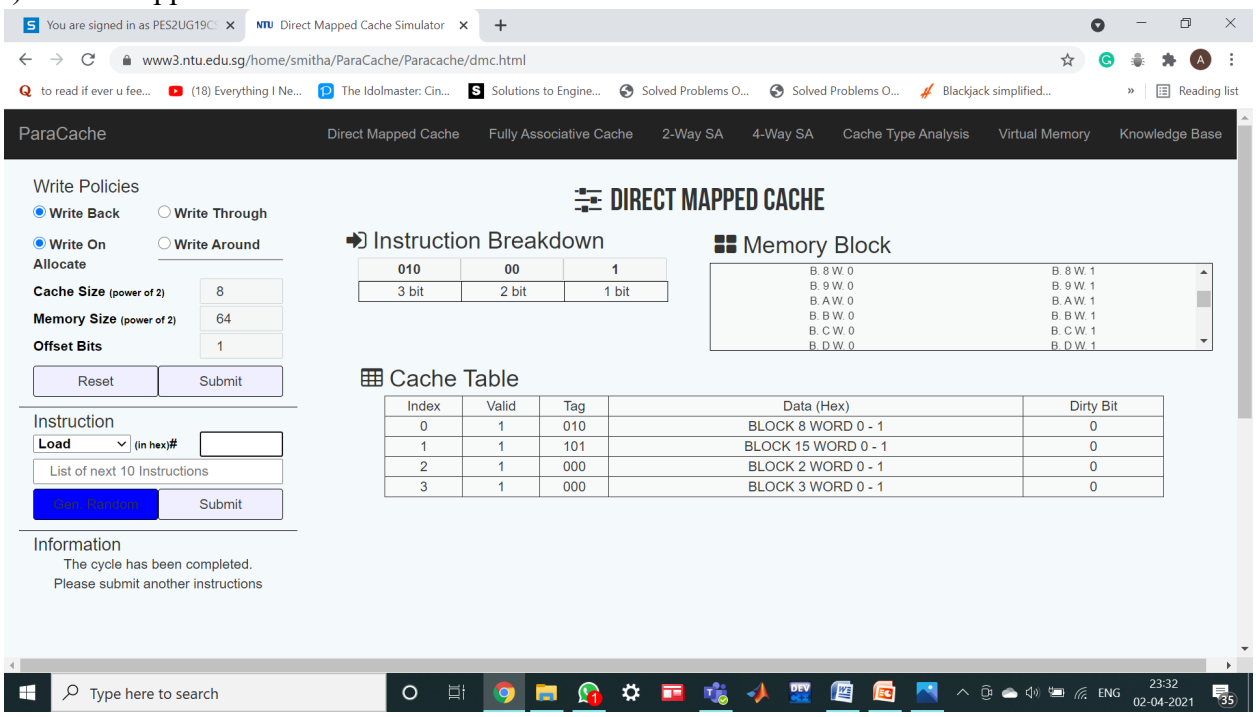
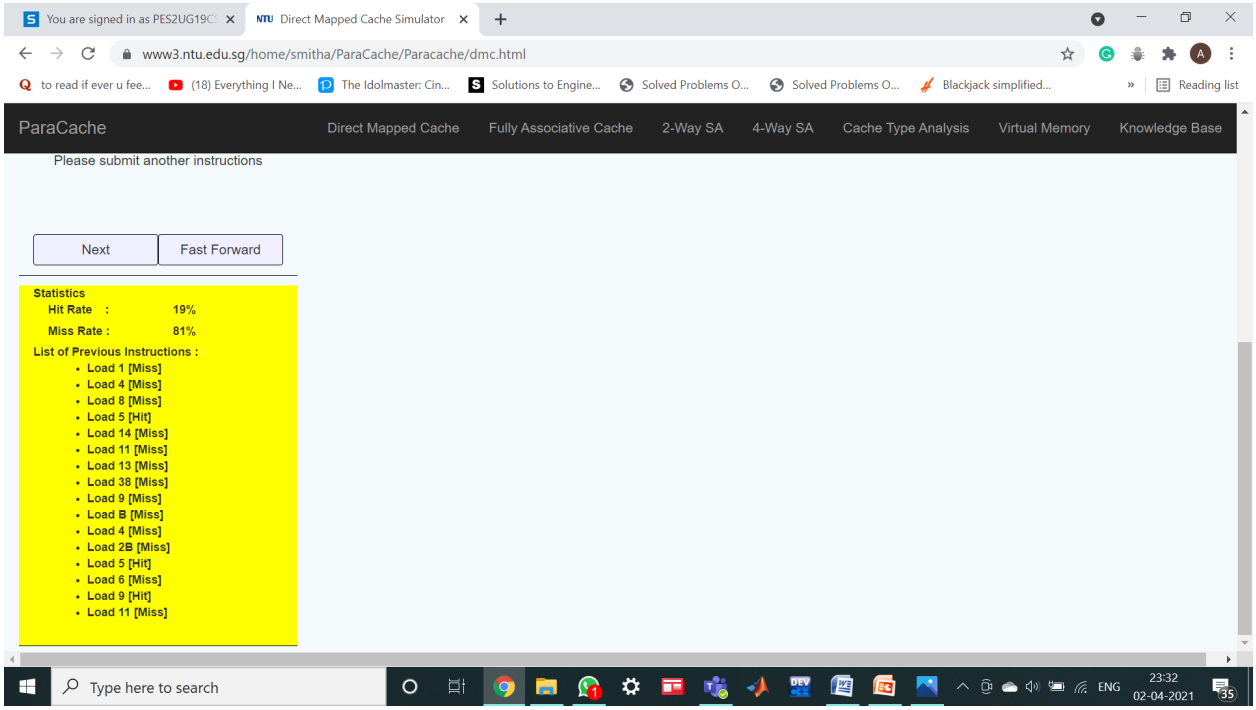
Load 14 [Hit]
Load 11 [Hit]
Load 13 [Hit]
Load 38 [Hit]
Load 9 [Hit]
Load B [Hit]
Load 4 [Hit]
Load 2B [Hit]
Load 5 [Hit]
Load 6 [Hit]
Load 9 [Hit]
Load 11 [Hit]
Type here to search
ENG
14:50
02-04-2021

Name:	SRN:	Section:

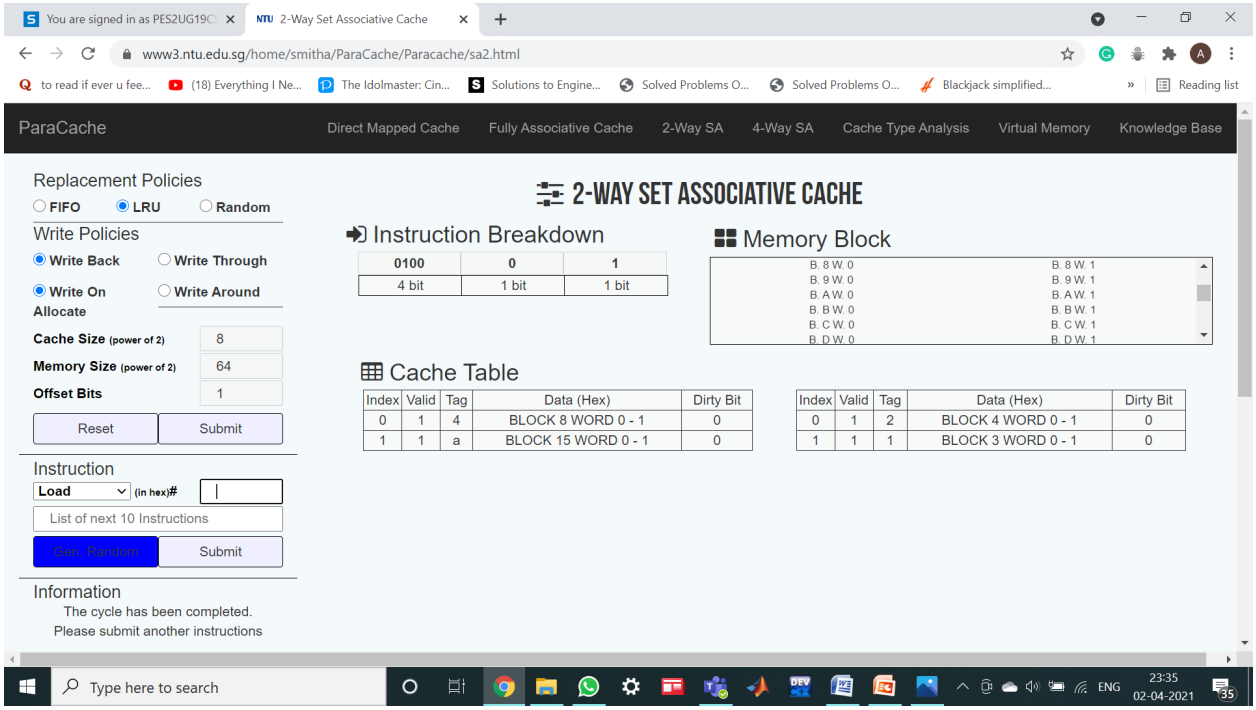
Week#____9_____Program Number: __4____

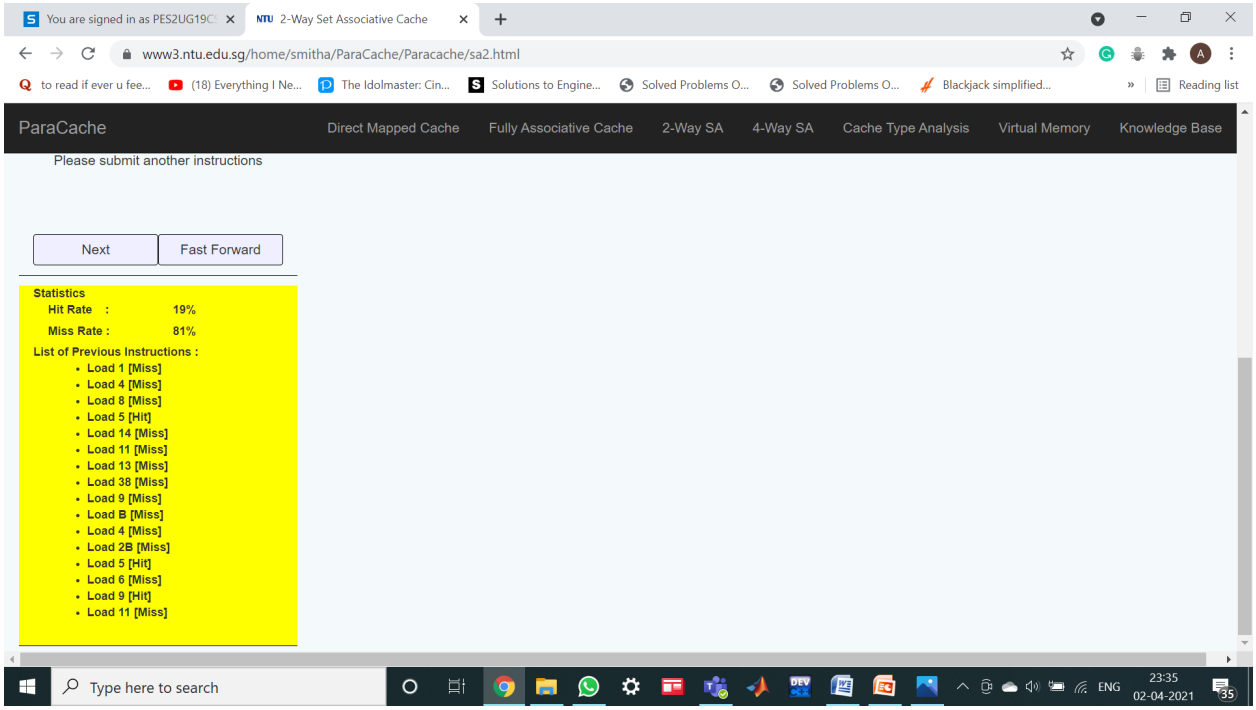
4.Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty
The following addresses are generated by the CPU.All values in hexadecimal
Clearly label data that is replaced in cache lines
Show the cache memory table and filled data in the cache lines of block size 1 byte
LRU Policy is used.
The cache is mapped as
a)Direct Mapped



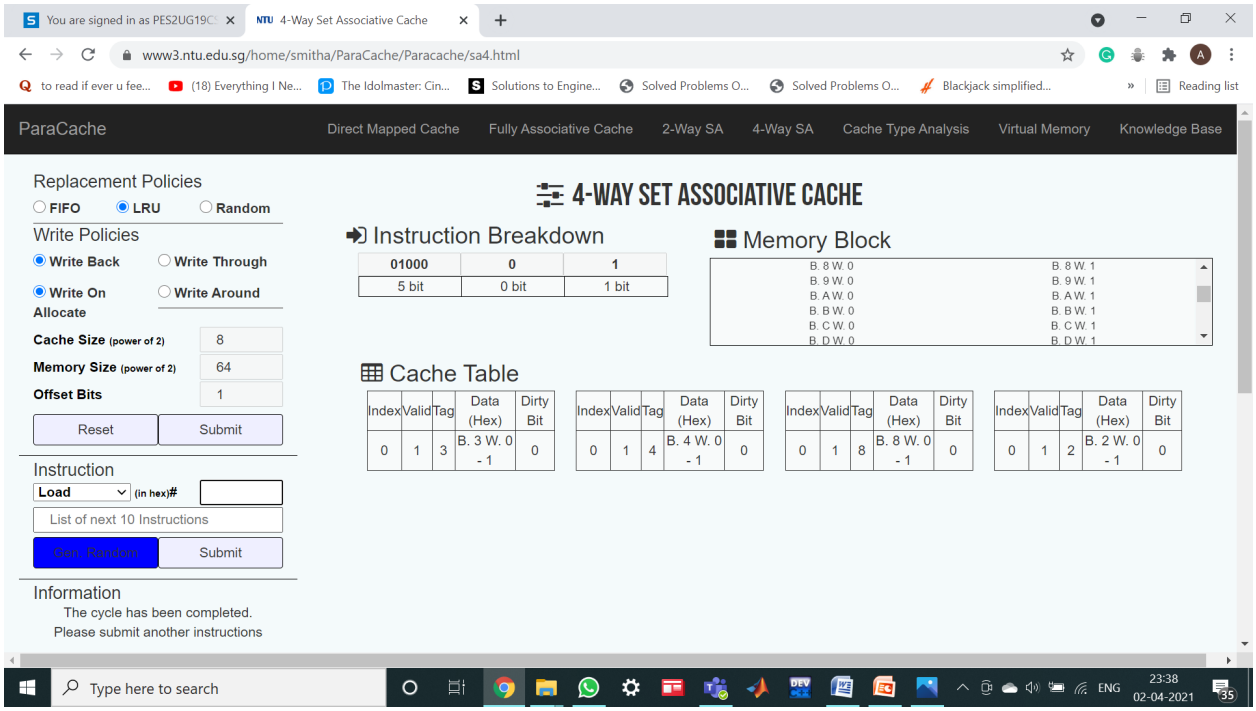


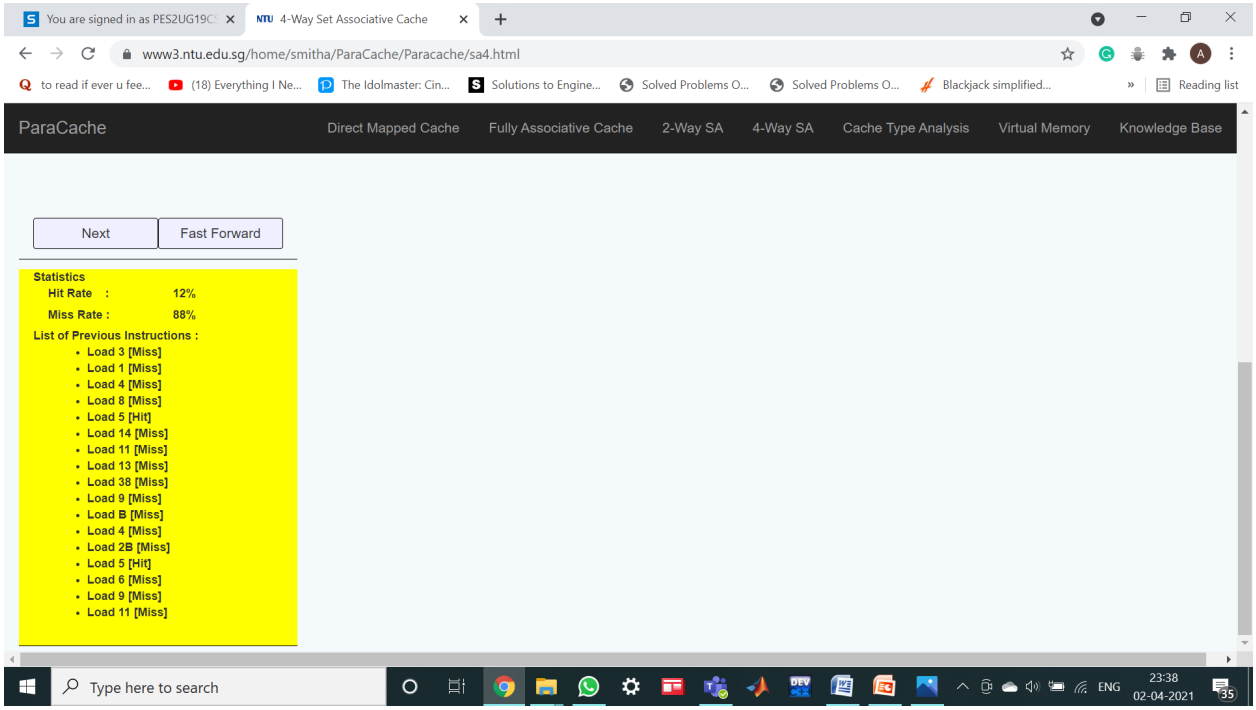
b)Two way set Associative



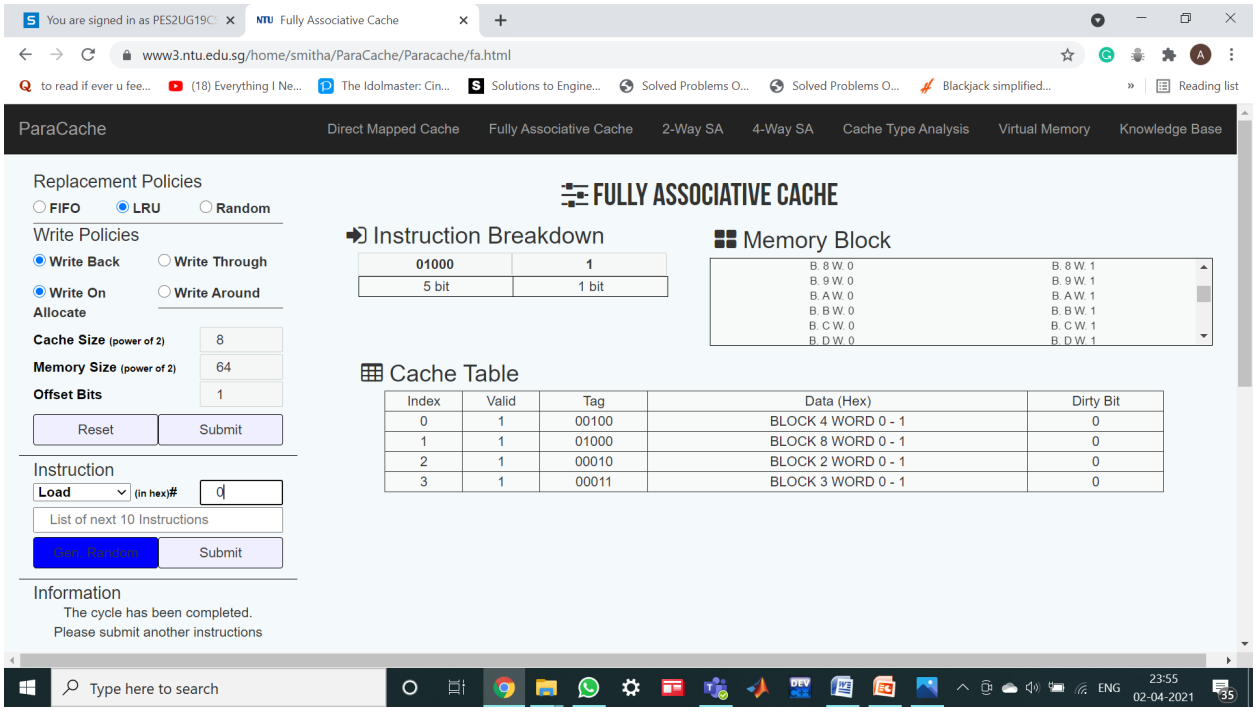


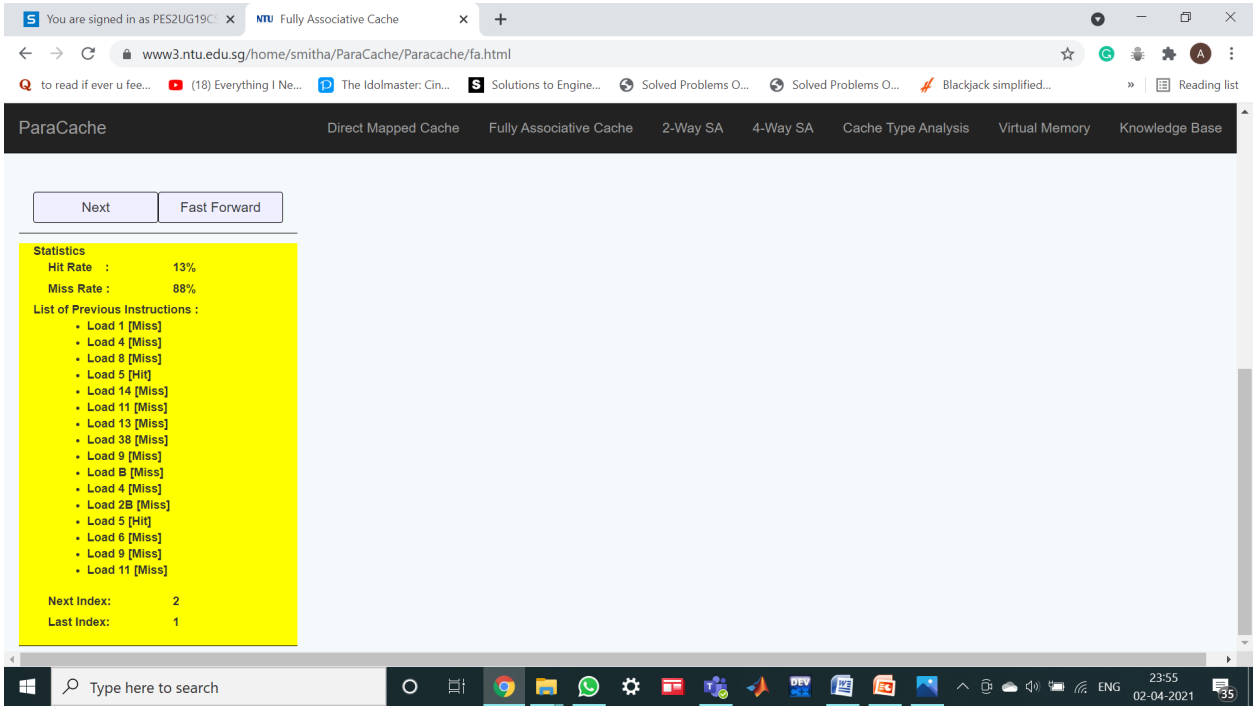
c)Four Way Set associative





d)Fully Associative




You are signed in as PES2UG19C
Fully Associative Cache
www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/fa.html
to read if ever u fee...
(18) Everything I Ne...
The Idolmaster: Cin...
Solutions to Engine...
Solved Problems O...
Solved Problems O...
Blackjack simplified...
Reading list
ParaCache
Direct Mapped Cache
Fully Associative Cache
2-Way SA
4-Way SA
Cache Type Analysis
Virtual Memory
Knowledge Base
Next
Fast Forward
Statistics
Hit Rate : 13%
Miss Rate : 88%
List of Previous Instructions :
Load 1 [Miss]
Load 4 [Miss]
Load 8 [Miss]
Load 5 [Hit]
Load 14 [Miss]
Load 11 [Miss]
Load 13 [Miss]
Load 38 [Miss]
Load 9 [Miss]
Load B [Miss]
Load 4 [Miss]
Load 2B [Miss]
Load 5 [Hit]
Load 6 [Miss]
Load 9 [Miss]
Load 11 [Miss]
Next Index: 2
Last Index: 1
Type here to search
ENG
23:55
02-04-2021