

# Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:3-4-2020

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Week# 9 Program Number: 1

## Title of the Program

1. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

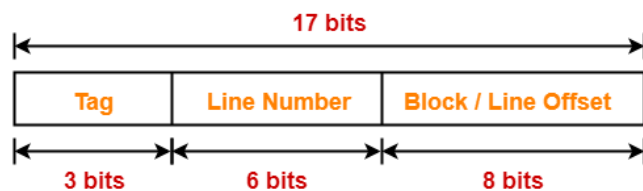
**Solution:**

**Given-**

**Cache memory size = 16 KB**

**Block size = Frame size = Line size = 256 bytes**

**Main memory size = 128 KB =  $2^{17}$**



Write Policies  
☒ Write Back ☐ Write Through  
☒ Write On ☐ Write Around  
Allocate  
Cache Size (power of 2) 16384  
Memory Size (power of 2) 131072  
Offset Bits 8  
Reset Submit

## DIRECT MAPPED CACHE

### Instruction Breakdown

000	000000	00010001
3 bit	6 bit	8 bit

### Memory Block

B 0 W 0	B 0 W 1	B 0 W 2	B 0 W 3	B 0 W 4	B 0 W 5	B 0 W 6	B 0 W 7	I
B 1 W 0	B 1 W 1	B 1 W 2	B 1 W 3	B 1 W 4	B 1 W 5	B 1 W 6	B 1 W 7	I
B 2 W 0	B 2 W 1	B 2 W 2	B 2 W 3	B 2 W 4	B 2 W 5	B 2 W 6	B 2 W 7	I
B 3 W 0	B 3 W 1	B 3 W 2	B 3 W 3	B 3 W 4	B 3 W 5	B 3 W 6	B 3 W 7	I
R 4 W 0	R 4 W 1	R 4 W 2	R 4 W 3	R 4 W 4	R 4 W 5	R 4 W 6	R 4 W 7	I

### Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0

Instruction  
Load (in hex)#  
List of next 10 Instructions  
Scan Random Submit

Information  
The cycle has been completed.  
Please submit another instructions

Next Fast Forward

Statistics  
Hit Rate : 94%  
Miss Rate : 6%  
List of Previous Instructions :  
• Load 1 [Miss]  
• Load 4 [Hit]  
• Load 8 [Hit]  
• Load 5 [Hit]  
• Load 14 [Hit]  
• Load 11 [Hit]  
• Load 13 [Hit]  
• Load 38 [Hit]  
• Load 9 [Hit]  
• Load 8 [Hit]  
• Load 4 [Hit]  
• Load 28 [Hit]  
• Load 5 [Hit]  
• Load 6 [Hit]  
• Load 11 [Hit]

11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0

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Week# 9 Program Number: 2

2. computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

(b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

**A) Tag = 5, Block = 5, Word = 6**

The screenshot shows the ParaCache simulator interface. The top navigation bar includes links for Direct Mapped Cache, Fully Associative Cache, 2-Way SA, 4-Way SA, Cache Type Analysis, Virtual Memory, and Knowledge Base. The main interface is titled "DIRECT MAPPED CACHE".

**Write Policies:** Write Back (selected), Write Through, Write On Allocate, Write Around.

**Cache Size (power of 2):** 2048

**Memory Size (power of 2):** 65536

**Offset Bits:** 6

**Reset** **Submit**

**Instruction Breakdown:**

00000	00000	010001
5 bit	5 bit	6 bit

**Memory Block:**

B.0W.0	B.0W.1	B.0W.2	B.0W.3	B.0W.4	B.0W.5	B.0W.6	B.0W.7
B.1W.0	B.1W.1	B.1W.2	B.1W.3	B.1W.4	B.1W.5	B.1W.6	B.1W.7
B.2W.0	B.2W.1	B.2W.2	B.2W.3	B.2W.4	B.2W.5	B.2W.6	B.2W.7
B.3W.0	B.3W.1	B.3W.2	B.3W.3	B.3W.4	B.3W.5	B.3W.6	B.3W.7
R.4W.0	R.4W.1	R.4W.2	R.4W.3	R.4W.4	R.4W.5	R.4W.6	R.4W.7

**Cache Table:**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000	BLOCK 0 WORD 0 - 63	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0

**Instruction:** Load (in hex)# [ ]

**List of next 10 Instructions:**

**Generate Random** **Submit**

**Information:** The cycle has been completed. Please submit another instructions

Next Fast Forward

Statistics  
Hit Rate : 94%  
Miss Rate : 6%

List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Hit]
- Load 8 [Hit]
- Load 5 [Hit]
- Load 14 [Hit]
- Load 11 [Hit]
- Load 13 [Hit]
- Load 38 [Hit]
- Load 9 [Hit]
- Load 8 [Hit]
- Load 4 [Hit]
- Load 2B [Hit]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Hit]
- Load 11 [Hit]

10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

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Week# 9 Program Number: 3

3. Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Randomly generate 10 addresses and find hit rate and miss rate.

### Solution:

- Given-
- Cache memory size = 16 KB
  - Block size = Frame size = Line size = 256 bytes
  - Main memory size = 128 KB = 217 bytes
- Thus, Number of bits in physical address = 17 bits

The screenshot shows the ParaCache simulator interface. The main title is "2-WAY SET ASSOCIATIVE CACHE". The interface includes several sections:

- Replacement Policies:** FIFO (selected), LRU, Random.
- Write Policies:** Write Back (selected), Write Through, Write On, Write Around.
- Allocate:** Cache Size (power of 2) set to 16384, Memory Size (power of 2) set to 131072, Offset Bits set to 8. Buttons for Reset and Submit are present.
- Instruction Breakdown:** A table showing instruction addresses and their bit lengths.
 

Address	0000	00000	00010001
	4 bit	5 bit	8 bit
- Memory Block:** A grid showing memory blocks with addresses from B.0W.0 to R.4W.7.
- Cache Table:** Two tables showing the state of the cache sets.
 

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B.0W.0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0

At the bottom, there is an "Instruction" section with a "Load" button and a "List of next 10 Instructions" field. An "Information" section at the bottom right states: "The cycle has been completed. Please submit another instructions".

ParaCache

Direct Mapped CacheFully Associative Cache2-Way SA4-Way SACache Type AnalysisVirtual MemoryKnowledge Base

NextFast Forward

Statistics

Hit Rate : 94%

Miss Rate : 6%

List of Previous Instructions :

• Load 1 [Miss]

• Load 4 [Hit]

• Load 8 [Hit]

• Load 5 [Hit]

• Load 14 [Hit]

• Load 11 [Hit]

• Load 13 [Hit]

• Load 38 [Hit]

• Load 9 [Hit]

• Load 8 [Hit]

• Load 4 [Hit]

• Load 28 [Hit]

• Load 5 [Hit]

• Load 6 [Hit]

• Load 9 [Hit]

• Load 11 [Hit]

13	0	-	0	0	13	0	-	0	0
14	0	-	0	0	14	0	-	0	0
15	0	-	0	0	15	0	-	0	0
16	0	-	0	0	16	0	-	0	0
17	0	-	0	0	17	0	-	0	0
18	0	-	0	0	18	0	-	0	0
19	0	-	0	0	19	0	-	0	0
20	0	-	0	0	20	0	-	0	0
21	0	-	0	0	21	0	-	0	0
22	0	-	0	0	22	0	-	0	0
23	0	-	0	0	23	0	-	0	0
24	0	-	0	0	24	0	-	0	0
25	0	-	0	0	25	0	-	0	0
26	0	-	0	0	26	0	-	0	0
27	0	-	0	0	27	0	-	0	0
28	0	-	0	0	28	0	-	0	0
29	0	-	0	0	29	0	-	0	0
30	0	-	0	0	30	0	-	0	0
31	0	-	0	0	31	0	-	0	0

Type here to search

ENG

14:50

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Week# 9 Program Number: 4

4. Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty. The following addresses are generated by the CPU. All values in hexadecimal.

Clearly label data that is replaced in cache lines.

Show the cache memory table and filled data in the cache lines of block size 1 byte.

LRU Policy is used.

The cache is mapped as

a) Direct Mapped

**ParaCache** Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

**Write Policies**  
☒ Write Back ☐ Write Through  
☒ Write On ☐ Write Around

**Allocate**  
 Cache Size (power of 2): 8  
 Memory Size (power of 2): 64  
 Offset Bits: 1  
 Reset Submit

**Instruction Breakdown**

010	00	1
3 bit	2 bit	1 bit

**Memory Block**

B 8 W 0	B 8 W 1
B 9 W 0	B 9 W 1
B A W 0	B A W 1
B B W 0	B B W 1
B C W 0	B C W 1
B D W 0	B D W 1

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	010	BLOCK 8 WORD 0 - 1	0
1	1	101	BLOCK 15 WORD 0 - 1	0
2	1	000	BLOCK 2 WORD 0 - 1	0
3	1	000	BLOCK 3 WORD 0 - 1	0

**Instruction**  
 Load (in hex)#  
 List of next 10 Instructions  
 Get Random Submit

**Information**  
 The cycle has been completed.  
 Please submit another instructions

You are signed in as PES2UG19C... NTU Direct Mapped Cache Simulator

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html

to read if ever u fee... (18) Everything I Ne... The Idolmaster: Cin... Solutions to Engine... Solved Problems O... Solved Problems O... Blackjack simplified... Reading list

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Please submit another instructions

Next Fast Forward

**Statistics**

Hit Rate : 19%

Miss Rate : 81%

List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Miss]
- Load 38 [Miss]
- Load 9 [Miss]
- Load B [Miss]
- Load 4 [Miss]
- Load 2B [Miss]
- Load 5 [Hit]
- Load 6 [Miss]
- Load 9 [Hit]
- Load 11 [Miss]

Type here to search

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## b)Two way set Associative

You are signed in as PES2UG19C... NTU 2-Way Set Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa2.html

to read if ever u fee... (18) Everything I Ne... The Idolmaster: Cin... Solutions to Engine... Solved Problems O... Solved Problems O... Blackjack simplified... Reading list

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

**Replacement Policies**

☐ FIFO ☒ LRU ☐ Random

**Write Policies**

☒ Write Back ☐ Write Through

☒ Write On ☐ Write Around

**Allocate**

Cache Size (power of 2) 8

Memory Size (power of 2) 64

Offset Bits 1

Reset Submit

**Instruction**

Load (in hex)#

List of next 10 Instructions

Get Random Submit

**Information**

The cycle has been completed.

Please submit another instructions

**2-WAY SET ASSOCIATIVE CACHE**

**Instruction Breakdown**

0100	0	1
4 bit	1 bit	1 bit

**Memory Block**

B 8 W 0	B 8 W 1
B 9 W 0	B 9 W 1
B A W 0	B A W 1
B B W 0	B B W 1
B C W 0	B C W 1
B D W 0	B D W 1

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 8 WORD 0 - 1	0
1	1	a	BLOCK 15 WORD 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 4 WORD 0 - 1	0
1	1	1	BLOCK 3 WORD 0 - 1	0

Type here to search

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You are signed in as PES2UG19C: x NTU 2-Way Set Associative Cache x +

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa2.html

to read if ever u fee... (18) Everything I Ne... The Idolmaster: Cin... Solutions to Engine... Solved Problems O... Solved Problems O... Blackjack simplified... Reading list

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Please submit another instructions

Next Fast Forward

**Statistics**

Hit Rate : 19%

Miss Rate : 81%

List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Miss]
- Load 38 [Miss]
- Load 9 [Miss]
- Load B [Miss]
- Load 4 [Miss]
- Load 2B [Miss]
- Load 5 [Hit]
- Load 6 [Miss]
- Load 9 [Hit]
- Load 11 [Miss]

Type here to search

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### c) Four Way Set associative

You are signed in as PES2UG19C: x NTU 4-Way Set Associative Cache x +

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa4.html

to read if ever u fee... (18) Everything I Ne... The Idolmaster: Cin... Solutions to Engine... Solved Problems O... Solved Problems O... Blackjack simplified... Reading list

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

☐ FIFO ☒ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On ☐ Write Around

Allocate

Cache Size (power of 2) 8

Memory Size (power of 2) 64

Offset Bits 1

Reset Submit

Instruction

Load (in hex)#

List of next 10 Instructions

Get Random Submit

Information

The cycle has been completed.

Please submit another instructions

## 4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

01000	0	1
5 bit	0 bit	1 bit

Memory Block

B.8.W.0	B.8.W.1
B.9.W.0	B.9.W.1
B.A.W.0	B.A.W.1
B.B.W.0	B.B.W.1
B.C.W.0	B.C.W.1
B.D.W.0	B.D.W.1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B.3.W.0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	B.4.W.0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	B.8.W.0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B.2.W.0	0

Type here to search

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NTU 4-Way Set Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/sa4.html

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Next Fast Forward

**Statistics**  
 Hit Rate : 12%  
 Miss Rate : 88%

**List of Previous Instructions :**

- Load 3 [Miss]
- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Miss]
- Load 38 [Miss]
- Load 9 [Miss]
- Load 8 [Miss]
- Load 4 [Miss]
- Load 2B [Miss]
- Load 5 [Hit]
- Load 6 [Miss]
- Load 9 [Miss]
- Load 11 [Miss]

## d)Fully Associative

NTU Fully Associative Cache

www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/fa.html

ParaCache Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

**Replacement Policies**  
☐ FIFO ☒ LRU ☐ Random

**Write Policies**  
☒ Write Back ☐ Write Through  
☒ Write On ☐ Write Around

**Allocate**  
 Cache Size (power of 2): 8  
 Memory Size (power of 2): 64  
 Offset Bits: 1  
 Reset Submit

**Instruction**  
 Load (in hex)# 0  
 List of next 10 Instructions  
 Get Random Submit

**Information**  
 The cycle has been completed.  
 Please submit another instructions

**FULLY ASSOCIATIVE CACHE**

**Instruction Breakdown**

01000	1
5 bit	1 bit

**Memory Block**

B 8 W 0	B 8 W 1
B 9 W 0	B 9 W 1
B A W 0	B A W 1
B B W 0	B B W 1
B C W 0	B C W 1
B D W 0	B D W 1

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00100	BLOCK 4 WORD 0 - 1	0
1	1	01000	BLOCK 8 WORD 0 - 1	0
2	1	00010	BLOCK 2 WORD 0 - 1	0
3	1	00011	BLOCK 3 WORD 0 - 1	0

