

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: Achyut Jagini	SRN:PES2UG19CS013	Section A
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Week# 4

Program Number: 1

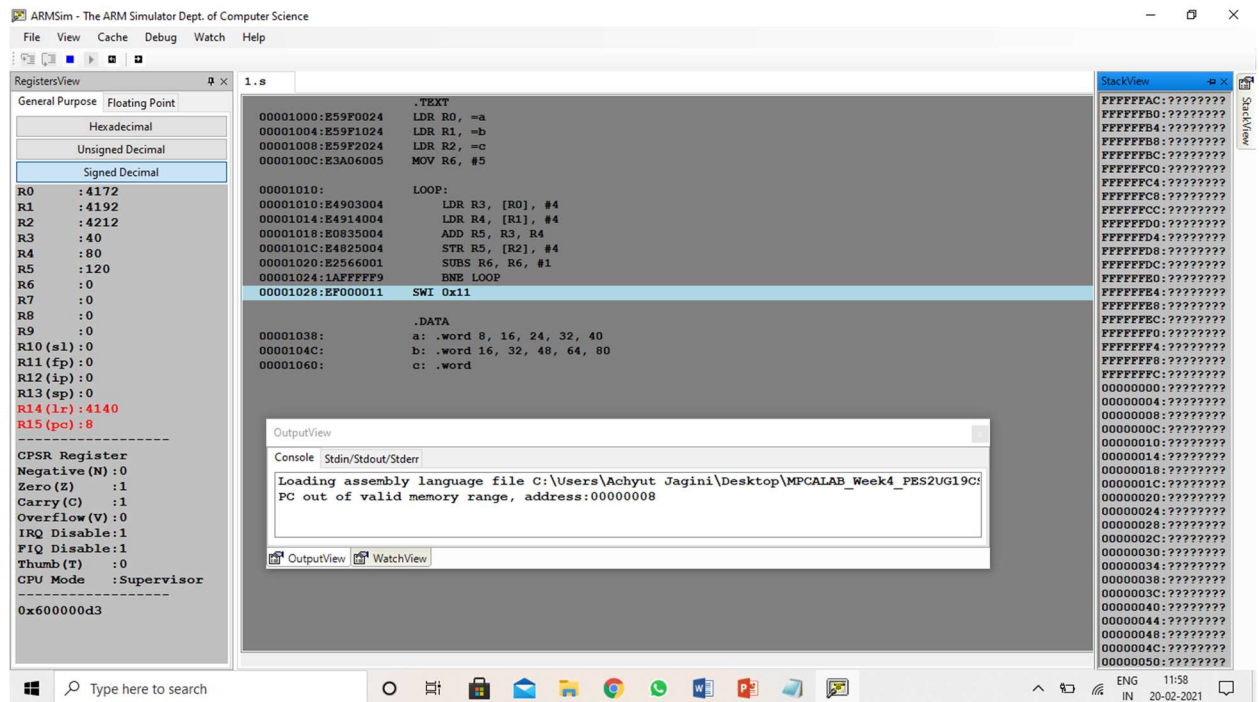
Write an ALP to implement $C[k] = a[i] + b[j]$

```
1 - Notepad
File Edit Format View Help
.TEXT
LDR R0, =a
LDR R1, =b
LDR R2, =c
MOV R6, #5

LOOP:
    LDR R3, [R0], #4
    LDR R4, [R1], #4
    ADD R5, R3, R4
    STR R5, [R2], #4
    SUBS R6, R6, #1
    BNE LOOP
SWI 0x11

.DATA
a: .word 8, 16, 24, 32, 40
b: .word 16, 32, 48, 64, 80
c: .word
```





Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name:	SRN:	Section

Week# 4

Program Number: 2

Write an ALP to implement $c[k] = a[i] * b[j]$

```
2 - Notepad
File Edit Format View Help

.TEXT
LDR R0, =a
LDR R1, =b
LDR R2, =c
MOV R6, #5

LOOP:
    LDR R3, [R0], #4
    LDR R4, [R1], #4
    MUL R5, R3, R4
    STR R5, [R2], #4
    SUB R6, R6, #1
    CMP R6, #0
    BNE LOOP
SWI 0x11

.DATA
a: .word 8, 16, 24, 32, 40
b: .word 16, 32, 48, 64, 80
c: .word
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose	Floating Point
Hexadecimal	
Unsigned Decimal	
Signed Decimal	

R0 : 4176
R1 : 4196
R2 : 4216
R3 : 40
R4 : 80
R5 : 3200
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 0
R14 (lr) : 4144
R15 (pc) : 8

CPSR Register
Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : Supervisor
0x600000d3

```
.TEXT
00001000:E59F0028 LDR R0, =a
00001004:E59F1028 LDR R1, =b
00001008:E59F2028 LDR R2, =c
0000100C:E3A06005 MOV R6, #5

00001010: LOOP:
00001010:E4903004 LDR R3, [R0], #4
00001014:E4914004 LDR R4, [R1], #4
00001018:E0050493 MUL R5, R3, R4
0000101C:E4825004 STR R5, [R2], #4
00001020:E2466001 SUB R6, R6, #1
00001024:E3560000 CMP R6, #0
00001028:1AFFFFF8 BNE LOOP
0000102C:EF000011 SWI 0x11

.DATA
0000103C: a: .word 8, 16, 24, 32, 40
00001050: b: .word 16, 32, 48, 64, 80
00001064: c: .word
```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Achyut Jagini\Desktop\MPCALAB_Week4_PES2UG19C
Execution starting ...
PC out of valid memory range, address:00000008

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0294204
Instructions per second:0

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name:	SRN:	Section

Week# ____4____

Program Number: ____3__

- a. Write an ALP to perform Convolution using MUL instruction (Addition of multiplication of respective numbers of loc A and loc B)**
- b. Write an ALP to perform Convolution using MLA instruction (Addition of multiplication of respective numbers of loc A and loc B).**

A

```
3a - Notepad
File Edit Format View Help

.TEXT
LDR R0, =a
LDR R1, =b
MOV R2, #5
MOV R5, #0

LOOP:
    LDR R3, [R0], #4
    LDR R4, [R1], #4
    MUL R6, R3, R4
    ADD R5, R5, R6
    SUBS R2, R2, #1
    BNE LOOP

SWI 0x11

.DATA
a: .word 5, 10, 15, 20, 25
b: .word 2, 4, 6, 8, 10
c: .word
```

ARMsim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4168
R1 : 4188
R2 : 0
R3 : 25
R4 : 10
R5 : 550
R6 : 250
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 0
R14 (lr) : 4140
R15 (pc) : 8

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : Supervisor

0x600000d3

3a.s

```
.TEXT
00001000:E59F0024 LDR R0, =a
00001004:E59F1024 LDR R1, =b
00001008:E3A02005 MOV R2, #5
0000100C:E3A05000 MOV R5, #0

00001010: LOOP:
00001010:E4903004 LDR R3, [R0], #4
00001014:E4914004 LDR R4, [R1], #4
00001018:E0060493 MUL R6, R3, R4
0000101C:E0855006 ADD R5, R5, R6
00001020:E2522001 SUBS R2, R2, #1
00001024:1AFFFFFF9 BNE LOOP
00001028:EF000011 SWI 0x11

00001034: .DATA
00001048: a: .word 5, 10, 15, 20, 25
0000105C: b: .word 2, 4, 6, 8, 10
c: .word
```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Achyut Jagini\Desktop\MPCALAB_Week4_PES2UG19C
Execution starting ...
PC out of valid memory range, address:00000008

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0239356
Instructions per second:0

B

```
3b - Notepad
File Edit Format View Help

.TEXT
LDR R0, =a
LDR R1, =b
MOV R2, #5
MOV R5, #0

LOOP:
    LDR R3, [R0], #4
    LDR R4, [R1], #4
    MLA R5, R3, R4, R5
    SUBS R2, R2, #1
    BNE LOOP
SWI 0x11

.DATA
a: .word 5, 10, 15, 20, 25
b: .word 2, 4, 6, 8, 10
c: .word
```

ARMsim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4164

R1 : 4184

R2 : 0

R3 : 25

R4 : 10

R5 : 550

R6 : 0

R7 : 0

R8 : 0

R9 : 0

R10 (s1) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 0

R14 (lr) : 4136

R15 (pc) : 8

CPSR Register

Negative (N) : 0

Zero (Z) : 1

Carry (C) : 1

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : Supervisor

0x600000d3

3b.s

```
.TEXT
00001000:E59F0020 LDR R0, =a
00001004:E59F1020 LDR R1, =b
00001008:E3A02005 MOV R2, #5
0000100C:E3A05000 MOV R5, #0

00001010:      LOOP:
00001010:E4903004 LDR R3, [R0], #4
00001014:E4914004 LDR R4, [R1], #4
00001018:E0255493 MLA R5, R3, R4, R5
0000101C:E2522001 SUBS R2, R2, #1
00001020:1AFFFFFFFA BNE LOOP
00001024:EF000011 SWI 0x11

.DATA
00001030:      a: .word 5, 10, 15, 20, 25
00001044:      b: .word 2, 4, 6, 8, 10
00001058:      c: .word
```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Achyut Jagini\Desktop\MPCALAB_Week4_PES2UG19CS

Execution starting ...

PC out of valid memory range, address:00000008

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0249343

Instructions per second:0

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name:	SRN:	Section

Week# 4

Program Number: 4

Write an ALP to read from a 2D array such that

B=a[i] [j]

```

4 - Notepad
File Edit Format View Help
|.TEXT
LDR R0, =a
LDR R1, =b
MOV R2, #3 @ #Rows and #Columns (Square Matrix)
MOV R3, #4 @ Size of Word

MOV R4, #0 @ i = 0
FOR_I:
    MOV R5, #0 @ j = 0
    FOR_J:
        MLA R6, R4, R2, R5
        MLA R6, R3, R6, R0 @ Required Address of Matrix A
        LDR R7, [R6]
        MLA R6, R4, R2, R5
        MLA R6, R3, R6, R1 @ Required Address of Matrix B
        STR R7, [R6]
        ADD R5, R5, #1
        CMP R5, R2
        BNE FOR_J
    ADD R4, R4, #1
    CMP R4, R2
    BNE FOR_I
SWI 0x11

.DATA
a: .word 3, 6, 9, 12, 15, 18, 21, 24, 27
b: .word

```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0	:4180
R1	:4216
R2	:3
R3	:4
R4	:3
R5	:3
R6	:4248
R7	:27
R8	:0
R9	:0
R10 (s1)	:0
R11 (fp)	:0
R12 (ip)	:0
R13 (sp)	:0
R14 (lr)	:4172
R15 (pc)	:8

CPSR Register

Negative (N) : 0

Zero (Z) : 1

Carry (C) : 1

Overflow (V) : 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T) : 0

CPU Mode : Supervisor

0x600000d3

4.s

```

|.TEXT
00001000:E59F0044 LDR R0, =a
00001004:E59F1044 LDR R1, =b
00001008:E3A02003 MOV R2, #3 @ #Rows and #Columns (Square Matrix)
0000100C:E3A03004 MOV R3, #4 @ Size of Word

00001010:E3A04000 MOV R4, #0 @ i = 0
00001014:
FOR_I:
    MOV R5, #0 @ j = 0
    FOR_J:
        MLA R6, R4, R2, R5
        MLA R6, R3, R6, R0 @ Required Address of Matrix A
        LDR R7, [R6]
        MLA R6, R4, R2, R5
        MLA R6, R3, R6, R1 @ Required Address of Matrix B
        STR R7, [R6]
        ADD R5, R5, #1
        CMP R5, R2
        BNE FOR_J
    ADD R4, R4, #1
    CMP R4, R2
    BNE FOR_I
SWI 0x11

.DATA
00001054: a: .word 3, 6, 9, 12, 15, 18, 21, 24, 27
00001078: b: .word

```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Achyut Jagini\Desktop\MPCALAB_Week4_PES2UG19C...

Execution starting ...

PC out of valid memory range, address:00000008

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0199479

Instructions per second:0

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name:	SRN:	Section

Week# 4

Program Number: 5

Write an ALP to implement $C[i][j] = a[i][j] + b[i][j]$

```

5 - Notepad
File Edit Format View Help

.TEXT
LDR R0, =a
LDR R1, =b
LDR R2, =c
MOV R3, #3 @ #Rows and #Columns (Square Matrix)
MOV R4, #4 @ Size of Word

MOV R5, #0 @ i
FOR_I:
    MOV R6, #0 @ j
    FOR_J:
        MLA R7, R5, R3, R6
        MLA R7, R4, R7, R0 @ Required Address of Matrix A
        LDR R8, [R7]
        MLA R7, R5, R3, R6
        MLA R7, R4, R7, R1 @ Required Address of Matrix B
        LDR R9, [R7]
        ADD R7, R8, R9 @ Sum
        MLA R8, R5, R3, R6
        MLA R8, R4, R8, R2 @ Required Address of Matrix C
        STR R7, [R8]
        ADD R6, R6, #1
        CMP R6, R3
        BNE FOR_J
    ADD R5, R5, #1
    CMP R5, R3
    BNE FOR_I
SWI 0x11

.DATA
a: .word 3, 6, 9, 12, 15, 18, 21, 24, 27
b: .word 1, 2, 3, 4, 5, 6, 7, 8, 9
c: .word

```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal	Unsigned Decimal	Signed Decimal
R0	:4204	
R1	:4240	
R2	:4276	
R3	:3	
R4	:4	
R5	:3	
R6	:3	
R7	:36	
R8	:4308	
R9	:9	
R10 (s1)	:0	
R11 (fp)	:0	
R12 (ip)	:0	
R13 (sp)	:0	
R14 (lr)	:4192	
R15 (pc)	:8	

CPSR Register

Negative (N): 0

Zero (Z): 1

Carry (C): 1

Overflow (V): 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T): 0

CPU Mode: Supervisor

0x600000d3

5.s

```

.TEXT
00001000:E59F0058 LDR R0, =a
00001004:E59F1058 LDR R1, =b
00001008:E59F2058 LDR R2, =c
0000100C:E3A03003 MOV R3, #3 @ #Rows and #Columns (Square Matrix)
00001010:E3A04004 MOV R4, #4 @ Size of Word

00001014:E3A05000 MOV R5, #0 @ i
00001018:
FOR_I:
00001018:E3A06000 MOV R6, #0 @ j
0000101C:
FOR_J:
0000101C:E0276395 MLA R7, R5, R3, R6
00001020:E0270794 MLA R7, R4, R7, R0 @ Required Address of Matrix A
00001024:E5978000 LDR R8, [R7]
00001028:E0276395 MLA R7, R5, R3, R6
0000102C:E0271794 MLA R7, R4, R7, R1 @ Required Address of Matrix B
00001030:E5979000 LDR R9, [R7]
00001034:E0867009 ADD R7, R8, R9 @ Sum
00001038:E0286395 MLA R8, R5, R3, R6
0000103C:E0282894 MLA R8, R4, R8, R2 @ Required Address of Matrix C
00001040:E5887000 STR R7, [R8]
00001044:E2866001 ADD R6, R6, #1
00001048:E1560003 CMP R6, R3
0000104C:1AFFFFF2 BNE FOR_J
00001050:E2855001 ADD R5, R5, #1
00001054:E1550003 CMP R5, R3
00001058:1AFFFFE2 BNE FOR_I
0000105C:EF000011 SWI 0x11

```

OutputView

Console Stdin/Stdout/Stderr

```

Loading assembly language file C:\Users\Achyut Jagini\Desktop\MPCALAB_Week4_PES2UG19C
Execution starting ...
PC out of valid memory range, address:00000008

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0199453
Instructions per second:0

```

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

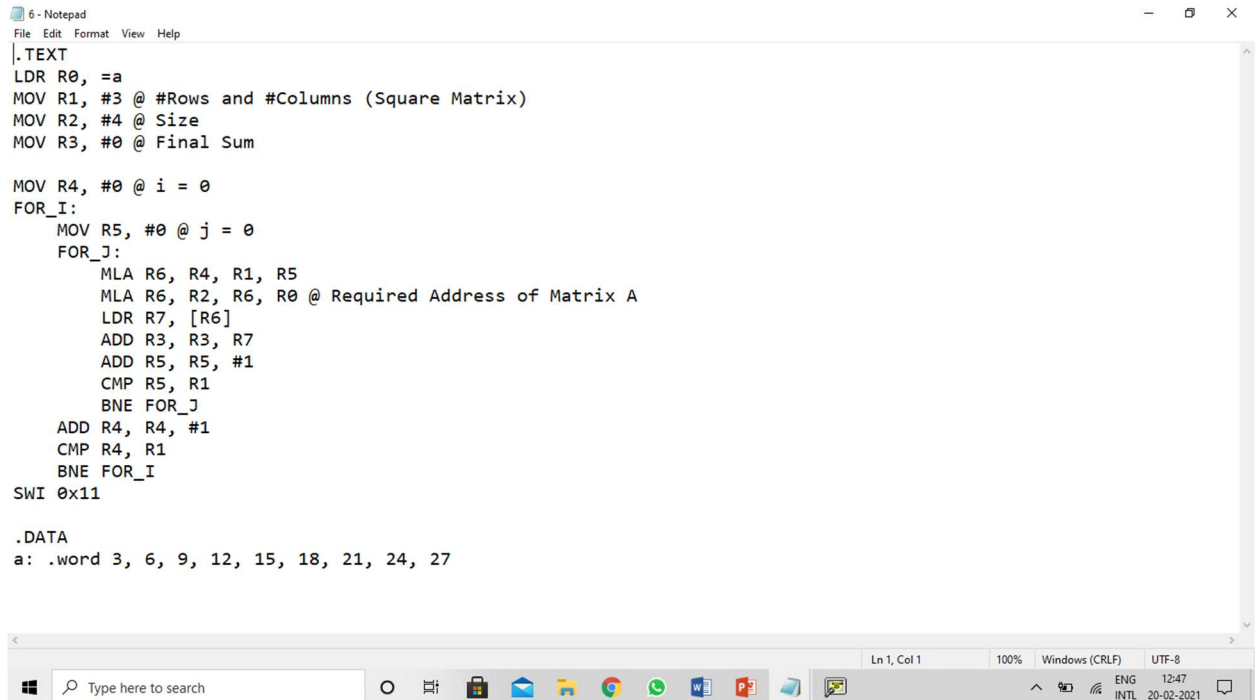
Date:

Name:	SRN:	Section
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Week# 4

Program Number: 6

Write an ALP to implement $\text{Sum}[i] += a[i][j]$



```
6 - Notepad
File Edit Format View Help
;.TEXT
LDR R0, =a
MOV R1, #3 @ #Rows and #Columns (Square Matrix)
MOV R2, #4 @ Size
MOV R3, #0 @ Final Sum

MOV R4, #0 @ i = 0
FOR_I:
    MOV R5, #0 @ j = 0
    FOR_J:
        MLA R6, R4, R1, R5
        MLA R6, R2, R6, R0 @ Required Address of Matrix A
        LDR R7, [R6]
        ADD R3, R3, R7
        ADD R5, R5, #1
        CMP R5, R1
        BNE FOR_J
        ADD R4, R4, #1
        CMP R4, R1
        BNE FOR_I
    SWI 0x11

.DATA
a: .word 3, 6, 9, 12, 15, 18, 21, 24, 27
```

