HW2 – Due 30 / 05 / 2020 23:00pm (No late submission)

Questions

Q.1 - 4.6 from 5th edition (4.6.1, 4.6.2, 4.6.3 included)

Q.2 - 4.8 from 5th edition (4.8.1, 4.8.2, 4.8.3, 4.8.4, 4.8.6 included)

Q.3 -We wish to add the instruction **addi (add immediate)** to the single-cycle datapath described in the chapter. Add any necessary datapaths and control signals to the single-cycle datapath of the Figure 4.24 which represents the datapath and show the necessary additions (if any) to the Figure 4.18 which represents the setting of the control lines.

Q.4. - Assume that you are required to extend our single-cycle MIPS implementation so that it handles the "jnew" instruction, where "jnew" has R-type instruction format where rd field is 0. An example is given below:
Example: jnew $s3, $s4 # unconditionally jump to the address given in Memory[$s3+$s4]

PC← Memory[$s3+$s4]

Explain your design by listing the required changes in the complete single-cycle datapath clearly given in Figure 4.24 (additional wires, muxes and control and selector signals if necessary).

Note that no late submission will be accepted and the questions will be solved during the problem session. Note that a selected subset of these questions will be graded.

For the homework, you have to work alone and submit your own work. In case of any form of copying all parties will get 0 grade.