MULTILAYER COATINGS FOR ATHENA
Technical Notes 8 - Coated full substrates, deposition process and stress results

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1 Introduction

This presents the description of coated full substrates for WP4000, including improvements in the calibration procedure and results from qualification and stress tests. The deposition process along with coating equipment are described in detail in TN4 [1], The calibration process has been improved and is described in this TN. The coating applied to the SPO substrates are the optimized coating recipes for ATHENA described in TNs 2 and 7 [2, 3] , those consist of bi/tri-layer coatings and linearly graded multilayers with 5 to 10 bilayers. The qualification procedure includes stress measurements performed at DTU Space.

2 Calibration

Calibration coatings of each individual material are necessary to determine the coating rate and affect directly the capacity of producing samples that match the desired coating recipe.

In short, a calibration coating is a coating of 10 bi-layers of constant d-spacing. Applying a single speed on the ring and producing 10 bilayers facilitates the measurements through X-ray Reflectometry (XRR) and allows for determination of the exact d-spacing and ratio between light and heavy material in each bilayer (Γ).

For WP3000, two calibration coatings were fit by a linear regression to get the coating rate for each materials in a bi-layer, under the assumption that the coating rate is constant for any material throughout the coating. The calibration procedure considered for WP3000 was not sufficient to closely reproduce the optimized recipes. The assumption of constant coating rate throughout the coating was not valid. The procedure for calibration is now improved and all samples for WP4000 have been produced considering the improved procedure.

The improvement consists of eliminating the change in Γ throughout a graded d-spacing coating. For W/Si coatings, the change in Γ can go from 0.55 to 0.65 depending on the d-space thickness. For a multilayer with five bi-layers and large variation of thickness of each bi-layer, variations in Γ can result in a significant difference on the coated layer thickness compared to desired recipe.

To address this issue, a thorough calibration was done for the material used for multilayer coating, W/Si and W/B_4C. Six calibration coatings of each material combination with varying d-spacing and ten bilayers were produced. The samples are measured and the d-spacing plotted against the reverse speed of the sample ring (since more speed on the sample ring results in thinner coatings), the data points are easily fit by a linear equation and that allows for the determination of the sample ring speed required for any particular thickness.

Since Γ changes according to layer thicknesses, it is desirable to separate the measured d-spacings into layer thickness of each material. This results in two data sets, one for each material, each with six data points that can be fit by a linear equation. When trying to create a linear graded multilayer with this information, the required sample ring speed is the same for both materials at low d-spacings (2 to 6 nm), but at higher d-spacings the sample ring speed are different for each material.

In the DTU coating chamber, a single bi-layer is made by letting the sample ring make a single revolution at a constant speed, therefor, the required speed has to be the same for both materials and that is a problem for higher d-spacings. To solve this problem, the power on the heavier material cathode is changed manually for each layer.

The calculations for each individual bilayer are done as follows:

For a bilayer with a thickness of 5 nm and a $\Gamma = 0.6$, the speed of the sample ring, v_{Si}, is calculated according to the Si layer thickness of 3 nm,

$$v_{Si} = \frac{a_{Si}}{d_{Si} - b_{Si}} , \tag{1}$$

where a_{Si} is the slope of the line fitted with the calibration data for Si in the W/Si calibration coatings and b_{Si} is the intersection of the line with the y-axis. d_{Si} is the desired thickness of the Si layer. The speed of the sample ring will of course be the same for W, but the power has to be corrected according to the equation:

$$P_W = P_0 \cdot \frac{a_W v_{Si}^{-1} + b_W}{d_W} \tag{2}$$

where P_W is the power of the cathode, P_0 is the power used during calibration of the material, a_W is the slope of the line fitted with the calibration data for W in the W/Si calibration coatings and b_W is the intersection of the line with the y-axis. d_W is the desired thickness of the W layer.

3 Coating of full substrates

The selection of coating recipes for production of full substrates was made considering the results obtained in WP3000 and reported in TNs 6 and 7 [4, 3]. The substrates used are standard SPO plates, wedged, ribbed and with no resist stripes. Plates without

Material	type	recipe	plate number
$Cr/Ir/B_4$	tri-layer	10/10/8 (nm)	05-03-07
Pt/B_4	bi-layer	11/11 (nm)	53-04-31
W/Si	multilayer	row 1, n=5	64-04-00
W/Si	multilayer	row 6, n=5	52-07-17
W/Si	multilayer	row 12, n=10	64-03-27
W/B_4C	multilayer	row 1, n=5	64-01-17
W/B_4C	multilayer	row 6, n=5	52-08-07
W/B_4C	multilayer	row 12, n=10	64-02-30

Table 1: Overview of coated samples.

Material	type	compressive stress
$Cr/Ir/B_4$	tri-layer	1004
Pt/B_4	bi-layer	303
W/Si	multilayer, row 1	268
W/Si	multilayer, row 6	482
W/Si	multilayer, row 12	229
W/B_4C	multilayer, row 1	2822
W/B_4C	multilayer, row 6	1927
W/B_4C	multilayer, row 12	2215

Table 2: Compressive stress measurements. Values listed in units of MPa^{-1}.

resist were used for the full substrate production due to the limited number of plates with resist layer available.

A total of 8 SPO plates were coated, those are: $Cr/Ir/B_4C$ tri-layer, Pt/B_4C bi-layer, W/Si multilayer considering optimized recipes for rows 1, 6 and 12, and W/B_4C multilayer considering optimized recipes for row 1, 6 and 12. Table 1 summarizes the full substrates samples. Pt/B_4C multilayer recipes were not coated during this campaign because of the high surface roughness observed for this coating in WP3000.

4 Stress tests

Stress tests were performed using the same procedure described in TN 5 [5] for all samples coated. The stress values observed are listed in table 2. Figure 1 shows the comparison between stress measurements obtained for WP4000 and previous measurements.

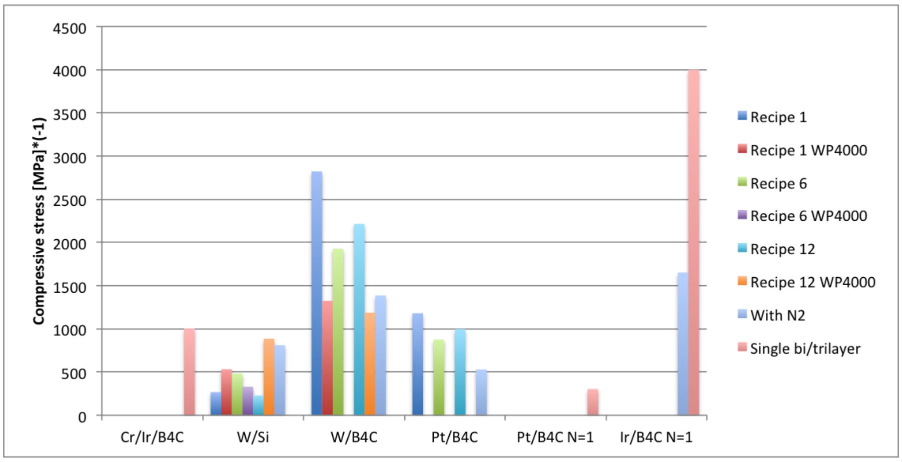

Figure 1: Comparison between compressive stress measurements obtained for WP4000 and previous measurements.

References

[1] D. D. M. Ferreira, A. C. Jakobsen, and F. E. Christensen. Technical Notes 4, v.2, IXO/DTUS/SYS/TN/0004. Technical report, September 2011.

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[5] A. C. Jakobsen, D. D. M. Ferreira, and F. E. Christensen. Technical Notes 5, v.2, IXO/DTUS/SYS/TN/0005. Technical report, August 2012.