# AppKit:
## Using the LTC1298 12-bit Analog-to-Digital Converter

This AppKit shows how to use the Linear Technology LTC 1298 12-bit ADC chip with PIC microcontrollers and the Parallax BASIC Stamp® single-board computer.

### Description

The LTC1298 is a 12-bit analog-to-digital converter (ADC). It is internally referenced to the 5-volt power supply, providing voltage measurements with 1.22-millivolt resolution. It has an internal sample-and-hold feature that prevents errors when it is used to measure rapidly changing signals.

The LTC1298 can be configured as a two-channel ADC or single-channel differential ADC. In two-channel mode, the selected channel's voltage is measured relative to ground and returned as a value between 0 and 4095. In differential mode, the voltage difference between the two inputs is measured and returned as a value between 0 and 4095.

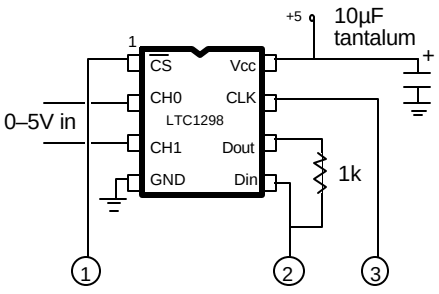
Supply current is typically 250 µA when the unit is operating, 1 nA (one-billionth of an ampere) when it is not. The maximum clock rate for the LTC1298's three-wire serial interface is 200 kHz, permitting up to 11,100 samples to be taken per second.

### Hardware interface

The LTC1298 interfaces with controllers through four pins: chip select (CS), clock (CLK), data in (DIN) and data out (DOUT). Since PICs can readily switch between input and output on the fly, the interface shown in the figure combines DIN and DOUT into a single connection.

As shown in the figure, the manufacturer recommends a 1- to 10-µF bypass capacitor with good high-frequency qualities; a ceramic unit at the low end of the scale, tantalum at the higher end. Since the supply voltage also serves as the ADC's voltage reference, it must be well regulated to avoid measurement errors. Since the LTC1298 draws very little current, you may use a precision voltage reference Zener diode (such as the LM336) as a regulator.

See the manufacturer's documentation at the end of this App Kit for pcb design notes and analog characteristics.




| | PIC | Stamp |
|---|---|---|
| ① | ra.0 | pin 0 |
| ② | ra.2 | pin 2 |
| ③ | ra.1 | pin 1 |

## Software Interface

From a software standpoint, using the LTC1298 boils down to this:

(1) Activate CS by taking it low.
(2) Send (shift out) configuration bits to the LTC1298.
(3) Read (shift in) the 12-bit measurement from the LTC1298.
(4) Deactivate CS by taking it high.

The program listings and data sheets show these processes in detail.

## PIC Program Listing

```
; PROGRAM: LTC1298.SRC (Read LTC1298 analog-to-digital converter).
; Program demonstrates the use of an external serial ADC (Linear Tech
; LTC1298) with PIC16C5x-series controllers. Variable dc voltages
; (0-5V) at pins 2 or 3 of the ADC control the 12-bit value of the
; variable ADres.

CS          =       ra.0            ; Connect to CS pin of 1298.
CLK         =       ra.1            ; Connect to CLK pin.
DATA        =       ra.2            ; Connect to Din and Dout pins.

; Put variable storage above special-purpose registers.
            org     8
clocks      ds      1               ; Clock-cycle counter.
ADresH      ds      1               ; High byte of 12-bit ADC result.
ADresL      ds      1               ; Low byte of 12-bit ADC result.
cnfig       ds      1               ; Holds configuration bits for ADC.

startb      =       cnfig.0         ; Start-bit for conversation with ADC (always 1).
sglDif      =       cnfig.1         ; 1=single-ended, 2-ch; 0=differential, 1-ch
oddSign     =       cnfig.2         ; Selects ch 0 or 1 for input or + polarity.
msbf        =       cnfig.3         ; MSBF mode select (always 1).
xmit        =       0               ; TRIS setting to send data to LTC1298.
recv        =       100b            ; TRIS setting to receive data from LTC1298.
fixBs       =       1001b           ; Fixed bits for configuration setting.
outClk      =       4               ; Number of bits sent to LTC1298.
inClk       =       13              ; Number of bits received from LTC1298.

; Remember to change device info when programming part.
            device  pic16c55,xt_osc,wdt_off,protect_off
            reset   start

; Set starting point in program ROM to zero
            org     0
start       mov     !ra, #xmit      ; Set TRIS ra to send configuration to ADC.
            mov     !rb,#0          ; Set TRIS rb and rc to output.
            mov     !rc,#0
            setb    CS              ; Deselect LTC1298 for now.

; Set up the configuration bits. A 1 in sglDif means a single-ended conversion;
; 0 meansdifferential. For single-ended measurements, oddSign selects the channel:
; 0 = channel 0; 1 = channel 1. For differential conversions, oddSign selects polarity: 1
;  = channel 1 +, 0 = channel 0 +.

            setb    sglDif          ; Set for single-ended.
            clrb    oddSign         ; Sample channel 0.
```

## PIC Program Listing (cont.)

```
; Call the ADC subroutine.
                call    convert
                mov     rb, ADresL          ; Put the bits of ADC result on rb and rc.
                mov     rb, ADresH
                jmp     $                   ; Stop program: results in registers 9 and A.

; This is the subroutine that gets the conversion from the LTC1298. Upon
; entry, the configuration bits must be set up in the cnfig register.
; Upon exit, the 12-bit result will be in ADresH/L. The cnfig register
; will have been restored to its original state.

; This conversion routine will work properly at PIC clock speeds up to 8 MHz.
; Faster clocks will violate the LTC1298's max clock rate of 200 kHz. To slow
; the conversion routine, add more "jmp $+1" 2-cycle delays in :loop1 and
; :loop2.

convert
                mov     !rb,#xmit           ; Ready to transmit configuration to ADC.
                clrb    CLK                 ; Begin with clock low.
                clrb    CS
                OR      cnfig,#fixBs        ; Write 1s to start and msbf bits
                mov     clocks,#outClk      ; Set up number of config bits to write.
                clr     ADresL              ; Clear results registers.
                clr     ADresH
:loop1          rr      cnfig               ; Rotate bit 0 into carry.
                movb    DATA,c              ; Move carry bit to DATA pin.
                setb    CLK                 ; Pulse the clock line.
                jmp     $+1
                clrb    CLK
                djnz    clocks,:loop1       ; Repeat for all config bits.
                rr      cnfig               ; Rearrange config register to original state.
                swap    cnfig
                mov     !rb,#recv           ; Change TRIS to input data.
                mov     clocks,#inClk       ; Set up number of data bits to receive.
:loop2          rl      ADresL              ; Rotate 16-bit ADres register left.
                rl      ADresH
                snb     DATA                ; Copy data bit to lsb of ADres.
                setb    ADresL.0
                sb      DATA
                clrb    ADresL.0
                setb    CLK                 ; Pulse the clock line.
                jmp     $+1
                clrb    CLK
                djnz    clocks,:loop2       ; Repeat for all data bits.
                setb    CS                  ; Deactivate the LTC1298.
                ret
```

## BASIC Stamp I (BS1-IC) and BASIC Stamp Ver. D Program Listing

```
' Program: LTC1298.BS1 (LTC1298 analog-to-digital converter)

' The LTC1298 is a 12-bit, two-channel ADC. Its high resolution, low
' supply current, low cost, and built-in sample/hold feature make it a
' great companion for the Stamp in sensor and data-logging applications.
' With its 12-bit resolution, the LTC1298 can measure tiny changes in
' input voltage; 1.22 millivolts (5-volt reference/4096).

' =========================================================
'               ADC Interface Pins
' =========================================================

' The 1298 uses a four-pin interface, consisting of chip-select, clock,
' data input, and data output. In this application, we tie the data lines
' together with a 1k resistor and connect the Stamp pin designated DIO
' to the data-in side of the resistor. The resistor limits the current
' flowing between DIO and the 1298's data out in case a programming error
' or other fault causes a "bus conflict." This happens when both pins are
' in output mode and in opposite states (1 vs 0). Without the resistor,
' such a conflict would cause large currents to flow between pins,
' possibly damaging the Stamp and/or ADC.

SYMBOL      CS = 0              ' Chip select; 0 = active.
SYMBOL      CLK = 1             ' Clock to ADC; out on rising, in on falling edge.
SYMBOL      DIO_n = 2           ' Pin _number_ of data input/output.
SYMBOL      DIO_p = pin2      ' Variable_name_ of data input/output.
SYMBOL      ADbits = b1         ' Counter variable for serial bit reception.
SYMBOL      AD = w1             ' 12-bit ADC conversion result.

' =========================================================
'               ADC Setup Bits
' =========================================================

' The 1298 has two modes. As a single-ended ADC, it measures the
' voltage at one of its inputs with respect to ground. As a differential
' ADC, it measures the difference in voltage between the two inputs.
' The sglDif bit determines the mode; 1 = single-ended, 0 = differential.
' When the 1298 is single-ended, the oddSign bit selects the active input
' channel; 0 = channel 0 (pin 2), 1 = channel 1 (pin 3).
' When the 1298 is differential, the oddSign bit selects the polarity
' between the two inputs; 0 = channel 0 is +, 1 = channel 1 is +.
' The msbf bit determines whether clock cycles _after_ the 12 data bits
' have been sent will send 0s (msbf = 1) or a least-significant-bit-first
' copy of the data (msbf = 0). This program doesn't continue clocking after
' the data has been obtained, so this bit doesn't matter.

' You probably won't need to change the basic mode (single/differential)
' or the format of the post-data bits while the program is running, so
' these are assigned as constants. You probably will want to be able to
' change channels, so oddSign (the channel selector) is a bit variable.
```

## BASIC Stamp I and Ver. D Program Listing (cont.)

```
SYMBOL      sglDif = 1              ' Single-ended, two-channel mode.
SYMBOL      msbf = 1                ' Output 0s after data transfer is complete.
SYMBOL      oddSign = bit0      ' Program writes channel # to this bit.
' ========================================================
'               Demo Program
' ========================================================

' This program demonstrates the LTC1298 by alternately sampling the two
' input channels and presenting the results on the PC screen using Debug.

high CS                             ' Deactivate the ADC to begin.
Again:                              ' Main loop.
  For oddSign = 0 to 1          ' Toggle between input channels.
    gosub Convert                   ' Get data from ADC.
    debug "ch ",#oddSign,":",#AD,cr     ' Show the data on PC screen.
    pause 500                   ' Wait a half second.
  next                              ' Change input channels.
goto Again                      ' Endless loop.

' ========================================================
'               ADC Subroutine
' ========================================================

' Here's where the conversion occurs. The Stamp first sends the setup
' bits to the 1298, then clocks in one null bit (a dummy bit that always
' reads 0) followed by the conversion data.

Convert:
  low CLK                       ' Low clock--output on rising edge.
  high DIO_n                    ' Switch DIO to output high (start bit).
  low CS                            ' Activate the 1298.
  pulsout CLK,5                     ' Send start bit.
  let DIO_p = sglDif                ' First setup bit.
  pulsout CLK,5                     ' Send bit.
  let DIO_p = oddSign           ' Second setup bit.
  pulsout CLK,5                     ' Send bit.
  let DIO_p = msbf                  ' Final setup bit.
  pulsout CLK,5                     ' Send bit.
  input DIO_n                   ' Get ready for input from DIO.
  let AD = 0                    ' Clear old ADC result.
  for ADbits = 1 to 13          ' Get null bit + 12 data bits.
    let AD = AD*2+DIO_p         ' Shift AD left, add new data bit.
    pulsout CLK,5                   ' Clock next data bit in.
  next                              ' Get next data bit.
  high CS                       ' Turn off the ADC
return                              ' Return to program.
```

## BASIC Stamp II (BS2-IC) Program Listing

```
' Program: LTC1298.BS2 (LTC1298 analog-to-digital converter)

' The LTC1298 is a 12-bit, two-channel ADC. Its high resolution, low
' supply current, low cost, and built-in sample/hold feature make it a
' great companion for the Stamp in sensor and data-logging applications.
' With its 12-bit resolution, the LTC1298 can measure tiny changes in
' input voltage; 1.22 millivolts (5-volt reference/4096).

' =====================================================
'               ADC Interface Pins
' =====================================================

' The 1298 uses a four-pin interface, consisting of chip-select, clock,
' data input, and data output. In this application, we tie the data lines
' together with a 1k resistor and connect the Stamp pin designated DIO
' to the data-in side of the resistor. The resistor limits the current
' flowing between DIO and the 1298's data out in case a programming error
' or other fault causes a "bus conflict." This happens when both pins are
' in output mode and in opposite states (1 vs 0). Without the resistor,
' such a conflict would cause large currents to flow between pins,
' possibly damaging the Stamp and/or ADC.

CS     con     0           ' Chip select; 0 = active
CLK    con     1           ' Clock to ADC; out on rising, in on falling edge.
DIO_n  con     2                   ' Data I/O pin _number_.
config var     nib         ' Configuration bits for ADC.
AD     var     word        ' Variable to hold 12-bit AD result.

' =====================================================
'               ADC Setup Bits
' =====================================================

' The 1298 has two modes. As a single-ended ADC, it measures the
' voltage at one of its inputs with respect to ground. As a differential
' ADC, it measures the difference in voltage between the two inputs.
' The sglDif bit determines the mode; 1 = single-ended, 0 = differential.
' When the 1298 is single-ended, the oddSign bit selects the active input
' channel; 0 = channel 0 (pin 2), 1 = channel 1 (pin 3).
' When the 1298 is differential, the oddSign bit selects the polarity
' between the two inputs; 0 = channel 0 is +, 1 = channel 1 is +.
' The msbf bit determines whether clock cycles _after_ the 12 data bits
' have been sent will send 0s (msbf = 1) or a least-significant-bit-first
' copy of the data (msbf = 0). This program doesn't continue clocking after
' the data has been obtained, so this bit doesn't matter.

' You probably won't need to change the basic mode (single/differential)
' or the format of the post-data bits while the program is running, so
' these are assigned as constants. You probably will want to be able to
' change channels, so oddSign (the channel selector) is a bit variable.
```

## BASIC Stamp II Program Listing (cont.)

```
startB var      config.bit0     ' Start bit for comm with ADC.
sglDif var      config.bit1     ' Single-ended or differential mode.
oddSign         var             config.bit2         ' Channel selection.
msbf  var       config.bit3     ' Output 0s after data xfer complete.

' ===================================================
'               Demo Program
' ===================================================

' This program demonstrates the LTC1298 by alternately sampling the two
' input channels and presenting the results on the PC screen using Debug.

high CS                                         ' Deactivate ADC to begin.
high DIO_n                  ' Set data pin for first start bit.
again:                                          ' Main loop.
  for oddSign = 0 to 1      ' Toggle between input channels.
    gosub convert           ' Get data from ADC.
    debug "channel ",DEC oddSign, ": ",DEC AD,cr ' Display data.
    pause 500               ' Wait a half second.
  next                      ' Change channels.
goto again                  ' Endless loop.

' ===================================================
'               ADC Subroutine
' ===================================================

' Here's where the conversion occurs. The Stamp first sends the config
' bits to the 1298, then clocks in the conversion data. Note the use of
' the new BS2 instructions Shiftout and Shiftin. Their use is pretty
' straightforward here: Shiftout sends data bits to pin DIO and clock
' the CLK pin. Sending the least-significant bit first, it shifts out
' the four bits of the variable config. Then Shiftin changes DIO to
' input and clocks in the data bits--most-significant bit first, post
' clock (valid after clock pulse). It shifts in 12 bits to the
' variable AD.

convert:
  config = config | %1011   ' Set all bits except oddSign.
  low CS                                        ' Activate the ADC.
  shiftout DIO_n,CLK,lsbfirst,[config\4]        ' Send config bits.
  shiftin DIO_n,CLK,msbpost,[AD\12]                 ' Get data bits.
  high CS                   ' Deactivate the ADC.
return                                          ' Return to program.
```

LTC1286/LTC1298

# Micropower Sampling 12-Bit A/D Converters in SO-8 Packages

## FEATURES

- **12-Bit Resolution**
- **8-Pin SOIC Plastic Package**
- **Low Cost**
- **Low Supply Current: 250μA Typ.**
- Auto Shutdown to 1nA Typ.
- Guaranteed ±3/4LSB Max DNL
- Single Supply 5V to 9V Operation
- On-Chip Sample-and-Hold
- 60μs Conversion Time
- Sampling Rates:
  - 12.5 ksps (LTC1286)
  - 11.1 ksps (LTC1298)
- I/O Compatible with SPI, Microwire, etc.
- Differential Inputs (LTC1286)
- 2-Channel MUX (LTC1298)
- 3V Versions Available: LTC1285/LTC1288

## APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Handheld Terminal Interface
- Temperature Measurement
- Isolated Data Acquisition

## DESCRIPTION

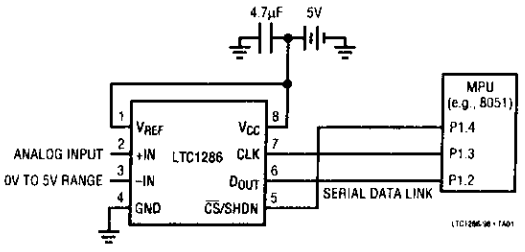
The LTC1286/LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. They typically draw only 250μA of supply current when converting and automatically power down to a typical supply current of 1nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 5V to 9V supplies. These 12-bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1286 has a single differential analog input. The LTC1298 offers a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

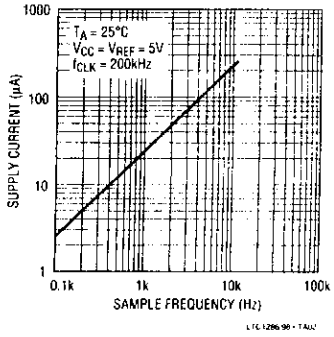
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

## TYPICAL APPLICATIONS

**25μW, SO-8 Package, 12-Bit ADC Samples at 200Hz and Runs Off a 5V Supply**




**Supply Current vs Sample Rate**

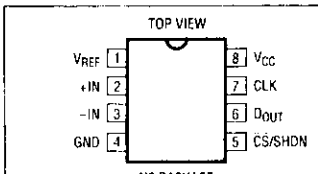


## ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage ($V_{CC}$) to GND ..... 12V
Voltage
  Analog and Reference ..... −0.3V to $V_{CC}$ + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Output ..... −0.3V to $V_{CC}$ + 0.3V

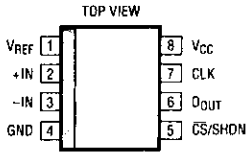
Power Dissipation ..... 500mW
Operating Temperature Range
  LTC1286C/LTC1298C ..... 0°C to 70°C
  LTC1286I/LTC1298I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

## PACKAGE/ORDER INFORMATION



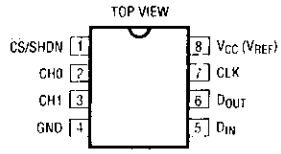

N8 PACKAGE
8-LEAD PLASTIC DIP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W

| ORDER PART NUMBER |
|---|
| LTC1286CN8 |
| LTC1286IN8 |



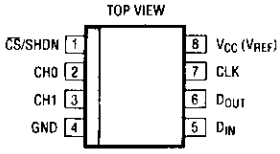

S8 PACKAGE
8-LEAD PLASTIC SOIC
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 175°C/W

| ORDER PART NUMBER |
|---|
| LTC1286CS8 |
| LTC1286IS8 |
| PART MARKING |
| 1286C |
| 1286I |




N8 PACKAGE
8-LEAD PLASTIC DIP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W

| ORDER PART NUMBER |
|---|
| LTC1298CN8 |
| LTC1298IN8 |




S8 PACKAGE
8-LEAD PLASTIC SOIC
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 175°C/W

| ORDER PART NUMBER |
|---|
| LTC1298CS8 |
| LTC1298IS8 |
| PART MARKING |
| 1298C |
| 1298I |

Consult factory for military grade parts.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage (Note 3) | LTC1286<br>LTC1298 | 4.5<br>4.5 | | 9.0<br>5.5 | V<br>V |
| $f_{CLK}$ | Clock Frequency | $V_{CC}$ = 5V | (Note 4) | | 200 | kHz |
| $t_{CYC}$ | Total Cycle Time | LTC1286, $f_{CLK}$ = 200kHz<br>LTC1298, $f_{CLK}$ = 200kHz | 80<br>90 | | | µs<br>µs |
| $t_{hDI}$ | Hold Time, $D_{IN}$ After CLK↑ | $V_{CC}$ = 5V | 150 | | | ns |
| $t_{suCS}$ | Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence) | LTC1286, $V_{CC}$ = 5V<br>LTC1298, $V_{CC}$ = 5V | 2<br>2 | | | µs<br>µs |
| $t_{suDI}$ | Setup Time, $D_{IN}$ Stable Before CLK↑ | $V_{CC}$ = 5V | 400 | | | ns |
| $t_{WHCLK}$ | CLK High Time | $V_{CC}$ = 5V | 2 | | | µs |
| $t_{WLCLK}$ | CLK Low Time | $V_{CC}$ = 5V | 2 | | | µs |
| $t_{WH\overline{CS}}$ | $\overline{CS}$ High Time Between Data Transfer Cycles | $V_{CC}$ = 5V | 2 | | | µs |
| $t_{WL\overline{CS}}$ | $\overline{CS}$ Low Time During Data Transfer | LTC1286, $f_{CLK}$ = 200kHz<br>LTC1298, $f_{CLK}$ = 200kHz | 75<br>85 | | | µs<br>µs |

## CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

| PARAMETER | CONDITIONS | | LTC1286 MIN | LTC1286 TYP | LTC1286 MAX | LTC1298 MIN | LTC1298 TYP | LTC1298 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution (No Missing Codes) | | ● | 12 | | | 12 | | | Bits |
| Integral Linearity Error | (Note 6) | ● | | ±3/4 | ±2 | | ±3/4 | ±2 | LSB |
| Differential Linearity Error | | ● | | ±1/4 | ±3/4 | | ±1/4 | ±3/4 | LSB |
| Offset Error | | ● | | 3/4 | ±3 | | 3/4 | ±3 | LSB |
| Gain Error | | ● | | ±2 | ±8 | | ±2 | ±8 | LSB |
| Analog Input Range | (Note 7 and 8) | ● | | −0.05V to $V_{CC}$ + 0.05V | | | | | V |
| REF Input Range (LTC1286) (Notes 7, 8, and 9) | 4.5 ≤ $V_{CC}$ ≤ 5.5V<br>5.5V < $V_{CC}$ ≤ 9V | | | 1.5V to $V_{CC}$ + 0.05V<br>1.5V to 5.55V | | | | | V<br>V |
| Analog Input Leakage Current (Note 10) | | ● | | ±1 | | | | ±1 | µA |

## DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = 5.25V | ● | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = 4.75V | ● | | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = $V_{CC}$ | ● | | | 2.5 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0V | ● | | | −2.5 | µA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 10µA<br>$V_{CC}$ = 4.75V, $I_O$ = 360µA | ●<br>● | 4.0<br>2.4 | 4.64<br>4.62 | | V<br>V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 1.6mA | ● | | | 0.4 | V |
| $I_{OZ}$ | Hi-Z Output Leakage | $\overline{CS}$ = High | ● | | | ±3 | µA |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | −25 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = $V_{CC}$ | | | 45 | | mA |
| $R_{REF}$ | Reference Input Resistance (LTC1286) | $\overline{CS}$ = $V_{CC}$<br>$\overline{CS}$ = GND | | | 5000<br>55 | | MΩ<br>kΩ |
| $I_{REF}$ | Reference Current (LTC1286) | $\overline{CS}$ = $V_{CC}$<br>$t_{CYC}$ ≥ 640µs, $f_{CLK}$ ≤ 25kHz<br>$t_{CYC}$ = 80µs, $f_{CLK}$ = 200kHz | ●<br>●<br>● | | 0.001<br>90<br>90 | 2.5<br>140<br>140 | µA<br>µA<br>µA |
| $I_{CC}$ | Supply Current | $\overline{CS}$ = $V_{CC}$ | ● | | 0.001 | ±3.0 | µA |
| | | LTC1286, $t_{CYC}$ ≥ 640µs, $f_{CLK}$ ≤ 25kHz<br>LTC1286, $t_{CYC}$ = 80µs, $f_{CLK}$ = 200kHz | ●<br>● | | 200<br>250 | 400<br>500 | µA<br>µA |
| | | LTC1298, $t_{CYC}$ ≥ 720µs, $f_{CLK}$ ≤ 25kHz<br>LTC1298, $t_{CYC}$ = 90µs, $f_{CLK}$ = 200kHz | ●<br>● | | 290<br>340 | 490<br>640 | µA<br>µA |

## DYNAMIC ACCURACY $f_{SMPL}$ = 12.5kHz (LTC1286), $f_{SMPL}$ = 11.1kHz (LTC1298) (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| S/(N +D) | Signal-to-Noise Plus Distortion Ratio | 1kHz/7kHz Input Signal | | 71/68 | | dB |
| THD | Total Harmonic Distortion (Up to 5th Harmonic) | 1kHz/7kHz Input Signal | | −84/−80 | | dB |
| SFDR | Spurious-Free Dynamic Range | 1kHz/7kHz Input Signal | | 90/86 | | dB |
| | Peak Harmonic or Spurious Noise | 1kHz/7kHz Input Signal | | −90/−86 | | dB |

## AC CHARACTERISTICS (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{SMPL}$ | Analog Input Sample Time | See Operating Sequence | | | 1.5 | | CLK Cycles |
| $f_{SMPL(MAX)}$ | Maximum Sampling Frequency | LTC1286<br>LTC1298 | ●<br>● | 12.5<br>11.1 | | | kHz<br>kHz |
| $t_{CONV}$ | Conversion Time | See Operating Sequence | | | 12 | | CLK Cycles |
| $t_{dDO}$ | Delay Time, CLK↓ to $D_{OUT}$ Data Valid | See Test Circuits | ● | | 250 | 600 | ns |
| $t_{dis}$ | Delay Time, $\overline{CS}$↑ to $D_{OUT}$ Hi-Z | See Test Circuits | ● | | 135 | 300 | ns |
| $t_{en}$ | Delay Time, CLK↓ to $D_{OUT}$ Enable | See Test Circuits | ● | | 75 | 200 | ns |
| $t_{hDO}$ | Time Output Data Remains Valid After CLK↓ | $C_{LOAD}$ = 100pF | | | 230 | | ns |
| $t_f$ | $D_{OUT}$ Fall Time | See Test Circuits | ● | | 20 | 75 | ns |
| | $D_{OUT}$ Rise Time | See Test Circuits | ● | | 20 | 75 | ns |
| $I_{IN}$ | Input Capacitance | Analog Inputs, On Channel<br>Analog Inputs, Off Channel<br>Digital Input | | | 20<br>5<br>5 | | pF<br>pF<br>pF |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute maximum ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** These devices are specified at 5V. For 3V specified devices, see LTC1285 and LTC1288.

**Note 4:** Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 120kHz$ at 85°C, $f_{CLK} \geq 75kHz$ at 70° and $f_{CLK} \geq 1kHz$ at 25°C.

**Note 5:** $V_{CC}$ = 5V, $V_{REF}$ = 5V and CLK = 200kHz unless otherwise specified.

**Note 6:** Linearity error is specified between the actual end points of the A/D transfer curve.

**Note 7:** Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above $V_{CC}$. This spec allows 50mV forward bias of either diode for $4.5V \leq V_{CC} \leq 5.5V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading. For $5.5V < V_{CC} \leq 9V$, reference and analog input range cannot exceed 5.55V. If reference and analog input range are greater than 5.55V, the output code will not be guaranteed to be correct.

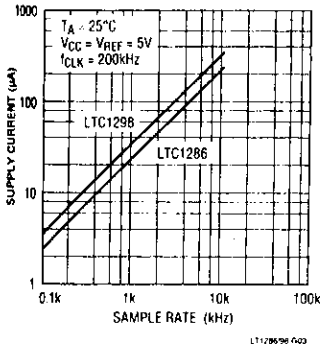
**Note 8:** The supply voltage range for the LTC1286 is from 4.5V to 9V, but the supply voltage range for the LTC1298 is only from 4.5V to 5.5V.

**Note 9:** Recommended operating conditions

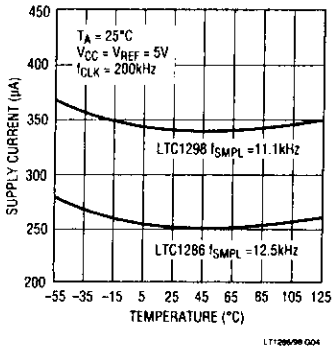
**Note 10:** Channel leakage current is measured after the channel selection.

## TYPICAL PERFORMANCE CHARACTERISTICS

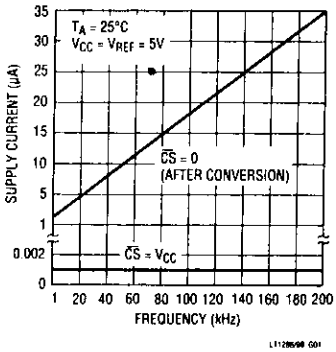
**Supply Current vs Sample Rate**




**Supply Current vs Temperature**

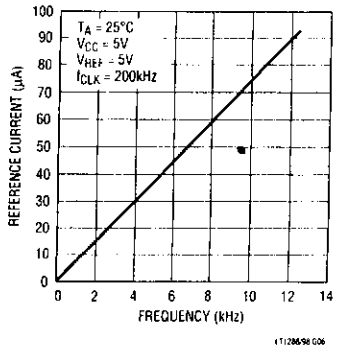



**Shutdown Supply Current vs Clock Rate with $\overline{CS}$ High and $\overline{CS}$ Low**

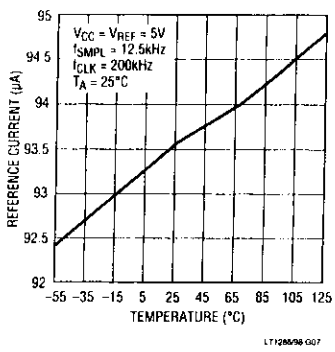


## TYPICAL PERFORMANCE CHARACTERISTICS

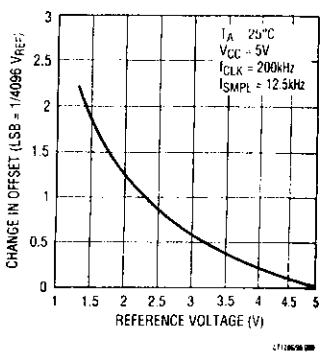
**Reference Current vs Sample Rate (LTC1286)**



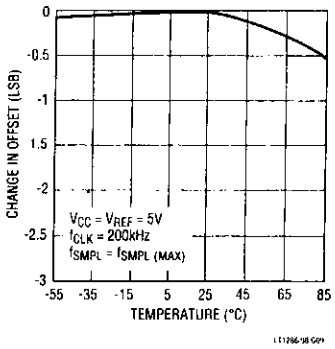

**Reference Current vs Temperature**



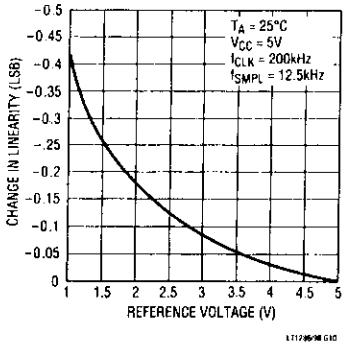

**Change in Offset vs Reference Voltage**



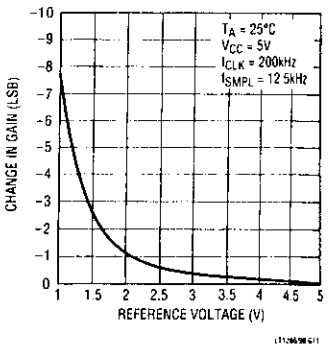

**Change in Offset vs Temperature**



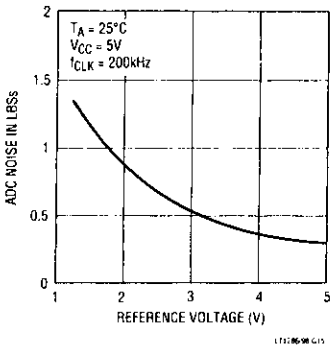

**Change In Linearity vs Reference Voltage**



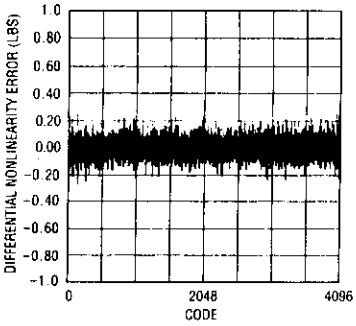

**Change In Gain vs Reference Voltage**



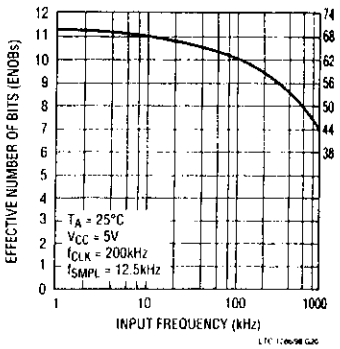

**Peak-to-Peak ADC Noise vs Reference Voltage**




**Differential Nonlinearity vs Code**

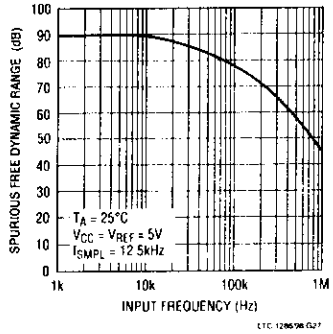



**Effective Bits and S/(N + D) vs Input Frequency**

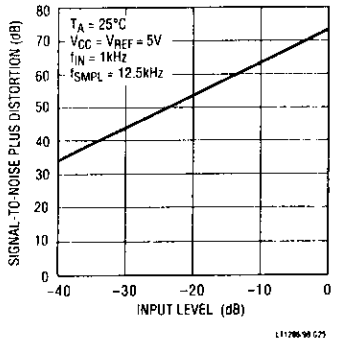


## TYPICAL PERFORMANCE CHARACTERISTICS

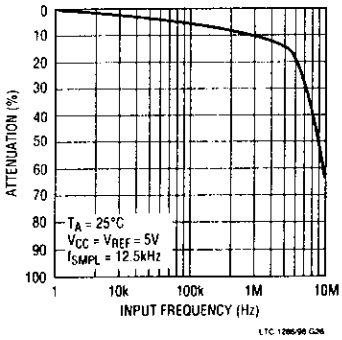
**Spurious Free Dynamic Range vs Frequency**



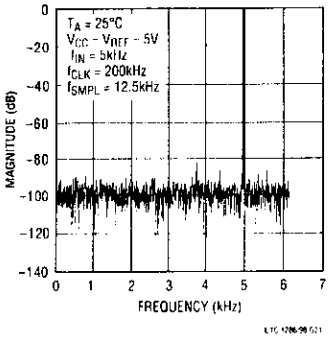

**S/(N+D) vs Input Level**



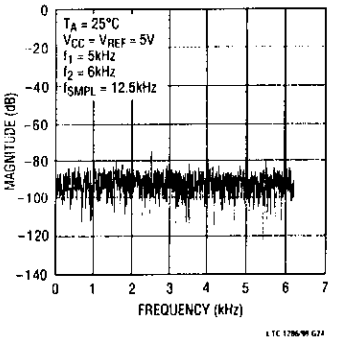

**Attenuation vs Input Frequency**



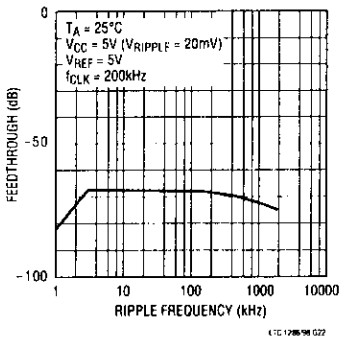

**4096 Point FFT Plot**



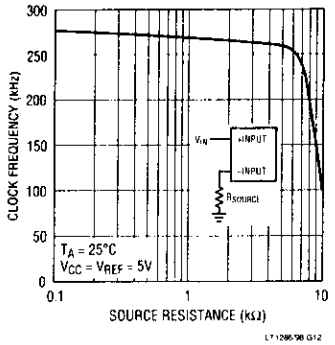

**Intermodulation Distortion**



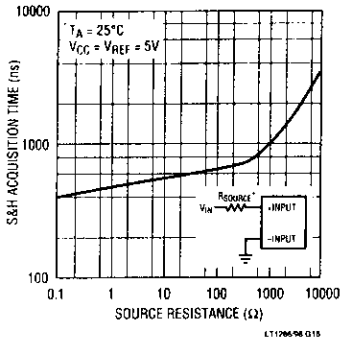

**Power Supply Feedthrough vs Ripple Frequency**



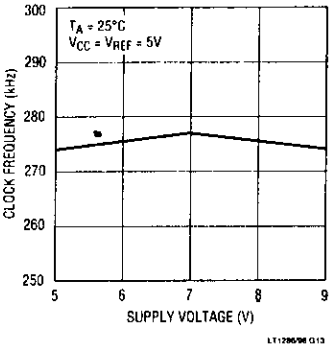

**Maximum Clock Frequency vs Source Resistance**




**Sample and Hold Aquisition Time vs Source Resistance**

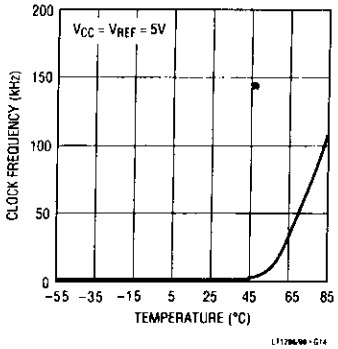



**Maximum Clock Frequency vs Supply Voltage**

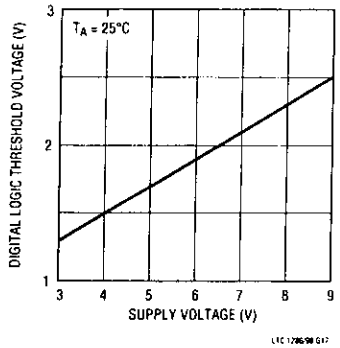


## TYPICAL PERFORMANCE CHARACTERISTICS

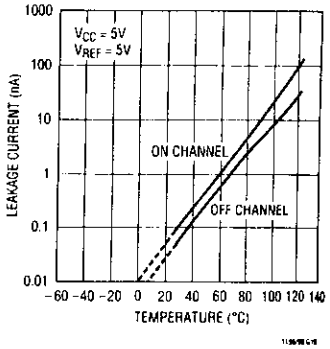
**Minimum Clock Frequency for 0.1 LSB Error vs Temperature**




**Digital Input Logic Threshold vs Supply Voltage**




**Input Channel Leakage Current vs Temperature**




## PIN FUNCTIONS

### LTC1286

**$V_{REF}$ (Pin 1):** Reference Input. The reference input defines the span of the A/D converter.

**$IN^+$ (Pin 2):** Positive Analog Input.

**$IN^-$ (Pin 3):** Negative Analog Input.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

**$\overline{CS}$/SHDN (Pin 5):** Chip Select Input. A logic low on this input enables the LTC1286. A logic high on this input disables and powers down the LTC1286.

**$D_{OUT}$ (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this output.

**CLK (Pin 7):** Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

**$V_{CC}$ (Pin 8):** Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane. .

### LTC1298

**$\overline{CS}$/SHDN (Pin 1):** Chip Select Input. A logic low on this input enables the LTC1298. A logic high on this input disables and powers down the LTC1298.

**CH0 (Pin 2):** Analog Input.

**CH1 (Pin 3):** Analog Input.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

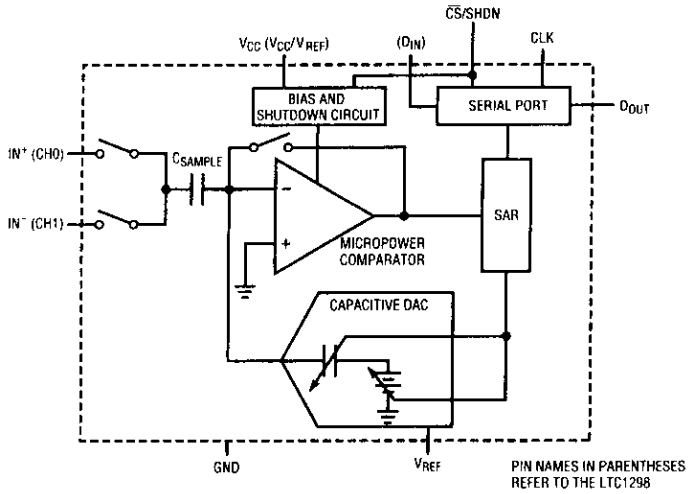
**$D_{IN}$ (Pin 5):** Digital Data Input. The multiplexer address is shifted into this input.

**$D_{OUT}$ (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this output.

**CLK (Pin 7):** Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

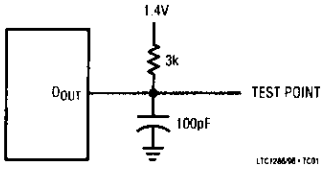
**$V_{CC}/V_{REF}$ (Pin 8):** Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

## BLOCK DIAGRAM

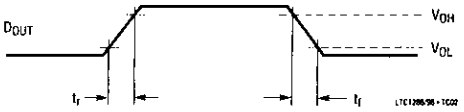



## TEST CIRCUITS

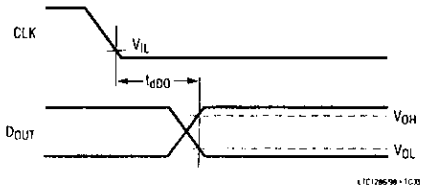
**Load Circuit for $t_{dDO}$, $t_r$ and $t_f$**



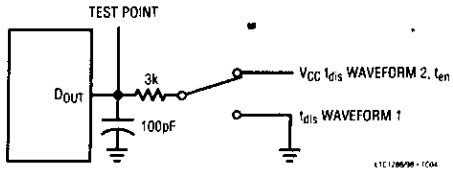

**Voltage Waveforms for $D_{OUT}$ Rise and Fall Times, $t_r$, $t_f$**




**Voltage Waveforms for $D_{OUT}$ Delay Times, $t_{dDO}$**

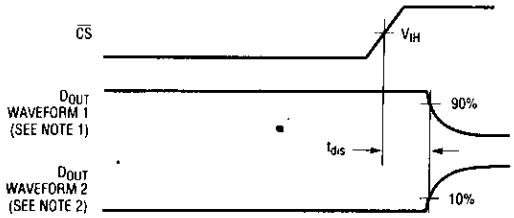



**Load Circuit for $t_{dis}$ and $t_{en}$**



## TEST CIRCUITS

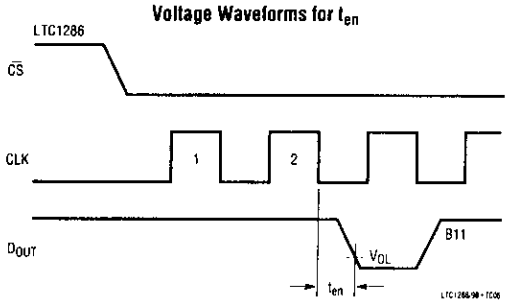
**Voltage Waveforms for $t_{dis}$**



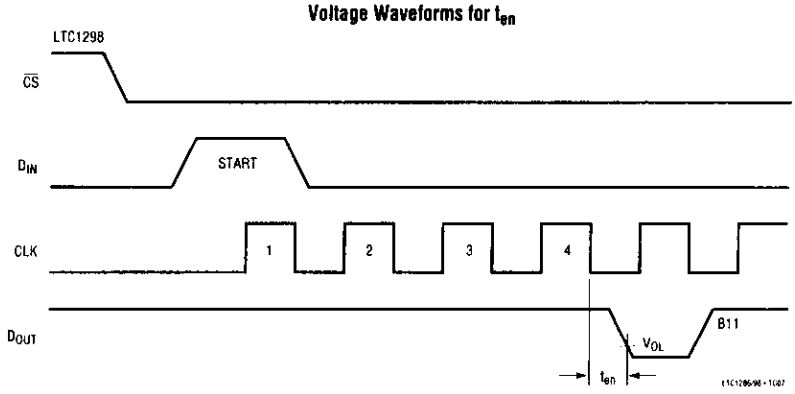

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

**Voltage Waveforms for $t_{en}$**




**Voltage Waveforms for $t_{en}$**




## APPLICATION INFORMATION

### OVERVIEW

The LTC1286 and LTC1298 are micropower, 12-bit, successive approximation sampling A/D converters. The LTC1286 typically draws 250µA of supply current when sampling at 12.5kHz while the LTC1298 nominally consumes 350µA of supply current when sampling at 11.1 kHz. The extra 100µA of supply current on the LTC1298 comes from the reference input which is intentionally tied to the supply. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. They are packaged in 8-pin SO and DIP packages. The LTC1286 operates on a single supply from 4.5V to 9V, while the LTC1298 operates from a 4.5V to 5.5V supply.

Both the LTC1286 and the LTC1298 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1286 and LTC1298 differ in some respects. The LTC1286 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans to 1V. Reducing the spans allows it to achieve 244µV resolution. The LTC1298 has a two-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. The reference input is tied to the supply pin.

## APPLICATION INFORMATION

### SERIAL INTERFACE

The 2-channel LTC1298 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The single channel LTC1286 uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

#### Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1286 does not require a configuration input word and has no $D_{IN}$ pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1286 operating sequence. After $\overline{CS}$ falls the second CLK pulse enables $D_{OUT}$. After one null bit the A/D conversion result is output on the $D_{OUT}$ line. Bringing $\overline{CS}$ high resets the LTC1286 for the next data exchange.

The LTC1298 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, $D_{IN}$ and $D_{OUT}$ may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA ($D_{IN}/D_{OUT}$).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1298 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the $D_{IN}$ input which configures the LTC1298 and starts the conversion. After one null bit, the result of the conversion is output on the $D_{OUT}$ line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1298 in preparation for the next data exchange.

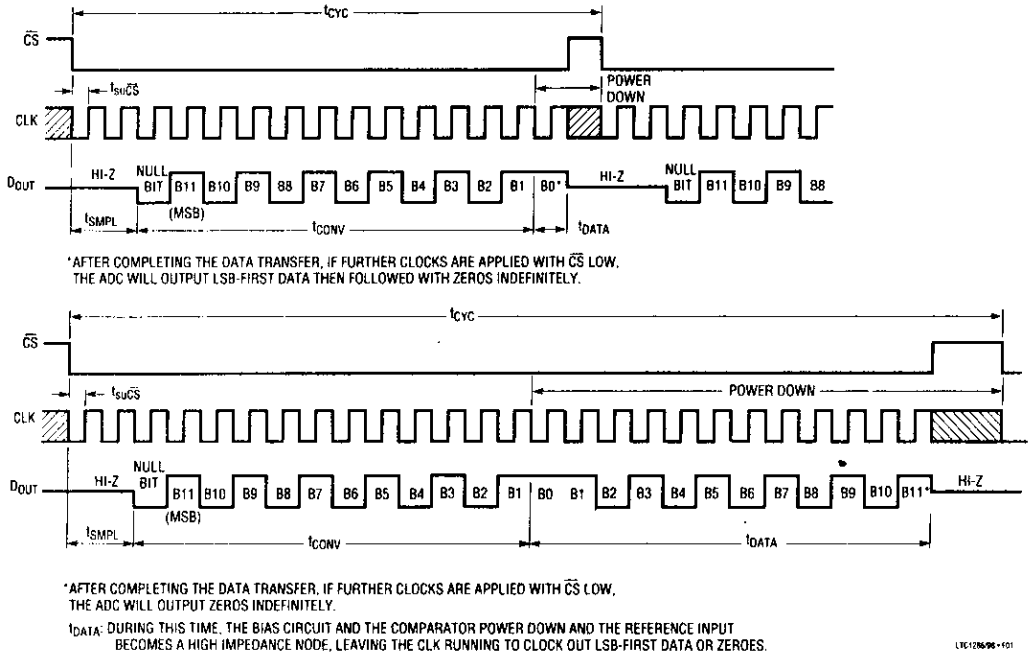
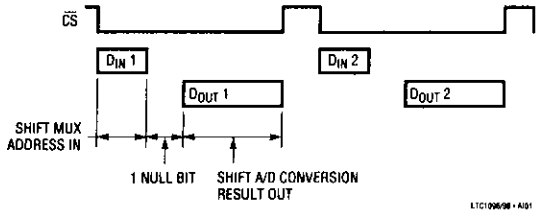
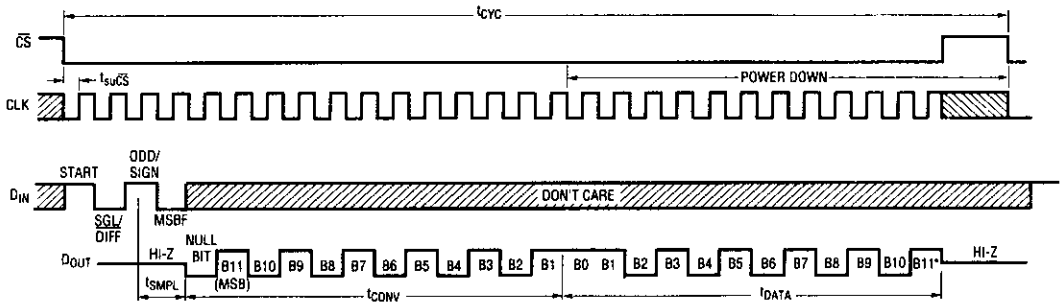



**Figure 1. LTC1286 Operating Sequence**

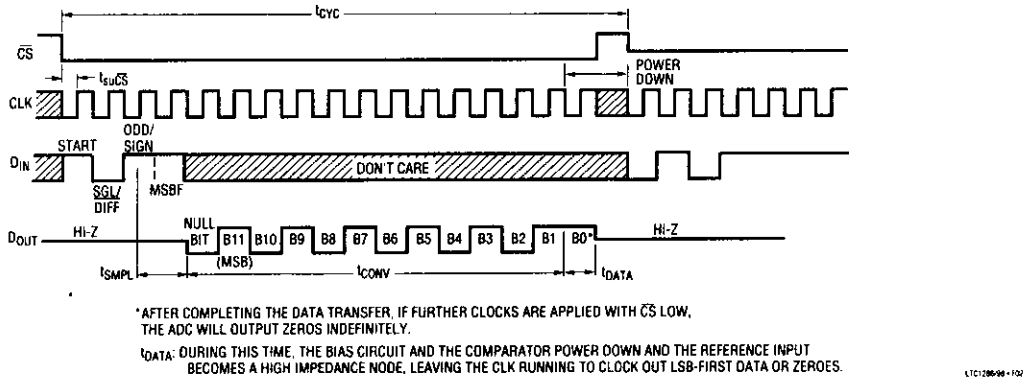
## APPLICATION INFORMATION




**MSB-First Data (MSBF = 0)**




**MSB-First Data (MSBF = 1)**




*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

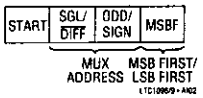
$t_{DATA}$: DURING THIS TIME, THE BIAS CIRCUIT AND THE COMPARATOR POWER DOWN AND THE REFERENCE INPUT BECOMES A HIGH IMPEDANCE NODE, LEAVING THE CLK RUNNING TO CLOCK OUT LSB-FIRST DATA OR ZEROES.

**Figure 2. LTC1298 Operating Sequence Example: Differential Inputs (CH+, CH–)**

## APPLICATION INFORMATION

### Input Data Word

The LTC1286 requires no $D_{IN}$ word. It is permanently configured to have a single differential input. The conversion result appears on the $D_{OUT}$ line. The data format is MSB first followed by the LSB sequence. This provides easy interface to MSB or LSB first serial ports. For MSB first data the $\overline{CS}$ signal can be taken high after B0 (see Figure 1). The LTC1298 clocks data into the $D_{IN}$ input on the rising edge of the clock. The input data words are defined as follows:




### Start Bit

The first "logical one" clocked into the $D_{IN}$ input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1298 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the $D_{IN}$ pin are then ignored until the next $\overline{CS}$ cycle.

### Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND.

**LTC1298 Channel Selection**

| | MUX ADDRESS SGL/DIFF | MUX ADDRESS ODD/SIGN | CHANNEL # 0 | CHANNEL # 1 | GND |
|---|---|---|---|---|---|
| SINGLE-ENDED MUX MODE | 1 | 0 | + | | – |
| | 1 | 1 | | + | – |
| DIFFERENTIAL MUX MODE | 0 | 0 | + | – | |
| | 0 | 1 | – | + | |

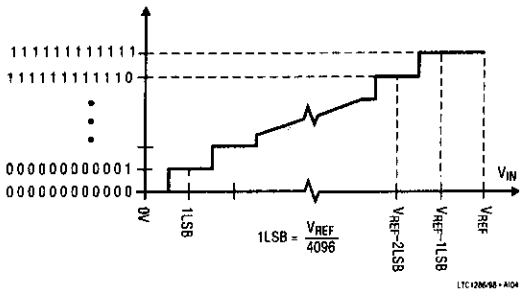
### MSB First/LSB First (MSBF)

The output data of the LTC1298 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the $D_{OUT}$ line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the $D_{OUT}$ line. (see Operating Sequence)

### Transfer Curve

The LTC1286/LTC1298 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

**Transfer Curve**




**Output Code**

| OUTPUT CODE | INPUT VOLTAGE | INPUT VOLTAGE ($V_{REF}$ = 5.000V) |
|---|---|---|
| 111111111111111 | $V_{REF}$ – 1LSB | 4.99878V |
| 111111111111110 | $V_{REF}$ – 2LSB | 4.99756V |
| • | • | • |
| • | • | • |
| • | • | • |
| 000000000000001 | 1LSB | 0.00122V |
| 000000000000000 | 0V | 0V |

### Operation with $D_{IN}$ and $D_{OUT}$ Tied Together

The LTC1298 can be operated with $D_{IN}$ and $D_{OUT}$ tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1298 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1298 with $D_{IN}$ and $D_{OUT}$ tied together to the Intel 8051 MPU.

## APPLICATION INFORMATION

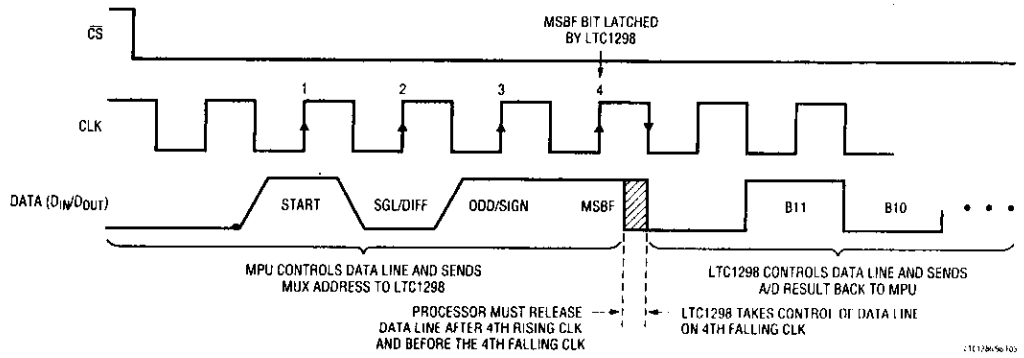



**Figure 3. LTC1298 Operation with $D_{IN}$ and $D_{OUT}$ Tied Together**

### ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 250μA and automatic shutdown between conversions, the LTC1286/LTC1298 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). The auto-shutdown allows the supply curve to drop with reduced sample rate. Several things must be taken into account to achieve such a low power consumption.

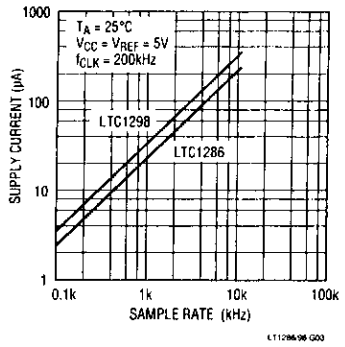



**Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate.**

### Shutdown

The LTC1286/LTC1298 are equipped with automatic shutdown features. They draw power when the $\overline{CS}$ pin is low and shut down completely when that pin is high. The bias circuit and comparator powers down and the reference input becomes high impedance at the end of each conversion leaving the CLK running to clock out the LSB first data or zeroes (see Figures 1 and 2). If the $\overline{CS}$ is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the $\overline{CS}$ pin to ground when it is low and to supply voltage when it is high.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the $D_{IN}$ and CLK input have no effect on supply current during this time. There is no need to stop $D_{IN}$ and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

### Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. After a conversion the ADC automatically shuts down even if $\overline{CS}$ is held low (see Figures 1 and 2). If the clock is left running to clock out LSB-data or zero, the logic will draw a small current. Figure 5 shows that the typical supply current with $\overline{CS}$ = ground varies from 1μA at 1kHz to 35μA at 200kHz. When $\overline{CS}$ = $V_{CC}$, the logic is gated off and no supply current is drawn regardless of the clock frequency.

## APPLICATION INFORMATION

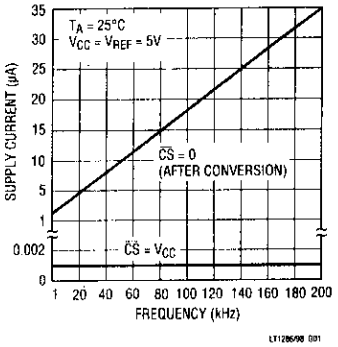



**Figure 5. Shutdown current with $\overline{CS}$ high is 1nA typically, regardless of the clock. Shutdown current with $\overline{CS}$ = ground varies from 1μA at 1kHz to 35μA at 200kHz.**

### $D_{OUT}$ Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the $D_{OUT}$ pin can add more than 50μA to the supply current at a 200kHz clock frequency. An extra 50μA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The C × V × f currents must be evaluated and the troublesome ones minimized.

### OPERATING ON OTHER THAN 5V SUPPLIES (LTC1286)

The LTC1286 operates from 4.5V to 9V supplies and the LTC1298 operates from a 5V supply. To operate the LTC1286 on other than 5V supplies a few things must be kept in mind.

#### Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and $D_{IN}$ are made to meet TTL on a 5V supply. When the supply voltage varies, the input logic levels also change. For the LTC1286 to sample and convert correctly, the digital inputs have to be in the proper logical low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

#### Clock Frequency

The maximum recommended clock frequency is 200kHz for the LTC1286/LTC1298 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

#### Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1286 operating on a 9V supply. The requirement to achieve this is that the outputs of $\overline{CS}$ and CLK from the MPU have to be able to trip the equivalent inputs of the LTC1286 and the output of $D_{OUT}$ from the LTC1286 must be able to toggle the equivalent input of the MPU (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1286 operating on a 9V supply, the output of $D_{OUT}$ may go between 0V and 9V. The 9V output may damage the MPU running off a 5V supply. The way to get around this possibility is to have a resistor divider on $D_{OUT}$ (Figure 6) and connect the center point to the MPU input. It should be noted that to get full shutdown, the $\overline{CS}$ input of the LTC1286 must be driven to the $V_{CC}$ voltage to keep the $\overline{CS}$ input buffer from drawing current. An alternative is to leave $\overline{CS}$ low after a conversion, clock data until $D_{OUT}$ outputs zeros, and then stop the clock low.

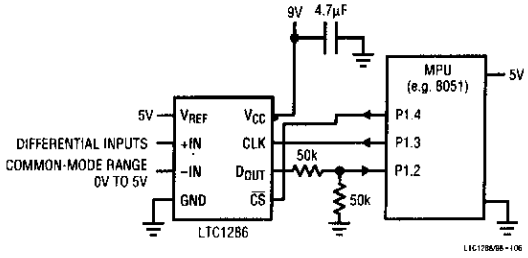



**Figure 6. Interfacing a 9V Powered LTC1286 to a 5V System**

## APPLICATION INFORMATION

### BOARD LAYOUT CONSIDERATIONS

#### Grounding and Bypassing

The LTC1286/LTC1298 are easy to use if some care is taken. They should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The $V_{CC}$ pin should be bypassed to the ground plane with a 10µF tantalum capacitor with leads as short as possible. If the power supply is clean, the LTC1286/LTC1298 can also operate with smaller 1µF or less surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

### SAMPLE-AND-HOLD

Both the LTC1286 and the LTC1298 provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1286 acquires input signals from "+" input relative to "–" input during the $t_{SMPL}$ time (see Figure 1). However, the S&H of the LTC1298 can sample input signals in the single-ended mode or in the differential inputs during the $t_{SMPL}$ time (see Figure 7).

#### Single-Ended Inputs

The sample-and-hold of the LTC1298 allows conversion of rapidly varying signals. The input voltage is sampled during the $t_{SMPL}$ time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

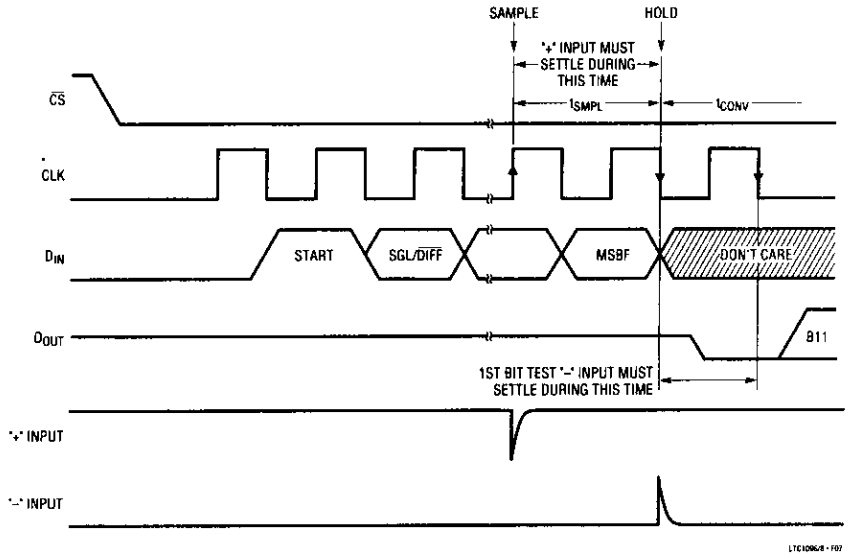



**Figure 7. LTC1298 "+" and "–" Input Settling Windows**

## APPLICATION INFORMATION

### Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 12 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 12/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, $V_{PEAK}$ is its peak amplitude and $f_{CLK}$ is the frequency of the CLK. In most cases $V_{ERROR}$ will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (305μV) with the converter running at CLK = 200kHz, its peak value would have to be 13.48mV.

### ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1286/LTC1298 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

### "+" Input Settling

The input capacitor of the LTC1286 is switched onto "+" input during the $t_{SMPL}$ time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1298 is switched onto "+" input during the sample phase ($t_{SMPL}$, see Figure 7). The sample phase is 1 1/2 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within $t_{SMPLE}$ for the LTC1286 and the LTC1298 respectively. Minimizing $R_{SOURCE}^+$ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

### "–" Input Settling

At the end of the $t_{SMPL}$, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing $R_{SOURCE}^-$ and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

### Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 6μs ("+" input) which occur at the maximum clock rate of 200kHz.

### Source Resistance

The analog inputs of the LTC1286/LTC1298 look like a 20pF capacitor ($C_{IN}$) in series with a 500Ω resistor ($R_{ON}$) as shown in Figure 8. $C_{IN}$ gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances

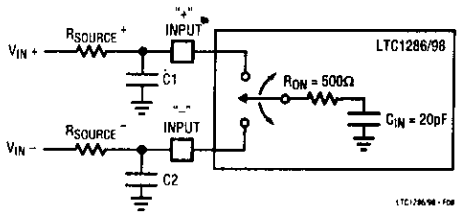



**Figure 8. Analog Input Equivalent Circuit**

## APPLICATION INFORMATION

will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

### RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of $C_F$ (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF \times V_{IN}/t_{CYC}$ and is roughly proportional to $V_{IN}$. When running at the minimum cycle time of 64µs, the input current equals 1.56µA at $V_{IN} = 5V$. In this case, a filter resistor of 75Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

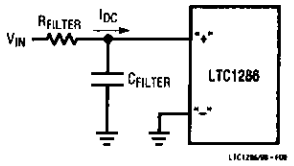



**Figure 9. RC Input Filtering**

### Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 240Ω will cause a voltage drop of 240µV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

### REFERENCE INPUTS

The reference input of the LTC1286 is effectively a 50kΩ resistor from the time $\overline{CS}$ goes low to the end of the conversion. The reference input becomes a high impedence node at any other time (see Figure 10). Since the voltage on the reference input defines the voltage span of the A/D converter, the reference input should be driven by a reference with low $R_{OUT}$ (ex. LT1004, LT1019 and LT1021) or a voltage source with low $R_{OUT}$.

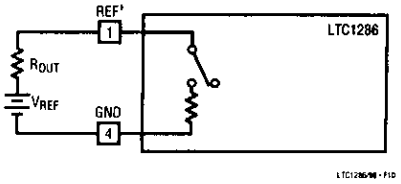



**Figure 10. Reference Input Equivalent Circuit**

### Reduced Reference Operation

The minimum reference voltage of the LTC1298 is limited to 4.5V because the $V_{CC}$ supply and reference are internally tied together. However, the LTC1286 can operate with reference voltages below 1V.

The effective resolution of the LTC1286 can be increased by reducing the input span of the converter. The LTC1286 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Change in Linearity vs Reference Voltage and Change in Gain vs Reference Voltage). However, care must be taken when operating at low values of $V_{REF}$ because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low $V_{REF}$ values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

### Offset with Reduced $V_{REF}$

The offset of the LTC1286 has a larger effect on the output code. When the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Change in Offset vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of $V_{OS}$. For example, a $V_{OS}$ of 122µV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a

## APPLICATION INFORMATION

0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1286.

### Noise with Reduced $V_{REF}$

The total input referred noise of the LTC1286 can be reduced to approximately 400µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 400µV noise is only 0.33LSB peak-to-peak. In this case, the LTC1286 noise will contribute virtually no uncertainty to the output code. However, for reduced references the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 2.5V reference this same 400µV noise is 0.66LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 1V, the 400µV noise becomes equal to 1.65LSBs and a stable code may be difficult to achieve. In this case averaging multiple readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on $V_{CC}$, $V_{REF}$ or $V_{IN}$) will add to the internal noise. The lower the reference voltage to be used the more critical it becomes to have a clean, noise free setup.

### Conversion Speed with Reduced $V_{REF}$

With reduced reference voltages, the LSB step size is reduced and the LTC1286 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of $V_{REF}$ are used.

### DYNAMIC PERFORMANCE

The LTC1286/LTC1298 have exceptional sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1286 plot.

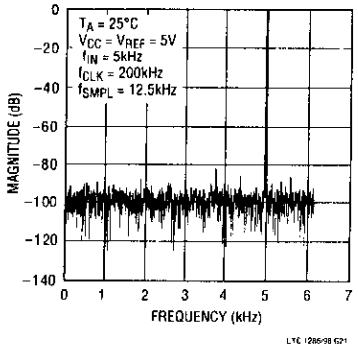



**Figure 11. LTC1286 Non-Averaged, 4096 Point FFT Plot**

### Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio (S/N + D) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 12 shows a typical spectral content with a 12.5kHz sampling rate.

### Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N+D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 12.5kHz with a 5V supply, the LTC1286 maintains above 11 ENOBs at 10kHz input frequency. Above 10kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains low.

## APPLICATION INFORMATION

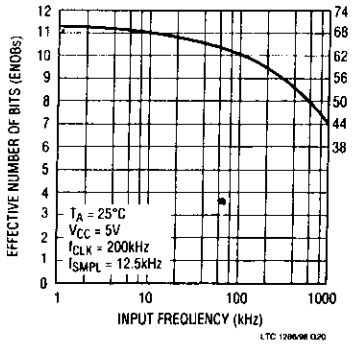



**Figure 12. Effective Bits and S/(N + D) vs Input Frequency**

### Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where $V_1$ is the RMS amplitude of the fundamental frequency and $V_2$ through $V_N$ are the amplitudes of the second through the $N^{th}$ harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 7kHz input signal, the LTC1286/LTC1298 have typical THD of 80dB with $V_{CC}$ = 5V.

### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies $f_a$ and $f_b$ are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20\log\left[\frac{\text{amplitude}\,(f_a \pm f_b)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 5kHz and 6kHz, the IMD of the LTC1286/LTC1298 is 73dB with a 5V supply.

### Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

### Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 11 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1286/LTC1298 have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency.