

Computer Architecture Experiment

Topic 5. Pipelined CPU supporting 31 MIPS Instructions

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实验操作流程



- 口阅读实验文档,理解31条MIPS指令实现方式
- 口以前一次实验为基础,支持31条MIPS指令, 使处理器功能更加丰富
- □对处理器进行仿真,检验处理器的仿真结 果是否符合要求。
- □综合工程并下载至开发板,在单步执行的过程中检查调试屏幕的输出,检验处理器的执行过程是否正确。



实验验收标准



口仿真执行过程中,处理器的行为和内部控制信号均符合要求。

□下载至开发板后的单步执行过程中,寄存 器的变化过程和最终执行结果与测试程序 相吻合。



Outline



- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures
- Precaution
- Checkpoints



Experiment Purpose



- Understand 31 MIPS instructions.
- Master the design methods of pipelined CPU executing 31 MIPS instructions.
- master methods of program verification of Pipelined CPU executing 31 MIPS instructions



Experiment Task



- Design of Pipelined CPU executing 31 MIPS instructions.
 - Design datapath
 - Design CPU Controller
- Verify the Pipelined CPU with program and observe the execution of program



Pipelined CPU supporting execution of 31 MIPS instruction

| | | | | | MIPS I | nstruct | ions | WG UNITYS |
|--------|--------|-------|--------------------------|-------|--------|---------|--|-----------|
| Bit # | 3126 | 2521 | 2016 | 1511 | 106 | 50 | Operations | |
| R-type | op | rs | rt | rd | sa | func | | |
| add | | rs | rt | rd | 00000 | 100000 | rd = rs + rt; with overflow | PC+=4 |
| addu | | rs | rt | rd | 00000 | 100001 | rd = rs + rt; without overflow | PC+=4 |
| sub | | rs | rt | rd | 00000 | 100010 | rd = rs - rt; with overflow | PC+=4 |
| subu | | rs | rt | rd | 00000 | 100011 | rd = rs - rt; without overflow | PC+=4 |
| and | | rs | rt | rd | 00000 | 100100 | rd = rs & rt; | PC+=4 |
| or | | rs | rt | rd | 00000 | 100101 | rd = rs rt; | PC+=4 |
| xor | | rs | rt | rd | 00000 | 100110 | rd = rs ^ rt; | PC+=4 |
| nor | | rs | rt | rd | 00000 | 100111 | rd = ~(rs rt); | PC+=4 |
| slt | 000000 | rs | rt | rd | 00000 | 101010 | if(rs < rt)rd = 1; else $rd = 0$; <(signed) | PC+=4 |
| sltu | | rs | rt | rd | 00000 | 101011 | if(rs < rt)rd = 1; else $rd = 0$; <(unsigned) | PC+=4 |
| sll | | 00000 | rt | rd | sa | 000000 | rd = rt << sa; | PC+=4 |
| srl | | 00000 | rt | rd | sa | 000010 | rd = rt >> sa (logical); | PC+=4 |
| sra | | 00000 | rt | rd | sa | 000011 | rd = rt >> sa (arithmetic); | PC+=4 |
| sllv | | rs | rt | rd | 00000 | 000100 | rd = rt << rs; | PC+=4 |
| srlv | | rs | rd = rt >> rs (logical); | PC+=4 | | | | |
| srav | | rs | rt | rd | 00000 | 000111 | rd = rt >> rs(arithmetic); | PC+=4 |
| HT. | 1.14 | rs | 00000 | 00000 | 00000 | 001000 | | PC=rs |

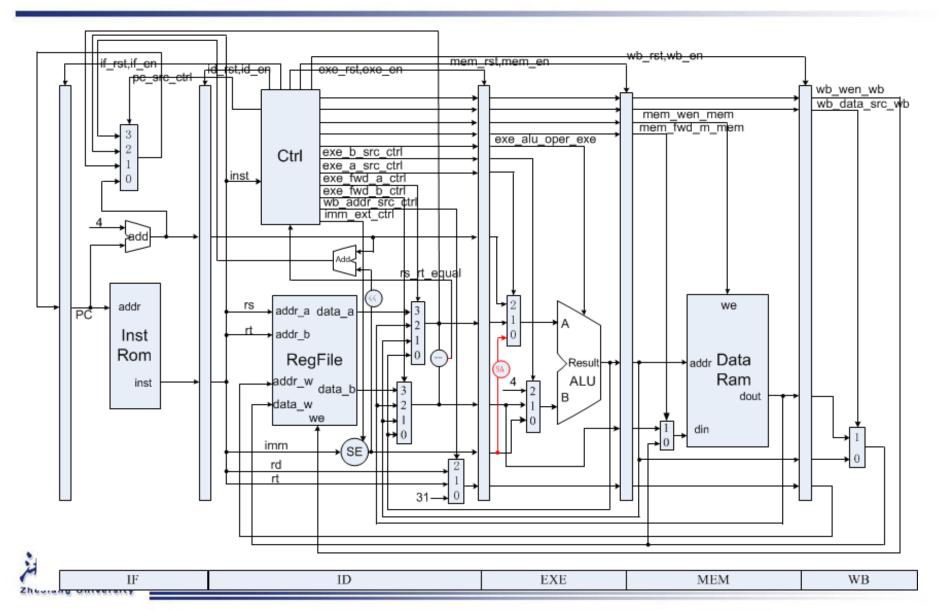
Pipelined CPU supporting execution of 31 MIPS instruction

| | | | | | MIPS In | nstruct | ions | WG UNIVERS | | | | | | | | |
|--------|--------|-------|------|---------|-----------|---------|---|------------|--|--|--|--|--|--|--|--|
| Bit # | 3126 | 2521 | 2016 | 1511 | 106 | 50 | Operations | | | | | | | | | |
| I-type | op | rs | rt | | immediate | e | | | | | | | | | | |
| addi | 001000 | rs | rt | | imm | | $rt = rs + (sign_extend)imm;$ with overflow | PC+=4 | | | | | | | | |
| addiu | 001001 | rs | rt | | imm | | $rt = rs + (sign_extend)imm;$ without overflow | PC+=4 | | | | | | | | |
| andi | 001100 | rs | rt | | imm | | rt = rs & (zero_extend)imm; | PC+=4 | | | | | | | | |
| ori | 001101 | rs | rt | | imm | | rt = rs (zero_extend)imm; | | | | | | | | | |
| xori | 001110 | rs | rt | | imm | | rt = rs ^ (zero_extend)imm; | | | | | | | | | |
| lui | 001111 | 00000 | rt | | imm | | rt = imm * 65536; | PC+=4 | | | | | | | | |
| lw | 100011 | rs | rt | | imm | | rt = memory[rs + (sign_extend)imm]; | PC+=4 | | | | | | | | |
| sw | 101011 | rs | rt | | imm | | memory[rs + (sign_extend)imm] < rt; | PC+=4 | | | | | | | | |
| beq | 000100 | rs | rt | | imm | | if (rs == rt) PC+=4 + (sign_extend)imm <<2; | PC+=4 | | | | | | | | |
| bne | 000101 | rs | rt | | imm | | if (rs != rt) PC+=4 + (sign_extend)imm <<2; | PC+=4 | | | | | | | | |
| slti | 001010 | rs | rt | | imm | | if (rs < (sign_extend)imm) rt =1 else rt = 0; less than signed | PC+=4 | | | | | | | | |
| sltiu | 001011 | rs | rt | | imm | | if (rs < (zero_extend)imm) rt =1 else rt = 0; less than unsigned | PC+=4 | | | | | | | | |
| J-type | op | | | address | | | | | | | | | | | | |
| j | 000010 | | | address | | | PC = (PC+4)[3128],address<<2 | | | | | | | | | |
| jal | 000011 | | | address | | | PC = (PC+4)[3128],address<<2; \$31 = PC+ | -4 | | | | | | | | |



Datapath of CPU supporting 31 MIPS Instr.





signed and unsigned type



reg and wire are unsigned type in Default

Signed Type:

- reg signed
- wire signed

Type Conversion Function

- \$signed()
- \$unsiged()



ALU



```
case (oper)
         EXE_ALU_SLT: begin
                  if (sign)
                           result = $signed(a) < $signed(b);
                  else
                           result = .....
         EXE_ALU_LUI: begin
                  result = .....
         end
         EXE_ALU_SR: begin
                  if (sign)
                  else
```

endcase



Instr. Mem.(1)



```
0:3c010000;
                % (00) main:
                                lui $1, 0 # address of data[0] %
1:34240050;
                % (04)
                                ori $4, $1, 80 # address of data[0] %
2:0c00001b;
                % (08) call:
                                jal sum # call function %
3:20050004;
                % (0c) dslot1:
                                addi $5, $0, 4 # counter, DELYED SLOT(DS) %
4: ac820000;
                % (10) return:
                                sw $2, 0($4) # store result %
5:8c890000;
                                lw $9, 0($4) # check sw %
                % (14)
                                sub $8, $9, $4 # sub: $8 <- $9 - $4 %
                % (18)
6:01244022;
                                addi $5, $0, 3 # counter %
7:20050003;
                % (1c)
                % (20) loop2:
                                addi $5, $5, -1 # counter - 1 %
8:20a5ffff;
                                ori $8, $5, 0xffff # zero-extend: 0000ffff %
                % (24)
9:34a8ffff;
                % (28)
                                xori $8, $8, 0x5555 # zero-extend: 0000aaaa %
A: 39085555;
B: 2009ffff;
                % (2c)
                                addi $9, $0, -1 # sign-extend: ffffffff %
```

Instr. Mem.(2)



```
C: 312affff; % (30) andi $10, $9, 0xffff # zero-extend: 0000ffff %
```

11:00000000; % (44) dslot2: nop # DS %

12:08000008; % (48) j loop2 # jump loop2 %

13:00000000; % (4c) dslot3: nop # DS %

14: 2005ffff; % (50) shift: addi \$5, \$0, -1 # \$5 = ffffffff %

15:000543c0; % (54) sll \$8, \$5, 15 # <<15 = ffff8000 %

16:00084400; % (58) sll \$8, \$8, 16 # <<16 = 80000000 %

17:00084403; % (5c) sra \$8, \$8, 16 # >>16 = ffff8000 (arith) %

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Instr. Mem.(3)



```
18:000843c2; % (60) srl $8, $8, 15 # >>15 = 0001ffff (logic) %
```



Data Mem.



```
0: BF800000;  % 1 01111111 00..0 fp -1 %
```

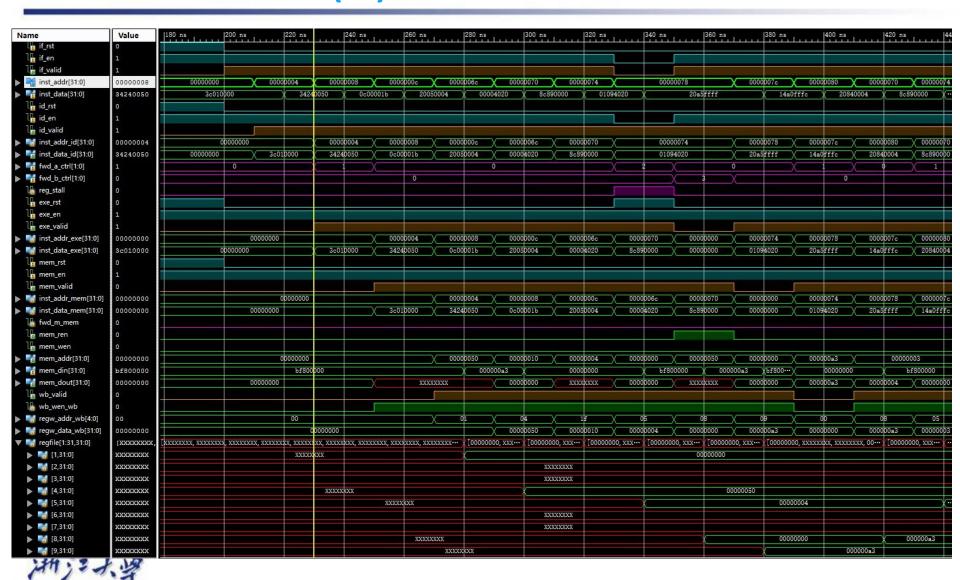
```
14:000000A3; % (50) data[0] %
```



Simulation (1)

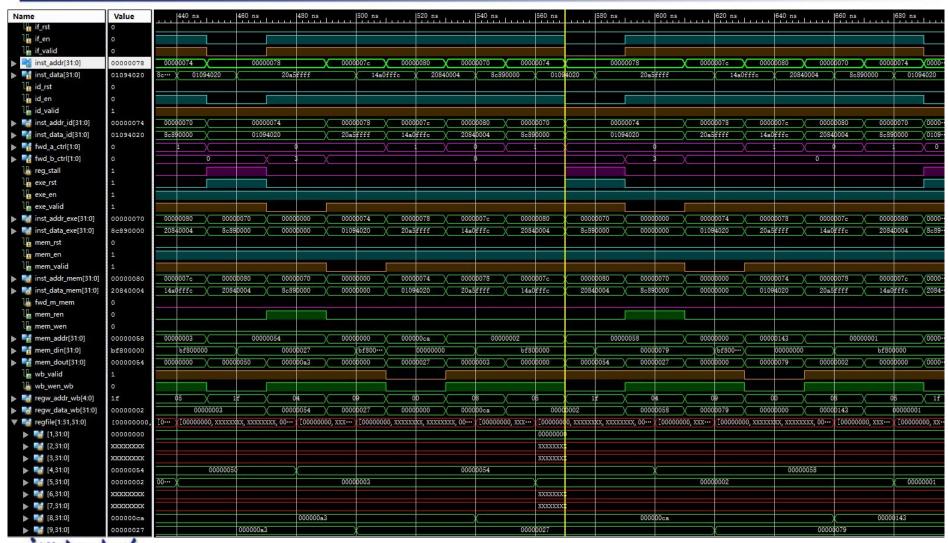
ZheJiang University





Simulation (2)



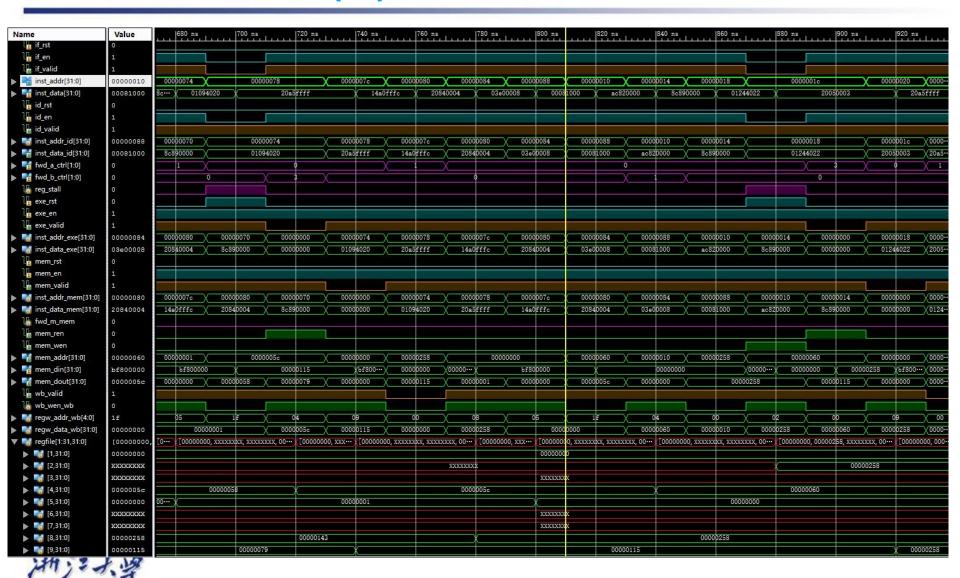




Simulation (3)

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Simulation (4)



| me | Value | 19 | 20 ns | L | 9. | 40 ns | Îm | 960 | ns | | 980 ns | Ú. | 1,000 | ns | 1, 02 | 0 ns | 1, | 040 ns | | 1,060 r | 15 | 1,0 |)80 ns | | 1, 10 | ns | | 1, 120 | 15 | 1, 14 | 40 ns | | 1, 160 | ns |
|---------------------|------------|------|---------|--|---------|---------|----------|---------------|---------------|---------|--------|-------------|----------|-----------------------|---------|---------------|-------------|---------------------|-------|---------|----------|--------|------------|--------|-------|--------|------|--------|----------------|----------|-------------|----------|---------|------------|
| La if_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| if_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| m if_valid | 1 | | | _ | | | _ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr[31:0] | 00000034 | 0000 | = | _ | 000000 | | _ | 0000028 | _X | 0000 | | | 00000030 | | 0000034 | | 000000 | | 0000 | | _ | 000004 | | | 00044 | X_ | 0000 | | | 0000004c | | 0000 | | X00 |
| inst_data[31:0] | 312affff | 2 | 20a | ffff | | 34s | 8ffff | | 390858 | 555 | 20 | 09ffff | 3 | 12sffff | | 01493025 | | 01494 | 026 | 014 | 63824 | | 10a00 | 003 | * | 000000 | 00 | 080 | 80000 | | 00000 | 000 | 20 | a5fff |
| id_rst | 0 | | | | | | | | | | | | | | - 12 | | | | | | | | | | | | | | | | | | | |
| id_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| id_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr_id[31:0] | 00000030 | 0000 | - | _ | 000000 | | _ | 0000024 | X | 0000 | - | | 0000002c | | 0000030 | | 00000 | 34 | 0000 | 0038 |)(0 | 000003 | c)(| 000 | 00040 | X_ | 0000 | | _ | 00000048 | | | 004c | _)(0C |
| inst_data_id[31:0] | 312afffff | 2005 | 0003 | X = | 20a5f f | fff | X 3 | 4a8ffff | =X | 3908 | 5555 | $X \subset$ | 2009ffff | 3 | 12sffff | \rightarrow | 14930 | 25 | 0149 | 4026 |) 0 | 146382 | 4)(| 10ε | 00003 | =X $=$ | 0000 | | X | 08000008 | \square X | 0000 | 0000 | (20 |
| fwd_a_ctrl[1:0] | 1 | 0 | | X | | | | | | | | \times | • | | | 1 | | X | - 2 | | X | | | | | | | 0 | | | | | | |
| fwd_b_ctrl[1:0] | 0 | | | | | | | | 0 | | | | | | | \rightarrow | 2 | \longrightarrow X | | | X | 2 | $=$ χ | | | | | | 0 | | | | | |
| reg_stall | 0 | | | | | | | | | | | | | | | | | | | | | | | | _ | | | | | | | | | |
| exe_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| exe_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| exe_valid | 1 | | | COLUMN TO SERVICE SERV | 1 | | | | - | | | | | | | | | | | | | 7 | 100 | | | | | | to the same of | | | | | |
| inst_addr_exe[31:0] | 0000002c | 0000 | 0018 | X = | 000000 | 01c | χ 0 | 0000020 | =X | 0000 | 0024 | X | 00000028 | 0 | 000002c | \rightarrow | 000000 | 30 \ | 0000 | 0034 | X 0 | 000003 | 8 X | 000 | 0003c | =X $=$ | 0000 | 0040 | X | 00000044 | X | 0000 | 0048 | _\(00 |
| inst_data_exe[31:0] | 2009ffff | 0124 | 4022 | X = | 200500 | 003 | X 2 | a5ffff | =X | 34a8 | ffff | \propto | 39085555 | 2 | 009ffff | $\equiv \chi$ | 312sff | ff X | 0149 | 3025 | χ 0 | 149402 | 6 X | 014 | 63824 | =X $=$ | 10a0 | 0003 | X | 00000000 | \square X | 0800 | 8000 | (00 |
| mem_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_valid | 1 | | | | | | | | | | | - | | | | | | | | | _ | | | | | | | | | | | | | - |
| inst_addr_mem[31:0] | 00000028 | 0000 | 0000 | X = | 000000 | 018 | χ 0 | 000001c | =X | 0000 | 0020 | \propto | 00000024 | 0 | 0000028 | | 000000 | 2c \ | 0000 | 0030 | X 0 | 000003 | 4 X | 000 | 00038 | =X $=$ | 0000 | 003c | X | 00000040 | \square X | 0000 | 0044 | (00 |
| inst_data_mem[31:0] | 39085555 | 0000 | 0000 | X = | 012440 | 022 | X 2 | 0050003 | =X | 20a5 | ffff | \propto | 34a8ffff | 3 | 085555 | | 2009ff | ff | 312a | ffff | X 0 | 149302 | 5 X | 014 | 94026 | | 0146 | 3824 | X | 10a00003 | \square X | 0000 | 0000 | 08 |
| fwd_m_mem | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_ren | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_wen | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_addr[31:0] | 0000aaaa | 0000 | 0000 | X | 000001 | 1f8 | χ 0 | 0000003 | $=$ χ | 0000 | 0002 | X | 0000ffff | _ 0 | 000аааа | | fffff | ff X | 0000 | ffff |) f | ffffff | f | ffi | f0000 | | 0000 | ffff | X | 00000002 | X | | 0000000 | 00 |
| mem_din[31:0] | 00000000 | 0 \E | bf800 | X | 00 | 000000 | 0 | \rightarrow | b | f800000 | | X | | | | | | | | 0000000 | 0 | | | | | | | | | | | bf80 | 0000 | |
| mem_dout[31:0] | 000001f8 | 0000 | 0000 | X | 000000 | 060 | X | | 000000 | 000 | | X | 0 | 000 <mark>01f8</mark> | | $-\chi$ | 000002 | 58 | XXXX | XXXX | X | | | ffi | fffff | | | | X | | 0 | 0000000 | | |
| wb_valid | 1 | | | ╙ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| wb_wen_wb | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| regw_addr_wb[4:0] | 08 | 01 | 9 | X | 00 | | X | 08 | $=$ χ | | | 05 | | \supset | | 08 | | X | 0 | 9 | X | 0a | $=$ χ | | 06 | | 0 | 8 | χ | 07 | $=$ χ | | 00 | |
| regw_data_wb[31:0] | 0000ffff | 0000 | 0258 | X | 000000 | 000 | χ ο | 00001f8 | $\equiv \chi$ | 0000 | 0003 | X | 00000002 | 0 | 000ffff | X | 0000aa | 88 X | ffff | ffff | χ 0 | 000fff | fχ | ffi | fffff | | ffff | 0000 | X | 0000fff | \equiv X | 0000 | 0002 | \(00 |
| regfile[1:31,31:0] | [00000000, | I)(I | [000000 | 00, 00 | 000258 | B, XXXX | XXXX, 00 | [000 | 00000 | , 000 | [00000 | 000,00 | 0000]00 | 0000,000 | [000 | 000000, 00 | 0 [0 | 00000000 | , 000 | [00000 | 000, 000 | [0 | 0000000 | 0, 000 | [000] | 00000, | 000 | [00000 | 000, 00 | 00] | 000000 | 0,000002 | 58, XXX | XXXX |
| [1,31:0] | 00000000 | | | | | | | | | | | | | | | | | 00000000 |) | | | | | | | | | | | | | | | |
| [2,31:0] | 00000258 | | | | | | | | | | | | | | | | | 00000258 | | | | | | | | | | | | | | | | |
| [3,31:0] | XXXXXXX | | | | | | | | | | | | | | | | | CXXXXXXX | | | | | | | | | | | | | | | | |
| [4,31:0] | 00000060 | | | | | | | | | | | | | | | | | 00000060 | | | | | | | | | | | | | | | | |
| [5,31:0] | 00000002 | | | | (| 000000 | 00 | | | | 00 | 000003 | X | | | | | | | | | | 00000 | 002 | | | | | | | | | | |
| [6,31:0] | XXXXXXX | | | | | | | | | | | | XXXX | CXX | | | | | | | | | | | | | | | | fffffff | | | | |
| [7,31:0] | XXXXXXX | | | | | | | | | | | | | | XXX | XXXXX | | | | | | | | | | | | | | | | 0000 | ffff | |
| [8,31:0] | 000001f8 | | | 000 | 00258 | | | | | | 00 | 0001f8 | | | | 0000ffff | - x- | | | | 0 | 000aaa | а. | | | | | | | | fffff0 | | | |
| [9,31:0] | 00000258 | | | | | | | | | | | 000258 | | | 7 × | | | | | | | | | | | | | ffff | | | | | | |

Simulation (5)



| me | Value | | 1, 160 ns | i. | 1, 18 | 0 ns | I | 1, 200 ns | 5 | 1, 22 | 0 ns | | 1, 240 n | 5 | 1, 2 | 60 ns | | 1, 280 | ns | 1, | 300 ns | | 1, 320 | ns | 1, | 340 ns | | 1, 360 n | ıs | 1, 380 | ns | 1, 400 |
|--------------------------|------------|--------|-----------|---------|---------|---------------------|---------------|-----------|--------|---------------|---------------------|------|----------|----------|---------------|--------------|-------|----------|-------------------------|---------|----------|----------|----------|-----------------|---------------|---------|-------|-----------|----------|---------------|---------------|------------|
| if_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| la if_en | 1 | | | | j | | | | | | | | | | | | | | | | | | | | | | | | | j | | |
| lm if_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr[31:0] | 00000034 | 0000 | | | 0000024 | | 00000 | | _ | 000002c | $=$ \times | | 0030 | 0(| 000003 | | | 00038 | | 000000 | | | 00040 | | 0000004 | | | 0048 | _ | 000004c | | 000020 |
| inst_data[31:0] | 312afffff | 00 | 20a5 | ffff | | 34a8fff | f | 3908 | 35555 | \rightarrow | 2009ff | ff | 312 | sffff | \Rightarrow | 01493 |)25 | 01 | 1494026 | | 0146 | 3824 | 10 | 0a00003 | \rightarrow | 00000 | 000 | 080 | 80000 | | 0000000 | 20e |
| id_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| id_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| m id_valid | 1 | | | | | | | | | | | | | | | | | | | | - | | | | | | | | | | 1122 | |
| inst_addr_id[31:0] | 00000030 | | 004c | | 0000020 | =X $=$ | 00000 | | _ | 0000028 | | | 002c | | 000003 | | | 00034 | | 000000 | | | 0003c | | 0000004 | | | 0044 | | 0000048 | | 00004c |
| inst_data_id[31:0] | 312afffff | 0000 | 0000 | 20 | a5ffff | =X $=$ | 34a8f | fff | X 3 | 9085555 | \rightarrow | 2009 | ffff | 3: | 12afff | f) | 0149 | 3025 | \supset | 014940 |)26 | 014 | 63824 | \supset | 10a0000 | 3 | 000 | 0000 | X 0 | 8000008 |)(O(| 000000 |
| fwd_a_ctrl[1:0] | 1 | | | 0 | | | | | 1 | | | | • | | | 1 | | | X | 2 | | | | | | | | 0 | | | | |
| fwd_b_ctrl[1:0] | 0 | | | | | | | | 0 | | | | | | | $=$ \times | | 2 | \rightarrow | 0 | | | 2 | \rightarrow | | | | | 0 | | | |
| 🖟 reg_stall | 0 | | | | | | | | | | | | | _ | | | | | | | | | | | | | | | | | | |
| exe_rst | 0 | | | | | | \rightarrow | | | | | | | | _ | | | _ | | _ | | | _ | | | | | | | | | |
| exe_en | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| exe_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr_exe[31:0] | 0000002c | 0000 | 0048 | (00 | 00004c | =X $=$ | 00000 | 020 | χ ο | 0000024 | =X $=$ | 0000 | 0028 | 00 | 000002 | c X | 0000 | 00030 | \supset X \equiv | 000000 | 34 | 000 | 00038 | | 0000003 | | 000 | 00040 | χ 0 | 0000044 | X 00 | 000048 |
| inst_data_exe[31:0] | 2009ffff | 0800 | 8000 | (00 | 000000 | \equiv X \equiv | 20a5f | fff | X 3. | 4a8ffff | =X $=$ | 3908 | 5555 | 20 | 009fff | f) | 312 | ffff | \supset X \subseteq | 014930 | 25 | 014 | 94026 | \supset | 0146382 | 4 X | 10a | 0003 | χ 0 | 0000000 | 30 | 800000 |
| mem_rst | 0 | | | | | | | | | | | | | | | | | | | | | | 1 | | | | | | | | | |
| mem_en | 1 | | | | ĵ | | | | | | | | | | | | | | | | | | | | | | | | | 1 | | |
| mem_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | - | | | | | | | |
| inst_addr_mem[31:0] | 00000028 | 0000 | 0044 | (00 | 0000048 | $\equiv \chi$ | 00000 | 04c | X 0 | 0000020 | =X $=$ | 0000 | 0024 | 00 | 000002 | 8 | 0000 | 0002c | \supset | 000000 | 30 | 000 | 00034 | | 0000003 | 8 X | 000 | 003c | χ 0 | 0000040 | X 00 | 000044 |
| inst_data_mem[31:0] | 39085555 | 0000 | 0000 | 08 | 8000008 | | 00000 | 000 | 2 | Oa5ffff | =X $=$ | 34a8 | ffff | 39 | 908555 | 5 (| 2009 | ffff | \supset X \subseteq | 312sff | ff | 014 | 93025 | \supset | 0149402 | 6 | 014 | 3824 | X 1 | 0a00003 | 00 | 000000 |
| 🔓 fwd_m_mem | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_ren | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_wen | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| mem_addr[31:0] | 0000aaaa | | | 0 | 0000000 | <u> </u> | | | (0 | 0000001 | $=$ \times | 0000 | ffff | 00 | 000aaa | a (| fff | fffff | X | 0000ff | ff | fff | fffff | \supset | ffff000 | 0 \ | 000 | ffff | X 0 | 0000001 | X | 0000000 |
| mem_din[31:0] | 00000000 | | | | | bf80000 | 00 | | | | | | | | | | | | | 00 | 0000000 | | | | | | | | | \rightarrow | bf | 800000 |
| mem_dout[31:0] | ffff0000 | | | 0 | 0000000 | | | | X 0 | 0000002 | | | fff | f0000 | | $=$ \times | fff | fffff | \supset X \subseteq | 0000ff | ff | | | | fffffff | f | | | X | | 000000 | 00 |
| wb_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| wb_wen_wb | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| regw_addr_wb[4:0] | 08 | | | | | 00 | | | | | $=$ \times | (| 5 | \times | | 08 | | | \supset X \equiv | 09 | | | 0a | \rightarrow X | 06 | X | | 8 | X | 07 | $\overline{}$ | 00 |
| gregw_data_wb[31:0] | 0000ffff | 0000 | 0002 | X | | | 00000 | 000 | | | \equiv X \equiv | 0000 | 0001 | 00 | 000fff | f X | 0000 | 08888 | $\overline{}$ | ffffff | ff) | 000 | 0ffff | X | fffffff | f X | fff | 0000 | χ 0 | 000ffff | X 00 | 000001 |
| d regfile[1:31,31:0] | [00000000, | [00000 | 000, 0000 | 0258, X | xxxxxx | , 000000 | 60, 000 | 100002, f | ffffff | f, 0000f | fff, ff | ff0 | [00000 | 000,000 | [0 | 0000000 | , 000 | [0000 | 0000, 0 | 0000258 | 3, XXXXX | XX, 0000 | 00060, 0 | 0000001 | , ffffff | ff, 000 | Offff | [00000 | 000, 000 | 00258, XX | XXXXXX, OC | 000060, 00 |
| [1,31:0] | 00000000 | | | | | | | | | | | | | | | | | 00000 | 000 | | | | | | | | | | | | | |
| [2,31:0] | 00000258 | | | | | | | | | | | | | | | | | 00000 | 258 | | | | | | | | | | | | | |
| [3,31:0] | xxxxxxx | | | | | | | | | | | | | | | | | XXXXX | XXX | | | | | | | | | | | | | |
| ► 1 [4,31:0] | 00000060 | | | | | | | | | | | | | | | | | 00000 | 060 | | | | | | | | | | | | | |
| [5,31:0] | 00000001 | | | | | 00 | 000002 | | | | | | | | | | | | | | | | 00 | 000001 | | | | | | | | |
| ► 6,31:0 [6,31:0] | ffffffff | | | | | | | | | | | | | | | | | fffff | fff | | | | | | | | | | | | | |
| [7,31:0] | 0000ffff | | | | | | | | | | | | | | | | | 0000f | fff | | | | | | | | | | | | | |
| ► ■ [8,31:0] | ffff0000 | | | | | | | ffff000 | 0 | | | | | | $\overline{}$ | 0000f | ff | x | | | | 000 | Оаааа | | | | | \bigvee | | fi | ff0000 | |
| [9,31:0] | ffffffff | | | | | | | | | | | | | | | | | fffff | 000 | | | | | | | | | 1 | | | | |



Simulation (6)



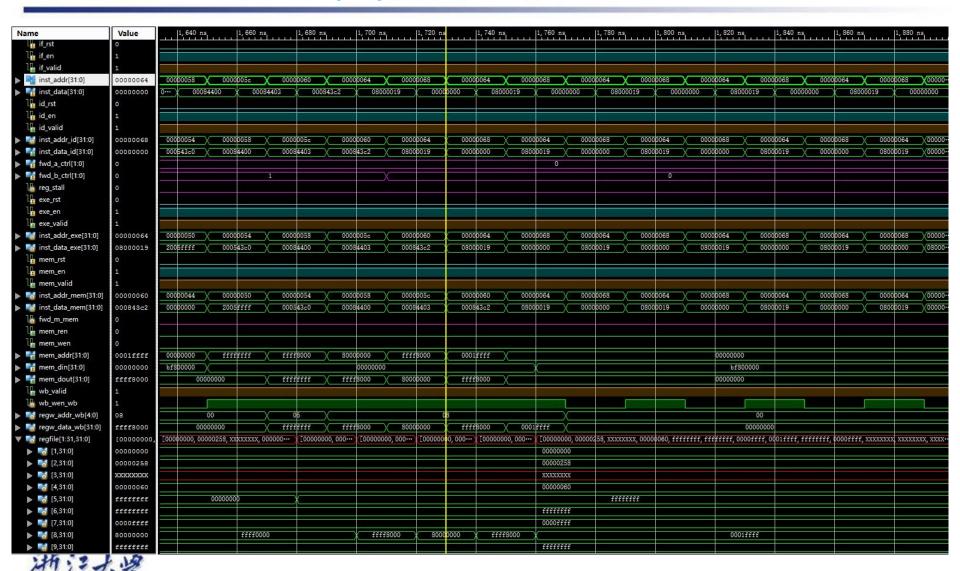
| ne | Value | 1, | 400 ns | | 1, 420 n | ıs | 1, 440 | ns | 1, 460 | ns | 1, 480 | ns | 1,500 | ns | 1,520 n | IS . | 1, 540 n | 5 | 1, 560 ns | s I I I I I I | 1,580 n | 5 | 1,600 ns | لبيب | 1,620 ns | 1 | 1,640 ns |
|---------------------------------|--|----------------|----------|----------|----------|---------|---|--------|------------------|----------|---------------|---------------|---|-----------|---------|-------|------------|--------|---|------------------|---------|--------|----------|----------------|----------|---------------|-----------|
| | 0 | | | | | | 27 | | | | | | | | | | | | | | | | 2 | | | | |
| | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| if_valid | 1 | | | | | _ | | | | | | | | | | | | | | | | | | | | | |
| inst_addr[31:0] | 00000034 | 00000 | | 0000 | | | 00028 | _ | 000 0 02c | | 0000030 | _1`_ | 00000034 | | 00038 | | 0003c | | 00040 | - | 00044 | 0000 | | 00000 | | 0000 | |
| inst_data[31:0] | 312afffff | 00 | 20a5f | fff | 34s | 8ffff | ¥ 39 | 085555 | X20 | 09ffff | 31 | 2sffff | | 493025 | 014 | 94026 | 014 | 63824 | 10a | 00003 | ¥ 000 | 00000 | 2005: | fff | 0005 | 43c0 | 00084 |
| A | 0 | | | | | | | | | | | | | | 100 | | | | | | | | | | | | |
| | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | 1 | 00000 | | 0000 | 0000 | V -00 | 100004 | | | | | | | V - 001 | 00004 | V 000 | | V | 200 | V 0000 | 00040 | V | 2011 | 0000 | 050 | | 2054 |
| inst_addr_id[31:0] | 00000030 | 00000 | | 0000 | | - | 00024 | | 0000028 | | 000002c | _1_ | 00000030 | | 00034 | | 00038 | | 003c | | 00040 | - | 0044 | 00000 | | | 0054 |
| | 312affff | 00000 | 000 X | 20a5 | ffff | X 34s | 8ffff | X 3 | 9085555 | _X2 | 009ffff | _ | 312sffff | X 014 | 93025 | X 014 | 94026 | X 014 | 3824 | X 10a0 | .00003 | χ 0000 | 0000 | 2005 | fff | χ 0005 | 43c0 X |
| | 1 | | | | | Х | | 1 | | _X | • | | | 1 | | ऱ— | Ť | X | | · · | | | 0 | | | | |
| | 0 | | | | | | | 0 | | | | | | | - | Х | 0 | Х | 2 | Х | | | 0 | | | X | 1 |
| <u> </u> | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| exe_valid | 2000000 | 00000 | 040 | 0000 | 004 | V 000 | 100000 | · · | 0000004 | | 0000028 | | 0000002c | V | 00030 | V 000 | 000034 | V 000 | 2022 | V | 0002- | V 0000 | 20040 | 00000 | 1044 | 0000 | 0050 |
| | 0000002c | 08000 | | | 0000 | | 100020 | | 0000024 | | 9085555 | _1_ | THE RESERVE TO SHARE THE PARTY NAMED IN | | | | | | 00038 | | 0003c | | 0040 | 00000 | | | |
| | 2009ffff | 08000 | 008 X | 0000 | 0000 | X 20s | 5ffff | | 4a8ffff | X3 | 9080555 | _ | 2009ffff | X 31 | affff | X 014 | 193025 | X 014 | 4026 | X 0148 | 63824 | X IUat | 0003 | 0000 | 1000 | X 2005 | ffff |
| | 0 | | | | | | | | | | | | | | | | | | | | | | 5 | | | | |
| 1 | 1 | | _ | | | | _ | _ | _ | | _ | _ | _ | | | | - | | | | | | | | | | |
| mem_valid | 00000028 | 00000 | · · | 0000 | 0040 | V 000 | 0004c | V . | 0000020 | | 0000024 | _ | 00000028 | V 000 | 0002c | V 000 | 000030 | V 000 | 00034 | V 000 | 00038 | V 0000 | 003c | 00000 | 1040 | 0000 | 0044 |
| | 39085555 | 00000 | | 0800 | | | 100000 | | Oa5ffff | | 4a8ffff | | 39085555 | | | | affff | | 3025 | | 94026 | | | 10a00 | | | 0000 |
| | STATE OF THE PARTY | 00000 | , DOO | 0800 | 0008 | X 000 | 00000 | | Uastiii | | 4807777 | _ | 39030333 | | 9ffff | . 312 | BIIII | N 014: | 3025 | X 014: | 34020 | 0146 | 3024 | 1080 | 1003 | X 0000 | 0000 |
| | 0 | | | | | | _ | | | | | | | | | | | | | | | | - | | | | |
| | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | 00 | 000000 | | | | | 2222000 | | 0000aaaa | V 55 | fffff | V 000 | Offff | V 555 | cccc | V 555 | f0000 | V 0000 | cece / | | 0000 | 00000 | |
| mem_addr[31:0] mem_din[31:0] | 00000aaaa | | | | | 800000 | | | | ➾ | 000ffff | | оооонна | A 111 | 11111 | X | 00000000 | | ffff | X | 10000 | X 0000 | , | $= \downarrow$ | 0000 | bf800000 | = |
| mem_dout[31:0] | ffff0000 | | | 000 | 00000 | 800000 | | V 0 | 0000001 | ➾ | | ff0000 | | V 55 | fffff | V 000 | Offff | · - | | 222 | fffff | | | <u> </u> | | 00000000 | |
| wb_valid | 1 | | | 000 | 00000 | | | | 0000001 | _^_ | - | 11,000 | | | 11111 | / 000 | ,01111 | X | | 9111 | 11111 | | / | | | 00000000 | |
| | 1 | | | _ | | | | | _ | _ | | _ | _ | _ | _ | _ | _ | _ | _ | _ | _ | _ | | _ | _ | 1 | |
| | 08 | | | _ | | 00 | | | _ | | 05 | \rightarrow | | 08 | | V | 00 | V | | V 7 | 06 | V . | le \ | | = | $\overline{}$ | 00 |
| regw_data_wb[31:0] | 0000ffff | 00000 | 001 V | | | 00 | 00 | 000000 | | _^_ | | \Rightarrow | 0000ffff | | Овава | √ fff | fffff | 0000 | ffff | √ fff | fffff | V ffff | 0000 | 0000 | eee | > | 00000000 |
| regfile[1:31,31:0] | [00000000, | THE OWNER WHEN | |)258 XXX | XXXXX O | 0000060 | | | ff, 0000ff | ff ffff. | . [0000 | _1_ | | 0000, 000 | - | | 0258, XXXX | | THE RESERVE TO SERVE | | | | | 0, 000002 | | XXX 0000 | |
| [1,31:0] | 00000000 | .000000 | -0, 0000 | acoo, na | annan, u | | .,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | | , 500011 | , | 10000 | 0,00 | 10000 | | 000000 | | , AAAA | | 000,000 | | 1111,00 | | _0000000 | J, 000002 | , | | 500, 0000 |
| [2,31:0] | 00000000 | | | | | | | | | | | | | | 000000 | | | | | | | | | | | | |
| | XXXXXXXX | | | | | | | | | | | | | | XXXXXX | | | | | | | | | | | | |
| [4,31:0] | 00000060 | | | | | | | | | | | | | | 000000 | | | | | | | | | | | | |
| [4,31:0] | 00000000 | | | | | 000000 | 01 | | | | \rightarrow | | | | 000000 | - | | | 0000 | 00000 | | | | | | | |
| [6,31:0] | ffffffff | | | | | 000000 | | | | | \rightarrow | | | | ffffff | ff | | | 0000 | 00000 | | | | | | | |
| [7,31:0] | 0000ffff | | | | | | | | | | | | | | 0000ff | | | | | | | | 0 | | | | |
| [8,31:0] | ffff0000 | | | | | | ffff00 | 000 | | | | | | 00ffff | 000011 | ** | | none | Daaaa | | | | V | | ffff | 0000 | |
| [0,51.0] | ffffffff | | | | | | | | | | | | | | ffffff | | | 000 | 222 | | | | \ | | | 5500 | |



Simulation (7)

ZheJiang University





Simulation (8)



| Name | Value | | 8 | 3, 700 | ns | | 8,800 n | ıs | 18 | ,900 ns | la cra | 9,000 п | s Luur | 9, 10 | 00 ns | 19 | 200 ns | Linite | 9, 300 r | 15 | 9,400 n | s | 9, 500 | ns | 9, | 600 ns | 1000 | 9, 700 | ns | 9,800 ns |
|--------------------------|------------|-----------|-----------|-----------------|----------|-----------|----------|--------|-----------|-----------------|-----------|---------------|---------------|-------|-------------|--------|---------------------|--------------|-----------------|------------------|-------------|-------------|------------|----------|---------|---------------------|------------|-------------|--------------|------------------|
| inst_addr[31:0] | 00000064 | X 0 | 000003c | $=$ \times | 00 | 000040 | =X | 000 | 00044 | $=$ \times | 0000005 | · X | 000000 | 4 | X 0000 | 00058 | \equiv X \equiv | 0000005 | X | 0000006 | X | 0000006 | X | 0000 | 0068 | \equiv X \equiv | 0000006 | 4 X | 0000006 | 8 X 00000 |
| inst_data[31:0] | 08000019 | 0149402 | 26 | 01463 | 824 | \propto | 10a000 | 003 | X | 0000000 | 0 / | 2005ff | ff | 000 |)543c0 | X | 00084400 | | 000844 | 103 | 000843 | c2 X | 08000 | 019 | X 0 | 000000 | 0 | 08000 | 019 | 00000000 |
| l∰ inst_ren | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| l <mark>∎</mark> id_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| l∰ id_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr_id[31:0] | 00000068 | | 0000038 | $=$ χ | 00 | 00003 | X | 000 | 00040 | $=$ \times | 0000004 | X | 000000 | 50 | 0000 | 00054 | =X $=$ | 0000005 | \$ X | 0000005 | 4 X | 0000006 | • X | 0000 | 0064 | =X $=$ | 0000006 | 8 X | 0000006 | 4 00000 |
| inst_data_id[31:0] | 00000000 | X 0 | 1494026 | $=$ χ | 01- | 463824 | X | 10s | 00003 | =X $=$ | 0000000 | • X | 2005ff | åf 🚛 | 000 | 43c0 | | 0008440 | • X | 0008440 | 3 X | 000843c | 2 X | 0800 | 0019 | | 0000000 | W X | 0800001 | 9 / 00000 |
| fwd_a_ctrl[2:0] | 0 | I)(I | 2 | | | | | | | | | | | | | | | | | 0 | | | | | | | | | | 1.360 |
| fwd_b_ctrl[2:0] | 0 | 2)(| 0 | $=$ χ | | 2 | | | | | 0 | | | | \times | | | | 1 | | | | $=$ χ | | | | | | 0 | |
| la exe_rst | 0 | | | | | | | | | | | | | | V-2.0 | | | | | | | | | | | | | | | |
| l exe_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr_exe[31:0] | 00000064 | X 0 | 0000034 | \equiv χ | 00 | 000038 | Х | 000 | 10003¢ | X | 0000004 | • X | 000000 | 14 | 0000 | 00050 | X | 0000005 | 4 X | 0000005 | 8 X | 0000005 | ¢χ | 0000 | 00060 | X | 0000006 | X | 0000006 | 8 × 00000 |
| inst_data_exe[31:0] | 08000019 | X 0 | 1493025 | $=$ χ | 01 | 494026 | =X | 014 | 63824 | X | 10a0000 | 3 X | 000000 | 00 | 200 | ffff | $\overline{}$ | 000543c | • X | 0008440 | X | 0008440 | 3 X | 0008 | 43c2 | =X $=$ | 0800001 | 9 (| 0000000 | 08000 |
| 🖟 reg_stall | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 mem_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 mem_valid | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| inst_addr_mem[31:0] | 00000068 | X 0 | 0000030 | $\equiv \chi$ | 00 | 000034 | X | 000 | 00038 | X | 0000003 | X | 000000 | 10 | 0000 | 00044 | $\overline{}$ | 0000005 | ♦ X | 0000005 | X | 0000005 | \$ X | 0000 | 005¢ | \equiv X \equiv | 000000€ | (X | 0000006 | 4 00000 |
| inst_data_mem[31:0] | 00000000 |)(3 | 12affff | $=\chi$ | 01 | 49302 | X | 014 | 94026 | \equiv χ | 0146382 | X | 10a000 |)3 | 0000 | 00000 | $\overline{}$ | 2005fff | † X | 0005 4 3c | • X | 0008440 | • X | 0008 | 4403 | | 000843 | 2 (| 0800001 | 9 \ 00000 |
| la fwd_m_ctrl | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| la mem_ren_mem | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ll mem_wen_mem | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| → 📆 mem_addr[31:0] | 00000000 | X 0 | 0000ffff | $=$ χ | ff | fffffi | =X | fff | f0000 | X | 0000fff | f X | | 000 | 00000 | | =X $=$ | fffffff | ₹ X | ffff800 | • X | 8000000 | • X | ffff | 8000 | =X $=$ | 0001fff | (| | 0000000 |
| • 📑 mem_din[31:0] | bf800000 | | | | | | 000 | 00000 | | | | | $\overline{}$ | | bf80 | 00000 | | $=$ \times | | | | | 00000 | 000 | | | | | | bf8 |
| - 📆 mem_dout[31:0] | 00000000 | \ | 000ffff | $=$ \times | | | | fff | fffff | | | \rightarrow | | | 0000 | 00000 | | N.C.I.O. | \rightarrow X | fffffff | | ffff800 | | 8000 | 0000 | $=$ \times | ffff800 | (1 | | 0000000 |
| ାଳ wb_rst | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| l | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | - |
| ା _ଲ wb_wen_wb | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| regw_addr_wb[4:0] | 00 | \propto | 09 | $=\chi$ | | 0a | =X | | 06 | =X $=$ | 08 | -x | 07 | | \times | | 00 | | \perp X | 05 | -x | | | | | 08 | | | | X |
| regw_data_wb[31:0] | 00000000 | | fffffff | $=$ χ | 00 | 00fffi | X | fff | fffff | $=$ \times | ffff000 | • X | 0000ff | î e | X | | 00000000 |) | $\perp \times$ | fffffff | 1 (| ffff800 | • X | 8000 | 0000 | | ffff800 | 10 (| 0001fff | X |
| regfile[1:31,31:0] | [00000000] | [000000 | 00, 00000 | 0258, X | XXXXXXXX | x, 0000 | 0060, 00 | 000000 |), fffff: | f \([0 | 0000000,0 | 0000258, | XXXXXXXX, | 00000 | 060, 000000 | 00, ff | efffff, O | 000ffff, | ff)([| 00000000, 0 | 000 ([| 00000000, 0 | 000 | [0000000 | 0, 0000 | 0 \([0 | 0000000, 0 | 000 | [00000000, 0 | 0000258, XXXXXXX |
| [1,31:0] | 00000000 | | | | | | | | | | | | | | | | | 000 | 00000 | | | | | | | | | | | |
| 5 [2,31:0] | 00000258 | | | | | | | | | | | | | | | | | 000 | 00258 | | | | | | | | | | | |
| [3,31:0] | XXXXXXXX | | | | | | | | | | | | | | | | | XX | OCXXXX | | | | | | | | | | | |
| [4,31:0] | 00000060 | | | | | | | | | | | | | | | | | 000 | 00060 | | | | | | | | | | | |
| [5,31:0] | ffffffff | | | | | | | | | | 00000000 | | | | | | | | X | | | | | | | | fffffff | | | |
| > 5 [6,31:0] | ffffffff | | | | | | | | | | | | | | | | | ff | ffffff | | | | | | | | | | | |
| > [7,31:0] | 0000ffff | | | | | | | | | | | | | | | | | 000 | Offff | | | | | | | | | | | |
| 5 [8,31:0] | 0001ffff | | | | 0000 | aaaa | | | | X | | | | | fff | 0000 | | | | | \square X | ffff800 | ΦX | 8000 | 0000 | =X $=$ | ffff800 | (| | 0001fff: |
| [9,31:0] | ffffffff | | | | | | | | | | | | | | | | | ff: | fffff | | | | | | | | | | | |
| IN-12 011 IIII ■ | nnnnffff | | | | | | | | | | | | | | | | | 000 | Offff | | | | | | | | | | | |



Checkpoints



• CP 1:

Waveform Simulation of the Pipelined CPU with the verification program

• CP 2:

FPGA Implementation of the Pipelined CPU with the verification program





Thanks!

