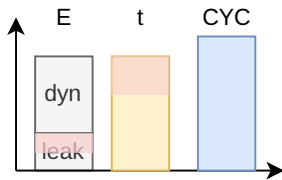
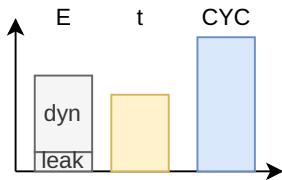


$$t = \frac{\text{CYC}}{f} \Rightarrow E_{\text{total}} = \underbrace{\alpha \cdot C \cdot \text{CYC} \cdot V^2}_{P_{\text{dyn}}} + \underbrace{V \cdot I_{\text{leak}} \cdot N \cdot k_{\text{design}} \cdot \frac{\text{CYC}}{f}}_{P_{\text{leak}}}$$

80 MHz

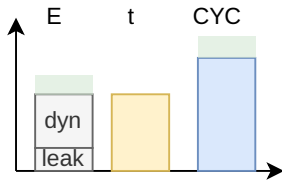
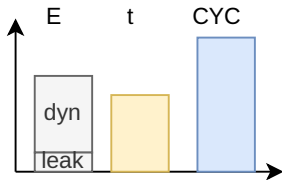
53 MHz

Scalable



Register/ RAM
intensive workloads

Bottleneck



Slow peripherals, I/O,
asynchronous
interactions