

(Due date: November 11th @ 7:30 pm)

PROBLEM 1 (100 PTS)

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- The diagram illustrates the proposed 3D CNN architecture. It features three parallel processing paths for input data IA and E . Each path consists of a DQ block, a LUT block (with functions $f(x) = x^{0.8}$, $g(x) = x^{0.49}$, and $h(x) = x^{0.23}$), and another DQ block. The outputs are OA , OB , and OC . A feedback path is also shown at the bottom.

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- Diagram illustrating the structure of a 3x3 matrix (likely representing a layer in a neural network) with 12 bits of precision. The matrix is divided into three horizontal sections, each representing a different function $f(x)$, $g(x)$, and $h(x)$.
- The top section is labeled $f(x) = x^{0.8}$ and contains 256 values, ranging from $f(0)$ to $f(255/128)$.
 - The middle section is labeled $g(x) = x^{0.49}$ and contains 256 values, ranging from $g(0)$ to $g(255/128)$.
 - The bottom section is labeled $h(x) = x^{0.23}$ and contains 256 values, ranging from $h(0)$ to $h(255/128)$.
- The total width of the matrix is 12 bits.

- Create a testbench to test your circuit. The testbench must generate all the possible input cases (from 00000000 to 11111111) and write the output results in a text file. For simplicity's sake, it is suggested that you write three 12-bit words per line (256 lines), where each 12-bit word represents the output of a different function.
- To verify the correct operation of your circuit, compare the text file you are generating on the Simulation with the input text file you created for Synthesis.
- Attach a printout of your i) VHDL code, ii) VHDL testbench, and iii) input and output text files.