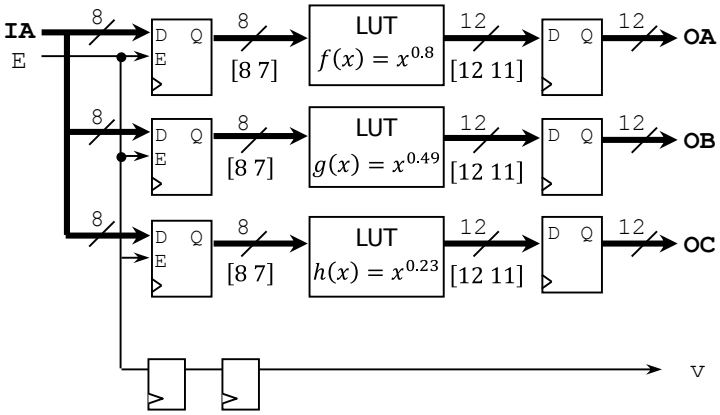
Homework 3

(Due date: November 11th @ 7:30 pm)

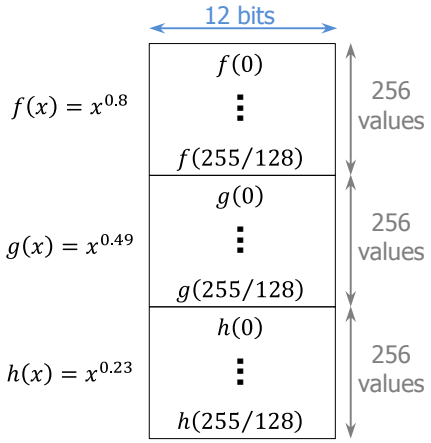
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (100 PTS)

- Implement the following circuit using the LUT approach.
  - ✓ Input format: [8 7]
  - ✓ Output format: [12 11]



- Pre-compute the LUT values and store them as binary numbers in a text file. Your VHDL code should read the text file.
- The text file should be divided as follows: the first 256 entries for the first function, the second 256 entries for the second function, and the third 256 entries for the third function:



SIMULATION

- Create a testbench to test your circuit. The testbench must generate all the possible input cases (from 00000000 to 11111111) and write the output results in a text file. For simplicity's sake, it is suggested that you write three 12-bit words per line (256 lines), where each 12-bit word represents the output of a different function.
- To verify the correct operation of your circuit, compare the text file you are generating on the Simulation with the input text file you created for Synthesis.
- Attach a printout of your i) VHDL code, ii) VHDL testbench, and iii) input and output text files.