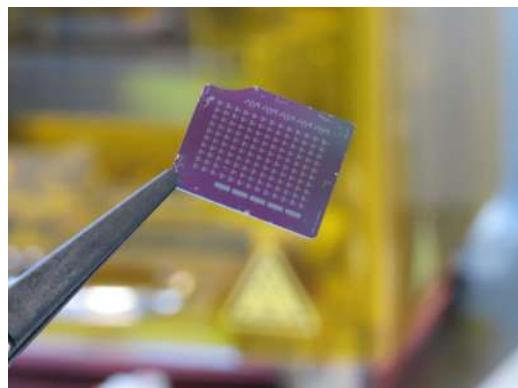




ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

MICROFABRICATION OF FILM BULK-ACOUSTIC WAVE RESONATORS FOR RF FILTERS



EPFL SEMESTER PROJECT

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December 10, 2025

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1 Introduction

1.1 CONTEXT

Since the advent of radio communications, there has been a growing base of devices using this technology, which led to more and more bandwidth usage and larger frequency allocations to avoid interferences. This implies that filters are needed to be able to select specific bands of frequencies to allow communication over the desired range. With the emergence of microfabrication and the demand for smaller and more compact electronic devices, components such as filters needed to adapt to those new scales. In particular for cell phones, which all throughout the years gained in complexity, needing ever more communication channels and bandwidth to respond to higher data rates and multiple communication protocols such as WiFi, Bluetooth or NFC just to name a few.

Acoustic Wave Resonator appeared as a solution for the design of smaller radio wave filters. They are a good candidate because of their capacity to be manufactured at the micro-scale and the fact that they can be embedded into semiconductor technology.

There exist different types of such resonators which are separated into two main categories: surface acoustic wave (SAW) and bulk acoustic wave (BAW) resonators.

1.2 PROJECT SCOPE

This project is aimed to investigate the effect of the top metal thickness of the electrodes on lithium niobate resonators.

The objective of the project are the followings

- Learn to use the various pieces of equipment relevant to the project at the CMi
- Manufacture the acoustic wave resonators according to the process flow
- Perform a back etching to create the membrane
- Assess the frequency response and the quality factor of the resonators

2 Clean room trainings & equipment

The clean room is accessible from 7am to 7pm from Monday to Friday. Getting access to the clean room requires a training given in two parts; an introduction course about safety and behaviour followed by a visit of the cleanroom and facilities. It takes place twice a month and takes around 2h30 [1].

On top of that, each machine/equipment in the facility requires its own separate instruction. Training request can be made on the CMi site only after a processflow, describing the different operations of the project, has been validated by the CMi staff.

This project requires a total of 8 different machines. For a new CMi user, as I was, a lot of trainings are required before being autonomous in the lab. Trainings aren't always available and, in general, they can be scheduled as soon as 4 working days after the training request. Trainings also require you to bring your own sample which means you need to book them in the order of the process flow. Moreover, machines may need maintenance or might be busy for multiple days. All these factors combined can significantly delay the work flow, thus future new users must be proactive and book trainings as soon as possible, even considering trainings before the start of the semester if possible.

2.1 LIST OF PERSONAL EQUIPMENT

The CMi provides free uniforms for all users. Safety glasses as well as card holders are available to borrow in the anteroom, the latter being less often available. Here is a list of the material given by my supervisor:

- 2 chips made of high resistive silicon with a layer of lithium niobate on top
- a dummy wafer
- a black box for the chips
- a transparent box for the dummy wafer
- a notebook with a pen

Additionally, I ordered some extra equipment:

- a pair of tweezers with plastic tip for delicate manipulations of the chip
- a card holder for the camipro

3 Manufacturing

The full wafer with 400nm Lithium niobate has already been processed prior to the project, and then diced into 14mmx17mm chips. The chips are ready to be processed with Pt alignment marks on top.

The resonators will be made of aluminum with a very thin bottom layer of chromium for adhesion on the niobate substrate of the chip and a top layer of chromium to protect the aluminum during niobate etching.

The final desired layout is presented below in figure 3.1.

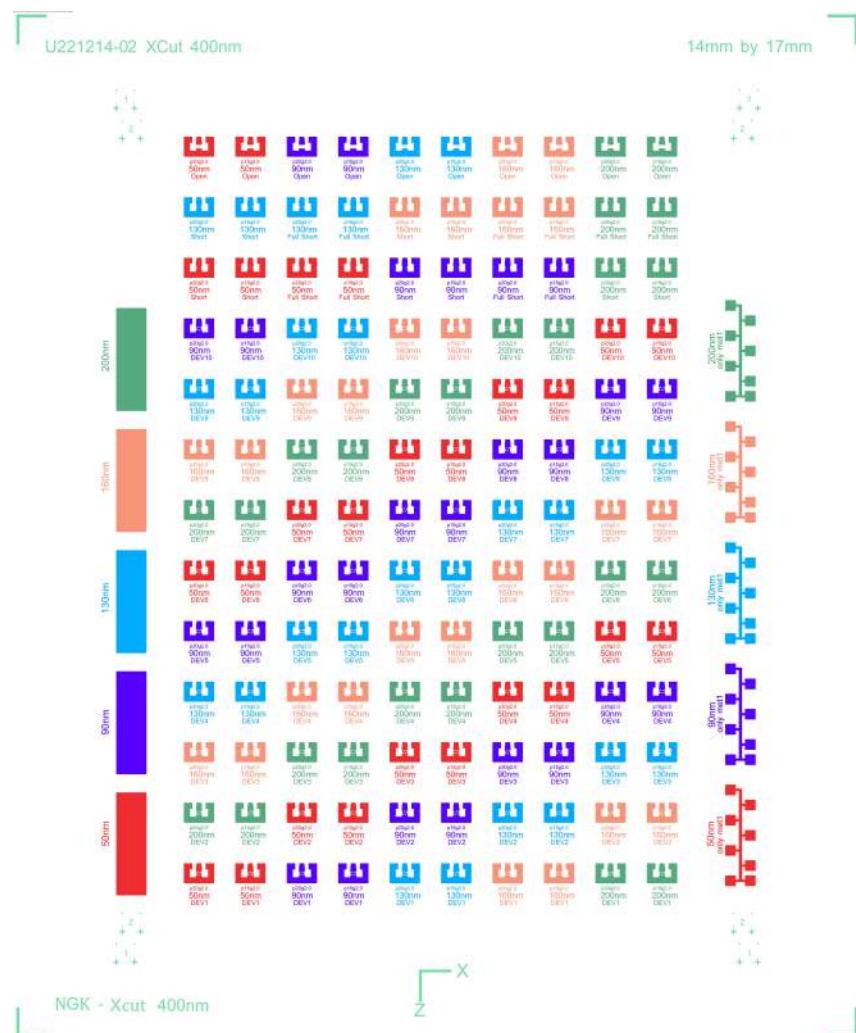


FIGURE 3.1
Final layout containing resonators of 5 different thicknesses

3.1 PROCESS FLOW

Figure 3.2 depicts the different steps needed for the whole fabrication of the front side of the device.

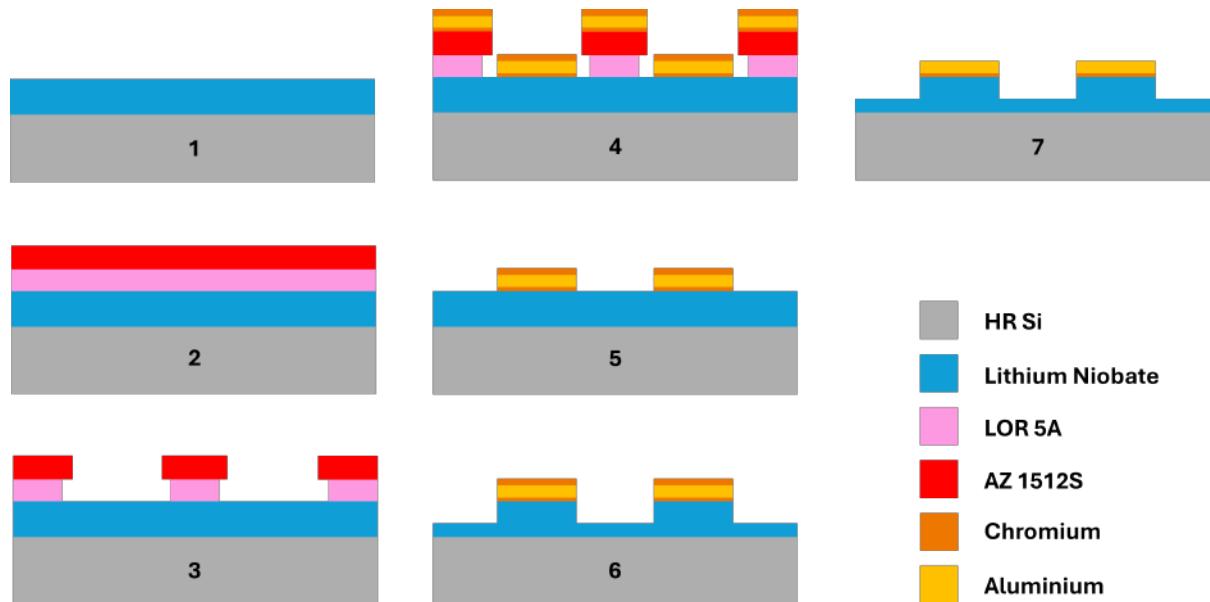


FIGURE 3.2
Process flow

Here is a summary of the process flow:

1. HR Si substrate with 400nm Lithium Niobate
2. Photoresist coating (LOR5A+AZ1512)
3. Laser exposure and development
4. Metal deposition Cr/Al/Cr
5. Lift-off
6. Lithium Niobate etching
7. Chromium etching (done in two steps)

The exact process flow can be found in the annex.

Next, the different steps are presented in more detail.

3.2 PHOTOLITHOGRAPHY

The goal of the photolithography is to create a pattern inside a positive photoresist for the metal to be deposited inside the developed regions.

3.2.1 RESIST COATING

Zone: 13

Machine: Sawatec SM-200 for photoresists[2]

Two photoresists are deposited on top each other. First, a layer of LOR 5A followed by a layer of AZ1512S. This allows for a double layer lift-off. After illumination, the bottom layer (LOR 5A) can be under-etched by the photoresist developer (step 3 in figure 3.2), which will facilitate the lift-off process, while the top layer ensures a higher pattern resolution during the metal evaporation. Detailed information on those photoresists is provided on the CMi's website [3].

The coating of the chip is done using a Sawatec SM-200 for photoresists. The bench used for this step is equipped with an HMDS hotplate, two hotplates, and the Sawatec coater. HMDS is a primer used for

enhancing the adhesion of the photoresist onto the chip, but, in our case, it will not be needed. A simple dehydration is enough to improve adhesion. The detailed procedure is the following:

1. Deposit the chip onto the HMDS hotplate for dehydartion during 10 minutes. As previously said, we won't be applying the HMDS, we just use the heat of the plate. During this time, choose the appropriate chuck (the chip needs to cover the whole chuck) and place it in the middle hole of the coater.
2. Once dehydrated, carefully place the chip on top of the chuck and make sure that it is centered. Activate the vacuum pump and slightly touch the chip to ensure proper fixation. The pressure gauge should indicate close to -0.8 bar.
3. Add LOR 5A using a pipette such that the whole chip is covered with photoresist. Use the pipette delicately as a brush to spread it across the entire surface and make sure the edges are properly covered. If this is not the case, the resist will form defects during curing, which will affect the next steps of the process. Choose the CHIP 6000 RPM program and press start.
4. When the coater has finished spinning, the lid will automatically open. Transfer the chip immediately onto a hotplate and let the LOR 5A cure at 180°C for 4'10".
5. Repeat steps 2 and 3 but this time using the AZ 1512 with the CHIP 5000 RPM program.
6. When the program has finished, bake the the chip onto a hotplate at 100°C for 1'30".

After the process is completed make sure to clean the bench, especially the spinning disk of the coater with the chuck, and logout. The RPM speeds are set to obtain a thickness of 0.4 μm for LOR 5A and 1.1 μm for AZ 1512. The values are derived from the website's charts, shown here in figure

The software interface of the Sawatec SM-200 is relatively straight forward. A stylus is available for easier navigation in the menu. If needed, further information is available on the machine's webpage [2].

3.2.2 EXPOSURE

Zone: 16

Machine: Heidelberg Instruments MLA150[4]

Once the chip has been coated with both photoresists, it is ready for photolithography. The machine used for this step is the Heidelberg MLA. MLA stands for Mask Less Aligner, which means that it allows to expose a design without a mask. It can convert CAD layouts, do alignements, and expose the layout onto the substrate.

Figure 3.1 shows the GDS file for the desired layout. The layout is made of 5 layers, shown as 5 different colors, one for each thickness (50/90/130/160/200 nm). Every layer contains 10 resonators with 4 cantilevers of 20 μm wide, 10 resonators with 6 cantilevers of 14 μm wide, 6 dummy resonators and a resistance test circuit. Only one layer is exposed at a time before metal evaporation, thus "4.2 photolithography" and "4.3 metal deposition" steps will be repeated for each layer.

To use the machine, one needs to load a file (for pexposure), give coordinates for reference marks, setup the laser wavelength and power ($\lambda = 405\text{nm}$ & $P = 100\%$), and then load the chip onto the receptacle inside the machine's chamber. Like for coating, the chip is held in place by a vacuum pump. When activated, make sure the chip is properly fixed by slightly touching it with the tweezers, then close the window of the chamber.

For an easier alignment, the chip should be placed as straight as possible with respect to the XY axis. Centering and alignement is then performed through the software. As a final step, specify the dose and the defocus, in our case we use a dose of 50 mJ/cm^2 and a defocus equal to 0.

3.2.3 DEVELOPMENT

Zone: 13

Machine: Arias Base wet bench[5]

Then, the chip is going to be soaked in the AZ 726 MIF developer for 60', which is the recommended developer for our photoresists. Rinse the chip immediately afterward in a beaker filled with deionized water, then dry it using the airgun. Be sure to leave the bench clean. After the development, features are visible under the microscope; see figure 3.3.

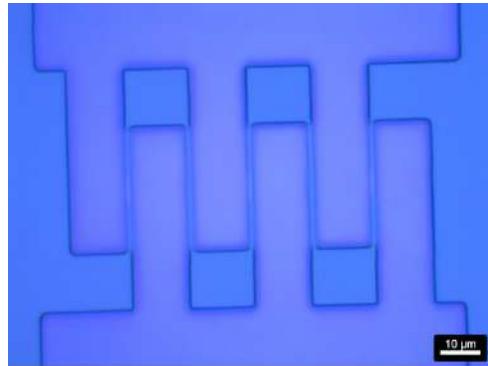


FIGURE 3.3
resonator cavity after photolithography, 100 x Zoom

3.2.4 DESCUM

Zone: 01 or 11

Machine: Tepla GigaBatch[6] or Tepla 300[7]

The chip is now almost ready for metal evaporation. In order to remove residual photoresist that did not properly dissolve during the development, a descum is required inside a plasma chamber. A low intensity program with O₂ is chosen, see table 3.1 for program parameters using the Tepla 300. This will ensure proper metal adhesion.

Program	Gas 1 (O ₂ , ml/min)	Gas 2 (CF ₄ , ml/min)	Power (W)	Time (mm:ss)	EPD (0, 1, 2)
45	400	0	200	00:10	

TABLE 3.1
Descum program

3.3 METAL DEPOSITION

3.3.1 METAL EVAPORATION

Zone: 06

Machine: Bühler Alzenau LTE 700 – Long Throw Evaporator (SYRUSpro 700LT)[8]

The equipment used for metal evaporation is the SyrusPro 700 LT Evaporator from Bühler. It consists of a chamber with a substrate holder mounted on top and the material crucibles on the bottom. The substrate holder can hold up to 6 wafers. The material is evaporated by heating up the crucible in which it is placed by electron beam. The throw distance is 1330 mm.

The chips need to be mounted on the dummy wafer using kapton tape. Four kapton tape discs are used to hold a chip from the corners with the lithium niobate side facing up. Here are the steps when using the SyrusPro:

1. The machine is always left under vacuum when not in use, thus **venting the room** is required before being able to open the door. This process takes 15 minutes.
2. In the meantime, **load the desired recipe**, Cr/Al/Cr in our case. The thickness of the first and last Chromium layers are always 5nm and 50nm respectively. The thickness of Aluminum depends on which layer from the layout we are building.
3. Once the chamber's pressure is back to atmospheric pressure, the door will automatically unlock. Contact the responsible of the machine if something looks unusual inside the chamber. **Place the dummy wafer with the chip taped inside the holder**. Use the step ladder if needed.
4. Only one crucible is visible at a time. The machine allows the user to rotate them by selecting the number of the desired crucible on the machine's interface and by pressing the *Crucible* button. **Enter the numbers corresponding to Cr & Al, verify that it is the correct material and that there is enough of it**. When making a reservation for the evaporator on the CMi's website, one can see which crucible corresponds to a given material. Also, Cr can easily be distinguished with its crystalline like surface.
5. Control that the rubber ring sealing the door is clean, then lock the door. Click on the blue *Release Evacuation* button and **start the program** from the interface. The machine will start by pumping the pressure down; you must remain next to the machine until the cryogenic pump is running. When a pressure of around 10^{-6} mbar is reached, actual metal evaporation will begin. The measured rate and deposited thickness can be viewed on the machine's interface.
6. At the end of the process, the tool will remain under vacuum in idle mode. Vent the tool like in step 1.
7. Retrieve the wafer and pump the chamber down if no user follows you. Make sure the cryogenic pump is running before leaving.

Detailed information for the interface software can be found online [8]. The chip should now be completely covered with metal and have a shiny appearance, see figure 3.4.

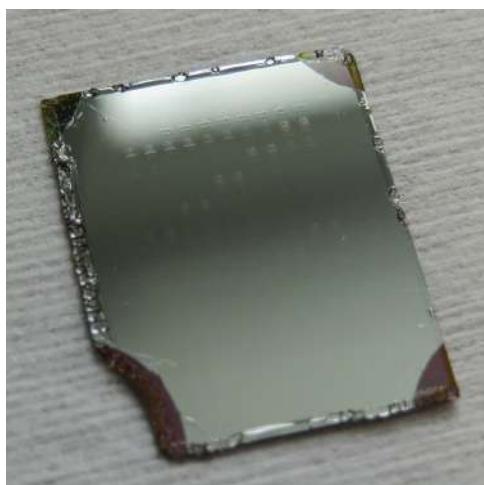


FIGURE 3.4
Chip after metal evaporation

3.3.2 LIFT-OFF

Zone: 12

Machine: Arias Lift-off[9]

The chip will then be immersed in a solution for lift-off. The solution used is the 1165. The chip needs to soak into the solution overnight or, in order to accelerate the process, can be soaked for 2-3 hours with the beaker placed inside a bain-marie for heating. The lift-off can be finished with an ultrasonic agitation for 5 minutes for a better dissolution. Dispose solvent waste in appropriate bottle, rinse the beakers and tools used on the bench.

After lift-off, the features should clearly be visible under an optical microscope; see figure 3.5. I scanned the surface for potential defects and zoomed where the cantilevers are since the gaps in between them represent the finer structures of the chip, thus being the most critical. As mentioned above, the microfabrication steps presented in Sections 4.2 and 4.3 describe how to create one layer (representing one thickness) of the final layout. Thus, those steps must be repeated for each layer/thickness. Here's a quick summary of the procedure:



FIGURE 3.5
Both resonator types after lift-off, 50 nm thick

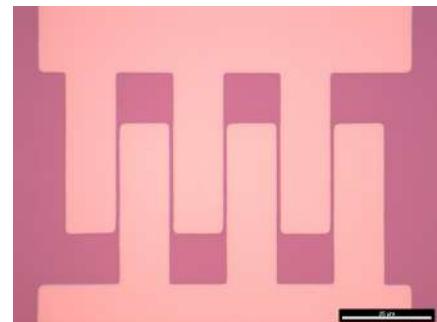


FIGURE 3.6
Zoomed picture of the cantilevers

3.4 ETTCHING

When the final metal deposition layer was done, towards the end of the semester, the SPTS APS, the machine for the Niobate etching, was under maintenance and overbooked when it was occasionally operational until the end of the semester. Thus, etching of lithium niobate and chromium was not performed. Nevertheless, I was trained on the Veeco IBE and the Wet Bench Acid for Cr etching using the dummy wafer. Here are the machines for the remaining steps:

Lithium Niobate etching

Zone: 02

Machine: SPTS APS[10]

Chromium etching

Zone: 11

Machine: Veeco IBE[11]

Chromium etching

Zone: 14

Machine: Wet Bench Acid[12]

3.5 TROUBLES

Although the machine instructions are very clear, I was not spared from problems during fabrication. The first problem I encountered was with photoresist coating. LOR5A was not curing properly and created large bubbles near the edges; see figure 3.7. The reason was because I was not covering the edges properly with the resist. Because of surface tension, the liquid cannot easily reach the edges. Spreading it with the pipette is required to ensure full surface coverage.



FIGURE 3.7
Defects near edges due to poor coverage from the resist

My next issue was damaging the chips. Being really thin, they are also very fragile. A slight pressure perpendicular to the substrate's surface can easily shatter them. It happened to me when I was removing kapton tape from the chips and when I used unappropriate tweezers for manipulations. One of the chips completely broke quite early in the process.

Finally, some of the early resonators contain defects. Metal has been deposited in undesired locations or hasn't deposited at all. The resonators of the second layer (90nm), have the most defects. In the following layers I was more cautious not to contaminate the surface and used the airgun to clean it before PR coating. I also cleaned the back of the chip before photolithography to be sure the whole surface is on the same level.



FIGURE 3.8
Poor metal deposition due to resist defects

3.6 FINAL RESULT

The resulting chip with the full layout is shown in figure 3.9. As can be seen, some edges have been damaged and the surface near the borders is scraped and contains traces of metal deposited in undesired regions. Fortunately, the central part containing the resonators is in very good condition and will probably be functional.



FIGURE 3.9
chip with the full layout

4 Conclusion

It was originally planned that after the process flow was completed, my supervisor would do the back-etching so that I could then test the resonators. Due to technical issues with the SPTS APS machine in the cleanroom, it was not possible to perform the etching. Nevertheless, I managed to obtain all five different thicknesses onto the chip with the majority of resonators being in good condition. In addition, creating the layout on the chip is the most tedious and time-consuming part of the project.

This project was a great introduction to the world of microfabrication. I had the opportunity to learn how to use multiple machines and pieces of equipment. I got familiar with the cleanroom environment and met people working on interesting projects. As a Microengineering student, I feel this was compulsory to complete my education with a practical application.

I want to thank:

- Seniz Esra Küçük and Florian Fernand Hartmann for their guidance, availability throughout the semester, passion for the subject and their kindness.
- Professor Guillermo Villanueva for his assistance and for proposing me a project which really matched my expectations.
- All the professional and supportive CMi staff who trained me and helped me in the lab.

A Process flow document

Metal thickness study

Description of the fabrication project

This project is aimed to investigate the effect of the top metal thickness of the electrodes on lithium niobate resonators. The main evaporation step will be carried out on new long-throw evaporator (SYRUSpro 700LT) which showed very promising electrical properties on our early investigations in our group.

Technologies used <i>!! remove non-used !!</i>																			
Evaporation, positive resist, Lift-off, Dry etching, Wet Etching, Four Point Measurement, SEM																			
Ebeam litho data - Photolitho masks - Laser direct write data																			
<table border="1"><thead><tr><th>Mask #</th><th>Critical Dimension</th><th>Critical Alignment</th><th>Remarks</th></tr></thead><tbody><tr><td>1</td><td>10um</td><td>First Mask</td><td>Alignment marks (already done prior to project)</td></tr><tr><td>2</td><td>10 um</td><td>2um</td><td>Metal Electrodes</td></tr><tr><td></td><td></td><td></td><td></td></tr></tbody></table>				Mask #	Critical Dimension	Critical Alignment	Remarks	1	10um	First Mask	Alignment marks (already done prior to project)	2	10 um	2um	Metal Electrodes				
Mask #	Critical Dimension	Critical Alignment	Remarks																
1	10um	First Mask	Alignment marks (already done prior to project)																
2	10 um	2um	Metal Electrodes																
Substrate Type and size																			
High resistive Silicon <100>, 250um thick, 400nm Lithium Niobate on Top with Pt Alignmet marks																			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

No Yes => confirm involved materials with CMi staff

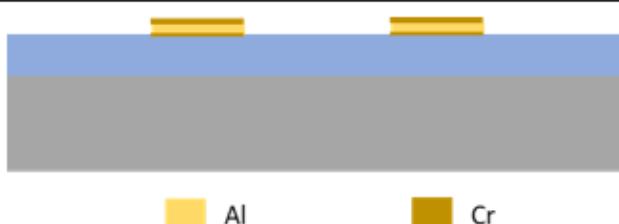
Dicing of the samples is required at some stage of the process.

No Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.

No Yes => confirm pads design (size, pitch) and involved materials with CMi staff

Step	Process description	Cross-section after process
01	Substrate (14mmx17mm Chip): <i>HR Si with 400nm Lithium Niobate</i>	
		The full wafer with 400nm Lithium niobate has already been processed prior to the project, and then diced. The chips are ready to be processed with Pt alignment marks on top. The alignment marks will not be drawn for the rest of the process flow for the sake of simplicity.
02	<i>Photolith LOR+PR coat</i> Machine: Z13 Manual Coater PR : LOR5A+AZ1512 Thickness : 400nm/1.2μm	
03	<i>Photolith expo+ develop</i> Machine: MLA + Z13 Developer Bench (double development) Mask : CD = 2μm <u>Align with Pt alignment marks</u> + short O2 plasma Descum (10s <u>Tepla</u> low – Z1)	 Legend: Lithium Niobate (blue), LOR5A (pink), 1512S (red)
	The chips will be mounted on a dummy wafer with kapton tapes at the corners after descum before the evaporation.	Below is the main step that will be investigated. The devices with different Al thickness will be fabricated (each thickness with a different lift-off). The thickness values for Cr/Al/Cr: 5nm/50nm/50nm, 5nm/75nm/50nm, 5nm/100nm/50nm, 5nm/125nm/50nm
04	<i>Metal1 Deposition</i> Material : Cr/Al/Cr (5nm/50nm/50nm) Machine: SYRUSpro 700LT (Top Cr layer will be later used as a hard mask in SPTS)	 Legend: Al (yellow), Cr (brown)

	The chips will be removed from the dummy wafer by removing the kapton tapes from the corners.	
05	<p><i>Lift-off</i></p> <p>Machine: Z12 Lift-off Bench Material: Remover1165 at 70C</p>	 <p style="text-align: center;">■ Al ■ Cr</p>
	The chips will be mounted on a dummy wafer with Quickstick before SPTS step.	
06	<p><i>Lithium Niobate Etching</i></p> <p>Machine: SPTS APS</p> <p>Recipe: <i>LiNbO₃_etching</i></p> <p>Time : 1min 30sec</p>	
07	<p><i>Cr Etching (Surface only)</i></p> <p>Machines: IBE</p> <p>Recipe: <i>Low_IBE</i></p> <p>Time: 15sec</p> <p>(This step is needed after SPTS before moving to the wet Cr etching, it only removes a few nm of Cr while leaving the rest for wet etching)</p>	
	The chips will be removed from the dummy wafer and the backside of the chips will be cleaned with acetone on a Q-tip.	

08	<p><i>Cr Etching</i> Machines: Z14 Acid Bench</p>	
09	<p><i>Film Resistance Tests</i> -Metal layers will also be coated on full wafers <u>in order</u> to examine the sheet resistance of each deposition. <i>Machine: R50 4PP Four Point Probe Measurements</i></p>	 <p>Full Wafer (Si test with SiO2) with Metal on Top</p>

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