## **CSCE 616 Lab 8**

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This lab was very straightforward. We built on the existing UVM structure to implement the RX Monitor and Scoreboard. The main difference between TX and RX monitors was that we waited for the vc\_gnt signal for the TX but we waited for a tx\_sot for the RX, which also means we had no business with dest\_port. The loop used to attach new data packets to the dynamic array associated with the RX monitor packet was almost identical to the one for TX.

For the scoreboard, we push to one of the four queues depending on the dest\_port of the tx\_mon\_pkt. We push to the front because for the RX side we pop from the back in order to compare with the reference model. The comparison happens in the write\_rx\_export functions which prints whether the data from the DUT matches the reference model. At the end of the simulation, we expected the sizes of all four queues to be zero to indicate that all data packets have been compared. But that is not enough to show that the entire simulation is correct, there also needs to be no UVM fatal errors, and a quick 'find' also shows that it never prints "Data mismatch..."

Figure 1. Scoreboard check with all queues empty

