

CSCE 616 Lab 2

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After filling in the modports in the interface file, we added three different types of stimuli. For all tests we used a scoreboard array that was written to any time we put a write request.

First, we did a brute force with a nested for loop to iterate through each memory address writing consecutive values (first 0-255 but reduced to 0-9 to keep output concise) and read immediately after within the same loop iteration.

Our second test was putting in 1000 write requests with random addresses and data followed by reading from each memory address in a separate loop to compare with the scoreboard, which only revealed 2/32 mismatches.

Finally, we did random regression over 100 iterations, reading first to access some address once, writing to the same random address with random data, and finally reading again to check with the scoreboard. The reason is that we found the bug in the write hit portion of the HDL design code, so the bug was revealed when a write request hits after any memory access to the same address consecutively.

Figure 1. Simulation with bug, Mismatch count: 474/552 cases

The screenshot displays a simulation environment with a terminal window on the left and a code editor on the right. The terminal window shows a list of read and write operations with their expected and actual values, indicating mismatches. The code editor shows the Verilog code for the cache memory, including a cache write hit condition that is commented out with a bug.

```
Read addr: 0, data: 36, expected: 124 Mismatch!  
Read addr: 14, data: 67, expected: 26 Mismatch!  
Write addr: 14, data: 187  
Read addr: 14, data: 67, expected: 187 Mismatch!  
Read addr: 10, data: 70, expected: 22 Mismatch!  
Write addr: 10, data: 183  
Read addr: 10, data: 70, expected: 183 Mismatch!  
Read addr: 25, data: 77, expected: 114 Mismatch!  
Write addr: 25, data: 7  
Read addr: 25, data: 77, expected: 7 Mismatch!  
Read addr: 6, data: 36, expected: 152 Mismatch!  
Write addr: 6, data: 40  
Read addr: 6, data: 36, expected: 40 Mismatch!  
Read addr: 29, data: 36, expected: 45 Mismatch!  
Write addr: 29, data: 165  
Read addr: 29, data: 36, expected: 165 Mismatch!  
Read addr: 9, data: 77, expected: 110 Mismatch!  
Write addr: 9, data: 231  
Read addr: 9, data: 77, expected: 231 Mismatch!  
Read addr: 13, data: 244, expected: 38 Mismatch!  
Write addr: 13, data: 218  
Read addr: 13, data: 244, expected: 218 Mismatch!  
Read addr: 3, data: 67, expected: 11 Mismatch!  
Write addr: 3, data: 70  
Read addr: 3, data: 67, expected: 70 Mismatch!  
Read addr: 23, data: 236 Mismatch!  
Write addr: 23, data: 233  
Read addr: 23, data: 70, expected: 233 Mismatch!  
Read addr: 2, data: 244, expected: 237 Mismatch!  
Write addr: 2, data: 87  
Read addr: 2, data: 244, expected: 87 Mismatch!  
Read addr: 6, data: 67, expected: 40 Mismatch!  
Write addr: 6, data: 144  
Read addr: 6, data: 67, expected: 144 Mismatch!  
Read addr: 14, data: 67, expected: 187 Mismatch!  
Write addr: 14, data: 100  
Read addr: 14, data: 67, expected: 100 Mismatch!  
Read addr: 2, data: 244, expected: 87 Mismatch!  
Write addr: 2, data: 136  
Read addr: 2, data: 244, expected: 136 Mismatch!  
Mismatches: 474  
Simulation complete via $finish(1) at time 40080 NS + 1  
..../tb/cache_mem_tb.sv:61 $finish;  
xceltums> exit  
T00L: xrun 22.03-s084: Exiting on Sep 12, 2022 at 11:44:32  
[acoskuner500]hera3 ~/csc616/lab2_cache_mem_tb/lab2/cache_mem  
::
```

Figure 2. Simulation with bug fixed. Mismatch count 0

The screenshot displays a simulation environment with a terminal window on the left and a code editor on the right. The terminal window shows a list of read and write operations with their expected and actual values, indicating no mismatches. The code editor shows the Verilog code for the cache memory, including a cache write hit condition that is commented out with a bug.

```
Read addr: 0, data: 124  
Read addr: 14, data: 26  
Write addr: 14, data: 187  
Read addr: 14, data: 187  
Read addr: 10, data: 22  
Write addr: 10, data: 183  
Read addr: 10, data: 183  
Read addr: 25, data: 114  
Write addr: 25, data: 7  
Read addr: 25, data: 7  
Read addr: 6, data: 152  
Write addr: 6, data: 40  
Read addr: 6, data: 40  
Read addr: 29, data: 45  
Write addr: 29, data: 165  
Read addr: 29, data: 165  
Read addr: 9, data: 110  
Write addr: 9, data: 231  
Read addr: 9, data: 231  
Read addr: 13, data: 38  
Write addr: 13, data: 218  
Read addr: 13, data: 218  
Read addr: 3, data: 11  
Write addr: 3, data: 70  
Read addr: 3, data: 70  
Read addr: 23, data: 236  
Write addr: 23, data: 233  
Read addr: 23, data: 233  
Read addr: 2, data: 237  
Write addr: 2, data: 87  
Read addr: 2, data: 87  
Read addr: 6, data: 40  
Write addr: 6, data: 144  
Read addr: 6, data: 144  
Read addr: 14, data: 187  
Write addr: 14, data: 100  
Read addr: 14, data: 100  
Read addr: 2, data: 87  
Write addr: 2, data: 136  
Read addr: 2, data: 136  
Mismatches: 0  
Simulation complete via $finish(1) at time 40080 NS + 1  
..../tb/cache_mem_tb.sv:61 $finish;  
xceltums> exit  
T00L: xrun 22.03-s084: Exiting on Sep 12, 2022 at 11:45:11  
[acoskuner500]hera3 ~/csc616/lab2_cache_mem_tb/lab2/cache_mem  
::
```