CSCE 616 Lab 7

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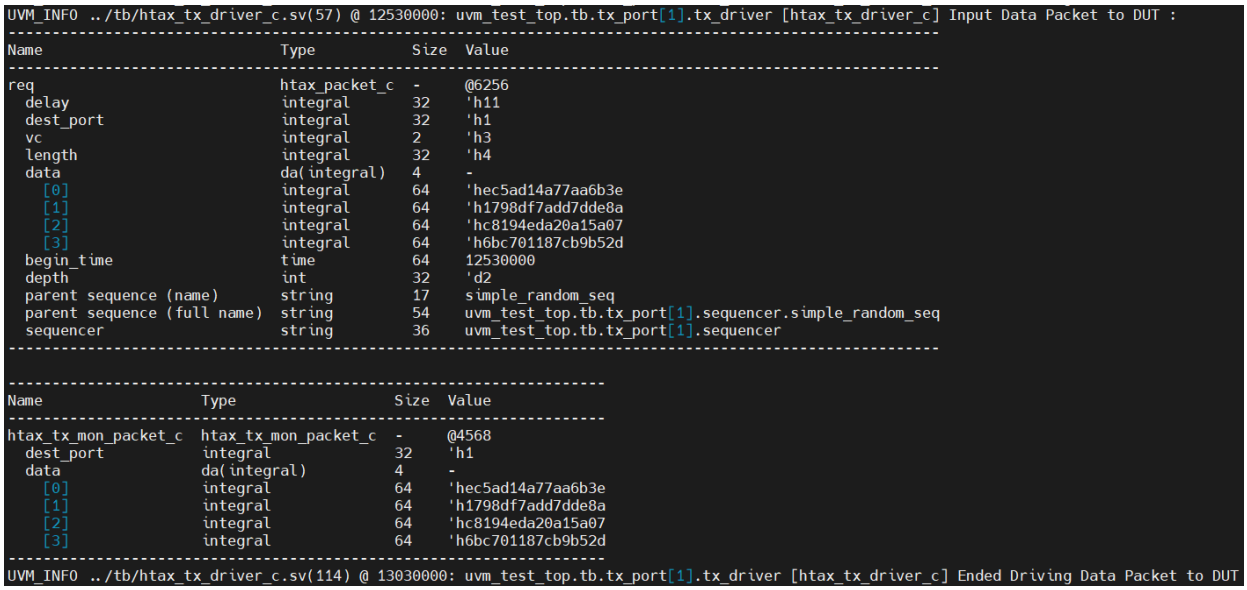
Driver

We left-shifted a 1 by as many times as pkt.dest_port and assigned that to outport_req and assigned vc_req with pkt.vc. We wait for a change on vc_gnt before continuing to assign tx_sot based on which channels are granted, as well as driving the first pkt.data[0] and resetting request signals to 0. Starting with the second data packet, we reset tx_sot and drive the pkt.data[i] to tx_data. We check if it is in the second to last or last packet to assert release_gnt and tx_eot accordingly. After all packets are sent, we reset tx_eot to 0 and tx_data to X.

Monitor

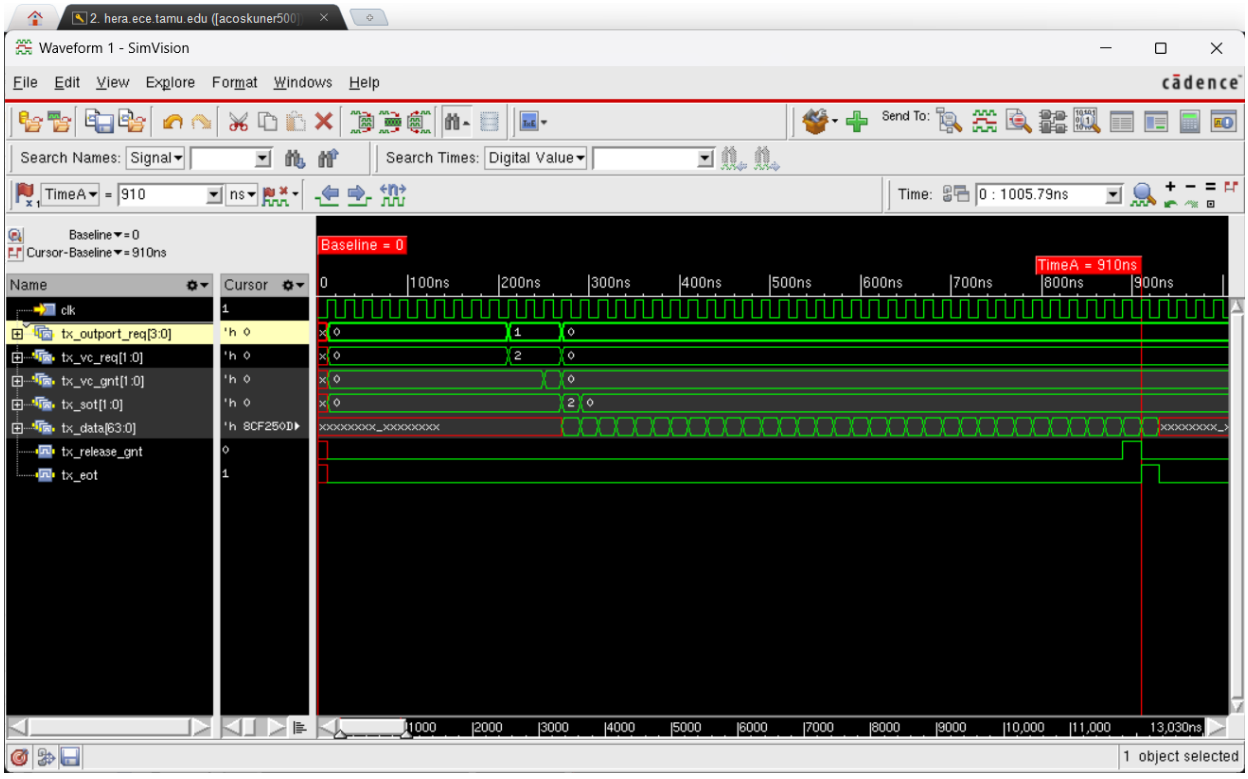
When a change is seen on vc_gnt, we use a case block to assign dest_port based on the value of outport_req. We wait a clock cycle and then begin a while loop which executes if tx_eot is low. In each iteration, we increase the size of the dynamic array with the pkt_len variable provided and concatenate the new value of tx_data to the old dynamic data array, and then wait a clock cycle. Once tx_eot goes high, the loop ends but we still need to append the last packet so we use the same code one more time.

We tried many things to get the condition right but this was the only thing that seemed to work. We tried SVA-style implications which caused syntax errors. We tried using a counter variable that was incremented if tx_eot was asserted and deasserted in consecutive cycles but that resulted in the last packet being cut off.



```
UVM_INFO ../tb/htax_tx_driver_c.sv(57) @ 12530000: uvm_test_top.tb.tx_port[1].tx_driver [htax_tx_driver_c] Input Data Packet to DUT :
----------------------------------------------------------------------------------------------------------------
Name                           Type           Size  Value
----------------------------------------------------------------------------------------------------------------
req                            htax_packet_c  -     @6256
  delay                        integral       32    'h11
  dest_port                    integral       32    'h1
  vc                           integral       2     'h3
  length                       integral       32    'h4
  data                         da(integral)   4     -
    [0]                        integral       64    'hec5ad14a77aa6b3e
    [1]                        integral       64    'h1798df7add7dde8a
    [2]                        integral       64    'hc8194eda20a15a07
    [3]                        integral       64    'h6bc701187cb9b52d
  begin_time                   time           64    12530000
  depth                        int            32    'd2
  parent sequence (name)       string         17    simple_random_seq
  parent sequence (full name)  string         54    uvm_test_top.tb.tx_port[1].sequencer.simple_random_seq
  sequencer                    string         36    uvm_test_top.tb.tx_port[1].sequencer
----------------------------------------------------------------------------------------------------------------

----------------------------------------------------------------
Name                  Type                  Size  Value
----------------------------------------------------------------
htax_tx_mon_packet_c  htax_tx_mon_packet_c  -     @4568
  dest_port           integral              32    'h1
  data                da(integral)          4     -
    [0]               integral              64    'hec5ad14a77aa6b3e
    [1]               integral              64    'h1798df7add7dde8a
    [2]               integral              64    'hc8194eda20a15a07
    [3]               integral              64    'h6bc701187cb9b52d
----------------------------------------------------------------
UVM_INFO ../tb/htax_tx_driver_c.sv(114) @ 13030000: uvm_test_top.tb.tx_port[1].tx_driver [htax_tx_driver_c] Ended Driving Data Packet to DUT
```


2. hera.ece.tamu.edu ([acoskuner500]
Waveform 1 - SimVision
File Edit View Explore Format Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Digital Value
TimeA = 910 ns
Time: 0 : 1005.79ns
Baseline = 0
Cursor-Baseline = 910ns
Name
Cursor
clk
tx_outport_req[3:0]
tx_vc_req[1:0]
tx_vc_gnt[1:0]
tx_sot[1:0]
tx_data[63:0]
tx_release_gnt
tx_eot
'h 8CF250D
Baseline = 0
TimeA = 910ns
0
100ns
200ns
300ns
400ns
500ns
600ns
700ns
800ns
900ns
1000
2000
3000
4000
5000
6000
7000
8000
9000
10,000
11,000
13,030ns
1 object selected