CSCE 616 Lab 10

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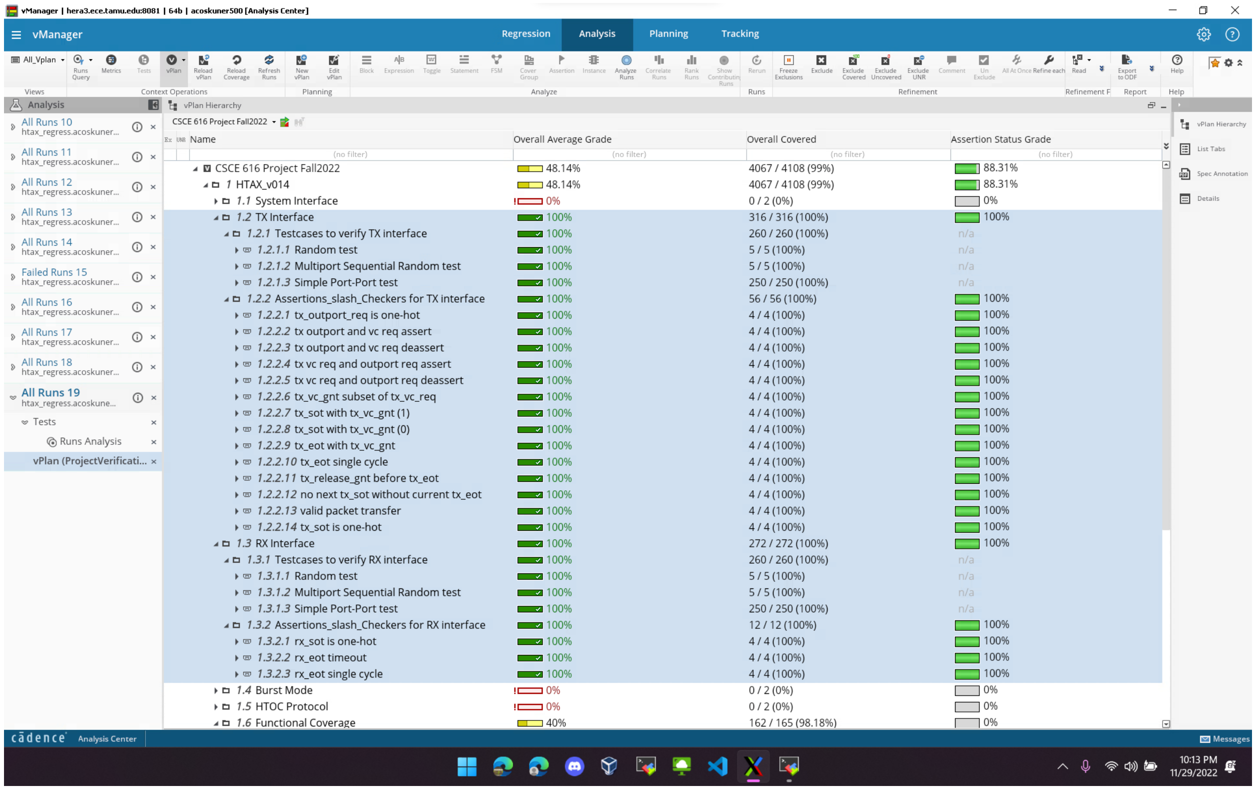
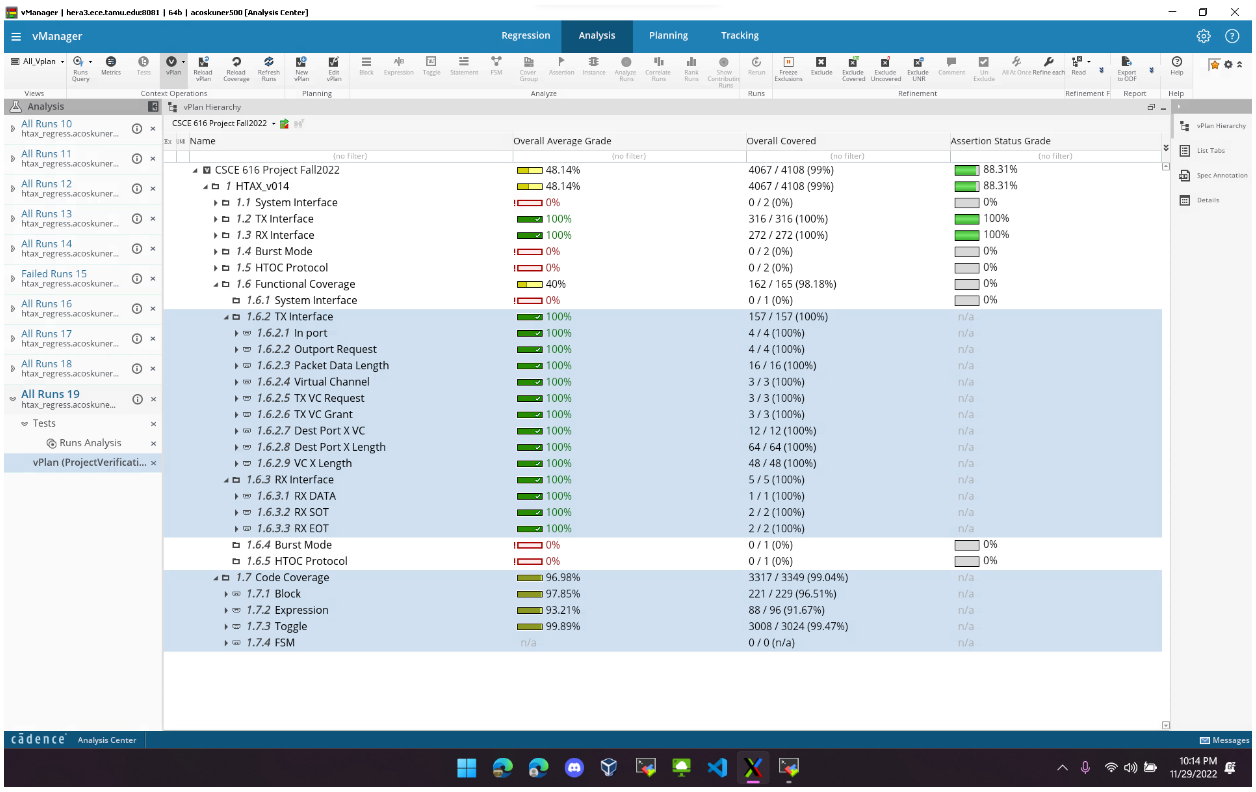
In order to find the bug, we utilized the hints provided by the instructors, namely constraining the length to less than 10 and the delay to less than 5 in our own new test file that we called Simple Port-Port test. We were also given a hint to create packets for each port in order to run the regressions in parallel. We increased the number of repetitions first 10, then 100, then 1000, then finally back down to 750. We also changed the number of regressions (test count in run_vm.vsif) to 250 to increase our chances of finding a failing test case or coverage hole. Another thing we experimented was the seed numbers, for which we used 616 and 11292022. As seen in Figure 6, the tests failed towards the end of the 260 tests. We spent most of our time trying to get full functional coverage.

Figure 1. Test cases and Assertions for TX and RX Interface all 100% passing



Name	Overall Average Grade	Overall Covered	Assertion Status Grade
(no filter)	(no filter)	(no filter)	(no filter)
CSCE 616 Project Fall2022	48.14%	4067 / 4108 (99%)	88.31%
1 HTAX_v014	48.14%	4067 / 4108 (99%)	88.31%
1.1 System Interface	0%	0 / 2 (0%)	0%
1.2 TX Interface	100%	316 / 316 (100%)	100%
1.2.1 Testcases to verify TX interface	100%	260 / 260 (100%)	n/a
1.2.1.1 Random test	100%	5 / 5 (100%)	n/a
1.2.1.2 Multiport Sequential Random test	100%	5 / 5 (100%)	n/a
1.2.1.3 Simple Port-Port test	100%	250 / 250 (100%)	n/a
1.2.2 Assertions_slash_Checkers for TX interface	100%	56 / 56 (100%)	100%
1.2.2.1 tx_outport_req is one-hot	100%	4 / 4 (100%)	100%
1.2.2.2 tx outport and vc req assert	100%	4 / 4 (100%)	100%
1.2.2.3 tx outport and vc req deassert	100%	4 / 4 (100%)	100%
1.2.2.4 tx vc req and outport req assert	100%	4 / 4 (100%)	100%
1.2.2.5 tx vc req and outport req deassert	100%	4 / 4 (100%)	100%
1.2.2.6 tx_vc_gnt subset of tx_vc_req	100%	4 / 4 (100%)	100%
1.2.2.7 tx_sot with tx_vc_gnt (1)	100%	4 / 4 (100%)	100%
1.2.2.8 tx_sot with tx_vc_gnt (0)	100%	4 / 4 (100%)	100%
1.2.2.9 tx_eot with tx_vc_gnt	100%	4 / 4 (100%)	100%
1.2.2.10 tx_eot single cycle	100%	4 / 4 (100%)	100%
1.2.2.11 tx_release_gnt before tx_eot	100%	4 / 4 (100%)	100%
1.2.2.12 no next tx_sot without current tx_eot	100%	4 / 4 (100%)	100%
1.2.2.13 valid packet transfer	100%	4 / 4 (100%)	100%
1.2.2.14 tx_sot is one-hot	100%	4 / 4 (100%)	100%
1.3 RX Interface	100%	272 / 272 (100%)	100%
1.3.1 Testcases to verify RX interface	100%	260 / 260 (100%)	n/a
1.3.1.1 Random test	100%	5 / 5 (100%)	n/a
1.3.1.2 Multiport Sequential Random test	100%	5 / 5 (100%)	n/a
1.3.1.3 Simple Port-Port test	100%	250 / 250 (100%)	n/a
1.3.2 Assertions_slash_Checkers for RX interface	100%	12 / 12 (100%)	100%
1.3.2.1 rx_sot is one-hot	100%	4 / 4 (100%)	100%
1.3.2.2 rx_eot timeout	100%	4 / 4 (100%)	100%
1.3.2.3 rx_eot single cycle	100%	4 / 4 (100%)	100%
1.4 Burst Mode	0%	0 / 2 (0%)	0%
1.5 HTOC Protocol	0%	0 / 2 (0%)	0%
1.6 Functional Coverage	40%	162 / 165 (98.18%)	0%

Figure 2. Functional and Code Coverage 100% closure



vManager | hera3.ece.tamu.edu:8081 | 64b | acoskuner500 [Analysis Center]

All Runs 10 — htax_regress.acoskuner...
All Runs 11 — htax_regress.acoskuner...
All Runs 12 — htax_regress.acoskuner...
All Runs 13 — htax_regress.acoskuner...
All Runs 14 — htax_regress.acoskuner...
Failed Runs 15 — htax_regress.acoskuner...
All Runs 16 — htax_regress.acoskuner...
All Runs 17 — htax_regress.acoskuner...
All Runs 18 — htax_regress.acoskuner...
All Runs 19 — htax_regress.acoskune...
Tests
Runs Analysis
vPlan (ProjectVerificati...

CSCE 616 Project Fall2022

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CSCE 616 Project Fall2022	48.14%	4067 / 4108 (99%)	88.31%
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1.2 TX Interface	100%	316 / 316 (100%)	100%
1.3 RX Interface	100%	272 / 272 (100%)	100%
1.4 Burst Mode	0%	0 / 2 (0%)	0%
1.5 HTOC Protocol	0%	0 / 2 (0%)	0%
1.6 Functional Coverage	40%	162 / 165 (98.18%)	0%
1.6.1 System Interface	0%	0 / 1 (0%)	0%
1.6.2 TX Interface	100%	157 / 157 (100%)	n/a
1.6.2.1 In port	100%	4 / 4 (100%)	n/a
1.6.2.2 Outport Request	100%	4 / 4 (100%)	n/a
1.6.2.3 Packet Data Length	100%	16 / 16 (100%)	n/a
1.6.2.4 Virtual Channel	100%	3 / 3 (100%)	n/a
1.6.2.5 TX VC Request	100%	3 / 3 (100%)	n/a
1.6.2.6 TX VC Grant	100%	3 / 3 (100%)	n/a
1.6.2.7 Dest Port X VC	100%	12 / 12 (100%)	n/a
1.6.2.8 Dest Port X Length	100%	64 / 64 (100%)	n/a
1.6.2.9 VC X Length	100%	48 / 48 (100%)	n/a
1.6.3 RX Interface	100%	5 / 5 (100%)	n/a
1.6.3.1 RX DATA	100%	1 / 1 (100%)	n/a
1.6.3.2 RX SOT	100%	2 / 2 (100%)	n/a
1.6.3.3 RX EOT	100%	2 / 2 (100%)	n/a
1.6.4 Burst Mode	0%	0 / 1 (0%)	0%
1.6.5 HTOC Protocol	0%	0 / 1 (0%)	0%
1.7 Code Coverage	96.98%	3317 / 3349 (99.04%)	n/a
1.7.1 Block	97.85%	221 / 229 (96.51%)	n/a
1.7.2 Expression	93.21%	88 / 96 (91.67%)	n/a
1.7.3 Toggle	99.89%	3008 / 3024 (99.47%)	n/a
1.7.4 FSM	n/a	0 / 0 (n/a)	n/a

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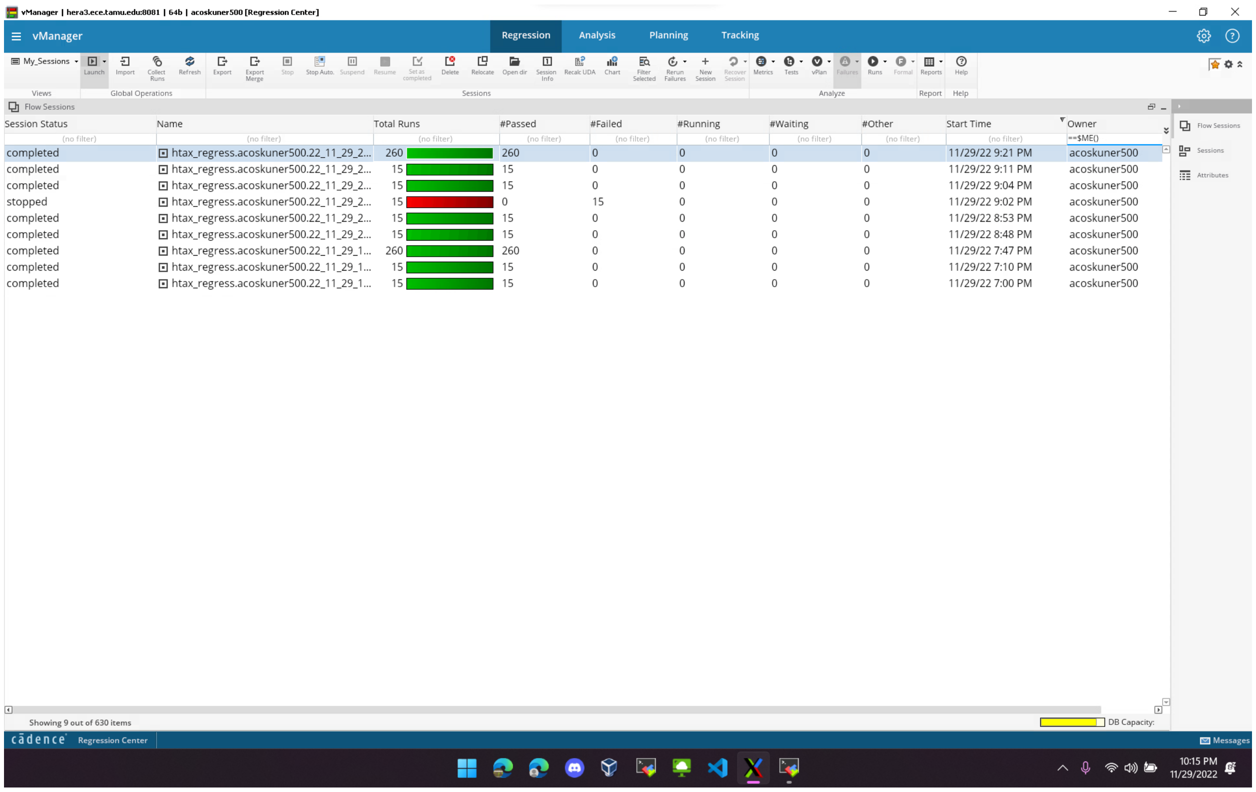
Figure 3. Regression tab with 260 test passing for debugged regression



vManager | hera3.ece.tamu.edu:8081 | 64b | acoskuner500 [Regression Center]

Flow Sessions

Session Status	Name	Total Runs	#Passed	#Failed	#Running	#Waiting	#Other	Start Time	Owner
completed	htax_regress.acoskuner500.22_11_29_2...	260	260	0	0	0	0	11/29/22 9:21 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_2...	15	15	0	0	0	0	11/29/22 9:11 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_2...	15	15	0	0	0	0	11/29/22 9:04 PM	acoskuner500
stopped	htax_regress.acoskuner500.22_11_29_2...	15	0	15	0	0	0	11/29/22 9:02 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_2...	15	15	0	0	0	0	11/29/22 8:53 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_2...	15	15	0	0	0	0	11/29/22 8:48 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_1...	260	260	0	0	0	0	11/29/22 7:47 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_1...	15	15	0	0	0	0	11/29/22 7:10 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_1...	15	15	0	0	0	0	11/29/22 7:00 PM	acoskuner500

Showing 9 out of 630 items

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Figure 4. Waveform of Debugged simulation

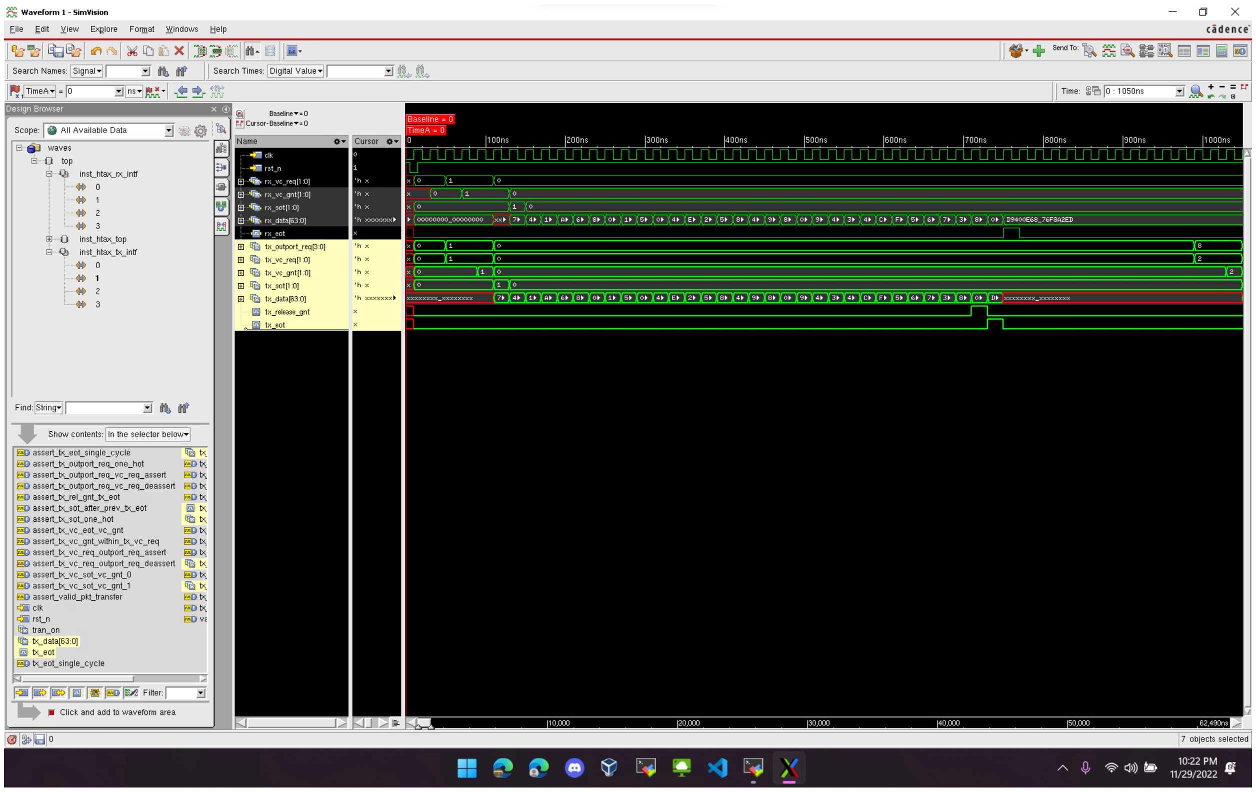
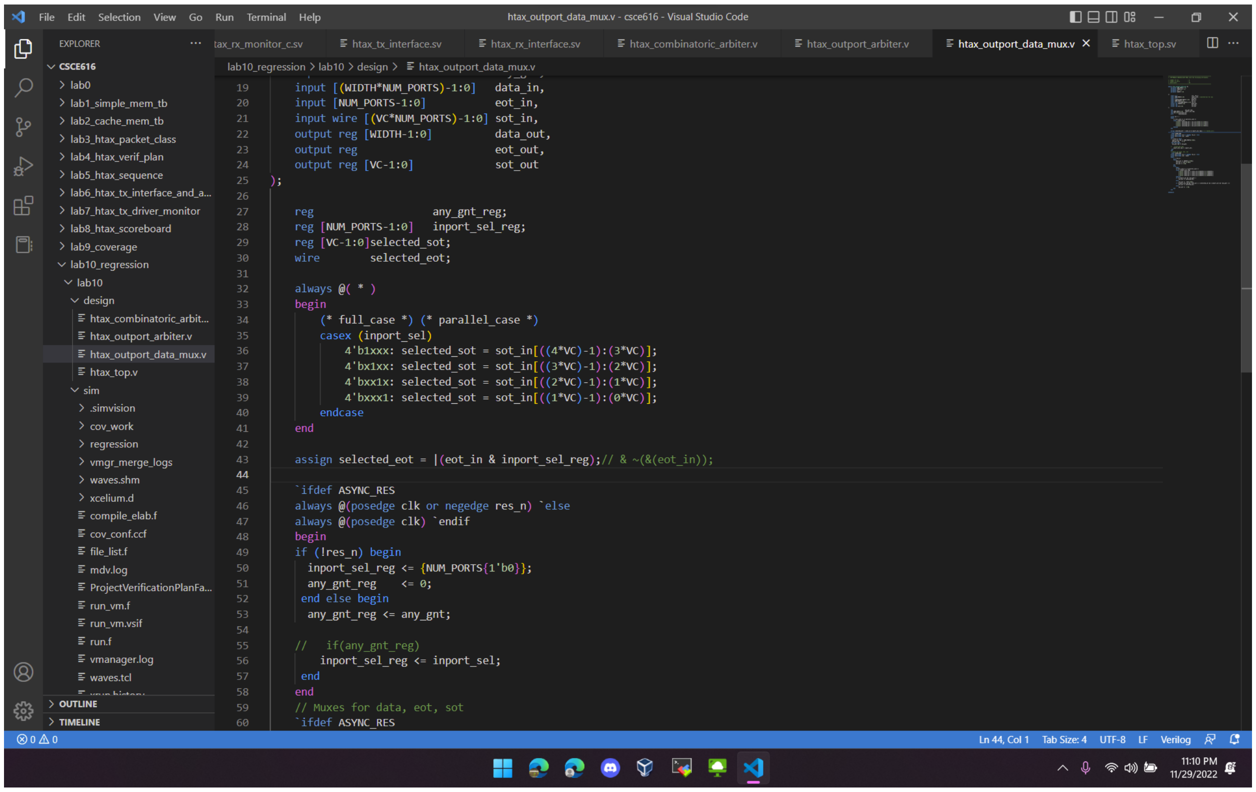
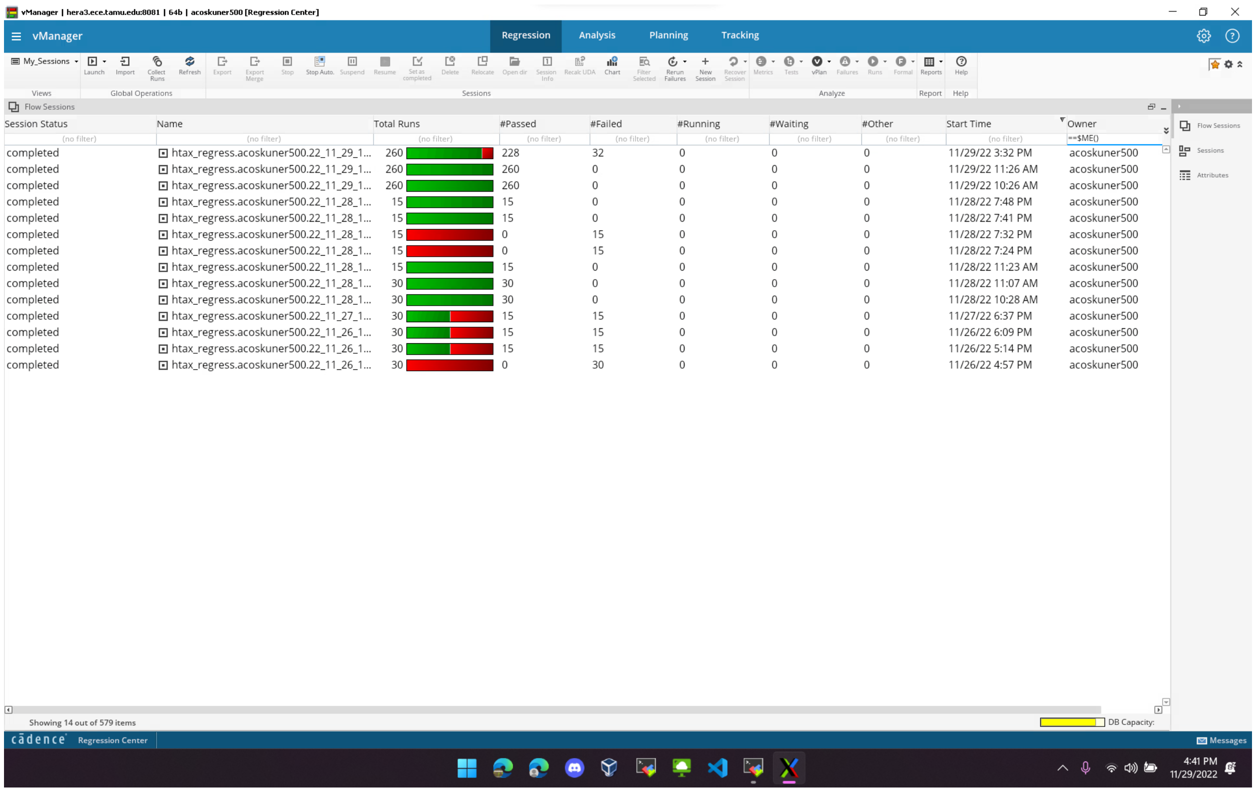

Waveform 1 - SimVision
Design Browser
Baseline = 0
TimeA = 0
clk
rst_n
rx_vc_req[1:0]
rx_vc_gnt[1:0]
rx_sot[1:0]
rx_data[63:0]
rx_eot
tx_outport_req[3:0]
tx_vc_req[1:0]
tx_vc_gnt[1:0]
tx_sot[1:0]
tx_data[63:0]
tx_release_gnt
tx_eot
assert_tx_eot_single_cycle
assert_tx_outport_req_one_hot
assert_tx_outport_req_vc_req_assert
assert_tx_outport_req_vc_req_deassert
assert_tx_rel_gnt_tx_eot
assert_tx_sot_after_prev_tx_eot
assert_tx_sot_one_hot
assert_tx_vc_eot_vc_gnt
assert_tx_vc_gnt_within_tx_vc_req
assert_tx_vc_req_outport_req_assert
assert_tx_vc_req_outport_req_deassert
assert_tx_vc_sot_vc_gnt_0
assert_tx_vc_sot_vc_gnt_1
assert_valid_pkt_transfer
Time: 0 : 1050ns
7 objects selected

Figure 5. Code with DUT bug commented out


htax_outport_data_mux.v - csce616 - Visual Studio Code
lab10_regression > lab10 > design > htax_outport_data_mux.v
Ln 44, Col 1   Tab Size: 4   UTF-8   LF   Verilog

```
    input [(WIDTH*NUM_PORTS)-1:0]   data_in,
    input [NUM_PORTS-1:0]           eot_in,
    input wire [(VC*NUM_PORTS)-1:0] sot_in,
    output reg [WIDTH-1:0]          data_out,
    output reg                      eot_out,
    output reg [VC-1:0]             sot_out
);

    reg                   any_gnt_reg;
    reg [NUM_PORTS-1:0]   inport_sel_reg;
    reg [VC-1:0]selected_sot;
    wire        selected_eot;

    always @( * )
    begin
        (* full_case *) (* parallel_case *)
        casex (inport_sel)
            4'b1xxx: selected_sot = sot_in[((4*VC)-1):(3*VC)];
            4'bx1xx: selected_sot = sot_in[((3*VC)-1):(2*VC)];
            4'bxx1x: selected_sot = sot_in[((2*VC)-1):(1*VC)];
            4'bxxx1: selected_sot = sot_in[((1*VC)-1):(0*VC)];
        endcase
    end

    assign selected_eot = |(eot_in & inport_sel_reg);// & ~(&(eot_in));

    `ifdef ASYNC_RES
    always @(posedge clk or negedge res_n) `else
    always @(posedge clk) `endif
    begin
    if (!res_n) begin
      inport_sel_reg <= {NUM_PORTS{1'b0}};
      any_gnt_reg    <= 0;
     end else begin
      any_gnt_reg <= any_gnt;

    //   if(any_gnt_reg)
        inport_sel_reg <= inport_sel;
     end
    end
    // Muxes for data, eot, sot
    `ifdef ASYNC_RES
```

Figure 6. Regression failing with buggy DUT


vManager | hera3.ece.tamu.edu:8081 | 64b | acoskuner500 [Regression Center]

Flow Sessions

Session Status	Name	Total Runs	#Passed	#Failed	#Running	#Waiting	#Other	Start Time	Owner
(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	==$ME()
completed	htax_regress.acoskuner500.22_11_29_1...	260	228	32	0	0	0	11/29/22 3:32 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_1...	260	260	0	0	0	0	11/29/22 11:26 AM	acoskuner500
completed	htax_regress.acoskuner500.22_11_29_1...	260	260	0	0	0	0	11/29/22 10:26 AM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	15	15	0	0	0	0	11/28/22 7:48 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	15	15	0	0	0	0	11/28/22 7:41 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	15	0	15	0	0	0	11/28/22 7:32 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	15	0	15	0	0	0	11/28/22 7:24 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	15	15	0	0	0	0	11/28/22 11:23 AM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	30	30	0	0	0	0	11/28/22 11:07 AM	acoskuner500
completed	htax_regress.acoskuner500.22_11_28_1...	30	30	0	0	0	0	11/28/22 10:28 AM	acoskuner500
completed	htax_regress.acoskuner500.22_11_27_1...	30	15	15	0	0	0	11/27/22 6:37 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_26_1...	30	15	15	0	0	0	11/26/22 6:09 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_26_1...	30	15	15	0	0	0	11/26/22 5:14 PM	acoskuner500
completed	htax_regress.acoskuner500.22_11_26_1...	30	0	30	0	0	0	11/26/22 4:57 PM	acoskuner500

Showing 14 out of 579 items