CSCE 616 Lab 5

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For the sequences, we used the **`uvm_do_with** macro to pass constraints to the HTAX packet parameters, namely a packet length between 3 and 10 for the short packet, 10 and 40 for medium packet, and between 40 and 50 for the long packet, as well as fixing the virtual channel number to be exactly 1 for the medium packet sequence and constraining the delay length to be less than 5 for the long packet sequence. For the random sequence, we passed an empty constraint to the second argument using empty curly braces {}, but we also tried it with the **`uvm_do** macro with only the first argument and it behaved the same. We learned about this macro function from this website https://verificationacademy.com/verification-methodology-reference/uvm/docs_1.2/html/files/macros/uvm_sequence_defines-svh.html

We ran our simulations with different seeds (we used 616 and 123) and the CSV output revealed that the constraints were working properly, including the default constraints for the random sequence. The long packet sequence was producing suspiciously too many packets with lengths 40, but as seen in the test with seed 616, and in other tests with no seed or other seeds it did produce other lengths.

Figure 1. Simulation with svseed 616

Sequence	dest port	vc	length	delay
fix_dest_port_seq_	'h2	'h2	'hb	'ha
fix_dest_port_seq_	'h2	'h3	'h1d	'h7
fix_dest_port_seq_	'h2	'h3	'h1b	'h9
fix_dest_port_seq_	'h2	'h1	'hc	'h6
fix_dest_port_seq_	'h2	'h1	'h4	'h2
short_packet_seq_	'h2	'h3	'h8	'h2
short_packet_seq_	'h3	'h1	'h8	'h8
short_packet_seq_	'h0	'h2	'h3	'h8
short_packet_seq_	'h3	'h3	'h3	'h6
short_packet_seq_	'h0	'h3	'h4	'h6
long_packet_short_delay_seq_	'h0	'h3	'h28	'h3
long_packet_short_delay_seq_	'h1	'h3	'h28	'h1
long_packet_short_delay_seq_	'h2	'h3	'h28	'h1
long_packet_short_delay_seq_	'h1	'h3	'h28	'h1
long_packet_short_delay_seq_	'h2	'h2	'h28	'h2
med_packet_fixed_vc_seq_	'h3	'h1	'hb	'h13
med_packet_fixed_vc_seq_	'h3	'h1	'h12	'h4
med_packet_fixed_vc_seq_	'h0	'h1	'hc	'h14
med_packet_fixed_vc_seq_	'h1	'h1	'h20	'hb
med_packet_fixed_vc_seq_	'h3	'h1	'h24	'h12
random_seq_	'h2	'h3	'hc	'hb
random_seq_	'h1	'h2	'h15	'h3
random_seq_	'h1	'h1	'h5	'hf
random_seq_	'h3	'h2	'h23	'h2
random_seq_	'h0	'h2	'he	'h7

FIgure 2. Simulation with svseed 123

Sequence	dest port	vc	length	delay
fix_dest_port_seq_	'h3	'h3	'h8	'h7
fix_dest_port_seq_	'h3	'h3	'h2d	'h9
fix_dest_port_seq_	'h3	'h1	'hc	'h4
fix_dest_port_seq_	'h3	'h2	'h14	'h4
fix_dest_port_seq_	'h3	'h2	'h14	'hf
short_packet_seq_	'h0	'h2	'h8	'h1
short_packet_seq_	'h1	'h3	'h8	'h12
short_packet_seq_	'h2	'h3	'ha	'h2
short_packet_seq_	'h1	'h3	'h8	'h4
short_packet_seq_	'h3	'h3	'h3	'h6
long_packet_short_delay_seq_	'h2	'h2	'h31	'h3
long_packet_short_delay_seq_	'h3	'h3	'h28	'h3
long_packet_short_delay_seq_	'h0	'h3	'h28	'h4
long_packet_short_delay_seq_	'h0	'h3	'h28	'h4
long_packet_short_delay_seq_	'h0	'h1	'h28	'h4
med_packet_fixed_vc_seq_	'h2	'h1	'h19	'h3
med_packet_fixed_vc_seq_	'h1	'h1	'h26	'h11
med_packet_fixed_vc_seq_	'h0	'h1	'he	'h10
med_packet_fixed_vc_seq_	'h3	'h1	'h11	'h2
med_packet_fixed_vc_seq_	'h0	'h1	'hd	'h14
random_seq_	'h0	'h2	'h12	'h4
random_seq_	'h1	'h3	'h28	'he
random_seq_	'h2	'h3	'h7	'ha
random_seq_	'h2	'h3	'h18	'h9
random_seq_	'h2	'h1	'h12	'h14