CSCE 616 Lab 2

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After filling in the modports in the interface file, we added three different types of stimuli. For all tests we used a scoreboard array that was written to any time we put a write request.

First, we did a brute force with a nested for loop to iterate through each memory address writing consecutive values (first 0-255 but reduced to 0-9 to keep output concise) and read immediately after within the same loop iteration.

Our second test was putting in 1000 write requests with random addresses and data followed by reading from each memory address in a separate loop to compare with the scoreboard, which only revealed 2/32 mismatches.

Finally, we did random regression over 100 iterations, reading first to access some address once, writing to the same random address with random data, and finally reading again to check with the scoreboard. The reason is that we found the bug in the write hit portion of the HDL design code, so the bug was revealed when a write request hits after any memory access to the same address consecutively.

Figure 1. Simulation with bug, Mismatch count: **474/552** cases

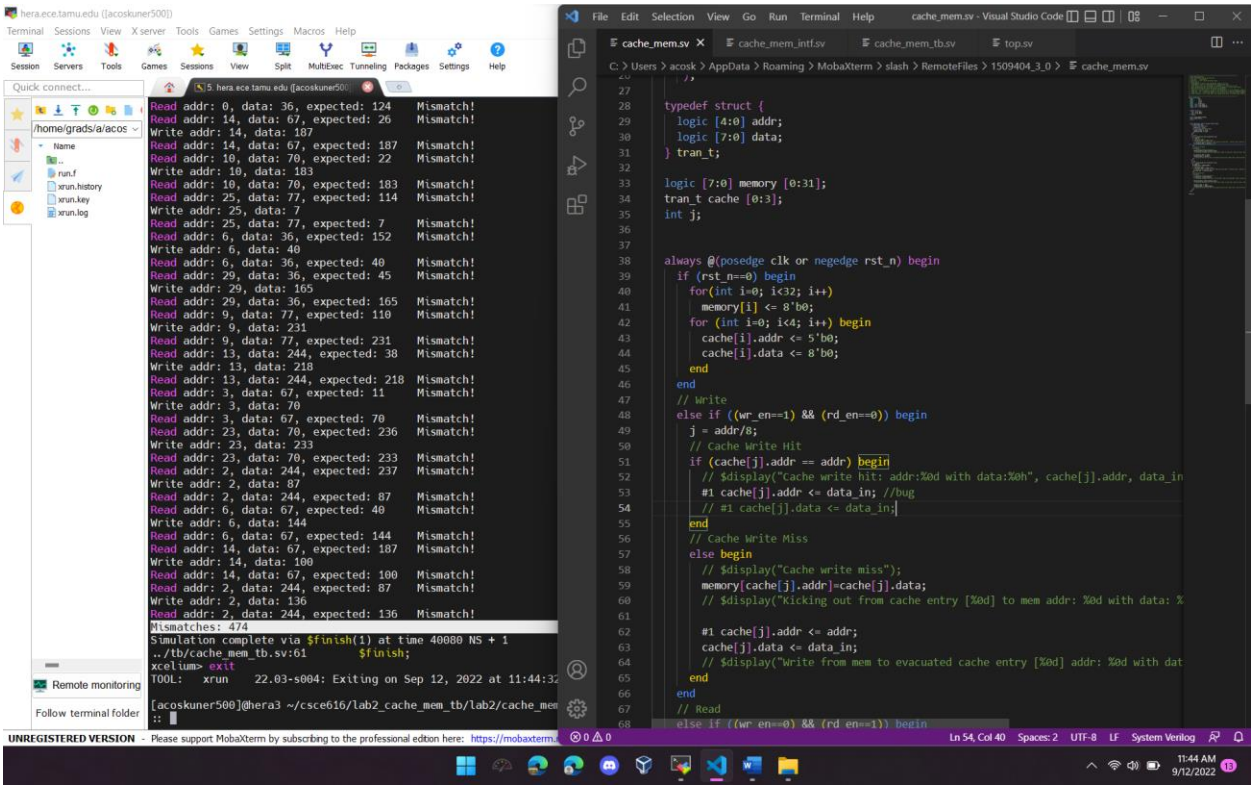

Figure 2. Simulation with bug fixed. Mismatch count **0**