Laboratory Exercise #3

Team 6

Ahmet Coskuner UIN : 126009366

Aswin Kumar Sakthivel UIN : 233005751

Santhosh Srinivasan UIN : 633002273

1 Observation and Conclusions

First we included the uvm macros header file named "uvm_marcos.svh". Secondly, the CPU transaction class was extended from a uvm class - "uvm_sequence_item". We added the UVM Macros for built-in automation and set UVM_ALL_ON for the class properties. The constraints were not edited.

We created 3 handles of the CPU transaction class type: trans1, trans2, and trans3. We created Objects for the 3 class handles and we randomized them. The default view of trans1 was printed using print(). Trans2 was printed in a tree view using trans2.print(uvm_default_tree_printer) method. trans1 and trans3 were compared using the .compare() method and relevant error messages were added if the comparison was unsuccessful.

Since we observed a miscomparsion in the contents, we changed the built-in automation method for the macro to UVM_NOCOMPARE instead of UVM_ALL_ON for address and data and observed a successful comparison between trans1 and trans3.

2 Images

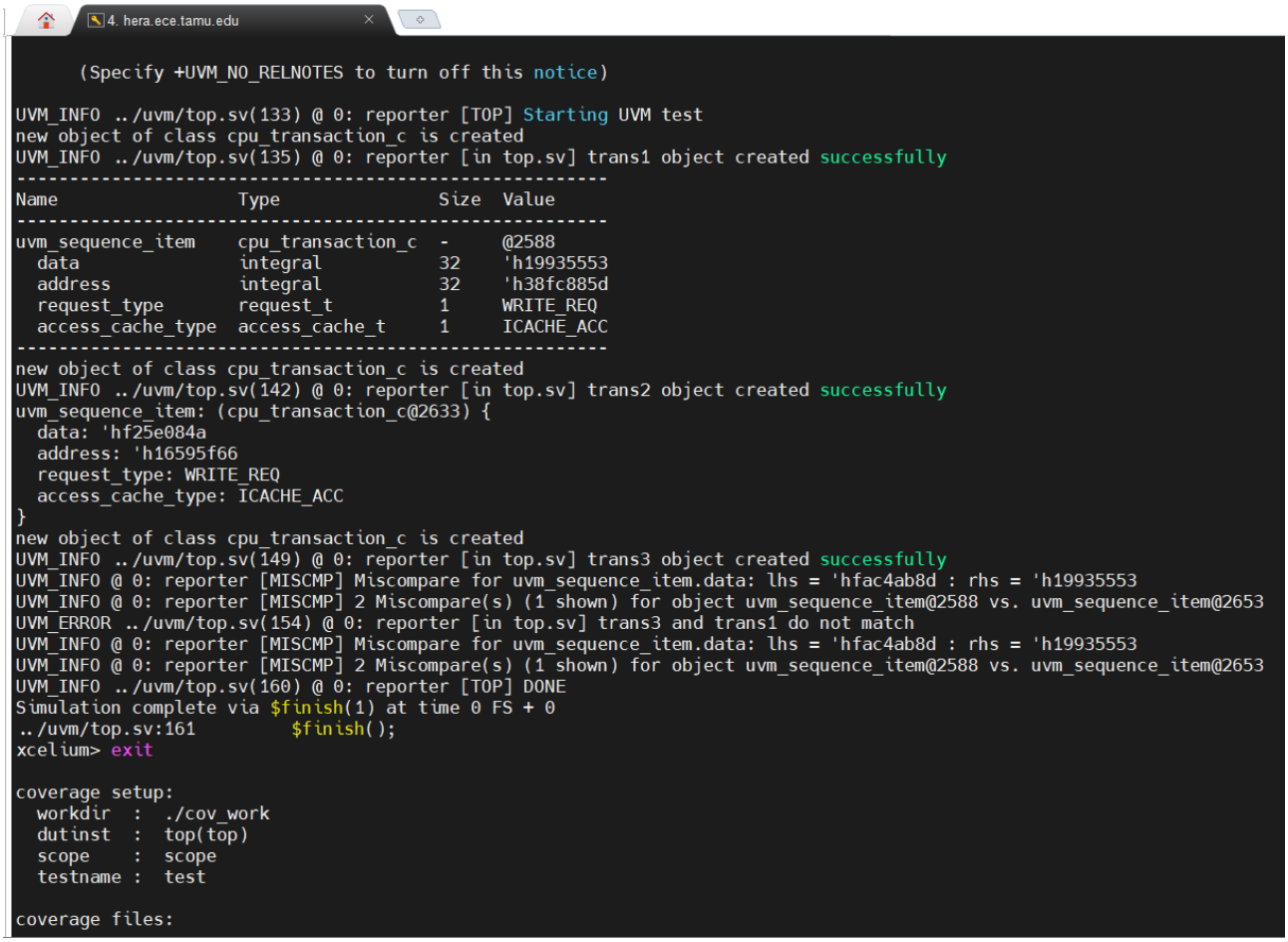

Figure 1: This illustrates the table view and the tree view of trans1 and trans2 objects respectively. We observe a mismatch between trans1 and trans3

xrun.log

```
  See http://www.eda.org/svdb/view.php?id=3313 for more details.

  You are using a version of the UVM library that has been compiled
  with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
  See http://www.eda.org/svdb/view.php?id=3770 for more details.

      (Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO ../uvm/top.sv(133) @ 0: reporter [TOP] Starting UVM test
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(135) @ 0: reporter [in top.sv] trans1 object created successfully
----------------------------------------------------------
Name                 Type               Size  Value
----------------------------------------------------------
uvm_sequence_item    cpu_transaction_c  -     @2588
  data               integral           32    'h19935553
  address            integral           32    'h38fc885d
  request_type       request_t          1     WRITE_REQ
  access_cache_type  access_cache_t     1     ICACHE_ACC
----------------------------------------------------------
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(142) @ 0: reporter [in top.sv] trans2 object created successfully
uvm_sequence_item: (cpu_transaction_c@2633) {
  data: 'hf25e084a
  address: 'h16595f66
  request_type: WRITE_REQ
  access_cache_type: ICACHE_ACC
}
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(149) @ 0: reporter [in top.sv] trans3 object created successfully
UVM_INFO @ 0: reporter [MISCMP] Miscompare for uvm_sequence_item.data: lhs = 'hfac4ab8d : rhs = 'h19935553
UVM_INFO @ 0: reporter [MISCMP] 2 Miscompare(s) (1 shown) for object uvm_sequence_item@2588 vs. uvm_sequence_item@2653
UVM_ERROR ../uvm/top.sv(154) @ 0: reporter [in top.sv] trans3 and trans1 do not match
UVM_INFO @ 0: reporter [MISCMP] Miscompare for uvm_sequence_item.data: lhs = 'hfac4ab8d : rhs = 'h19935553
UVM_INFO @ 0: reporter [MISCMP] 2 Miscompare(s) (1 shown) for object uvm_sequence_item@2588 vs. uvm_sequence_item@2653
UVM_INFO ../uvm/top.sv(160) @ 0: reporter [TOP] DONE
Simulation complete via $finish(1) at time 0 FS + 0
../uvm/top.sv:161         $finish();
xcelium> exit

coverage setup:
  workdir  :  ./cov_work
  dutinst  :  top(top)
  scope    :  scope
  testname :  test

coverage files:
  model(design data) :  ./cov_work/scope/icc_07e19792_6be4a234.ucm (reused)
  data               :  ./cov_work/scope/test/icc_07e19792_6be4a234.ucd
TOOL: xrun  22.03-s004: Exiting on Mar 21, 2023 at 16:51:26 CDT  (total: 00:00:03)

```

Figure 2: Output captured on xrun.log file

cpu_transaction_c.sv

uvm > cpu_transaction_c.sv

```
28      rand request_t                  request_type;
29      rand bit [DATA_WID_LV1-1 : 0]   data;
30      rand bit [ADDR_WID_LV1-1 : 0]   address;
31      rand access_cache_t             access_cache_type;
32
33  //Lab3: TO DO: Add UVM macros for built in automation
34  `uvm_object_utils_begin(cpu_transaction_c)
35  `uvm_field_int(data,UVM_NOCOMPARE)
36  //`uvm_field_int(data,UVM_ALL_ON)
37  `uvm_field_int(address,UVM_NOCOMPARE)
38  //`uvm_field_int(address,UVM_ALL_ON)
39  `uvm_field_enum(request_t,request_type,UVM_ALL_ON)
40  `uvm_field_enum(access_cache_t,access_cache_type,UVM_ALL_ON)
41  `uvm_object_utils_end
42
43  //Constraints on class properties which will be randomized
44  //Constraint 1: Set default access to I-cache.
45      constraint ct_cache_type {
46          soft access_cache_type == ICACHE_ACC;
47      }
```

Figure 3: Changes made in the "cpu_transaction_c.sv" to achieve a match between trans1 and trans3 objects

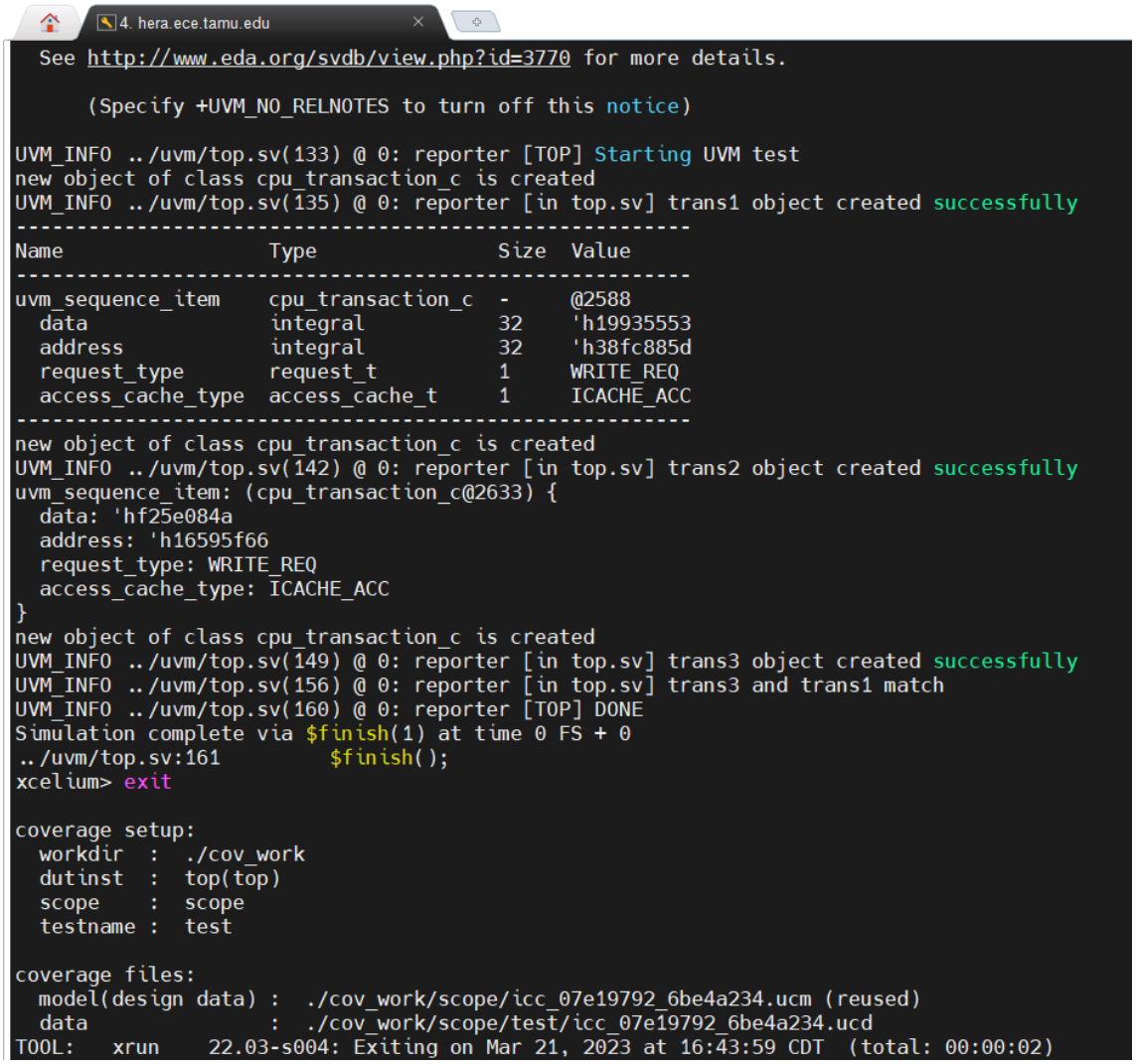

Figure 4: This illustrates the table view and the tree view of trans1 and trans2 objects respectively. We observe a match between trans1 and trans3

xrun.log

```
  ***********       IMPORTANT RELEASE NOTES         ************

  You are using a version of the UVM library that has been compiled
  with `UVM_NO_DEPRECATED undefined.
  See http://www.eda.org/svdb/view.php?id=3313 for more details.

  You are using a version of the UVM library that has been compiled
  with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
  See http://www.eda.org/svdb/view.php?id=3770 for more details.

      (Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO ../uvm/top.sv(133) @ 0: reporter [TOP] Starting UVM test
new object of class cpu_transaction_c is created
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  address            integral           32    'h38fc885d
  request_type       request_t          1     WRITE_REQ
  access_cache_type  access_cache_t     1     ICACHE_ACC
----------------------------------------------------------
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(142) @ 0: reporter [in top.sv] trans2 object created successfully
uvm_sequence_item: (cpu_transaction_c@2633) {
  data: 'hf25e084a
  address: 'h16595f66
  request_type: WRITE_REQ
  access_cache_type: ICACHE_ACC
}
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(149) @ 0: reporter [in top.sv] trans3 object created successfully
UVM_INFO ../uvm/top.sv(156) @ 0: reporter [in top.sv] trans3 and trans1 match
UVM_INFO ../uvm/top.sv(160) @ 0: reporter [TOP] DONE
Simulation complete via $finish(1) at time 0 FS + 0
../uvm/top.sv:161         $finish();
xcelium> exit

coverage setup:
  workdir  :  ./cov_work
  dutinst  :  top(top)
  scope    :  scope
  testname :  test

coverage files:
  model(design data) :  ./cov_work/scope/icc_07e19792_6be4a234.ucm (reused)
  data               :  ./cov_work/scope/test/icc_07e19792_6be4a234.ucd
TOOL: xrun  22.03-s004: Exiting on Mar 21, 2023 at 17:08:23 CDT  (total: 00:00:02)

```

Figure 5: Output captured on xrun.log file