

Laboratory Exercise #2

Team 6

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1 Observation and Conclusions

Class data members are declared as rand, and their constraints are defined based on the specification. Constraints made set the cache type to I- or D-Cache based on the address, but the default was set to I-Cache

In Lab 1, the read task was defined to accept 3 arguments (address, data, virtual interface). However, in this lab, the value of address and data are now obtained from the class properties and not as arguments. Hence it included only one argument (i.e. the virtual interface).

A handle is created on top.sv file and we randomized all the data members of the object with an inline constraint. When randomization was successful, a read operation was performed on processor 2 depending on the value of the read request.

UVM macros ('uvm_info, 'uvm_error) are included in the testbench and the SV testbench is now converted to a UVM testbench. Instead of using \$display and \$error statements, we used 'uvm_info, 'uvm_error macros to implement its message display functionality. We observed that verbosity level is not defined for 'uvm_error and it is only defined for 'uvm_info messages. Based on the verbosity level, the info messages are displayed (i.e. LOW, MEDIUM, HIGH)

2 Images

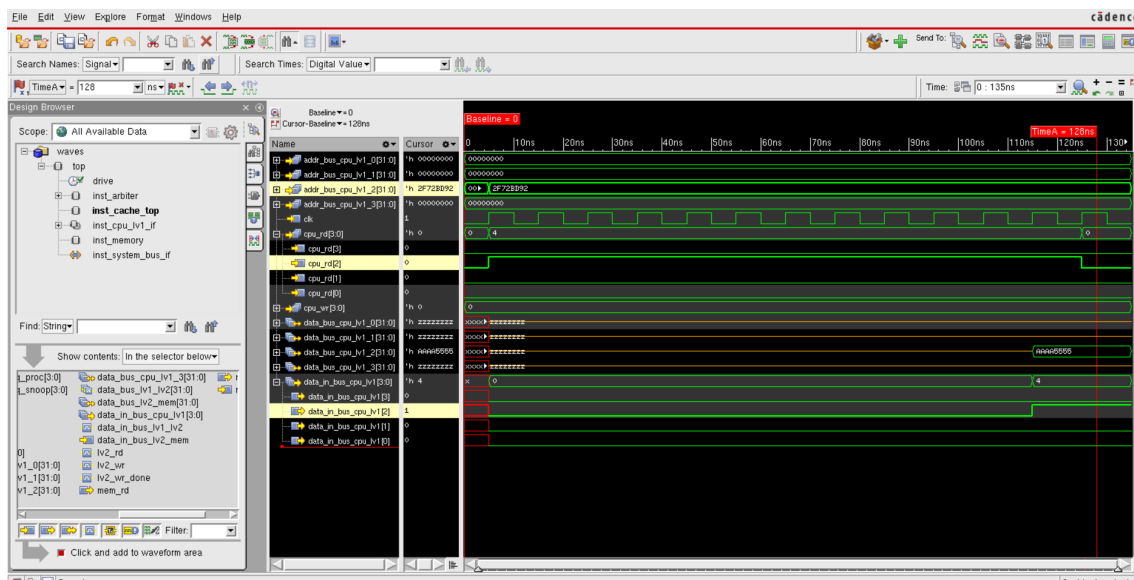


Figure 1: Output of the read transaction on PROC2

It is observed from the waveform, Bit 3 of the address 2F72BD92 is 0, and hence the default data is AAAA5555

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CDNS-UVM-1.1d (22.03-s004)
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(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.
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***** IMPORTANT RELEASE NOTES *****

You are using a version of the UVM library that has been compiled
with `UVM_NO_DEPRECATED undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO ../uvm/top.sv(160) @ 0: reporter [Verbosity Low] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(168) @ 0: reporter [Start of test] CSCE 714: Lab2
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(196) @ 0: reporter [MSG: checker starts] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(183) @ 125: reporter [End of test] CSCE 714: Lab2
Simulation complete via $finish(1) at time 135 NS + 0
../uvm/top.sv:188 $finish;
xcelium> exit

coverage setup:
  workdir : ./cov_work
  dutinst : top(top)
  scope   : scope
  testname: test

coverage files:
  model(design data) : ./cov_work/scope/icc_52f691ed_00000000.ucm
  data               : ./cov_work/scope/test/icc_52f691ed_00000000.ucd
TOOL:  xrun  22.03-s004: Exiting on Mar 06, 2023 at 15:51:14 CST (total: 00:00:02)

[santhosh_2897]@hera3 ~/CSCE_714_LAB2/csce_714_lab2/project/sim> (15:51:14 03/06/23)
::

```

Figure 2: Output of the Console with Verbosity - LOW

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CDNS-UVM-1.1d (22.03-s004)
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See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO ../uvm/top.sv(160) @ 0: reporter [Verbosity Low] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(161) @ 0: reporter [Verbosity Medium] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(168) @ 0: reporter [Start of test] CSCE 714: Lab2
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(196) @ 0: reporter [MSG: checker starts] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(183) @ 125: reporter [End of test] CSCE 714: Lab2
Simulation complete via $finish(1) at time 135 NS + 0
../uvm/top.sv:188 $finish;
xcelium> exit

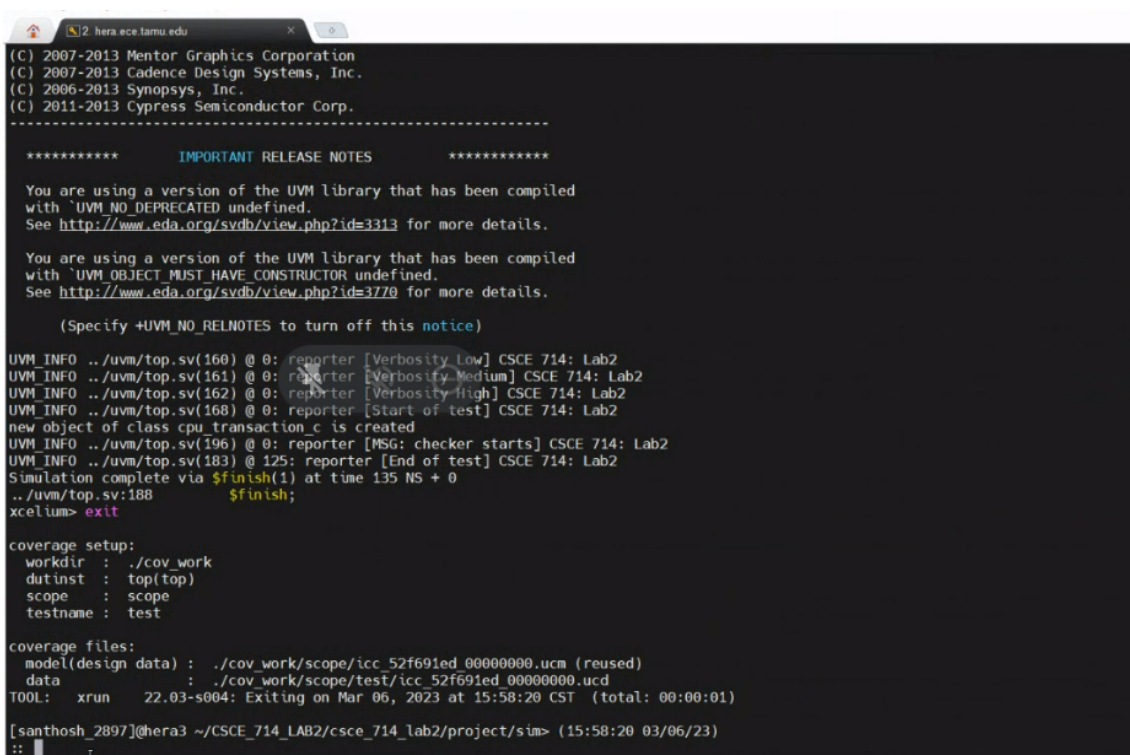
coverage setup:
  workdir : ./cov_work
  dutinst : top(top)
  scope   : scope
  testname: test

coverage files:
  model(design data) : ./cov_work/scope/icc_52f691ed_00000000.ucm (reused)
  data               : ./cov_work/scope/test/icc_52f691ed_00000000.ucd
TOOL:  xrun  22.03-s004: Exiting on Mar 06, 2023 at 15:56:59 CST (total: 00:00:02)

[santhosh_2897]@hera3 ~/CSCE_714_LAB2/csce_714_lab2/project/sim> (15:56:59 03/06/23)
::

```

Figure 3: Output of the Console with Verbosity - MEDIUM



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***** IMPORTANT RELEASE NOTES *****

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with 'UVM_NO_DEPRECATED undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with 'UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO ../uvm/top.sv(160) @ 0: reporter [Verbosity Low] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(161) @ 0: reporter [Verbosity Medium] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(162) @ 0: reporter [Verbosity High] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(168) @ 0: reporter [Start of test] CSCE 714: Lab2
new object of class cpu_transaction_c is created
UVM_INFO ../uvm/top.sv(196) @ 0: reporter [MSG: checker starts] CSCE 714: Lab2
UVM_INFO ../uvm/top.sv(183) @ 125: reporter [End of test] CSCE 714: Lab2
Simulation complete via $finish(1) at time 135 NS + 0
../uvm/top.sv:188      $finish;
xcelium> exit

coverage setup:
  workdir : ./cov_work
  dutinst : top(top)
  scope   : scope
  testname: test

coverage files:
  model(design data) : ./cov_work/scope/icc_52f691ed_00000000.ucm (reused)
  data               : ./cov_work/scope/test/icc_52f691ed_00000000.ucd
T00L:  xrun    22.03-s004: Exiting on Mar 06, 2023 at 15:58:20 CST (total: 00:00:01)

[santhosh.2897]@hera3 ~/CSCE_714_LAB2/csce_714_lab2/project/sim> (15:58:20 03/06/23)
:: █
```

Figure 4: Output of the Console with Verbosity - HIGH