CSCE 714

Laboratory Exercise #2

Team 6

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1 Observation and Conclusions

Class data members are declared as rand, and their constraints are defined based on the specification. Constraints made set the cache type to I- or D-Cache based on the address, but the default was set to I-Cache

In Lab 1, the read task was defined to accept 3 arguments (address, data, virtual interface). However, in this lab, the value of address and data are now obtained from the class properties and not as arguments. Hence it included only one argument (i.e. the virtual interface).

A handle is created on top.sv file and we randomized all the data members of the object with an inline constraint. When randomization was successful, a read operation was performed on processor 2 depending on the value of the read request.

UVM macros (‘uvm_info, ‘uvm_error) are included in the testbench and the SV testbench is now converted to a UVM testbench. Instead of using $display and $error statements, we used ‘uvm_info, ‘uvm_error macros to implement its message display functionality. We observed that verbosity level is not defined for ’uvm_error and it is only defined for ’uvm_info messages. Based on the verbosity level, the info messages are displayed (i.e. LOW, MEDIUM, HIGH)

2 Images

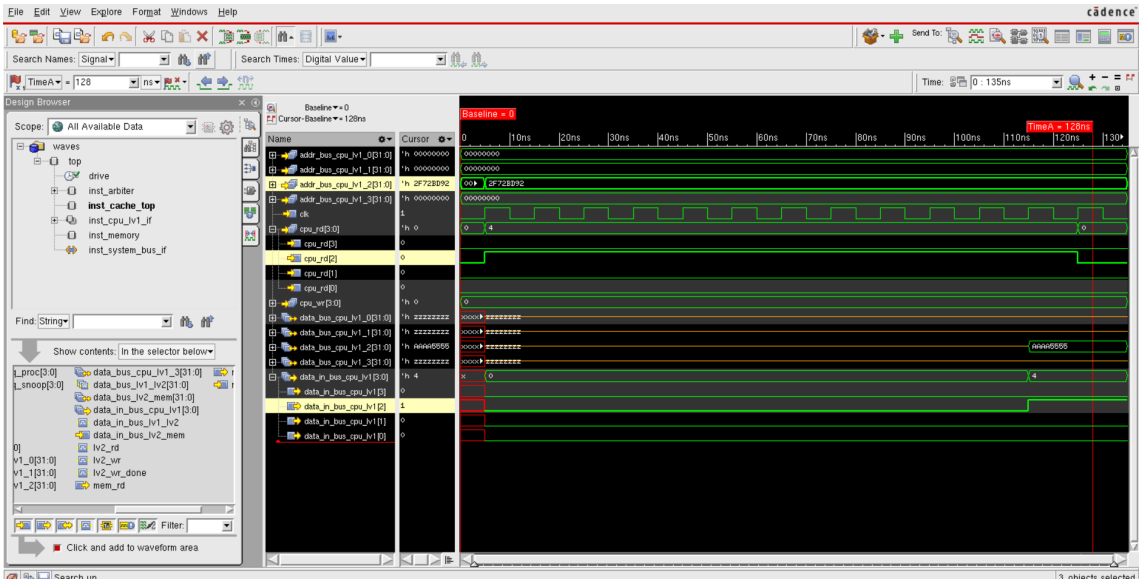

Figure 1: Output of the read transaction on PROC2

It is observed from the waveform, Bit 3 of the address 2F72BD92 is 0, and hence the default data is AAAA5555

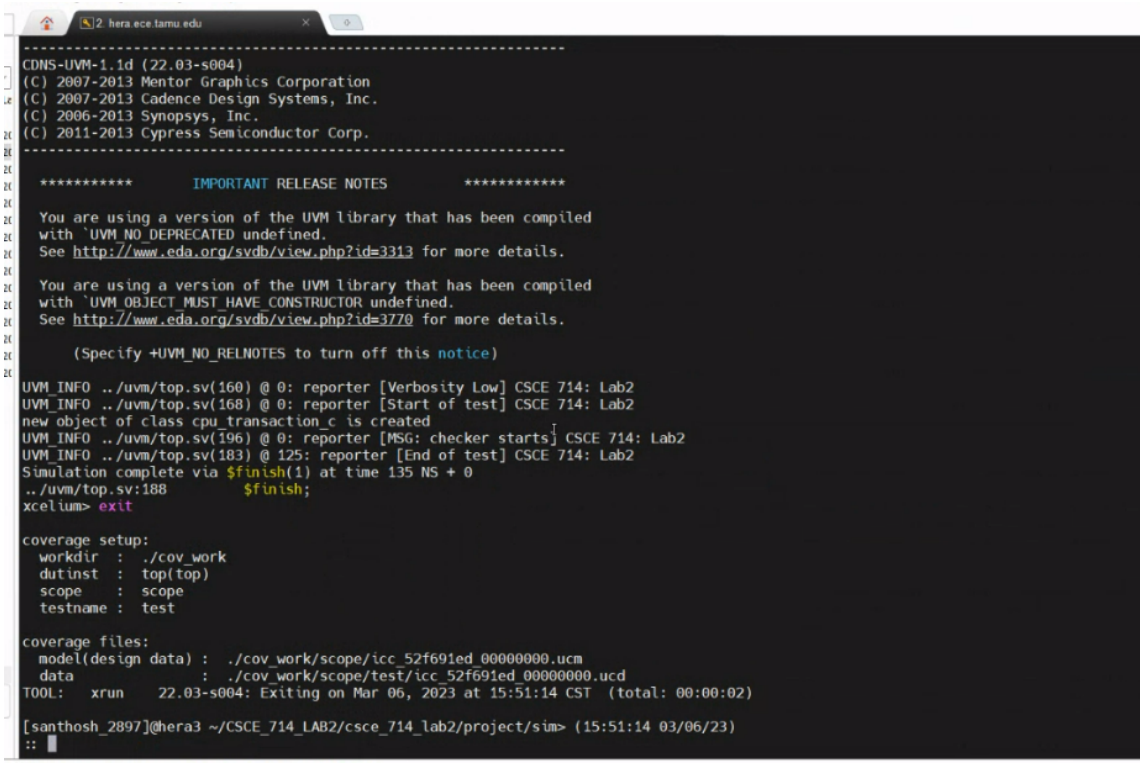

Figure 2: Output of the Console with Verbosity - LOW

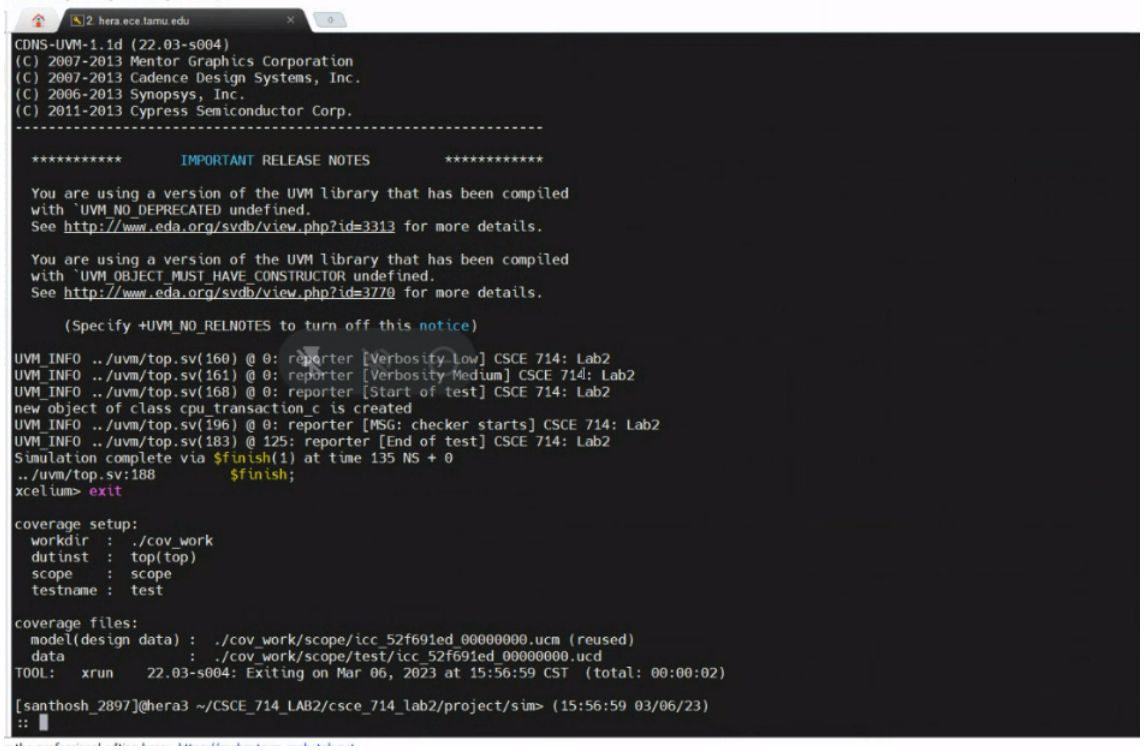

Figure 3: Output of the Console with Verbosity - MEDIUM

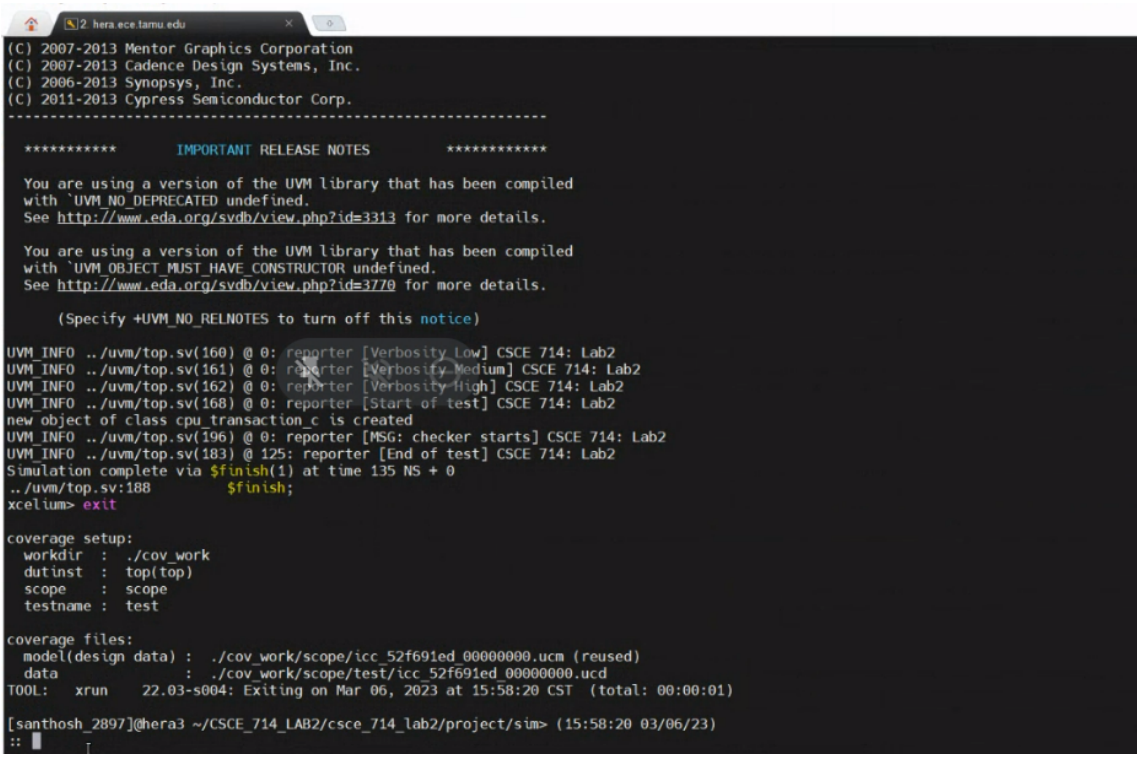

Figure 4: Output of the Console with Verbosity - HIGH