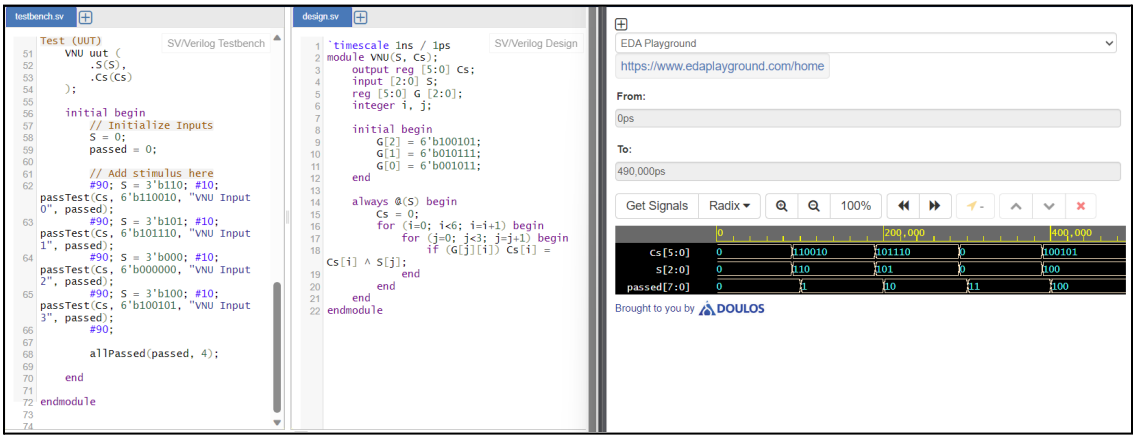
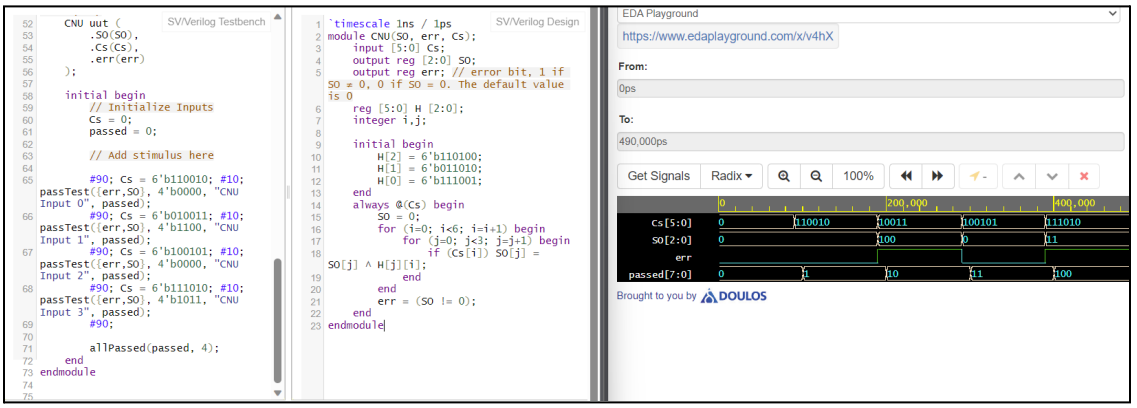
Task 1: Verilog Simulation

VNU Waveform and Output




```
[2023-10-17 22:19:24 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile VNU.vcd opened for output.
      VNU Input 0 passed
      VNU Input 1 passed
      VNU Input 2 passed
      VNU Input 3 passed
All tests passed
Finding VCD file...
./VNU.vcd
[2023-10-17 22:19:25 UTC] Opening EPWave...
Done
```

CNU Waveform and Output




```
[2023-10-17 22:15:52 UTC] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile CNU.vcd opened for output.
      CNU Input 0 passed
      CNU Input 1 passed
      CNU Input 2 passed
      CNU Input 3 passed
All tests passed
Finding VCD file...
./CNU.vcd
[2023-10-17 22:15:52 UTC] Opening EPWave...
Done
```

Task 2: Schematic Simulation

Note: G is indexed and assigned as follows

	5	4	3	2	1	0
2	G[17] = 1	G[14] = 0	G[11] = 0	G[8] = 1	G[5] = 0	G[2] = 1
1	G[16] = 0	G[13] = 1	G[10] = 0	G[7] = 1	G[4] = 1	G[1] = 1
0	G[15] = 0	G[12] = 0	G[9] = 1	G[6] = 0	G[3] = 1	G[0] = 1

VNU testfixture.verilog

```
initial
$monitor ($time, " S=%b, Cs=%b", S, Cs);

initial begin
   G = 18'b100_010_001_110_011_111;
   S = 0;
   #100; S = 3'b110;
   #100; S = 3'b101;
   #100; S = 3'b000;
   #100; S = 3'b100;
end
```

VNU simout.tmp

```
TOOL:  ncxlmode       15.20-s083: Started on Oct 19, 2023 at 03:02:02 CDT
ncxlmode
        +delay_mode_path
        +typdelays
        -l
        simout.tmp
        /home/grads/a/acoskuner500/ecen475/VNU_run1/testfixture.template
        -f /home/grads/a/acoskuner500/ecen475/VNU_run1/verilog.inpfiles

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xnor3/functional/verilog.v
                ihnl/cds1/netlist
                ihnl/cds2/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100
-pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input
/home/grads/a/acoskuner500/ecen475/VNU_run1/.simTmpNCCmd "
        +mpssession+virtuoso12943
        +mpshost+hera3.ece.tamu.edu

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Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                    0 S=000, Cs=000000
                  100 S=110, Cs=110010
                  200 S=101, Cs=101110
                  300 S=000, Cs=000000
                  400 S=100, Cs=100101
ncsim>
```
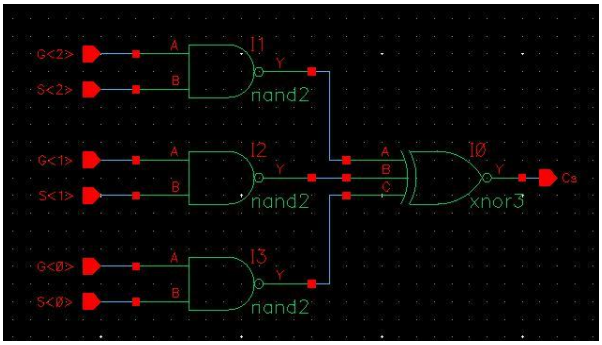

CNU testfixture.verilog

```
initial
$monitor ($time, " Cs=%b, SO=%b", Cs, {ERR, SO});

initial begin
   H = 18'b110100_011010_111001;
   Cs = 0;
   #100; Cs = 6'b110010;
   #100; Cs = 6'b010011;
   #100; Cs = 6'b100101;
   #100; Cs = 6'b111010;
end
```

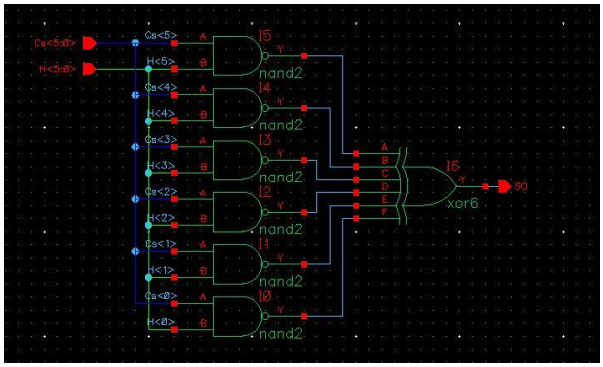
CNU simout.tmp

```
TOOL:  ncxlmode       15.20-s083: Started on Oct 19, 2023 at 03:15:34 CDT
ncxlmode
       +delay_mode_path
       +typdelays
       -l
       simout.tmp
       /home/grads/a/acoskuner500/ecen475/CNU_run1/testfixture.template
       -f /home/grads/a/acoskuner500/ecen475/CNU_run1/verilog.inpfiles

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nor3/functional/verilog.v

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/inv/functional/verilog.v

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor6/functional/verilog.v

/opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
              ihnl/cds0/netlist
              ihnl/cds2/netlist
              ihnl/cds1/netlist
       +nostdout
       +nocopyright
       +ncvlogargs+" -neverwarn -nostdout -nocopyright "
       +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100
-pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -nocopyright"
       +ncsimargs+" -neverwarn  -nocopyright -gui -input
/home/grads/a/acoskuner500/ecen475/CNU_run1/.simTmpNCCmd "
       +mpssession+virtuoso12943
       +mpshost+hera3.ece.tamu.edu

-------------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                  0 Cs=000000, SO=0000
                100 Cs=110010, SO=0000
                200 Cs=010011, SO=1100
                300 Cs=100101, SO=0000
                400 Cs=111010, SO=1011
ncsim>
```

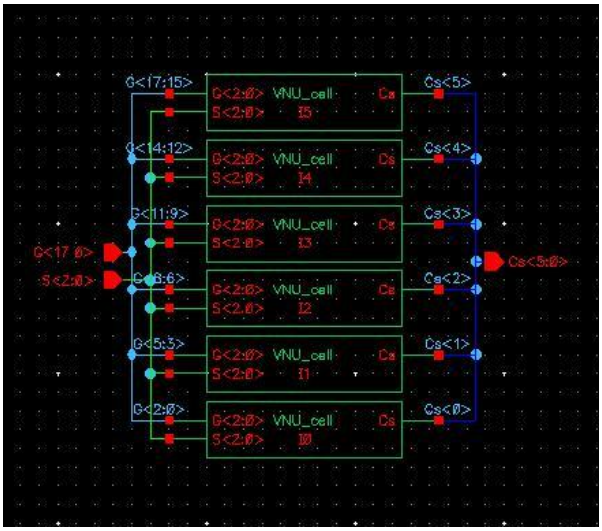
VNU_cell schematic and symbol



CNU_cell schematic and symbol



VNU schematic and symbol



CNU schematic and symbol