ECEN 454/714 – Lab0: Lab Overview

1. Introduction

In the labs for this course, you will use the Cadence set of tools for VLSI design. These tools are the state-of-the-art CAD tools widely used in the industry. It is hard to learn the whole software set in one semester. In this semester, you will focus on the part that is very useful in digital IC design.

2. Objective

Through Labs 1-9, you will be required to design an 8-bit Pipelined Adder. Following is the block diagram of the circuit.

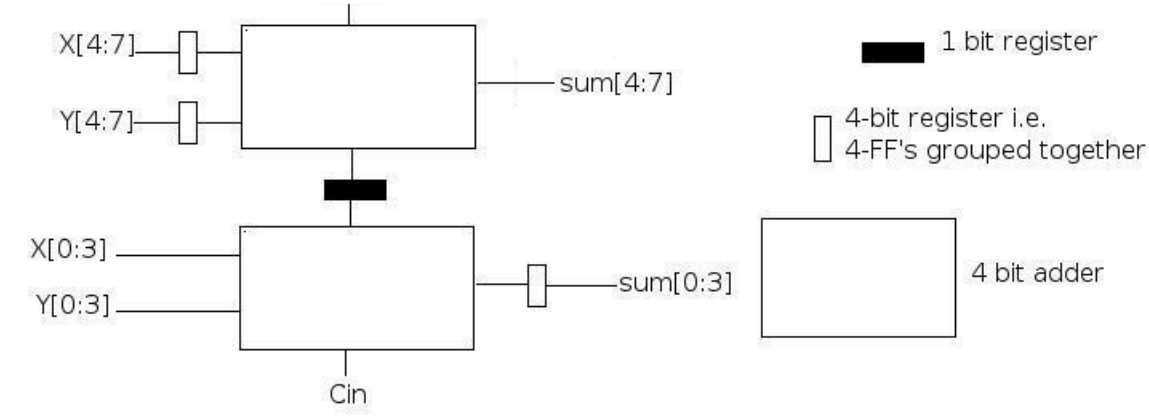

Fig 1. Block diagram for an 8 bit Pipelined adder.

Following is a brief description of the design flow you will be using over the next few lab sessions. The detailed requirements for each stage will be in the respective lab manuals.

• You will begin with the implementation of the schematic and its logic simulation. You will be guided to design each of the blocks (using logic gates such as And, Nand, Inv and Flip-Flops) in the above diagram.

• After verifying the logic design of the circuit, you will be designing the custom layout of the gates (standard cells) that were used in the design.

• The next stage involves performing the standard cell characterization which includes finding rise and fall delay times of the standard cells using transistor level implementation of the cells using Spectre.

• The next step would be to merge all the standard cell layouts to create a 1-bit full adder.

• Using the 1-bit full adders, design one sub-block (one 4-bit adder) of the entire design.

• You are then required to perform optimization of the circuit in terms of transistor sizes/ circuit area (an increased transistor size may occupy more area but is faster in terms of its delay and your design should keep such trade-offs in mind), delay of the circuit and power consumed.

• The next step requires you to design the layout and characterize a Flip-Flop. The characterization would include finding the setup and hold time of the FF. (FF stands for Flip-Flop in all the following sections and manuals).

• Finally, you will combine all the blocks designed (4-bit adders, FF's and the registers) to implement the entire design. The combined design should also include a buffered clock tree implemented as a H-tree.

The grading would be based on weekly reports and would be based on design metrics such as area, clock period and power consumption wherever applicable.

Through Lab 7, you will implement a circuit design using ASIC design flow.

1) You will begin by writing a behavioral description of a Cruise Control system of a car using verilog. You will be required to verify its operation.

2) Next you will synthesize the verilog code using Design Analyzer to generate a gate level netlist of the circuit you designed.

3) You will then use a tool called SoC Encounter to perform Place and Route for the netlist that you generated in the previous step.

4) Next you will be performing static timing analysis on this circuit and make any required modifications to improve the delay along any path which has a low slack.