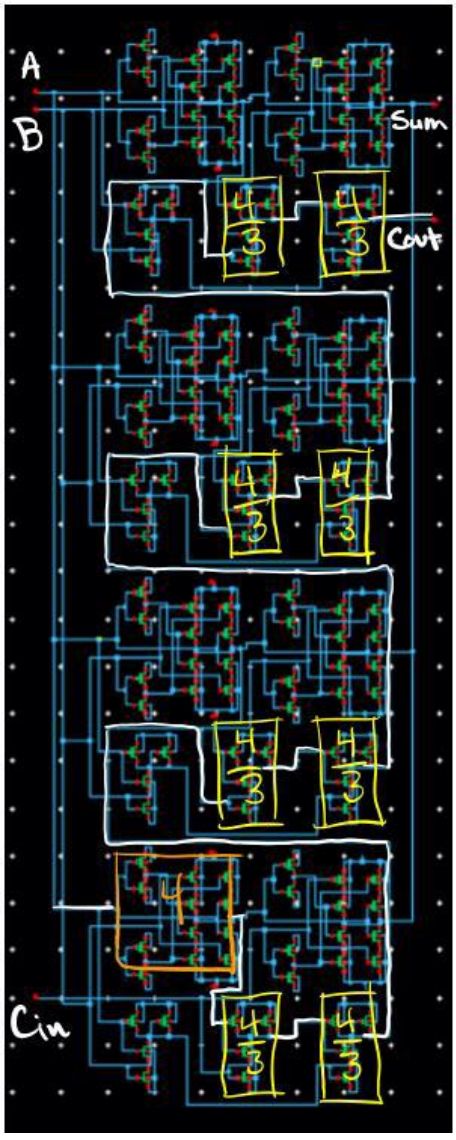
# ECEN 454/714 – Lab9: Optimization using Logical Effort

## 1. Introduction

In this lab you have to identify the critical path in your design (4-bit adder) and reduce the delay of this path by determining the optimal number of devices and sizes of the gates that lie along this path. You must use the Logical Effort and Gate sizing techniques you learn in the course.

## 2. Design transistor level schematic for 4-bit adder

Attached is a sample of the transistor level schematic of the 4-bit adder and its critical path. It is unwise to use symbols for nand/xor/1-bit adder. The reason is any changes made to any of the nand/xor/1-bit adder schematic will also be saved on other nand/xor/1-bit adders. For this reason, you need to draw the transistor level of the 4-bit adder to keep each gate independent from the others.



First, you should design your own transistor level schematic by substituting the blocks in your previous 4-bit adder design with the schematics of NAND2 and XOR2. You can put the new schematic in a new cell and create a symbol for it. Once you complete the design of the schematic, you can design and perform pre-layout simulations to verify if the design is logically or functionally correct.

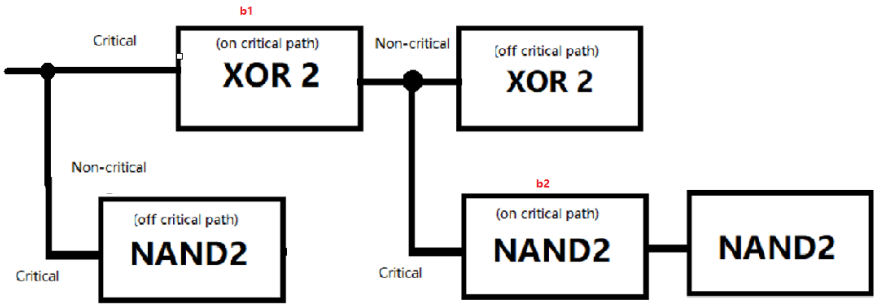
Second, please identify the critical path on your schematic by screenshot the schematic and draw a line along the critical path. The critical path is a logical path from an input pin to an output pin on your circuit that involves most logic gates. In the sample above, the critical path starts from one XOR2 and goes through 8 NAND2.

3. Logical Effort Calculation and Optimization

Complete the following calculation process of logical effort optimization.

- According to the sink capacitance measurement in Lab 3, look up the values of $C_{xor}$ and $C_{nand2}$ for your gate design.
- Compute Path Logical Effort $G = \prod g_i$ (i = 1, 2, 3, 4, …, 9)
  *Where $g_1 = g_{xor} = 4$, $g_{2, 3, \ldots 9} = g_{nand2} = 4/3$ (you can look at Sutherland_Ch1.pdf if you are curious about how to calculate logical effort $g_{xor}$ and $g_{nand2}$)*
- Compute *H = Path Electrical Effort* = $C_{out\_capacatance}/C_{in\_capaticance} = C_{load} / C_{xor}$
  *Where $C_{load}$ = 30fF, $C_{xor}$ is the value you got in Lab 3.*
- Compute *B = Path Branching Effort* = $\prod b_i$ (i = 1, 2, 3, 4, …, 9)
  Where $b_i = ( C_{on\_critical\_path} + C_{off\_critical\_path} )/ C_{on\_critical\_path}$

For example, $b_1 = (C_{xor} + C_{nand2}) / C_{xor}$, $b_{2,4,6,8} = (C_{xor} + C_{nand2}) / C_{nand2}$, $b_{3,5,7,9} = 1$ (since there is no branch, $C_{off\_critical\_path} = 0$)




- Compute F =Path Effort = GBH, $\hat{f}$ = Stage Effort = $F^{\frac{1}{9}}$ (9 is the number of stages)
- If $\hat{f} < 2.7$ or $\hat{f} > 4$, manipulate F (mainly B) by theoretically resizing either NAND2 or XOR2. (Hint: derive F in terms of $C_{xor}$ and $C_{nand2}$ and assume that sink capacitance is proportional to the transistor size. For example, if a transistor of 400nm width shows 1fF of gate capacitance, you can assume that a transistor of 800nm width will have 2fF of gate capacitance.)

- If $2.7 < \hat{f} < 4$, perform the following resizing:
  For the i-th gate, i = 9, 8, 7, ..., 1, calculate: $C_{in,i} = g_i C_{outi} / \hat{f}$
  (Resize from the last nand gate.)
- If $C_{in,i} < C_{gate}$, keep the size (New sizes should always grater or equal to old sizes.). Otherwise resize the i-th gate by $C_{in,i} / C_{gate}$ times the old size.
  For instance, if a nand gate needs to be resized by the value of 1.2, the width (Wn and Wp) of all 4 transistors in that gate should be modified with the same ratio. Resizing is done on the schematic level and only applied to the width (not length). There is no layout in this lab, update the sizes in your lab 9 schematic only.

**3 Report Requirements**

- Include your transistor level schematic and draw a line on it to indicate the critical path.
- Please report 4 optimized pre-layout simulation waveforms for the following in-put vectors:

A=0000, B=1111, CarryIn=1:
A=1010, B=0101, CarryIn=0:
A=1010, B=0101, CarryIn=1:
A=1100, B=1000, CarryIn=0:

And complete the following tables:

Delays:

| Case | Pin | Non-optimized (ps) | Optimized (ps) |
|---|---|---|---|
| A=0000 B=1111 Carry In=1 | SUM.0 | | |
| | SUM.1 | | |
| | SUM.2 | | |
| | SUM.3 | | |
| | CARRY | | |
| A=1010 B=0101 Carry In=0 | SUM.0 | | |
| | SUM.1 | | |
| | SUM.2 | | |
| | SUM.3 | | |
| | CARRY | | |
| A=1010 B=0101 Carry In=1 | SUM.0 | | |
| | SUM.1 | | |
| | SUM.2 | | |
| | SUM.3 | | |
| | CARRY | | |
| A=1100 B=1000 Carry In=0 | SUM.0 | | |
| | SUM.1 | | |
| | SUM.2 | | |
| | SUM.3 | | |
| | CARRY | | |

Power consumptions:

| Case | Optimized (uW) | Non-optimized (uW) |
|---|---|---|
| A=0000, B=1111, CarryIn=1 | | |
| A=1010, B=0101, CarryIn=0 | | |
| A=1010, B=0101, CarryIn=1 | | |
| A=1100, B=1000, CarryIn=0 | | |

Area:

| Optimized ($u^2m^2$) | Non-optimized ($u^2m^2$) |
|---|---|
| | |

Area is the sum up all the transistors' W*L.

Lab 9 Rubric:

1. Circuit with critical path (0.5)

2. Calculate G, B, H and attach the calculation procedure (0.5*3)

3. Resizing procedure & transistors' sizes (1.5)

4. Waveforms (0.5*4)

5. Table comparing delays and VDD power consumption (0.5*4, 0.5*4)

6. Table comparing area (0.5)