Name: Ahmet Coskuner
TA: Neha Gupta

ECEN 714-612 Lab 7
    1. Logic Synthesis
        a. Report_constraints.txt

```
Information: Updating design information... (UID-85)

****************************************
Report : constraint
        -all_violators
        -verbose
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Nov  2 17:20:43 2022
****************************************

This design has no violated constraints.
```

        b. Report_area.txt

```
****************************************
Report : area
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Nov  2 17:21:33 2022
****************************************

Library(s) Used:

        iit018_stdcells (File:
/home/grads/a/acoskuner500/cadence/synthesis/libraries/iit018_stdcells.db)

Number of ports:                        58
Number of nets:                         355
Number of cells:                        304
Number of combinational cells:          282
Number of sequential cells:             20
Number of macros/black boxes:           0
Number of buf/inv:                      73
Number of references:                   18

Combinational area:             8543.000000
Buf/Inv area:                   1576.000000
Noncombinational area:          1920.000000
Macro/Black Box area:           0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                10463.000000
Total area:                 undefined
```

        c. 20 Registers
    2. Static Timing Analysis
        a. max_paths.txt (Setup time)

```
*****************************************
Report : timing
    -path_type full
    -delay_type max
    -slack_lesser_than 5.00
    -max_paths 3
    -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Nov  2 18:03:25 2022
*****************************************


  Startpoint: cruisespeed_reg[6]
             (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[6]
             (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                              Incr    Path
  -------------------------------------------------------------------------------
  clock clk (rise edge)                              0.00    0.00
  clock network delay (ideal)                        0.00    0.00
  cruisespeed_reg[6]/CLK (DFFPOSX1)                  0.00    0.00 r
  cruisespeed_reg[6]/Q (DFFPOSX1)                    0.18    0.18 r
  U171/Y (INVX1)                                     0.27    0.44 f
  U170/Y (INVX8)                                     0.77    1.21 r
  cruisespeed[6] (out)                               0.00    1.21 r
  data arrival time                                          1.21

  clock clk (rise edge)                             10.00   10.00
  clock network delay (ideal)                        0.00   10.00
  clock reconvergence pessimism                      0.00   10.00
  output external delay                             -5.00            5.00
  data required time                                         5.00
  -------------------------------------------------------------------------------
  data required time                                         5.00
  data arrival time                                         -1.21
  -------------------------------------------------------------------------------
  slack (MET)                                                3.79


  Startpoint: cruisespeed_reg[0]
             (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[0]
             (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                              Incr    Path
  -------------------------------------------------------------------------------
  clock clk (rise edge)                              0.00    0.00
  clock network delay (ideal)                        0.00    0.00
  cruisespeed_reg[0]/CLK (DFFPOSX1)                  0.00    0.00 r
  cruisespeed_reg[0]/Q (DFFPOSX1)                    0.14    0.14 r
  U179/Y (INVX1)                                     0.26    0.40 f
  U178/Y (INVX8)                                     0.77    1.17 r
  cruisespeed[0] (out)                               0.00    1.17 r
  data arrival time                                          1.17

  clock clk (rise edge)                             10.00   10.00
  clock network delay (ideal)                        0.00   10.00
  clock reconvergence pessimism                      0.00   10.00
  output external delay                             -5.00            5.00
  data required time                                         5.00
  -------------------------------------------------------------------------------
  data required time                                         5.00
  data arrival time                                         -1.17
  -------------------------------------------------------------------------------
```

```
    slack (MET)                                               3.83


   Startpoint: cruisespeed_reg[5]
              (rising edge-triggered flip-flop clocked by clk)
   Endpoint: cruisespeed[5]
              (output port clocked by clk)
   Path Group: clk
   Path Type: max

   Point                                               Incr    Path
   -------------------------------------------------------------------------
   clock clk (rise edge)                               0.00    0.00
   clock network delay (ideal)                         0.00    0.00
   cruisespeed_reg[5]/CLK (DFFPOSX1)                   0.00    0.00 r
   cruisespeed_reg[5]/Q (DFFPOSX1)                     0.14    0.14 r
   U177/Y (INVX1)                                      0.23    0.37 f
   U176/Y (INVX8)                                      0.76    1.12 r
   cruisespeed[5] (out)                               0.00    1.12 r
   data arrival time                                           1.12

   clock clk (rise edge)                              10.00   10.00
   clock network delay (ideal)                         0.00   10.00
   clock reconvergence pessimism                       0.00   10.00
   output external delay                              -5.00            5.00
   data required time                                          5.00
   -------------------------------------------------------------------------
   data required time                                          5.00
   data arrival time                                          -1.12
   -------------------------------------------------------------------------
   slack (MET)                                                 3.88

Warning: report_timing has satisfied the max_paths criteria. There are 31 further endpoints
which have paths of interest with slack less than  5.00 that were not considered when
generating this report. (UITE-502)

1
```

b.   min_paths.txt (Hold time)

```
*****************************************
Report : timing
    -path_type full
    -delay_type min
    -slack_lesser_than 5.00
    -max_paths 3
    -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Nov  2 18:06:06 2022
*****************************************


  Startpoint: reset (input port clocked by clk)
  Endpoint: state_reg[1]
             (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                   Incr   Path
  ---------------------------------------------------------------
  clock clk (rise edge)                   0.00   0.00
  clock network delay (ideal)             0.00   0.00
  input external delay                    0.00   0.00 f
  reset (in)                              0.06   0.06 f
  U71/Y (OAI21X1)                         0.08   0.13 r
  state_reg[1]/D (DFFPOSX1)               0.00   0.13 r
  data arrival time                              0.13

  clock clk (rise edge)                   0.00   0.00
  clock network delay (ideal)             0.00   0.00
  clock reconvergence pessimism           0.00   0.00
  state_reg[1]/CLK (DFFPOSX1)                    0.00 r
  library hold time                       0.00   0.00
  data required time                             0.00
  ---------------------------------------------------------------
  data required time                             0.00
  data arrival time                             -0.13
  ---------------------------------------------------------------
  slack (MET)                                    0.13


  Startpoint: brake (input port clocked by clk)
  Endpoint: state_reg[0]
             (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                   Incr   Path
  ---------------------------------------------------------------
  clock clk (rise edge)                   0.00   0.00
  clock network delay (ideal)             0.00   0.00
  input external delay                    0.00   0.00 f
  brake (in)                              0.06   0.06 f
  U44/Y (OAI21X1)                         0.08   0.14 r
  state_reg[0]/D (DFFPOSX1)               0.00   0.14 r
  data arrival time                              0.14

  clock clk (rise edge)                   0.00   0.00
  clock network delay (ideal)             0.00   0.00
  clock reconvergence pessimism           0.00   0.00
  state_reg[0]/CLK (DFFPOSX1)                    0.00 r
  library hold time                       0.00   0.00
  data required time                             0.00
  ---------------------------------------------------------------
  data required time                             0.00
  data arrival time                             -0.14
  ---------------------------------------------------------------
  slack (MET)                                    0.13
```

```
    Startpoint: resume (input port clocked by clk)
    Endpoint: cruisectrl_reg
             (rising edge-triggered flip-flop clocked by clk)
    Path Group: clk
    Path Type: min

    Point                                         Incr    Path
    ----------------------------------------------------------------
    clock clk (rise edge)                         0.00    0.00
    clock network delay (ideal)                   0.00    0.00
    input external delay                          0.00    0.00 r
    resume (in)                                   0.05    0.05 r
    U40/Y (AOI22X1)                               0.06    0.11 f
    U38/Y (OAI21X1)                               0.07    0.18 r
    cruisectrl_reg/D (DFFPOSX1)                   0.00    0.18 r
    data arrival time                                     0.18

    clock clk (rise edge)                         0.00    0.00
    clock network delay (ideal)                   0.00    0.00
    clock reconvergence pessimism                 0.00    0.00
    cruisectrl_reg/CLK (DFFPOSX1)                         0.00 r
    library hold time                             0.00    0.00
    data required time                                    0.00
    ----------------------------------------------------------------
    data required time                                    0.00
    data arrival time                                    -0.18
    ----------------------------------------------------------------
    slack (MET)                                           0.18

Warning: report_timing has satisfied the max_paths criteria. There are 17 further endpoints
which have paths of interest with slack less than  5.00 that were not considered when
generating this report. (UITE-502)

1
```

3. Automatic Place and Route

    a. Standard cells: **302**, Total wire length: **9148** um, Total vias: **1572**

    b. innovus.log excerpt

```
#Complete Global Routing.
#Total wire length = 9148 um.
#Total half perimeter of net bounding box = 10143 um.
#Total wire length on LAYER metal1 = 255 um.
#Total wire length on LAYER metal2 = 2938 um.
#Total wire length on LAYER metal3 = 3705 um.
#Total wire length on LAYER metal4 = 1500 um.
#Total wire length on LAYER metal5 = 750 um.
#Total wire length on LAYER metal6 = 0 um.
#Total number of vias = 1572
#Up-Via Summary (total 1572):
```

    c. Screen capture