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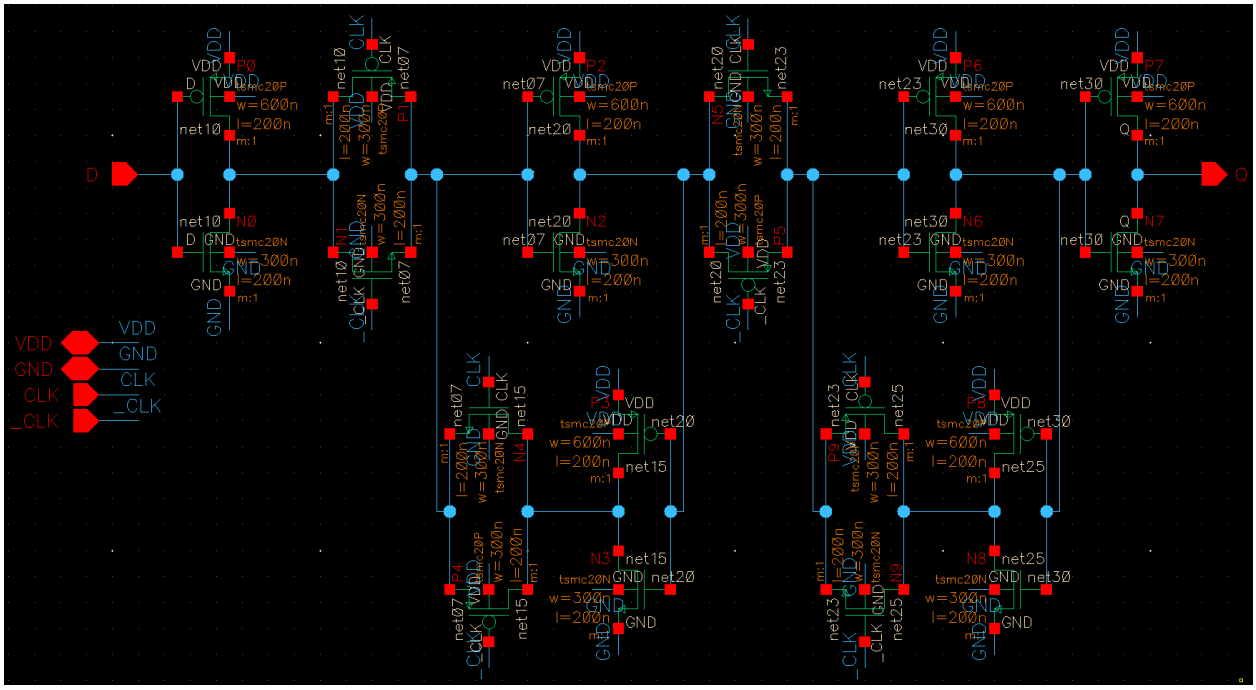
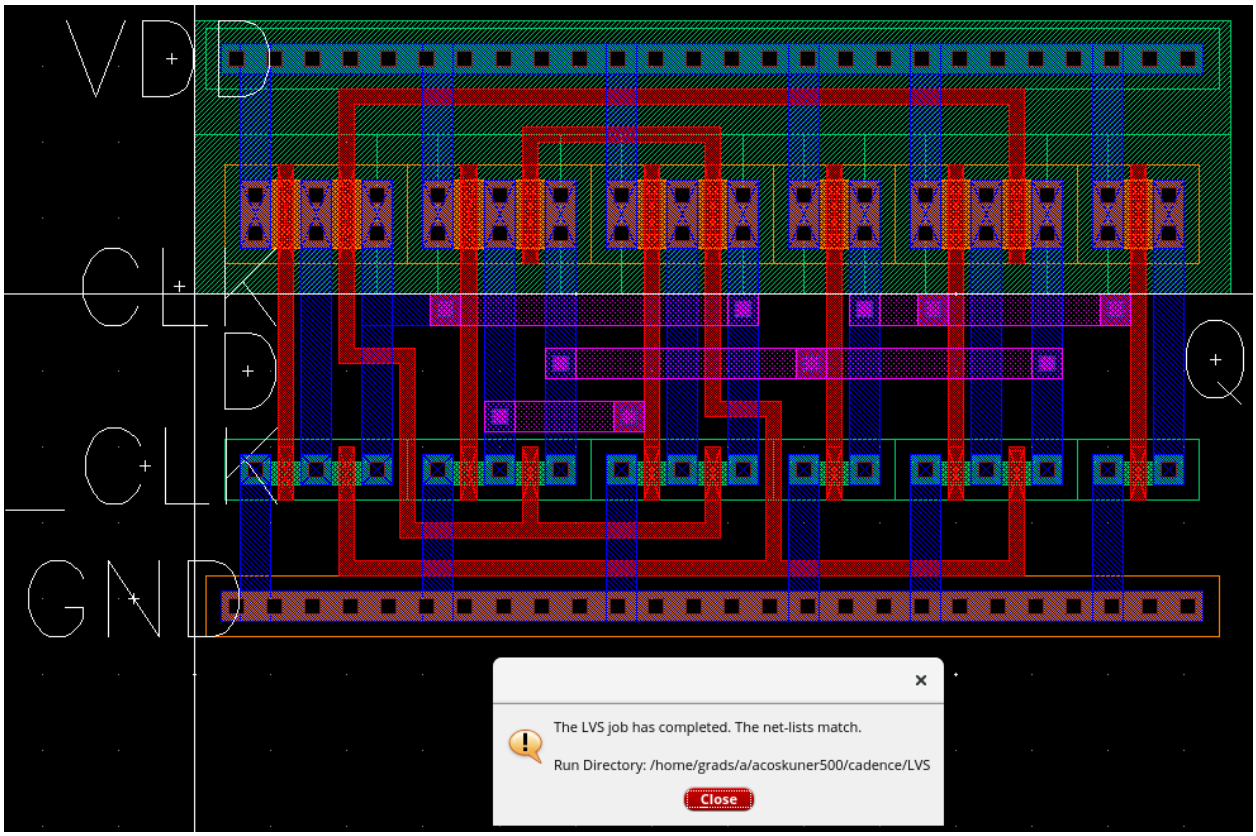
ECEN 714-612 Lab 6

1. Flip Flop (Schematic, Layout, LVS)



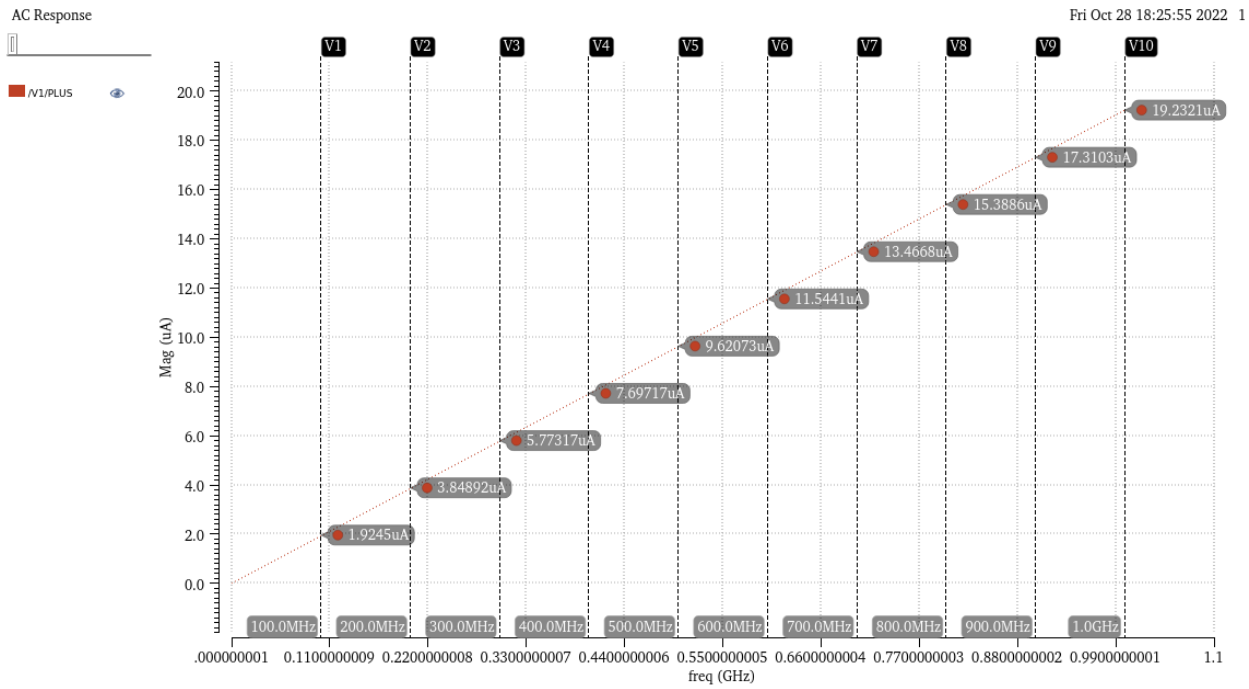


2. Cell Delay Table

Capacitance [fF]	Rise Time [ns]	Fall Time [ns]	Rising Delay [ns]	Falling Delay [ns]	% Error
100	10.8759	21.0667	0.6259	0.6167	1.469883368
90	10.8318	21.0225	0.5818	0.5725	1.598487453
80	10.7882	20.9785	0.5382	0.5285	1.802303976
70	10.7438	20.9346	0.4938	0.4846	1.863102471
60	10.7001	20.8906	0.4501	0.4406	2.11064208
50	10.6561	20.8468	0.4061	0.3968	2.290076336
30	10.5676	20.7587	0.3176	0.3087	2.802267003
20	10.5232	20.7144	0.2732	0.2644	3.221083455
10	10.478	20.6685	0.228	0.2185	4.166666667
1	10.4307	20.6183	0.1807	0.1683	6.862202546

3. Sink Capacitance

Frequency	**Current [µA]**	**Capacitance [fF]**	**Frequency**	**Current [µA]**	**Capacitance [fF]**
100 MHz	1.9245	3.06293688	600 MHz	11.5441	3.062167631
200 MHz	3.84892	3.062873218	700 MHz	13.4668	3.061868268
300 MHz	5.77317	3.062761809	800 MHz	15.3886	3.061464697
400 MHz	7.69717	3.062606633	900 MHz	17.3103	3.061133124
500 MHz	9.62073	3.062373471	1 GHz	19.2321	3.060883781
AVG = **3.062106951**					



4. Setup Time

setup_r	10n-**9.87n** = 0.13n
setup_f	20n-(10n+**9.75n**) = 0.25n
Setup Time	**0.25n**