ECEN 454/714 – Lab8: Design of 8-bit pipelined Adder with Buffered H-clock Tree

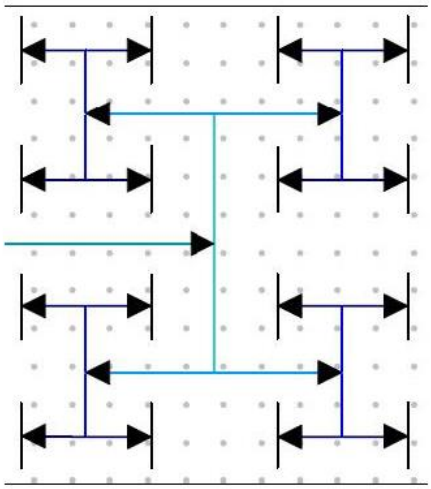
1. Introduction

At this stage you must have completed the design and verified the operation of all the logic (combinational and sequential) that you would need to complete the design of the 8-bit pipelined adder. Over the next two lab sessions you would be required to use these elements to complete the design of the pipelined adder.

2. H-clock tree

The design involves many sequential elements (Flip-Flop's) and it has to be made sure that they operate synchronously. To ensure this, the clock signal has to arrive at all the Flip-Flops at the same time i.e., to say the skew between the Flip-Flops must be zero or as close to zero as possible. This can be achieved by (i) maintaining the same wire length from the clock source to the destination and (ii) maintaining equal load at the receiving end of these wires (carrying the clock signal). This ensures that the propagation delay for signals following different paths will be similar. Any differences will manifest themselves as clock skew (the larger the differences the larger the skew will be).

The H-clock tree distribution method which distributes the clock signal through a hierarchy of "H" shaped structures is a commonly used technique to implement the zero clock skew requirements of the design. An example of a buffered H-clock tree structure is shown below.



The clock signal is applied to the center of the first "H" in the tree design and the clock signal appears at the corners of the first "H" at the same time since their path lengths are equal and the loads at the respective ends are balanced. This signal forms the source of the next "H" in the hierarchy. **Buffers are inserted at the intersection of the two successive hierarchy levels to reduce the latency of the clock signal.** The widths of the metal lines forming the H also become progressively smaller asthe signal travels down the hierarchy. **The widths of the metal lines become half the size of the line used in its predecessor "H".** This technique is generally used to avoid the formation of standing waves due to mismatched impedance at the terminals of the lines.

3. Construction of the 8-bit Pipelined Adder

• Use the buffered H-tree clock distribution scheme to provide clock signals to the sequential elements in your design. You may use the inverter standard cell that you designed earlier as buffers (You have to take care of the CLK and CLK_BAR logic appropriately).

• Draw just one H-tree clock network for CLK signal. Then, CLK_BAR can branch off from the network through an inverter at the front of CLK_BAR input pin of Flip-Flop.

• It would be easier for you to complete the design in stages. Otherwise, the number of issues you may face at the end of the whole design (when you perform a LVS check) could be overwhelming. You can start of by completing the layout for the first quarter of the circuit i.e. the sum of the first four bits (a3-a0 + b3-b0). This may include 4-bit adder logic and the flip flops that carry the "sum" (s3-s0) to the output pins. Perform regular DRC checks as you are implementing the layout.

NOTE: The levels of hierarchy depend on the number of flip flops in the design. It is difficult to design a perfectly symmetrical H tree since we have an odd number of flip flops. No need to perform a perfect H tree, and just try to balance it reasonably.

• After completing the layout of the first stage, perform a LVS check. It will be easier to deal with issues stage wise rather than facing them all at once towards the end.

• Complete the entire design in this manner. The above procedure to complete the design process is only a suggestion. You are the best judge to divide the process into appropriate stages and complete your design.

• 8-bit adder consists of 2 4-bit adders, 13 FFs, and inverters.

4. Report Requirements

1. Schematic, Layout, and LVS Report of 8-bit adder design.

2. Perform post-layout transient simulations for a period of 30ns with the following inputs vectors. Please apply the approach to generate input signal switching which we used at the last lab with Flip-Flop design. ie., please adjust all input signals switching simultaneously. Please clearly notify how you control CLK signal, and when the answer is generated from your adder circuit.

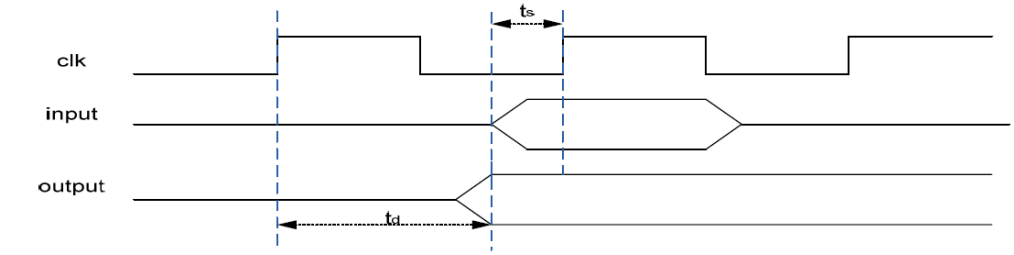
Plot an individual waveform for each input case. Please check if the answer is logically correct,

A) 0111 1110 + 1110 0111 + 0

B) 1111 1111 + 0000 0000 + 1

3. For each of the cases find the best possible clock period (take into account the setup time

constraint for the FF acquired in Lab7 and the clk-output delay of your 8-bit adder) and frequency. For each case, please measure **power consumed from VDD** at the circuit's peak performance, i.e. at its highest frequency.



$$t_s \geq t_{setup}, \quad t_d \geq \max(t_{delay}), \quad t_{clk} \geq t_s + t_d$$

t_d is the delay between clk rising edge and the output signal.

4. Report the total layout area. Please use a ruler by selecting "Tools>Create Ruler" or using a hot key "k". Unit of the ruler is micrometer (10^{-6} m), and please report the area of a minimum rectangle which covers whole of the layout of your 8-bit adder design.

Lab 8 Rubric:

1. Schematic, Layout, LVS report for 8-bit adder (2+3+2)
2. Post layout simulation with concise explanation (0.5*2)
3. Find best clock period for both input combinations (1)
4. Total area (1)