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## ECEN 714-612 Lab 4

### 1. Inverter Changes (Schematic, Layout, LVS)

The image displays the Cadence Virtuoso interface for an inverter design. The top window shows the schematic editor with an inverter circuit. The input 'in' is connected to the gate of a PMOS transistor (P0) and the gate of an NMOS transistor (N0). The PMOS transistor has parameters:  $t_{smc}20P$ ,  $w=900n$ ,  $l=200n$ , and  $m:1$ . The NMOS transistor has parameters:  $t_{smc}20N$ ,  $w=300n$ ,  $l=200n$ , and  $m:1$ . The output 'out' is connected to the drains of both transistors. The schematic is connected to VDD and GND power supplies.

The bottom window shows the layout editor with the physical layout of the inverter. The layout includes the PMOS and NMOS transistors, their gates, and the output node. The layout is connected to VDD and GND power supplies.

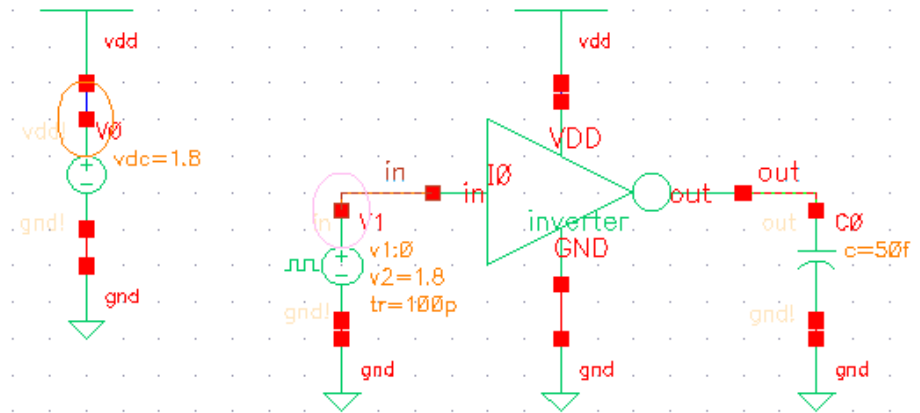
The bottom status bar shows the LVS job completion message:

```
LVS job is now started...  
The LVS job has completed. The net-lists match.  
Run Directory: /home/grads/a/acoskuner500/cadence/LVS
```

A dialog box is displayed with the message: "The LVS job has completed. The net-lists match. Run Directory: /home/grads/a/acoskuner500/cadence/LVS". The dialog box has a "Close" button.

## 2. Inverter simulation

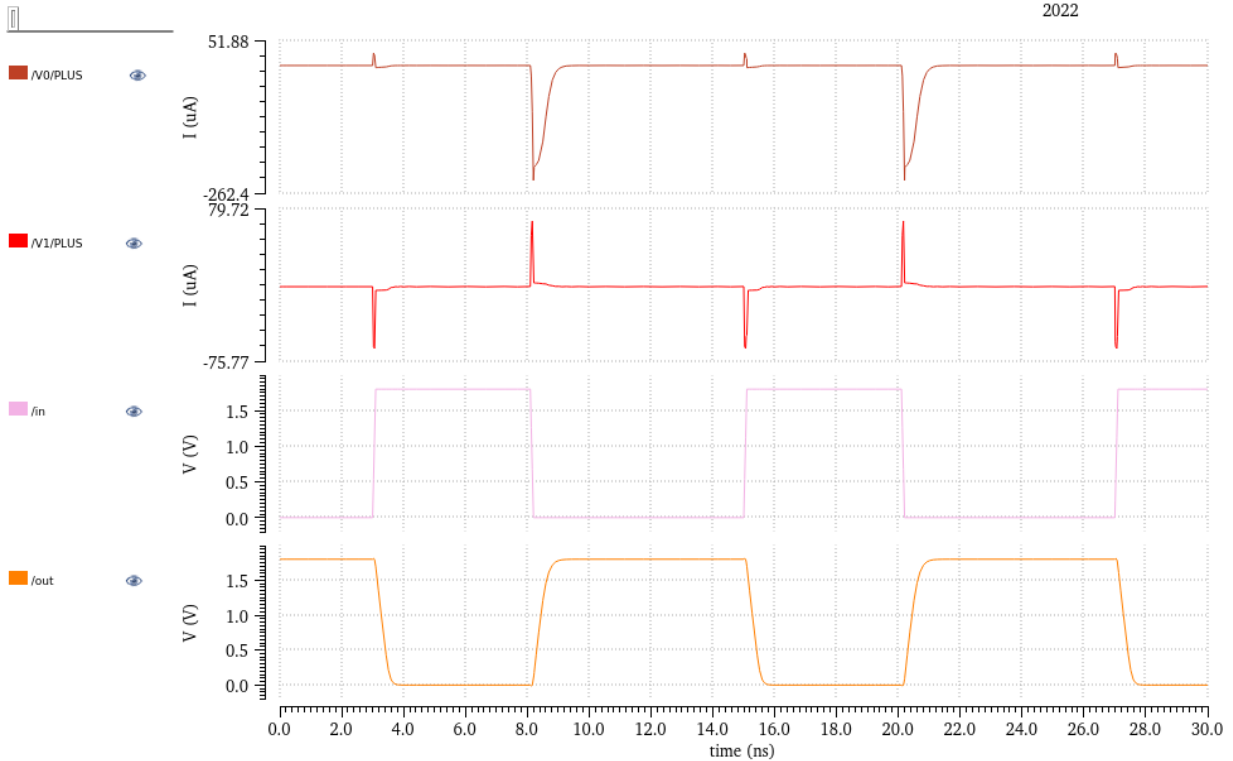
Inverter power VDD	-11.60E-6
Inverter vpulse average power	-183.2E-9
Inverter rising delay	8.150E-9    264.1E-12 20.15E-9    264.1E-12
Inverter falling delay	3.050E-9    257.1E-12 15.05E-9    257.1E-12 27.05E-9    257.1E-12



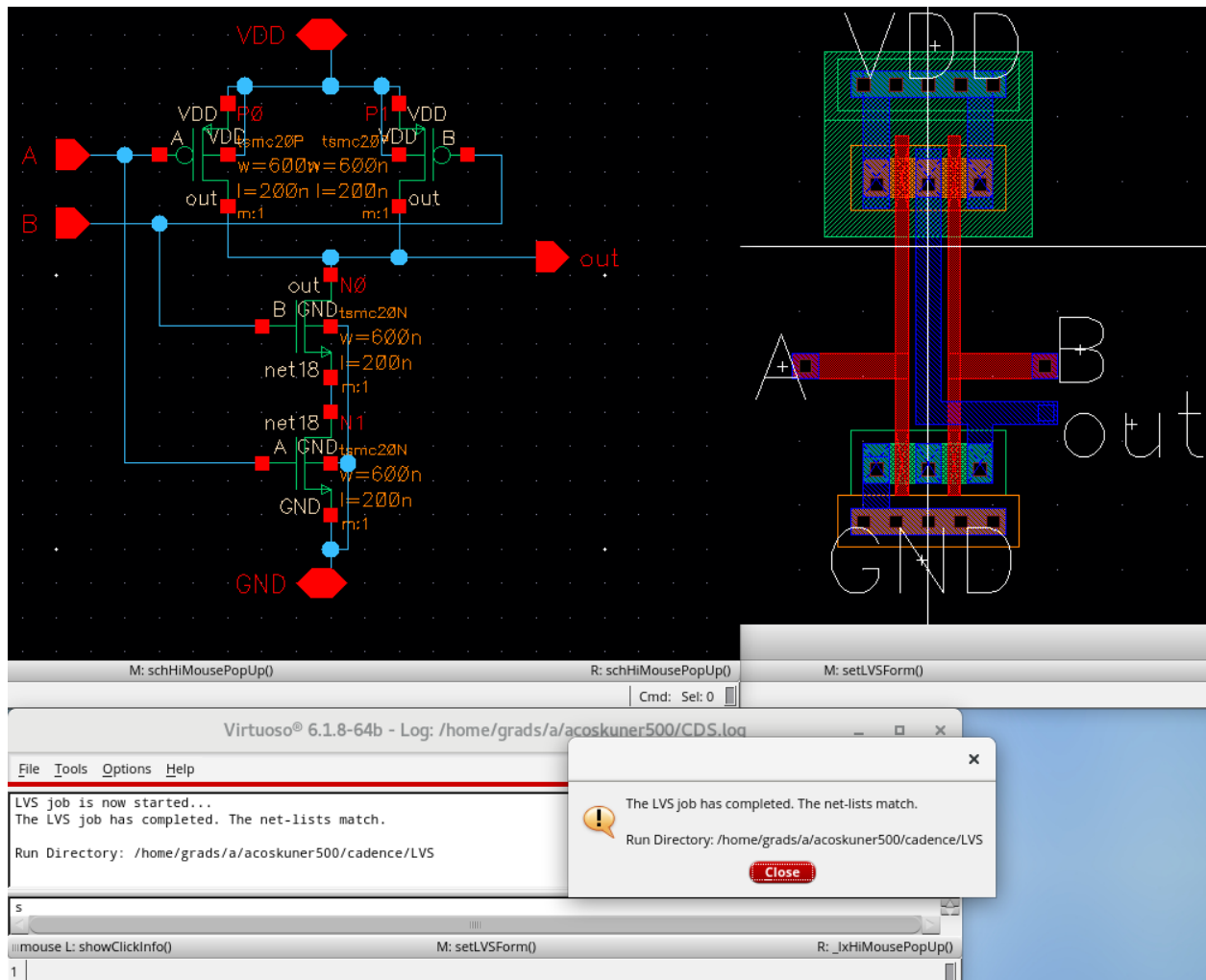
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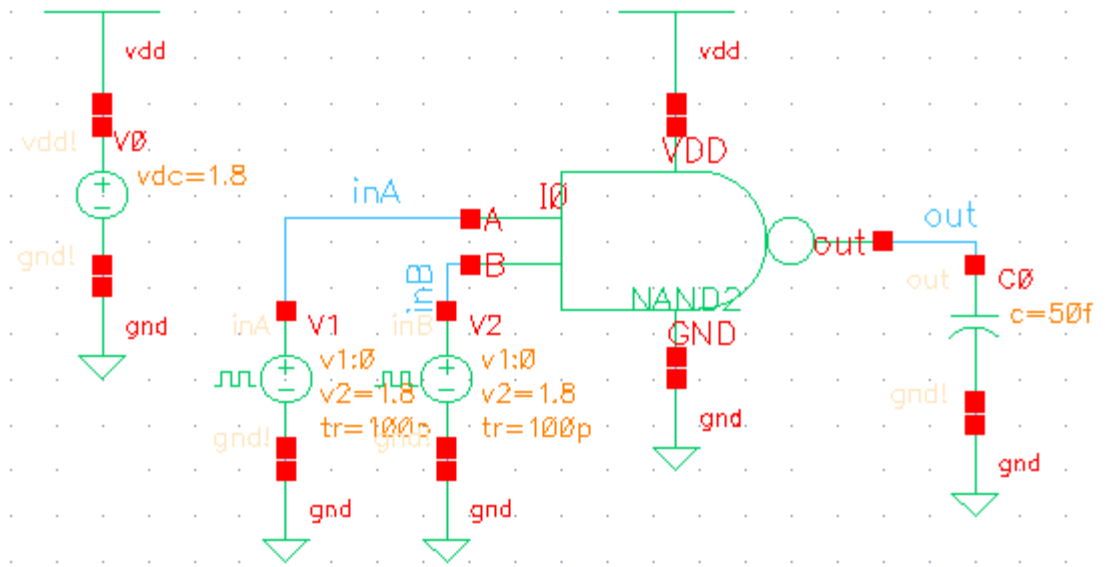


### 3. NAND2 Changes (Schematic, Layout, LVS)



### 4. NAND2 Simulation

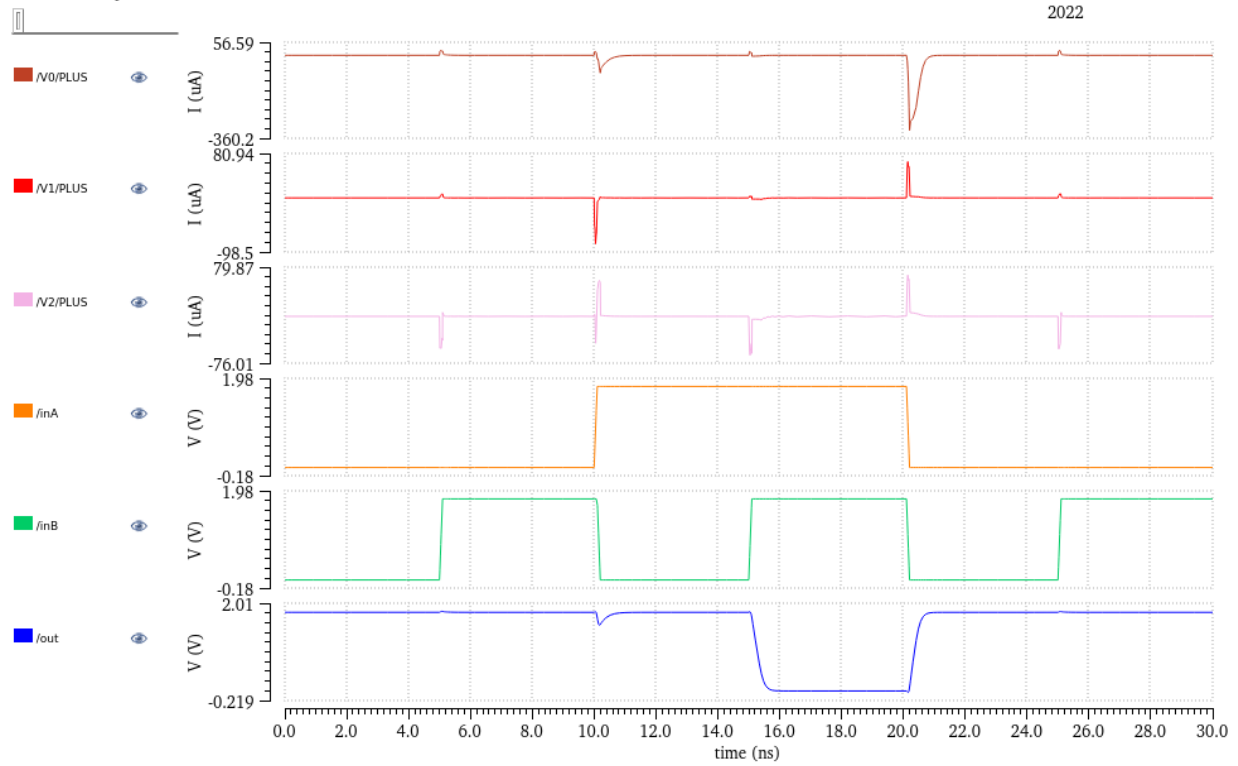
NAND2 power VDD	-6.865E-6
NAND2 inA vpulse average power	11.46E-9
NAND2 inB vpulse average power	-125.5E-9
NAND2 rising delay	2.09E-10
NAND2 falling delay	2.27E-10



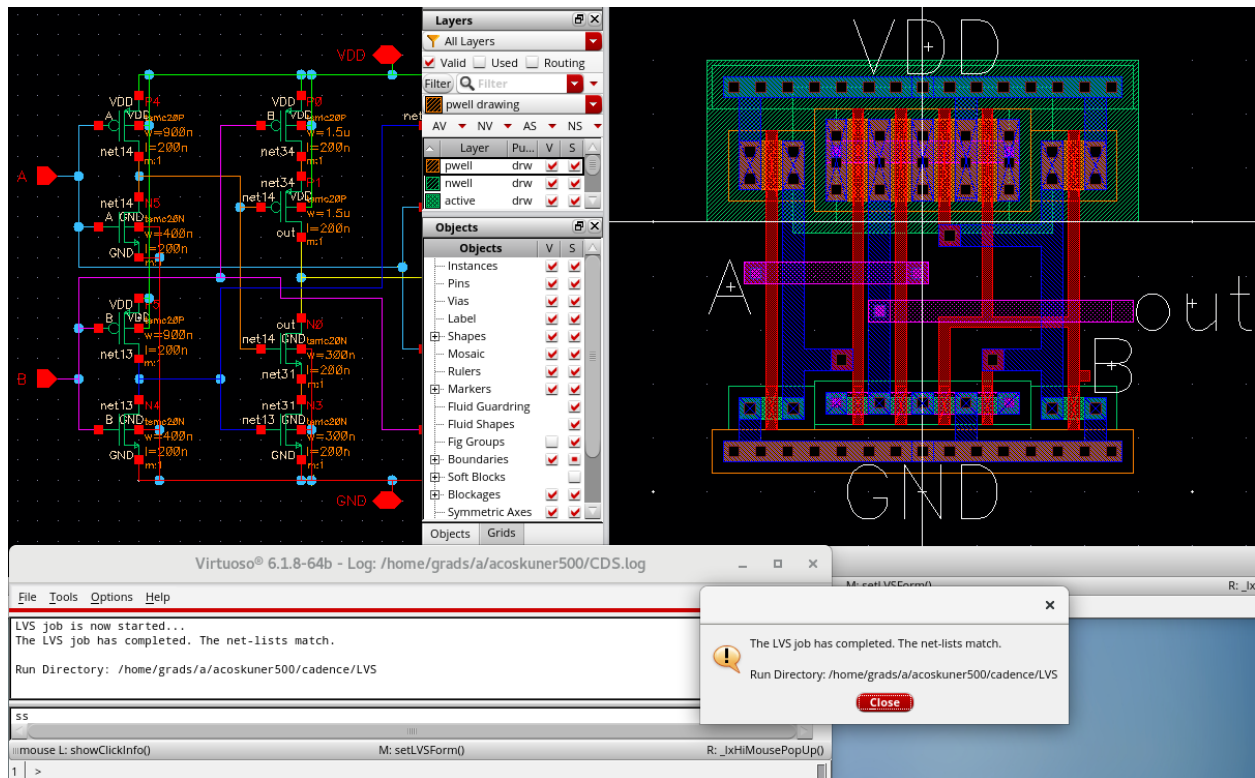
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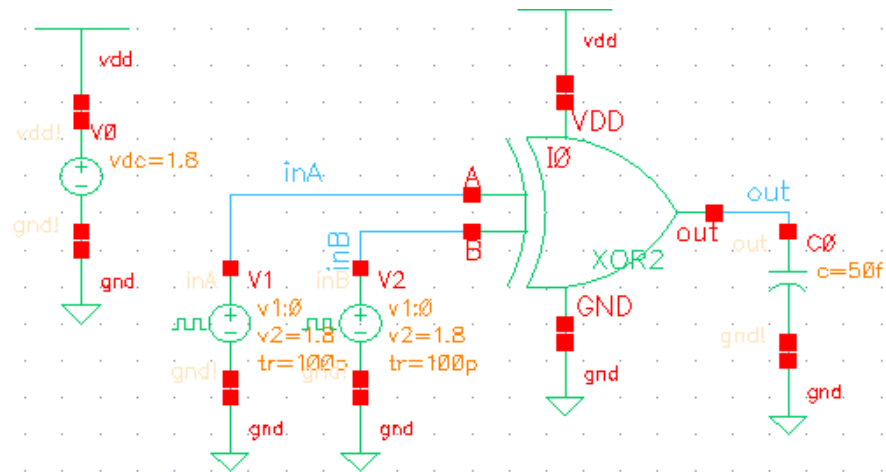


## 5. XOR2 Changes (Layout, LVS; no change to schematic)



## 6. XOR2 Simulation

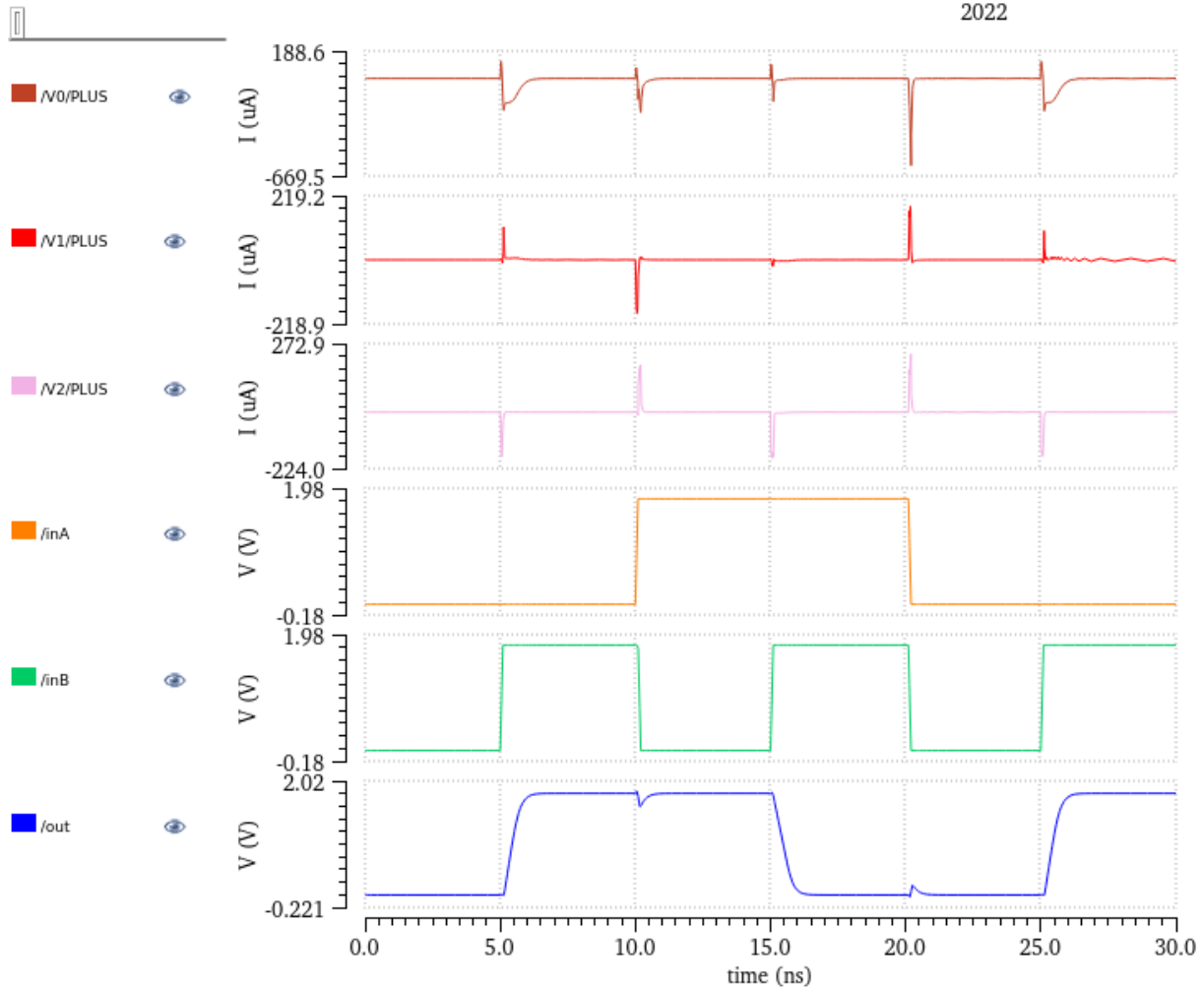
XOR2 power VDD	-17.05E-6
XOR2 inA vpulse average power	128.4E-9
XOR2 inB vpulse average power	-472.8E-9
XOR2 rising delay	3.85E-10
XOR2 falling delay	4.19E-10



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## 7. 1-bit adder (schematic, layout, DRC, LVS)

The image displays the Cadence Virtuoso environment for a 1-bit adder project. The top window shows the schematic of the adder, which uses three 2-input XOR gates (labeled XOR2) and two 2-input NAND gates (labeled NAND2). The inputs are A, B, and C. The outputs are SUM and CARRY. The schematic is connected to VDD and GND power rails.

The bottom window shows the layout of the adder, with the same components and connections as the schematic. The layout is color-coded to show different layers and materials.

The bottom status bar shows the Virtuoso version: Virtuoso® 6.1.8-64b - Log: //

The bottom status bar also shows the LVS job completion message:

File Tools Options Help

Getting schematic property bag  
Getting schematic property bag  
Getting schematic property bag  
LVS job is now started...  
The LVS job has completed. The net-lists match.

Run Directory: /home/grads/a/acoskuner500/cadence/LVS

The LVS job has completed. The net-lists match.

Run Directory: /home/grads/a/acoskuner500/cadence/LVS

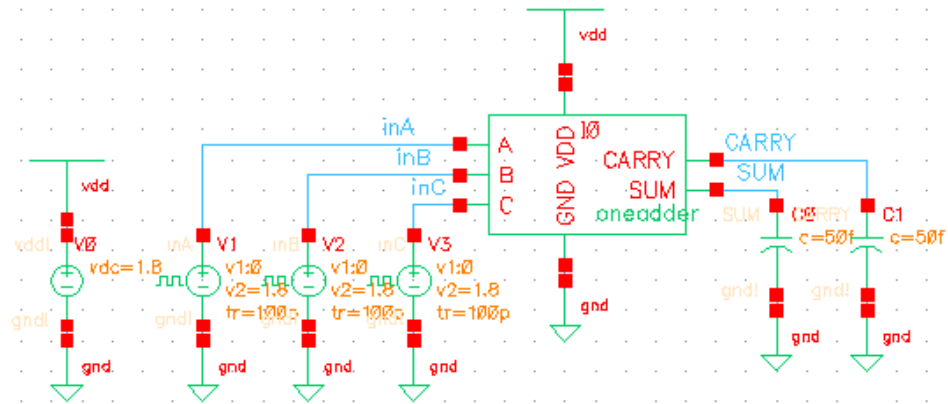
Close

mouse L: showClickInfo() M: schHiMousePopUp() R: schHiM

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## 8. 1-bit adder Simulation

Full Adder VDD Average power	-33.89E-6
Full Adder inA vpulse average power	-461.7E-9
Full Adder inB vpulse average power	-596.4E-9
Full Adder inC vpulse average power	-419.2E-9
Full Adder SUM rising delay	4.00E-10
Full Adder SUM falling delay	4.28E-10
Full Adder CARRY rising delay	4.37E-10
Full Adder CARRY falling delay	3.37E-10

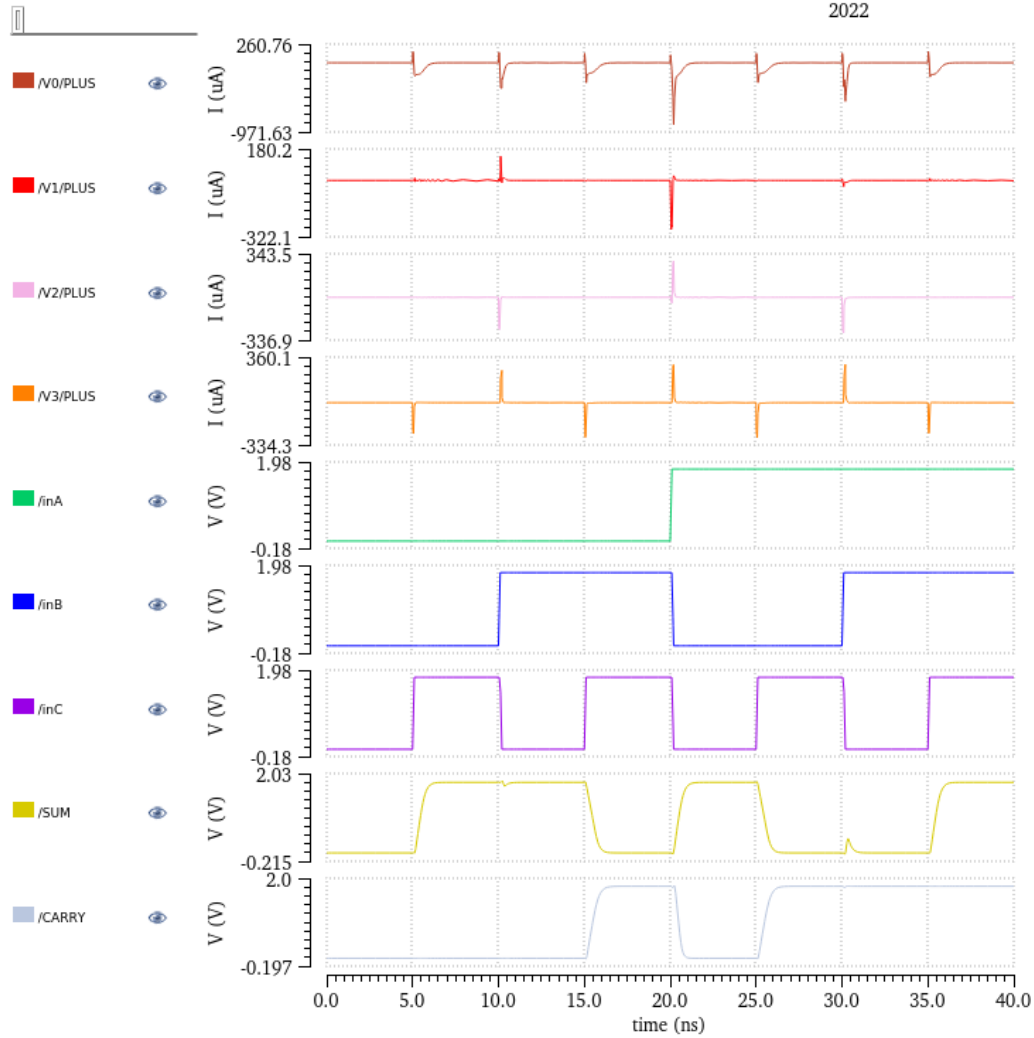




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## 9. 1-bit Adder Max Frequency: $1/3\text{ns} = 333\text{MHz}$

