ECEN 454 - Lab2: Cadence Custom layout: Design Rules, Extraction, and Verification

1. Introduction

In this lab you will create the physical layout of all the logic gates (Inverter, NAND2, and XOR2) that you used in the previous labs. This lab manual contains instructions to draw the schematic and layout of a basic inverter circuit. You will also perform extraction of the layout parameters and verifying if the layout drawn is equivalent to the schematic (of the corresponding gate) through an LVS (Layout versus schematic) check. You would have to implement the same for the other required gates. Make sure you have attached the "NCSU_TechLib_tsmc02" technology file to your library before you begin the lab. This technology will use design rules based on the 0.2 µm technology from TSMC. This means that the smallest feature size that can be implemented is 0.2 µm. All the layout dimensions would be in terms of "λ" which is equal to half the feature size (0.1 pm in this case).

2. Inverter circuit

a. Schematic view

• In the Library Manager window, please select "Design" library, and then File > New > Cell View. Create a cell named "inverter" in the "Design" library with its "schematic" view as seen in Figure 1.

Figure 1. Creating a new schematic cell view of inverter

- After the schematic window opens, we wish to add two transistors to form an inverter circuit. Select Create > Instance (keyboard shortcut: i) to open "Component Browser" window. (If you cannot use the shortcut, or "Component Browser" window won't come up, just ask TA. This implies your cadence setup has some problem.) Make sure that "NCSU_Analog_Parts" is selected in Library list as shown in Figure 2. Let us add a PMOS tranasistor first. Please select "P_Transistors" in the list, and you will find "PMOS4" from the list of P_Transistors. Switch to the schematic window again and click a position where you would like to add a PMOS transistor. In a similar way, you can add NMOS transistor in your schematic from Component Browser by selecting "NMOS4" from the list of N_Transistors. Press ESC to escape from Add Instance mode.

- Connect components with wires by selecting Add > Wire or use the “w” shortcut.

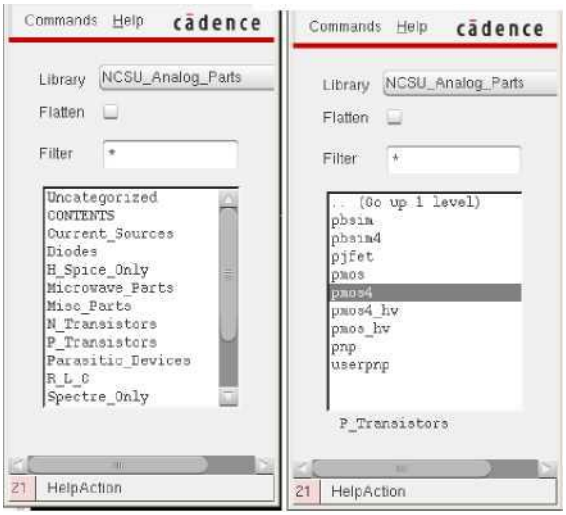


Figure 2. Adding a PMOS transistor from Component browser

- Add pins and give proper directions and names. Select Create > Pin or use the “p” shortcut. Please be very careful when you put name and direction of each pin since those must be consistent between schematic, layout, and symbol. For the power pins, DO NOT use the VDD and GND symbols. Instead, create two “inputOutput (Direction of pin)” pins with the names VDD or GND.

- To change the properties of a component, click Edit > Properties > Objects or use the “q” shortcut. Please try to change the width of transistors. To give similar logical strength to both rising and falling output, the width of a PMOS transistor will be at least twice larger than that of an NMOS transistor.
- When completed, please check your schematic with a sample circuit given in Figure 3.

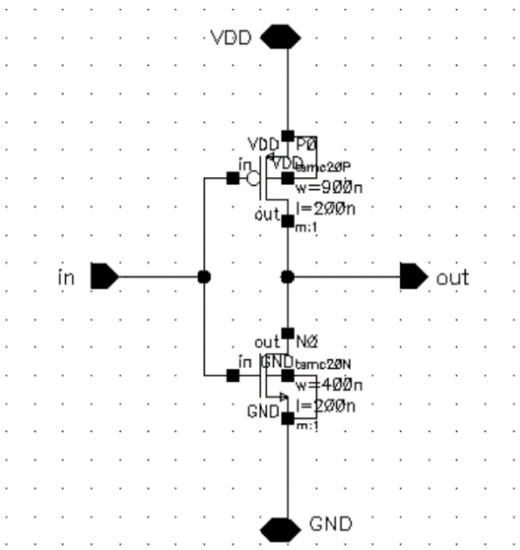


Figure 3. Inverter schematic

- Select File> Check and Save to verify your design and save it. Make sure you don't see any errors or warnings.

b. Symbol view

In the schematic view window, please select Create > Cellview > From Cellview. A window as Figure 4 will open. Press OK.

Figure 4. Create symbol from schematic view

- The symbol which is initially created will look like Figure 5. Please modify the symbol so that it resembles a general symbol of inverter as given in Figure 6 (See appendix). Then save it.

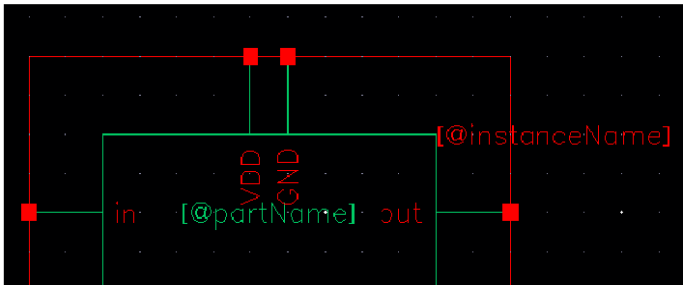


Figure 5. Default symbol of inverter

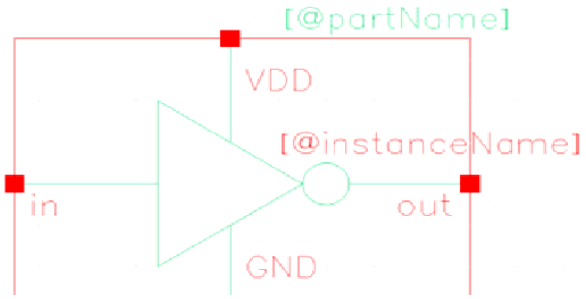


Figure 6. Complete inverter symbol

c. Layout view

- After the schematic and symbol of an inverter circuit are done, next step is to design layout. Create a new "layout" view by File > New > Cell View, and selecting “layout” as the type, as shown in Figure 7. The Virtuoso layout editor window and the layer selection window (LSW) window will pop up.

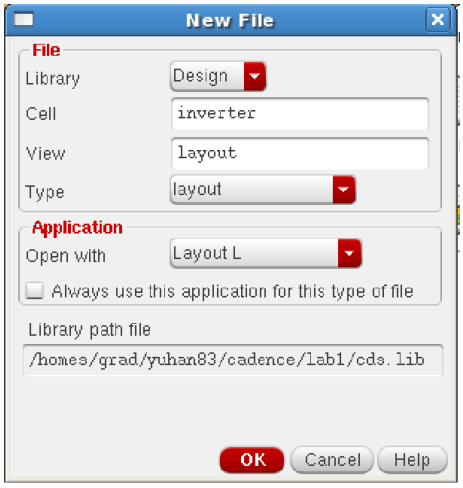


Figure 7. Creating a new layout view for the inverter

- You need a proper display setting to see the names of your pins. Select Options > Display and in "Display Controls" darken "Pin Names".

- You will draw the inverter layout in the layout editor window. You can change background grid resolution in "Options > Display" at “Minor Spacing” and “Major Spacing”. It is a good choice if you set Minor Spacing to 0.1 and set the Major Spacing to 0.5. However, do not change value at “X Snap Spacing” and “Y Snap Spacing” since that corresponds to your design rules. MOSIS Scalable design

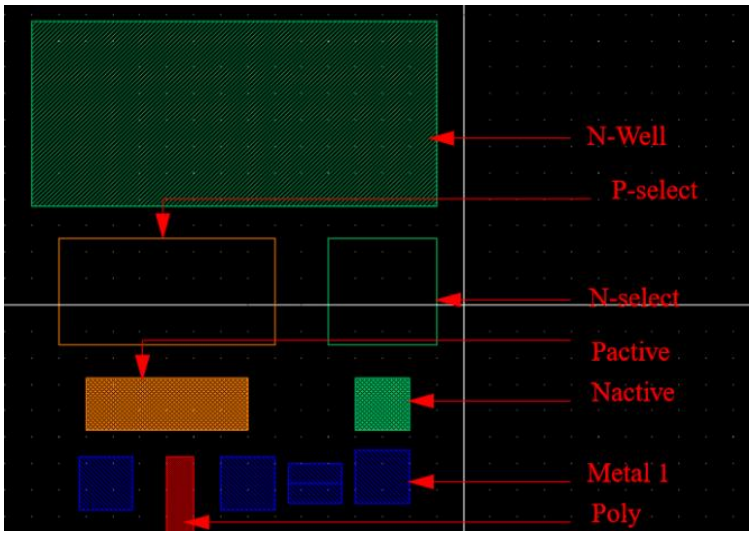


Figure 8. Common layers required to build a layout circuit

rules require that layout is on a 1/2 lambda grid. For the technology you used, since lambda = 0.10 um then minimum grid in X and Y Snap Spacing is 0.05 um as you see.

- When drawing CMOS transistors, please use the pre-drawn cells of NMOS and PMOS transistors found in NCSU_TechLib_tsmc02 technology library. Following directions show how to add the cells in your cell view.

- Select Create > Instance or use the "i" shortcut. Then, please look for "NMOS" or "PMOS" cell in the NCSU_TechLib_tsmc02 library. The "create instance" window looks as Figure 9. One important parameter in the window which you need to update is "Width". Please fill in the actual width of the transistor used in the schematic view. Go back to layout editor window and click any point where you would like to put the transistor on.

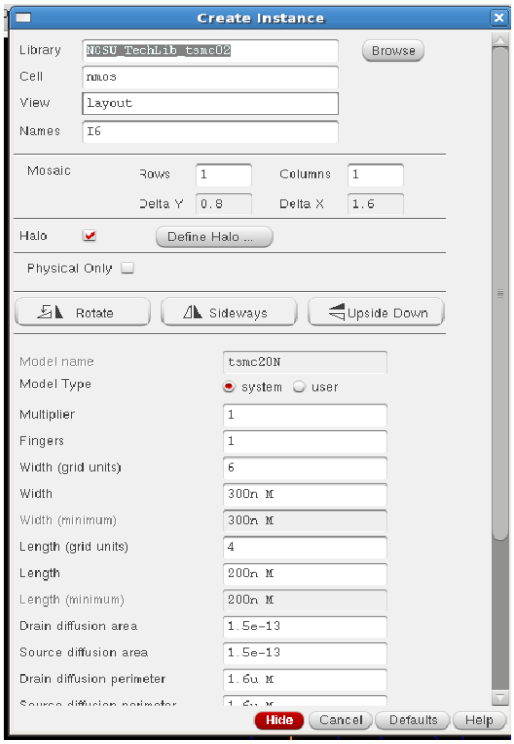


Figure 9. Adding a pre-drawn NMOS transistor layout into

- Another useful parameter in the "create instance" window (Figure 9) that you can apply in a larger design with many transistors is "Multiplier". Please try using this parameter later for the **NAND gate**.

- When you add a new NMOS or PMOS to a layout or reopen a saved layout from Library Manger, you may only see the component names like "PMOS" or "NMOS", in a rectangle. In this case, press "shift + f" on the layout editor window, then the layout with layers you expected will show up.

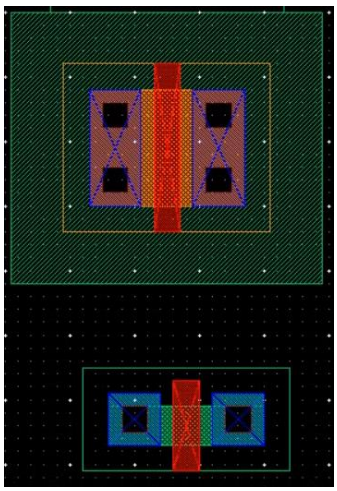


Figure 10. layout after adding pre-drawn NMOS (bottom) and PMOS (top) transistors

- To add wires to connect components, please draw rectangles with proper layer type. Click a layer type in LSW window (left side panel) and select "Create > Shape>Rectangle" or use "r" hot key.
    - A cell of transistor has 3 terminals: drain, source, and gate (Actually 4 terminals including substrate contact. Let us discuss this later). Layer type of drain and source is "Metal 1", and layer type of gate is "Poly".
    - Do not overlap or cross **same type** of wires if they are not electrically connected. Feel free to use "Metal 1" and "Metal 2" layers to interconnect complicated connection. In this case, please use contacts described below to connect 2 different layers.

- To insert contacts to connect 2 different layers, please select "Create > Instance" or use the "i" hot key (you could consider contact is a special instance like mos). Choose a proper Contact Type according to the layers you are connecting. Please refer to the **Figure 11** as an example which is creating a contact between "Metal 1" layer and "Poly" layer by choosing "m1_poly".
    - A transistor has a substrate, and you need to add contacts to connect the substrate to VDD or GND.
    - NMOS transistor has P-substrate (black area in the layout) and should have a contact between P and GND rail.
    - PMOS transistor has n-well substrate and should have a contact between N and VDD rail.
    - Try "Columns" parameter to extend the number of contacts which are serially connected.

- To create the power and ground rails for our inverter we need to add different contacts and expand the nwell area. Usually a circuit consists of many cells (gates), all of which need power and ground connections. Therefore, it is common to design cells with the same spacing between the power and ground so that they can easily connect together when placed side by side. This vertical spacing is called the **cell *pitch*** and it is generally standardized for all cells in the same library to facilitate combining cells in higher-level circuits.

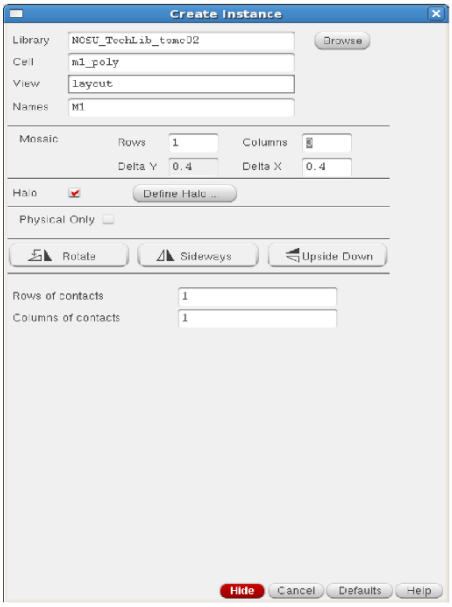


Figure 11. Adding a contact

- Figure 12 shows the types of contact used for building the power rail. After placing the m1_n contact and m1_p contact, expand the nwell area by selecting nwell from the left panel and creating a rectangle to cover the m1_n contact and PMOS transistor.

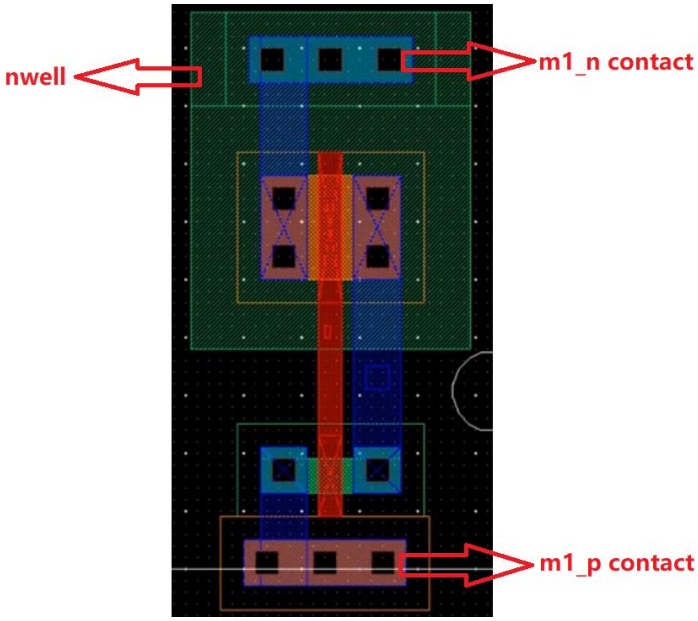


Figure 12.

- After placing the transistors and the power rails, we will connect transistor nodes to match the inverter schematic.
- In Figure 12, poly layer is used to connect the poly gate inputs of NMOS and PMOS transistors. Select layer M1 to:
    1. connect the source of the NMOS to GND rail.
    2. connect the source of the PMOS to VDD rail.
    3. connect the drains of the NMOS and PMOS transistors together.

- To add a pin, select Create > Pin. A several points you need to carefully check when adding a pin is given below. Please follow those carefully at all times, since a bunch of errors are coming from here. Refer to the Figure 13 as an example.
    - In the blank of "Terminal Names", make sure you type the same name in the schematic view. It is case sensitive. Select "**Display Terminal label**" option on, then the pin name will appear in the layout.
    - "I/O type" should be the same as defined in the schematic view.
    - "Pin Type" should be the layer to which the pin is connecting. Please do check which layer it should be. Pay attention that when you draw a pin, the corresponding layer should be selected on left side "layers" window.
    - Then drag a rectangular on the place where you want to put your pin.

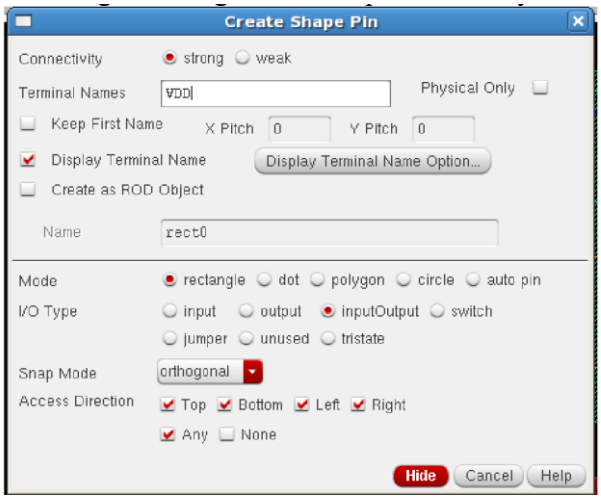


Figure 13. Adding a pin to layout

- After completing the above steps, your layout should resemble an example layout given in Figure 14.

- The position where pins are actually connected should be inside the layer where you specified when adding the pin, you could also verify whether the connection is correct by checking the character color of pin is the same as the color of the related layer.

- Please note that the substrate of each transistor is certainly connected to VDD or GND through contacts, as shown in Figure 14.

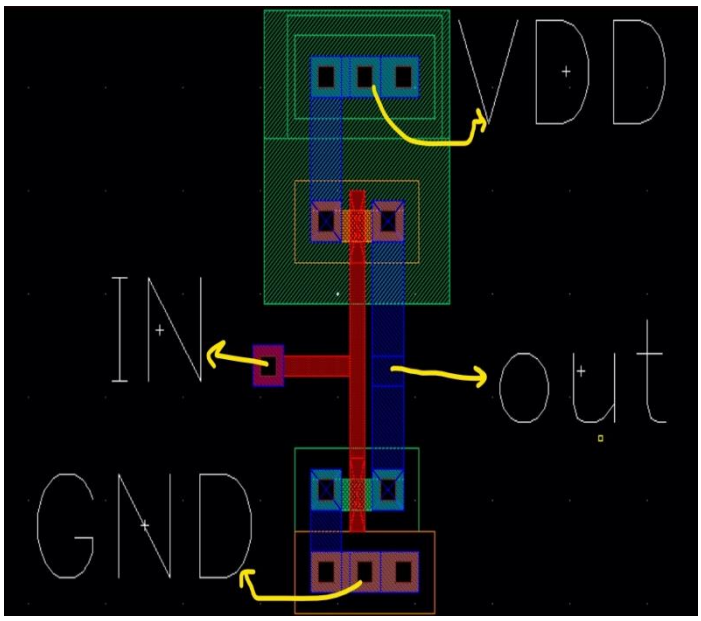


Figure 14. Inverter layout

3. Performing the Design Rule Check (DRC)

- Now that you have finished the layout, let's verify to see if this meets the design rule requirements. For this you will use the Design Rule Check (or DRC). It is considered to be a good practice to perform DRC periodically instead of waiting till the end, as you can have lot of errors to fix at the end. It is a lot easier to fix errors occasionally than to fix all the errors at the end.

- To start DRC choose "Verify > DRC". The DRC form appears. Click OK on the DRC form.
- In case you have errors: You should see various messages flashing in the CIW after which some error messages appear. The message looks something like the following.

  DRC started ..... Thu Jun 3 20:57:01 2008
  Completed ....Thu Jun 3 20:57:01 2008
  CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
  ********* Summary of rule violations for cell "inverter layout" *********
  # errors Violated Rules
  2 (SCMOS_SUBM Rule 2.3) source/drain active to well edge: 0.60 um 2 Total errors found

There are several markers in white color in the layout, which tell where the errors occurred.

- Choose "Verify > Marker > Explain" and click on the marker to find out what the error is. A window pops up explaining the error. This is particularly useful when you have more than one type of error. Close the pop up window explaining the errors. Also delete the markers using "Verify > Marker > Delete All". Referring to the design rules violated, fix the errors. The error message in the above example means, the minimum spacing between active to well is 0.6u (6 lambda). To fix the error,

move the NMOS transistor down until the spacing is satisfied. Note after moving, check DRC again, and adjust your design if new errors appear.

5. Layout Extraction

- Choose "Verify > Extract" in the layout window, then extract window appears. Click on the "set switches" option, select "Extract_parasitic_caps", and click OK. If you see the Extractor window as Figure 15, click OK, and the extraction process starts. If the process succeeds, and no errors appear on CIW, then the extracted view is created and shown in Library Manager.

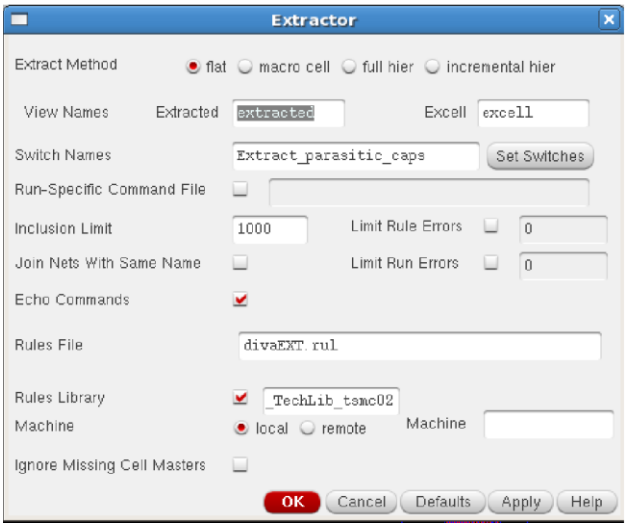


Figure 15. Extractor window

- Open the extracted view. You will see the boundary of each layer is extracted. You can see transistor parameters, such as width and length. Make sure if these values are the same as what you designed in the layout.

6. Layout Verification (LVS)

- This is the last step before finishing each design. Be sure to run DRC check and Layout extraction every time before running LVS if you update anything in your design views (schematic and layout).

- In the extracted view choose "Verify > LVS", then LVS form pops up. LVS comes from Layout Versus Schematic. In field "schematic" and "extracted", fill in proper names of Library, Cell and View. You can click button "Browse" to do it. Click "Run" to start with LVS. Please see the Figure 16 below.

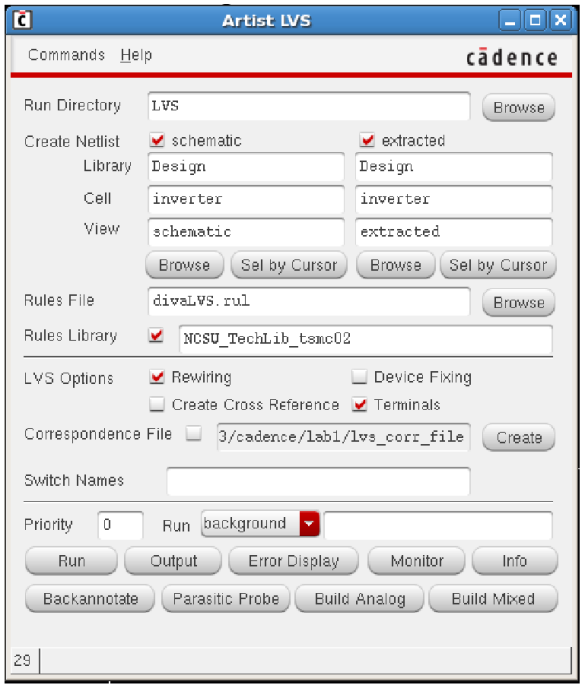


Figure 16. LVS window

- Note in CIW several messages flash and then show "LVS job is now started". Wait for a while and a window pops up saying whether the LVS job succeeds or failed. If the job succeeds, it does NOT mean that the layout and the schematic match. All it means that the job has completed.

- If the LVS job fails, please do check followings:

  - Have you done with DRC check and Layout extraction before LVS, especially if you made any updates in your schematic or layout view?
  - Is your schematic OK? Do you see any errors when you select "check and save" again?
  - Please select cells and views through "Browse" button in LVS window, both for schematic and extracted views.
  - The **last page** of the LVS report window reports the possible nets (exp: Net 17) or terminals that may have error. Some of these errors can be highlighted in the extracted view using this method:

    Open the extracted view, then from the top bar select window> Assistance>search Then type terminal or net name with error that were found in LVS report. They will get highlighted.

- If the LVS job succeeds, click button "Output" in LVS window, then a text file pops up. Check the file and find any unmatched items. The file contains summaries for instances, nets and terminals. You will have to submit the output file for the lab report.
  - You passed the LVS check if you can see "The net-lists match." in the file.
  - If you see "The netlists failed to match.", please follow the way below to find and correct errors.

7. Report Requirements

1. Please apply all the design steps above to Inverter, NAND2, and XOR2 gates.
2. Please submit your lab report **only in PDF** and include screenshots of schematic, symbol, layout and extracted for the "INVERTER", "NAND "and "XOR" gates as well as a screenshot from the **first page** of the LVS report window where it shows "the netlist match".

NOTE:

a) When drawing layouts, please refer to the lecture 3 note, p. 17, as a proper example view of your layout design.

b) Figure 17 is the schematic of XOR2 gate. This gate has 12 transistors. Figure 17 requires two inverters to generate /A and /B from input A and B.

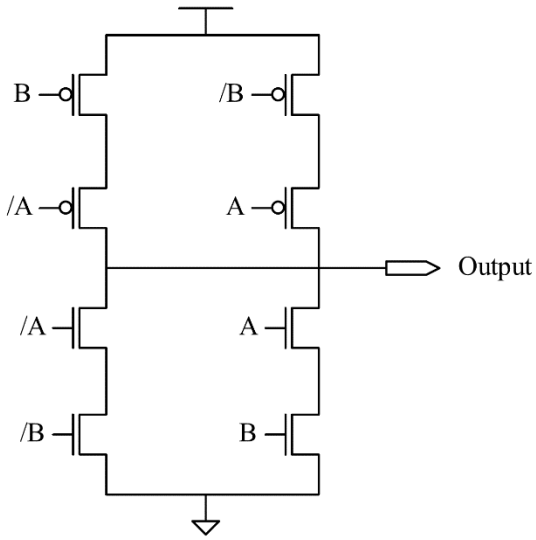


Figure 17. XOR2 gate

c) Feel free to use other metal layers (e.g. Metal-2) in your layouts, especially for XOR2. In case you need to connect M2 to poly, you need to have two contacts overlapped: M2-M1 with M1-poly.

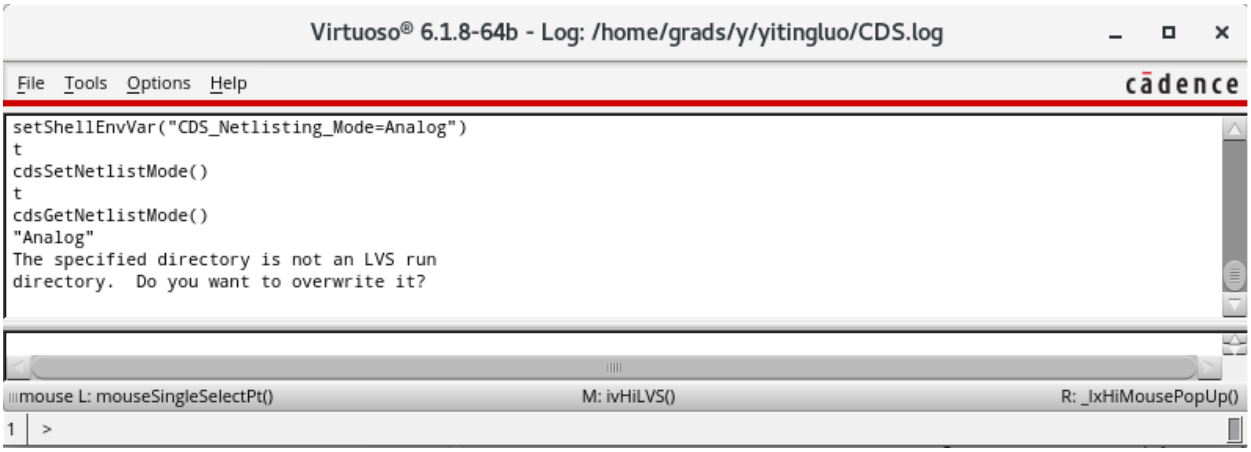
d) You eventually would need the entire standard gate layouts used (inverter, NAND, XOR) to be of the same height. This will help us make connections easily in future labs when you would use the individual layouts to build the overall circuit. This will have to be taken care of in future lab sessions.

When you face the following problem while running lvs:

global error:
Cannot find switch master cell for instance P0 in cellView (inverter schematic) from viewlist 'lvs schematic gate_sch cmos_sch ' in library 'Design'.
global error:
Cannot find switch master cell for instance N0 in cellView (inverter schematic) from viewlist 'lvs schematic gate_sch cmos_sch ' in library 'Design'.
si: Netlist did not complete successfully.

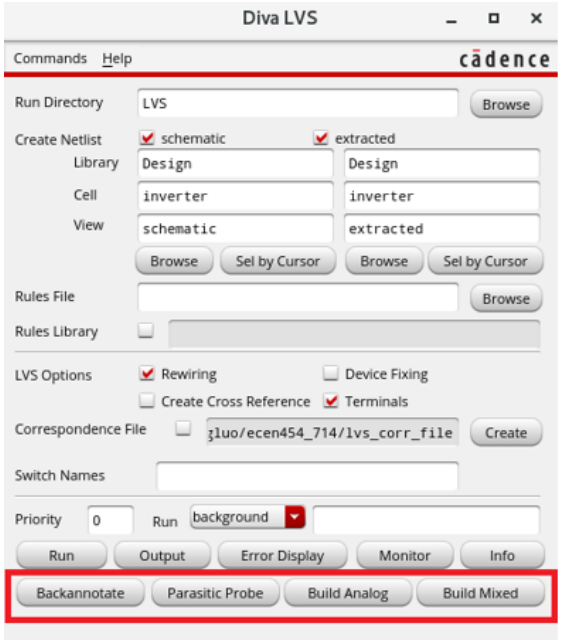
Please try to do the following:

First type in the following command in your CIW window. Make sure the last response is "Analog".



Then re-open your Diva LVS. If a window pops out asking if you want to rewrite, click "Yes".

After that, you will see the LVS window has an extra line in the red rectangle like the following



Appendix: Rubric & Draw custom cellviews

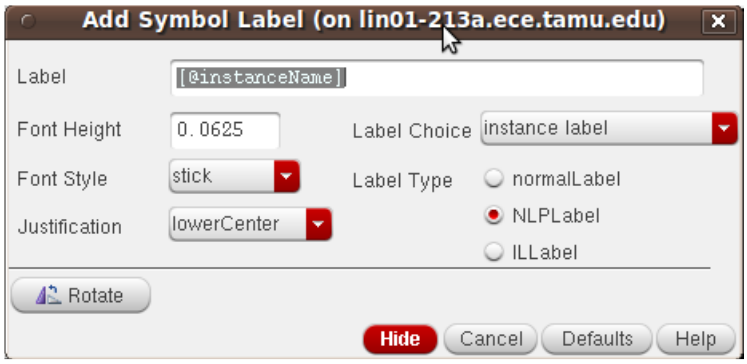
1. Schematic – 0.5 each (inverter, nand, and xor)
2. Symbol – 0.5 each (inverter, nand, and xor)
3. Layout – 1 each (inverter, nand, and xor)
4. Extracted - 0.5 each (inverter, nand, and xor)
5. LVS report – inverter (0.5), nand (1), and xor (1)

This section is providing instructions to draw custom symbols for gates created as schematic. You may first extract a symbol from your schematic and use this section to update and edit the symbol because

the symbol drawn automatically from your schematic will have only rectangle and pins deployed randomly.
As you saw in Lab1 you can create a symbol of any circuit that you design by using the inbuilt option in the Design Window to create a symbol for the current cellview. But you can also create custom symbols for the logic gates rather than the rectangular ones that are created by default. For example you would need to create a triangular symbol followed by a bubble for an inverter.
To create a custom symbol for any design you can create a new cellview "symbol" in the same cell. The following instructions explain how you can create a symbol for an inverter.
In the schematic window, choose Create > Cellview > From Cellview. Type in the cell name of the inverter you have designed as shown below. Click "OK" and a new window will pop-up.

Since you want to draw a triangle, now choose Create> Shape > Polygon and the following figure will pop-up.

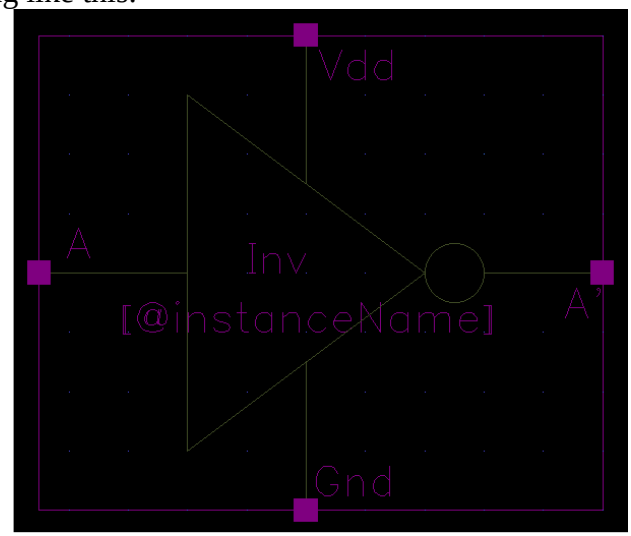
Choose Hide and begin at one of the desired vertices of the triangle that you want to draw. Choose all the vertices that you want in the polygon and then click back on the first vertex to complete the figure.
Choose Hide and begin at one of the desired vertices of the triangle that you want to draw. Choose all the vertices that you want in the polygon and then click back on the first vertex to complete the figure.
You can then draw a bubble in front of the triangle by choosing to draw a small circle in from of it. You can click on a point just in front of the triangle and then extend the mouse to indicate the radius of the circle that you want to create.
You should continuously perform "Check and Save" on the symbol by pressing "F8" or choosing "Design > Check > Save". The symbol will automatically be compared to the schematic in the same cell and at this point will give out some warnings. This is because the tool sees that you have not yet included the names of the pins defined in the schematic in the symbol.
You can add a pin by choosing "Add > Pin" and choose the appropriate direction (input, output or input/output) for it. Add pins for input A, output A', power lines (input/output) VDD and GND. You will see that the pin in this case is slightly different from the one that appears in a schematic. It is a small box with a line attached to it and the pin name on it towards the end. The box is the actual pin and so it must be pointing in the away from the rest of the symbol. Note after you add in all the appropriate pins with proper directions the warnings go away.
The next step is to create a label for the symbol. You do this by choosing "Add > Label" after which the following dialog box will appear.



The first label you add to the symbol is the [@InstanceName] which will be replaced by instance names such I0, I1 etc when the symbol will be used in other designs. This is to differentiate between different instances of the same cell.

The second label you add to the symbol will be the cell name. You do this by choosing "Add > Label". Then choose Label Type as "NormalLabel" and type in the cell name like "inv" in the Label field.

The final step is to create a selection box for the symbol which defines the area in which the symbol will be selected if you were to click in it. This is done by choosing "Add >Selection Box". Click on "Automatic" and a selection box will surround the symbol with pins on its boundary. The inverter symbol will look something like this.



Try to edit the symbol shape such that all its pin-names are within the selection box to avoid confusion later on when using the symbol for a higher level of design.

Basic idea about layout

1. ***Think of layout as 3-dimentional description for related circuits. You put all needed elements on silicon substrate, then connected with each other through metal layer, which means, you have to use "contact" to build connection with metal first, and then establish connection on metal layer.***
2. ***Metal layers are used for connection; make sure there is no crossing within same layer.***
3. ***There are limited contacts, including m1-p, m1-n, m1-poly, m2-m1, m3- m2, m4-m3 and m5-m4.***
4. ***Remember to put all your pins on metal layer.***
5. ***The background of your layout refers to p-substrate***
6. ***Make sure that your transistor "substrate" is connected to the "source".***
7. ***The width of PMOS should be at least double size of NMOS.***
8. ***Good procedure to draw layout is structure -> stick diagram -> layout***
9. ***Reference for how to efficiently draw a stick diagram:***
   http://www.ohio.edu/people/starzykj/webcad/ee415/VLSI/design/stick/stick.htm