



# ENDCAP MUON TRIGGER SYSTEM OVERVIEW

D.Acosta

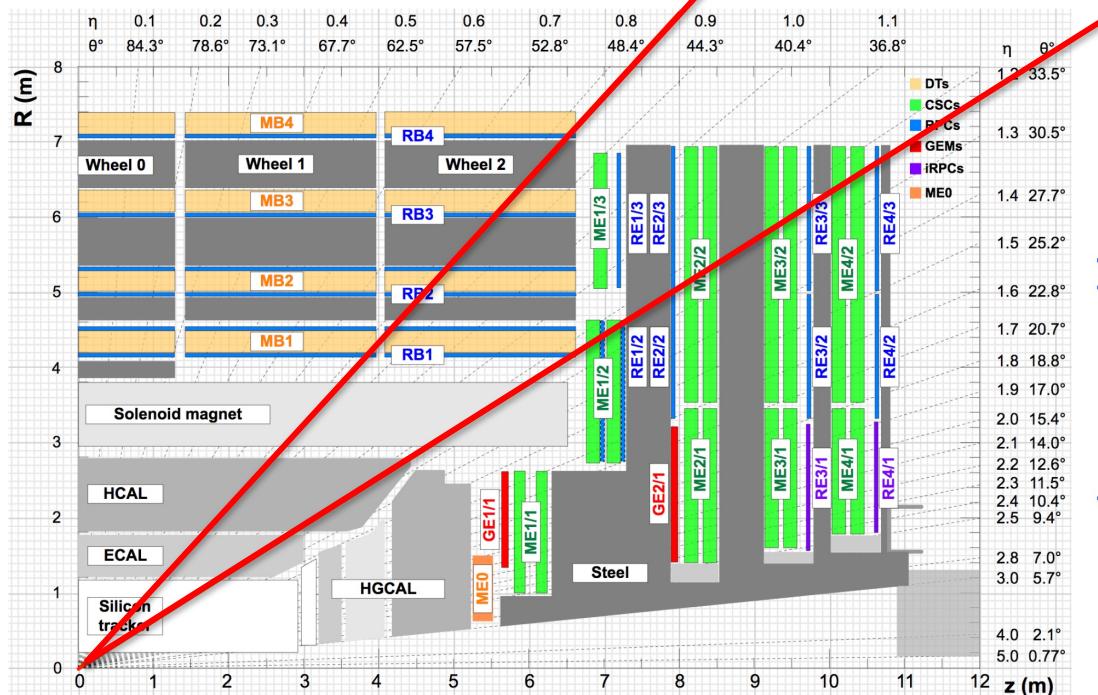


# CMS Muon System and Trigger

## Barrel:

Drift-Tubes (DT) and Resistive Plate Chambers (RPC)

Barrel (DT+RPC)



## Overlap:

DT, RPC, CSC

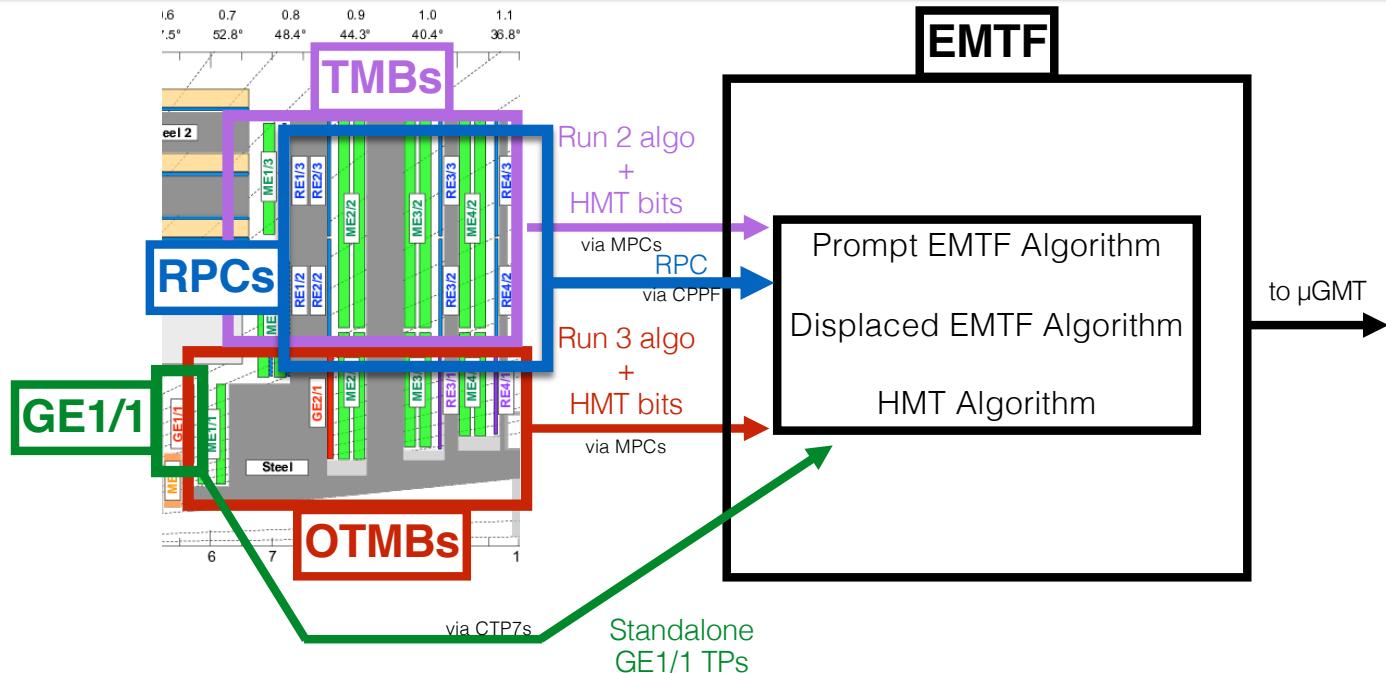
Segmented into  
3 regions

Overlap (DT+CSC+RPC)

Endcap (GEM+CSC+RPC)

Endcap:  
Cathode Strip  
Chambers  
(CSC),  
RPC endcap,  
and GEM GE1/1

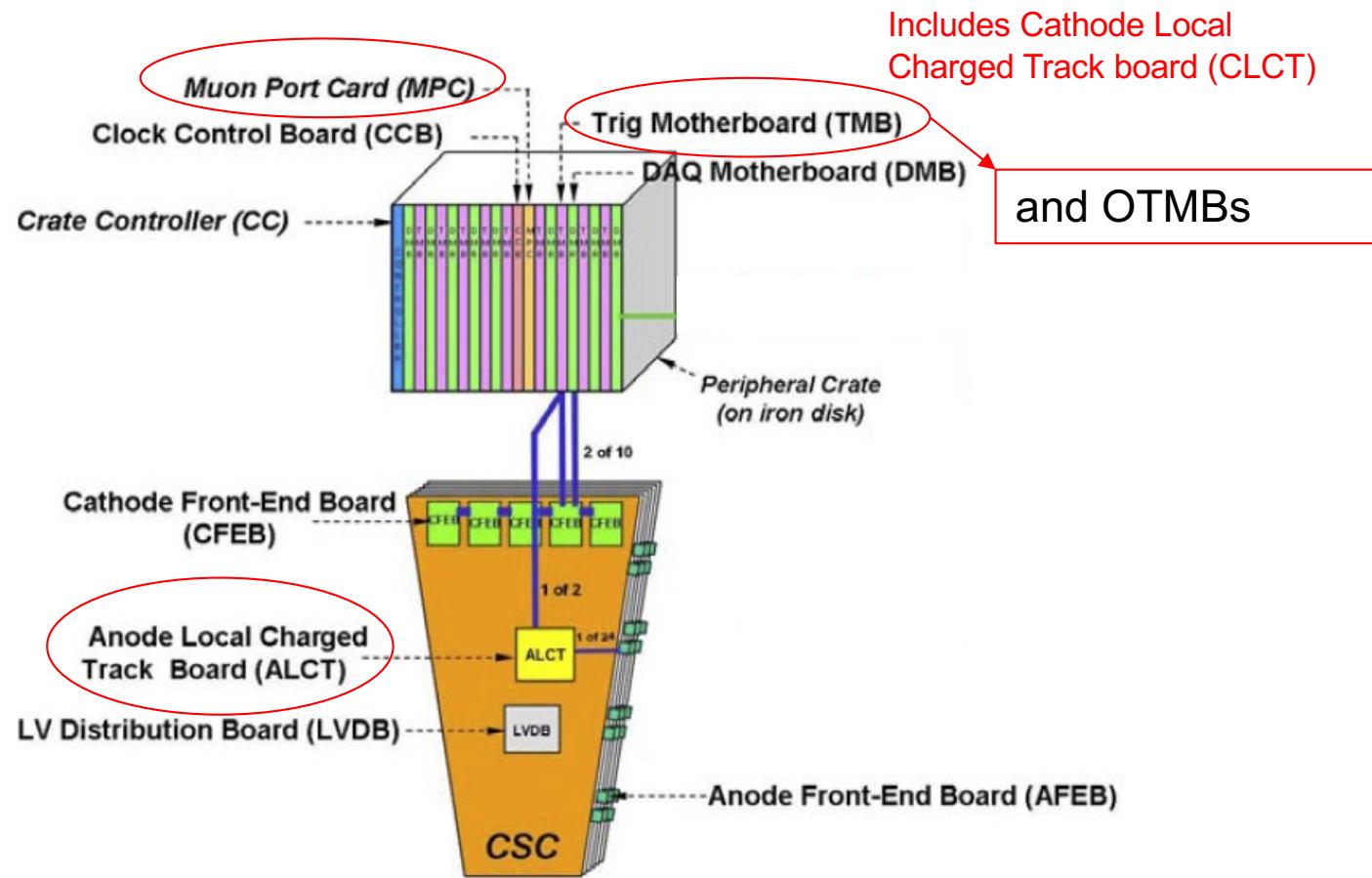
# Further Details for Run 3 EMTF Inputs



- **Old TMBs** in outer ring (MEX/2 and ME1/3) running Run 2 CSC algorithm and ALCT HMT algorithm
- **New OTMBs** in inner ring CSC chambers (MEX/1) running new Run 3 CSC algorithm and HMT algorithm
- **RPC endcap** data sent by **CPPF** as during Run 2
- **GE1/1**: TPs will be sent by two different paths:
  - Standalone TPs via CTP7s to EMTF
  - Combined GEM-CSC TPs via OTMBs in ME1/1 (so contained within CSC LCTs)



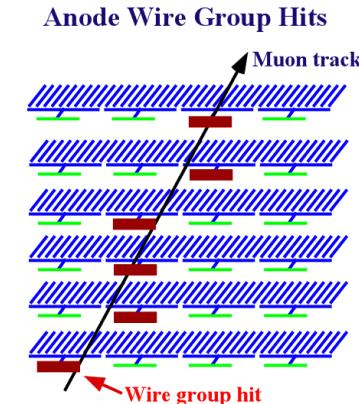
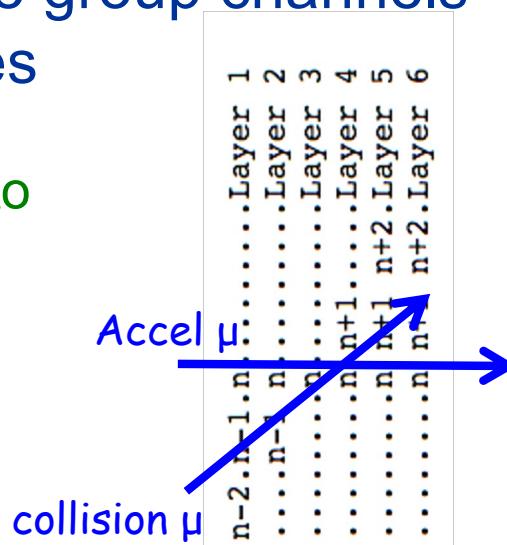
# CSC Trigger Primitives





# Anode Local Charged Track (ALCT)

- ★ Finds local wire group patterns indicative of a muon crossing a CSC in the non-bending plane
- ★ Due to the various types of CSCs, there are 3 sizes of ALCT boards, handling 288, 384, and 672 anode wire group channels
- ★ Xilinx Virtex FPGA stores pattern logic
  - Collision type (pointing to the IP) and accelerator muon type (horizontal)
    - Acceptance is not uniform for cosmic muons...

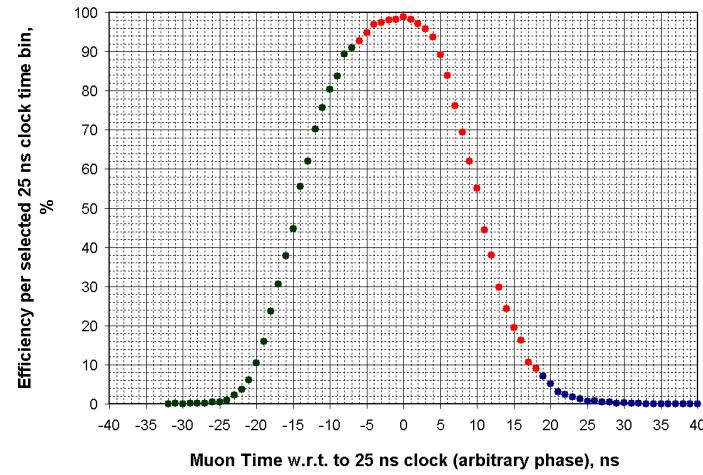
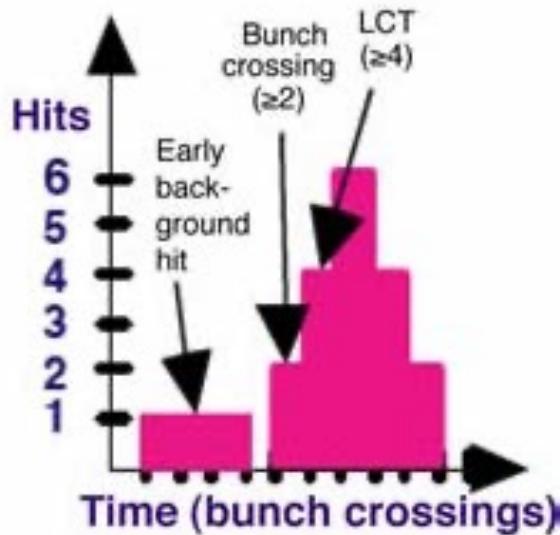




# Anode Local Charged Track (ALCT)

## \* Timing

- Timing established by earliest hits ( $\geq 2$ ), referred to as the “pre-trigger”
- Efficiency to get the right bunch crossing (at the optimal phase) is  $>98.5\%$





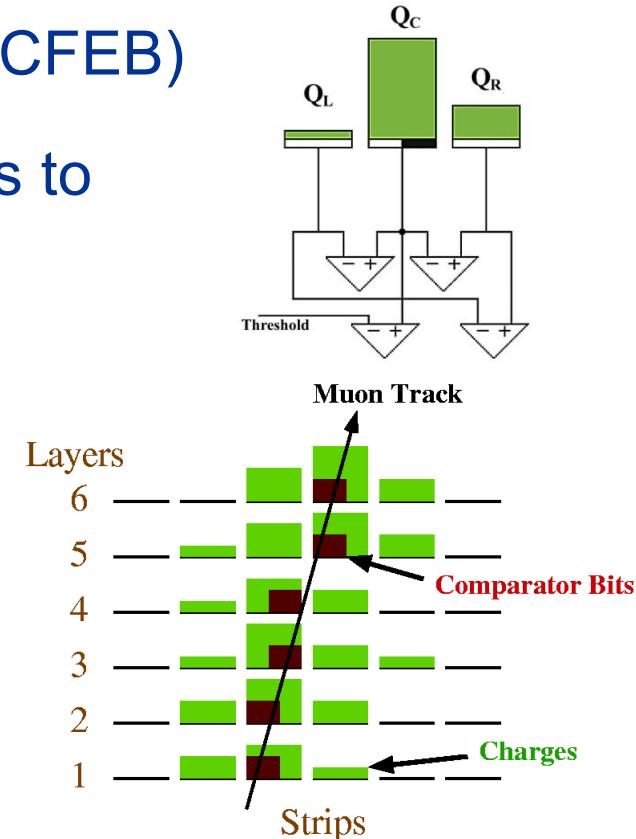
# Cathode Local Charged Track (CLCT)

- \* Comparator logic (an ASIC chip on CFEB) finds the local charge maximum on strips, and compares neighbor strips to determine the position to  $\frac{1}{2}$ -strip precision ( $\sim 5\text{mm}$ )

- Averaging over all 6 planes implies a precision of  $0.5/\sqrt{12} \sim 1.5\text{mm}$
- Track-Finder applies these corrections for hit position

- \* Pattern logic finds Local Charged Tracks (LCTs)

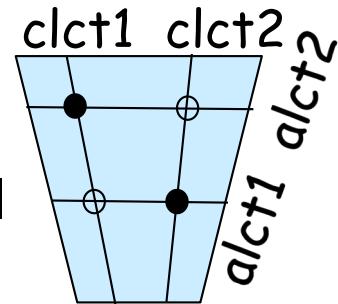
- Resides in (O)TMB board FPGA
- 11 patterns including straight and both bend directions in TMBs
- New patterns for OTMBs and Run 3





# Trigger MotherBoard (TMB)

- ★ The Trigger MotherBoard (TMB) associates ALCT and CLCT patterns from a CSC into a “correlated LCT”
  - ALCT and CLCT must match within a 1 BX (?) window, and the correlated LCT is assigned the BX of the ALCT which has better time resolution
  - Up to two correlated LCTs per CSC
  - But an ambiguity in association of ALCT and CLCT (ghost combinations)
    - Track-Finder effectively tries all with separate roads in  $\phi$  and  $n$

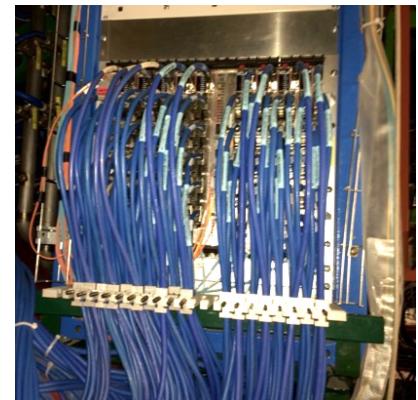




# Muon Port Card (MPC)

- ★ The Muon Port Card (MPC) receives LCT data from 9 TMBs in a peripheral crate and transmits to the Track-Finders
  - It simultaneously **transmits** all LCTs (up to 18) to the upgrade **Endcap Track-Finder** over 3.2 Gbps optical links
- ★ 60 peripheral crates in total

One peripheral crate corresponds to a  $60^\circ$  sector in ME2-ME4, and  $30^\circ$  in ME1

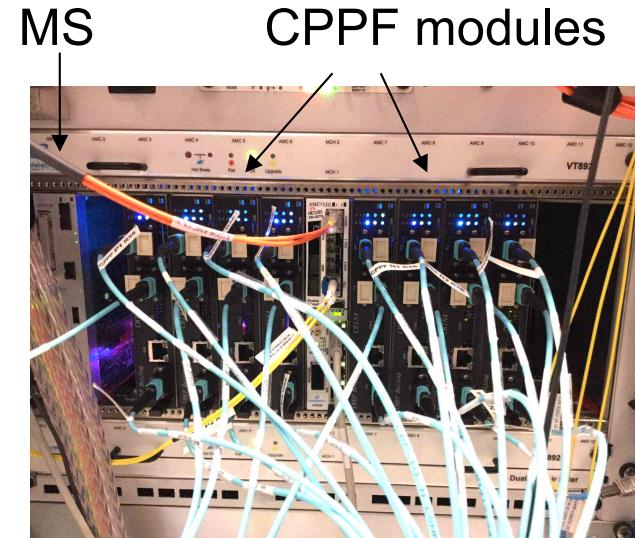




# CPPF Connection From RPC to EMTF

## \* CPPF $\mu$ TCA system installed in USC

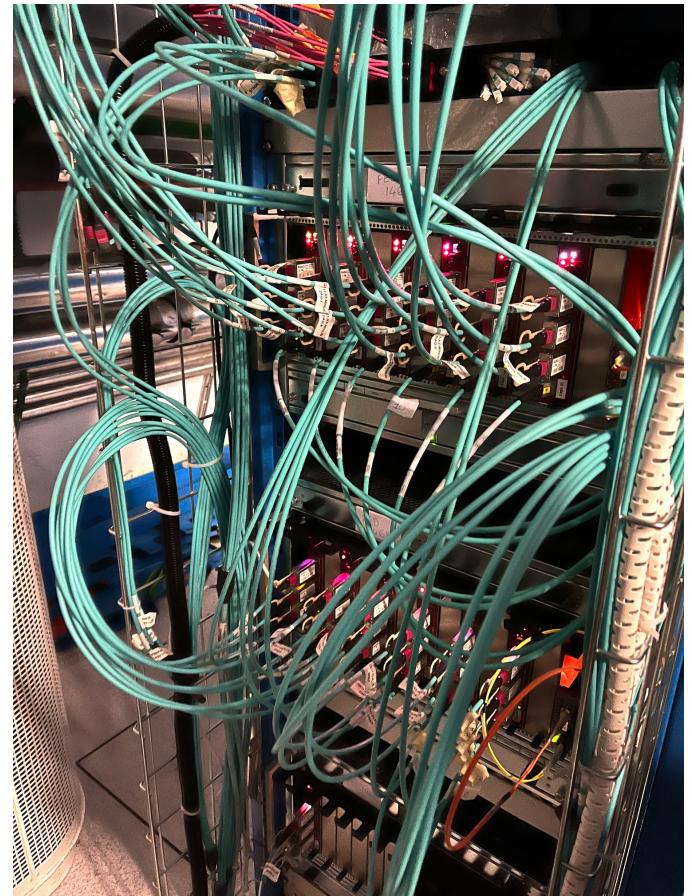
- Receives data from RPC Link Board system
- Maintained by Beijing group
- Converts pad clusters to EMTF  $\phi$ ,  $\theta$  units
- Concentrates and increases transmission bandwidth to 10 Gbps
- In our Muon Sorter crate
  - Muon sorter is used for CSC local runs





# GE1/1 Direct Connection to EMTF

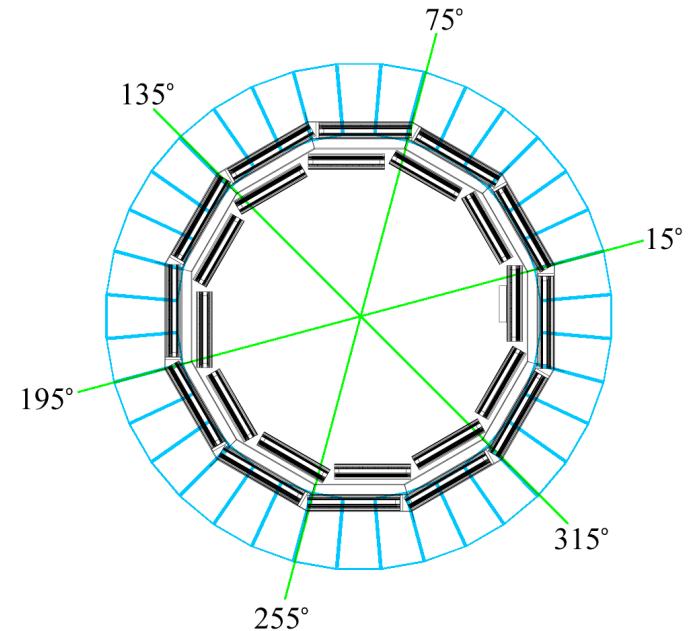
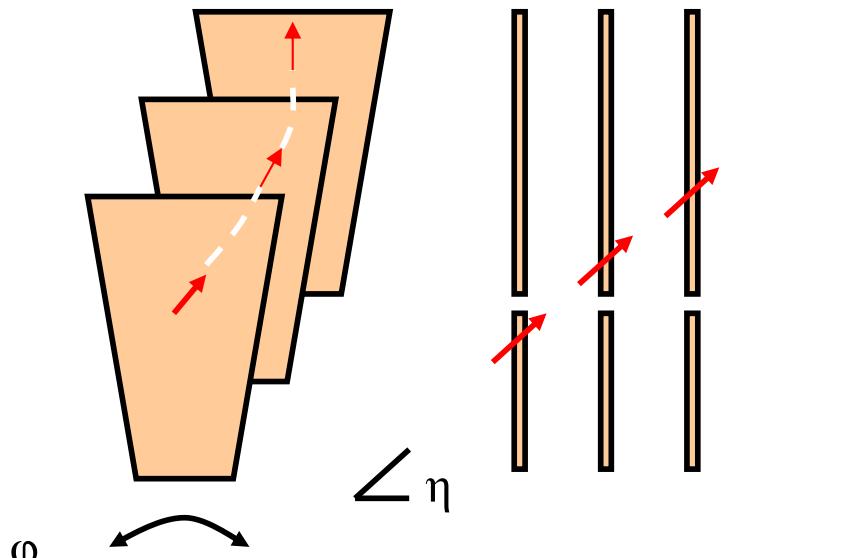
- ★ CTP7 μTCA cards collect GE1/1 data and send over fiber optic links to EMTF @ 10 Gbps





# Endcap Muon Track-Finding

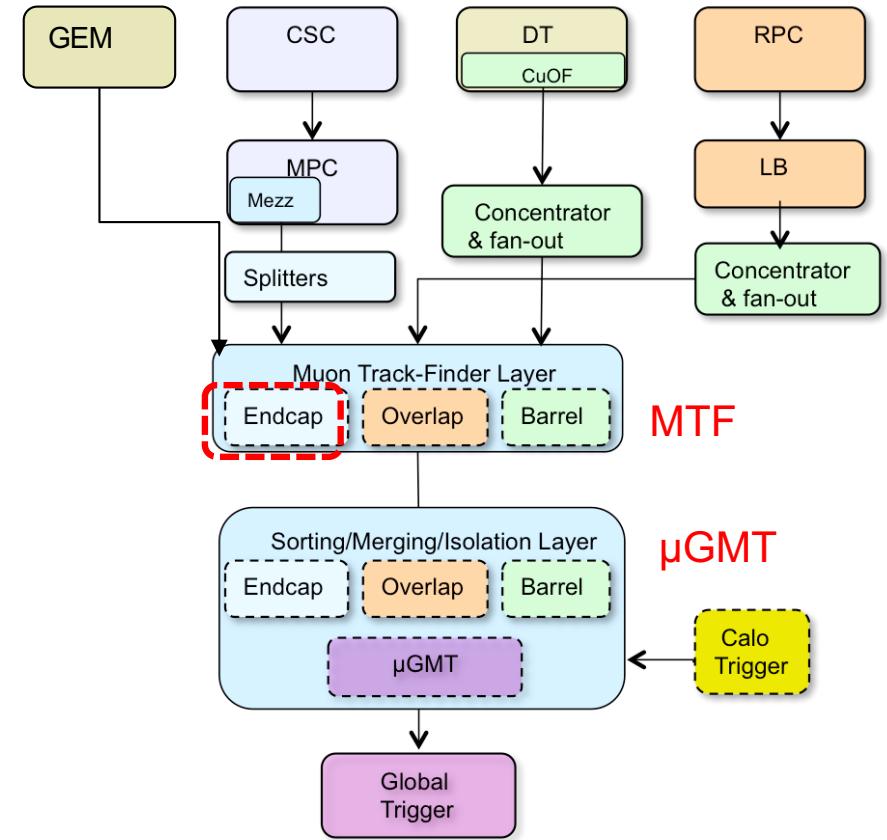
- Track-Finder links receive track segments and FPGA builds into distinct tracks through pattern recognition logic in firmware
  - 2-D tracks for barrel region, 3-D tracks for endcaps
- Performs a momentum measurement using the deflection of muon in the magnetic field (complicated in endcaps)
  - Use memory look-up for quick calculation (FPGA and external RAM)
  - Random access and data out in 25ns
- Logic partitioned into  $60^\circ$  sectors (12 total, 6 per endcap, and aligned with DT chambers for overlap region)





# Phase 1 Muon Trigger Upgrade (Deployed 2016)

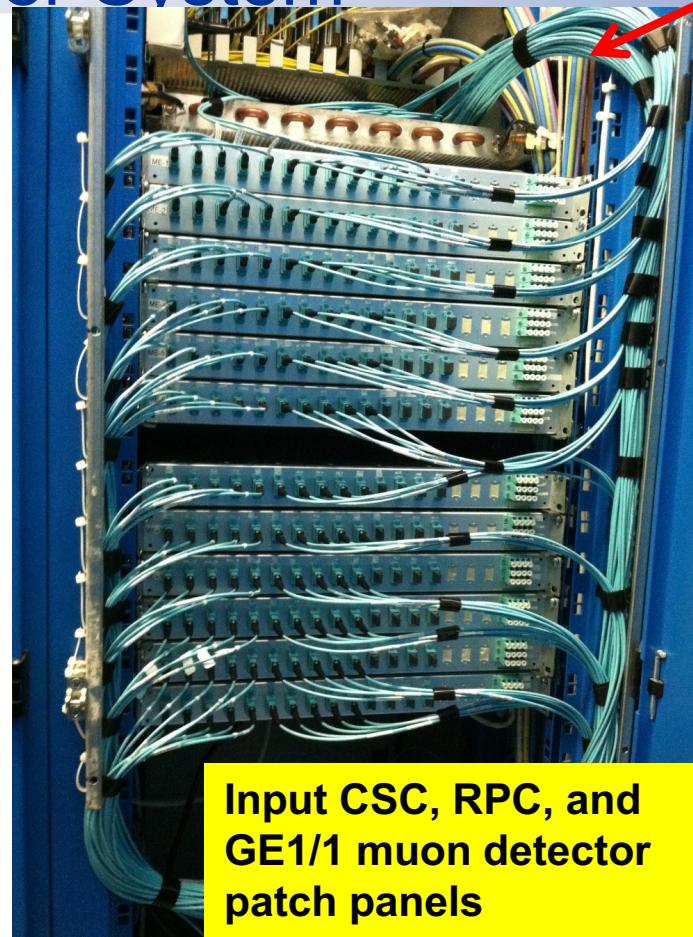
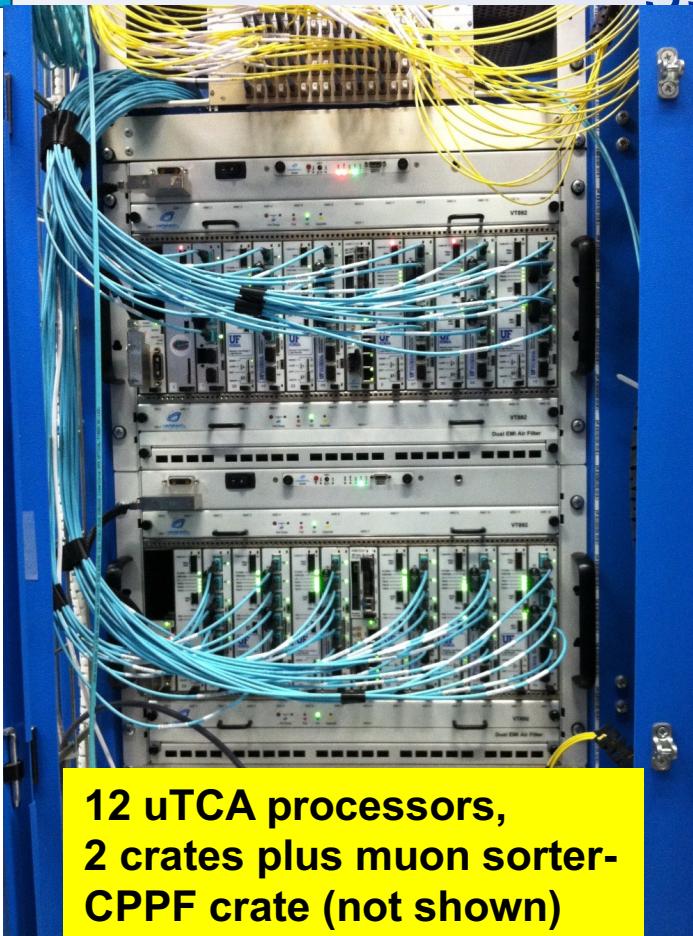
- ★ Improve upon successful features of current muon trigger
  - Enlarge LUT memory for  $p_T$  assignment from MBs to GBs, allowing use of more angles in "fit"
  - Larger FPGA to handle more hits from pile-up, additional chambers
  - Share signals across boundaries
- ★ Use the redundancy of the three four! muon detection systems earlier in the trigger chain
  - Create a higher resolution and more robust muon trigger rather than combine lower resolution ones
- ★ Report more muons and increase precision
  - Collect muons at the  **$\mu$ GMT**
  - Improved isolation, b-tagging, inv. mass, etc. at the **Global Trigger**





# CMS Endcap Muon Track-Finder Part of Level-1 Trigger System

In  
USC



From  
detectors

Fibers are  
bundled in  
groups of 12  
(or 24, 36) to  
connectors

Requires patch  
panel to re-  
route to  
destinations

About 550 input  
fibers at 3.2-10  
Gbit/s  
→ 2 Tbit/s

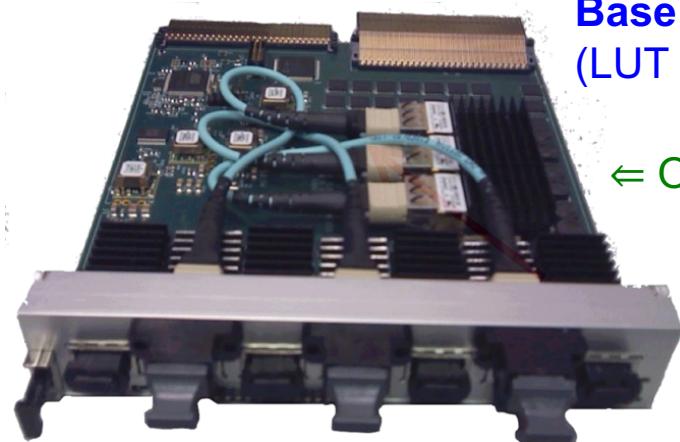
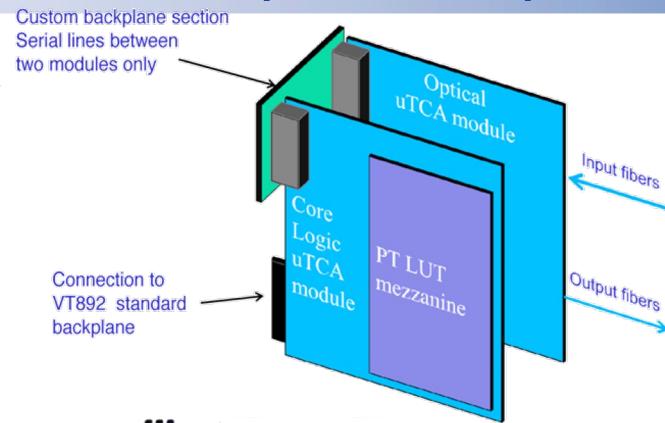
Next Gen  
systems:  
10's of Tbit/s



# Endcap Muon Track-Finder (EMTF)

## \* Muon Track Finder μTCA card: MTF7

- Optimized for maximum input from muon detectors (84 input links, 28 output links)
- Dual card w/large capacity for RAM (~1GB) to be used for  $p_T$  assignment in track finding



Base FPGA card ⇒  
(LUT not shown)

⇐ Optics card



Modules also used by CMS for the  
barrel/endcap overlap region



## PT LUT Mezzanine Card

- \*  $P_T$  calculated from Reduced Latency DRAM

- 1 GB → 30 bit address space
  - +8 address bits over previous CSCTF



- \* Algorithm

- Machine Learning: Boosted Decision Trees (BDTs) used for regression to assign  $P_T$
  - More data: Can use  $\Delta\phi$  bending between 4 detector stations, and  $\Delta\eta$ , and bend angle in first station
  - Algorithm is run offline and the result is stored in memory for look-up

- \* For Run 3: also a neural network in FPGA firmware