Chapter 5.10

1

a) Address stream = 12 bits
Initial state and final state of the TLB and page table

TLB:

Valid	Tag	Physical Page Number
1	3	6
1	7	4
1	1	13
1	2	14

Page table:

Valid	Physical page or in disk
1	5
1	13
1	14
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

valid	Hit/Miss/Page Fault
0	Miss
7	Hit
3	Miss
3	Hit
1	Page Fault
1	Hit
2	Page Fault

b) Address stream I Binary address: bits 15-12 virtual page, 11-0 page offset
Initial state and final state of the TLB and page table

TLB

Valid	Tag	Physical page Number
1	4	9
1	7	4
1	B	C
1	9	E

Valid	Phys. Page or in disk
1	5
0	Disk
1	D
1	6
1	9
1	B
0	Disk
1	4
0	Disk
1	E
1	3
1	C

Valid	Hit/miss/Page Fa
2 4EC	Page Fault
7 8F4	Hit
4 AC0	Miss
B 5A6	Miss
9 4DE	Page Fault
A 10D	Hit
13 D60	Hit

② → chap 5.10

a) Address stream = 14 Bits
Initial state and final state of the TLB and page table:

TLB

Valid	Tag	Physical Page Numb
1	1	13
1	7	4
1	3	6
1	0	5

Valid	Hit/Miss/Page Fault
0	Miss
3	Hit
1	Page Fault
1	Hit
0	Hit
0	Hit
1	Hit

Page table:

Valid	Physical page or in disk
1	5
1	13
0	Disk
1	6
1	9
1	11
0	Disk
1	4
	~~Disk~~
0	Disk
0	Disk
1	3
1	12

Advantages: It is include memory resources that are saved by use of larger page size and efficient thansfer of larger pages to and from secondary storage.

Disadvantages: Longer disk thanster

ⓑ Address stream = Binary address: bits 15-14 virtual page, 13-0 page offset
Initial state and final state of the TLB and page table

TLB

Valid	Tag	Physical Pags Numbe
1	B	C
1	1	D
1	2	E
1	0	5

Pg Valid	Hit/miss/Page Fault
0 24EC	Miss
1 38F4	Page Fault
1 0ACO	Hit
2 35A6	Page Fault
2 14DE	Hit
1 010D	Hit
2 3D60	Hit

Page table

Valid	Physical page or in disk
1	5
1	D
1	E
1	6
1	9
1	B
0	Disk
1	4
0	Disk
0	Disk
1	3
1	C

③ from chapt 5.10

step 1

ⓐ Address stream = 12 bits

0, 7, 3, 3, 1, 1, 2 = 0, 111, 011, 011, 001, 001, 010

2-way set associative:

Tag: VPN >> 1 bit

TLB

Valid	Tag	Physical PageNumb
1	0	5
1	0	13
1	01	14
1	01	6

step 2

Direct-mapped

Tag: VPN >> 2 bits

TLB

Valid	Tag	Physical Page
1	0	5
1	0	13
1	0	14
1	0	6

The TLB is important to avoiding paying high access times to memory in order to translate virtual address to physical addresses and without TLB page table would have to be retenced upon every access using a virtual addresses, causig a significant slowdown

step 3

ⓑ Binary Address (bits 15-12 virtual page, 11-0 page offset

2 4EC, Page Fault, disk = physical page D, (TLB set 0, slot 1)

7 8F4, Miss in TLB, (TLB set 0, slot 1)

1 AC0, Miss in TLB, (TLB set 0, slot 0)

B 5A6, Miss in TLB, (TLB set 1, slot 0)

9 1DE, page fault, disk = physical page E, (TLB, set 1, slot 1)

1 10D hit in TLB

B D60 hit in TLB

2-way set associative TLB (bits 15-12 virtual page = bits 15-13 ta
bits 12 se

Valid	Tag/Time	Physical Page Number
1	4/4	9
1	2/2	D
1	B/5	C
1	9/4	E

3 'Gpop 5.10

step 4

Binary address: (bits 15-12 virtual page, 11-0 page offset)

2 4EC Page Fault, disk = physical page D, (TLB slot 2)

7 8F4 hit in TLB

4 AC0 , miss in TLB (TLB slot 0)

B 5A6 , miss in TLB (TLB slot 3)

9 4DE, page Fault, disk ⇒ physical page F (⇒ TLB slot 1)

4 10D , hit in TLB

B D60, hit in TLB

Direct-mapped TLB (bits 15-12 virtual page = bits 13-12 slot

Valid	Tag	Physical Page Num
1	4	9
1	9	F
1	2	D
1	B	C

The TLB is importent to avoiding paying high access times to memory inorder to translatte virtual address to physical addresses and without TLB page table would have to be referenced upon every access using virtual addresses, causing a significant slowdown

④ of Chapter 5.10

ⓐ Given, The Page size = 4KB
= 12 offset bits, 20 page numb.bits

Therefore 2^{20} = 1M page table entries

For single application: 1M × 4bytes = 2^{22} bytes

ⓑ Given, The page size = 16KB
= 2^{14} page size

page table entry size = 8bytes
= 2^3 bytes

therefore 64-14 = 50 bits
= 20^{50} page table entries with 8 bytes per entry, yields total of 2^{53} bytes for each page table

Therefore for five applications: 5×2^{53} bytes

(5) of Chapter 5.10

(a) Given, The page size = 4KB
= 12 offset bits, 20 page number bits

256 entries (8 bits) for first level = 12 bits
= 4096 entries per second level.

Minimum: 128 first level entries used per application

128 entries × 4096 entries per second level = 524K = 2^{19} entries

524K × 4 bytes/entry = 2MB (2^{21}) second level page table per applicat

128 entries × 6 bytes/entry = 768 bytes first level page table per applicat

Therefore total five application = 10MB

Maximum: 256 first level entries used per application 256 entries × 40

entries per second level = 1M (2^{20}) entries

1M × 4 bytes/entry = 4MB (2^{22}) second level page table per applicati

256 entries × 6 byte/entry = 1536 bytes first level page table per applicato

Therefore 20.98 MB for total five applications

(b) Virtual address size of 64 bits

64 − 14 = 40 bits

2^{40} page table entries

256 (2^8) entries in main table

8 bytes per page table entry

Total of 2^{11} bytes i.e

2KB for main page table

40 − 8 = 32 bits or 2^{32} page table entries for 2^{nd} level table with 8 bytes per entry.

Yields total of 2^{35} bytes for each page table

Therefore for 5 applications = 5×(2KB * 2^{35} bytes)