Lab 5: Decoder and FPGA

Objective: To design a 3×8 decoder with 2×4 decoders; design adder/subtractor with Verilog and synthesize with FPGA Spartan 3.

Provided: 74X139 (2×4 DEC), 74008 (AND), 7404 (INVERTER), bread-board, Xilinx Spartan3.

Background A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n output lines. For any given input combination only one output line is active (if active high, only one output line is 1 and all others are 0; if active low, only one outline is 0 and all others are 1.) Hence if a active low 3-to-8 decoder with input 011 will set output line 3 to zero and set all other output lines to one.

3-to-8 DEC

EN1	S2	S1	S0	/Y0	/Y1	...	/Y7
0	X	X	X	1	1	1	1
1	X	X	X	1	1	1	1
1	X	X	X	1	1	1	1
1	0	0	0	0	1	1	1
1	0	0	1	1	0	1	1
1	.	.	.	1	1	.	1
1	1	1	1	1	1	1	0

A field-programmable gate array (FPGA)is a semiconductor device that can be programmed after manufacturing. The FPGA Spartan-3 Starter Board provides a powerful, self-contained development platform to experiment with any new design, from a simple logic circuit to an embedded processor core. It features a 200K or 1000K gates, on-board I/O devices, JTAG-programmable ROM, and 1MB fast asyncronous SRAM.

3.1 Preparation

Revise your four-bit adder designed with Verilog in Lab3 to performe both four-bit addition and subtraction. Refer to Figure 4.13 in the textbook (Mano

and Ciletti, Fifth Edition). Show the code to the instructor or TA at the beginning of lab.

3.2 Experiment: decoders

1. Use a 74X139 chip which can be used as either a DEC or De-Multiplexer (DEMUX). Note this chip contains two (dual) DECs/DEMUXs.

```
74139
Dual 1-of-4 inverting DEC/DEMUX.
     +---+--+---+            +---+---+---*---+---+---+---+
/1EN |1  +--+ 16| VCC        |/EN| S1| S0|/Y0|/Y1|/Y2|/Y3|
 1S0 |2       15| /2EN       +===+===+===*===+===+===+===+
 1S1 |3       14| 2S0        | 1 | X | X | 1 | 1 | 1 | 1 |
/1Y0 |4   74  13| 2S1        | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
/1Y1 |5  139  12| /2Y0       | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
/1Y2 |6       11| /2Y1       | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
/1Y3 |7       10| /2Y2       | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
 GND |8        9| /2Y3       +---+---+---*---+---+---+---+
     +----------+
```

2. Test the functionality of the DECs. Group the select lines and connect the corresponding select lines to the same input switches (2 switches). Connect each Enable line to its own input switch. Connect the eight output lines to different LEDs. Demonstrate your circuit to the instructor.

3. Use 2 2×4 DECs (1 chip) to build a 3×8 DEC. Note Enable (EN) and Output (Y?) lines are active low in 74X139 (they are preceded by a / representing a bar). Demonstrate your circuit to the instructor.

3.3 Synthesize adder/subtractor with FPGA Xilinx Spartan3

Use the eight switches for input data, a debounce button for mode switch, and one 7-segment for result display. The Verilog module of Hex to 7-segment encoder is provided. Demonstrate your result to TA or instructor.