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Lab 3 Notes

-Make sure the ex control out signals match the table from lab two when connecting these selection signals to the necessary mux. If the ALUDst and RegDst signals are flipped, then B will show as unknown (XXXX's) on the timing diagram during certain cycles.

-Always have a default case in your case structures.

Lab 3 requirements

Lab due dates are posted on the calendar.

Pace yourself and if you have any questions, feel free to email or text me and I will try to reply as soon as possible. I will get back to you much faster if you text me saying you sent an email.

Write-up Requirements

Introduction: 1 paragraph (5-7 sentences)

-Provide a description of the Lab and give a brief overview of what the top level module is intended to do. Also include any changes to the previous stages if required.

Summary: 1 paragraph + Timing Diagram and/or Detailed Simulation Log

-Provide an explanation behind the signals on your timing diagram and make sure to remove the unnecessary signals.

-The explanation should be thorough enough so that I can tell that you understand the timing diagram or detailed simulation log.

-Make sure you remove unconnected signals (I.E. high impedance ZZZZZZ…)

For those of you asking about Set on Less Than and the Zero signal, I have included the partial case structure for the ALU.

```
wire sign_mismatch;
assign sign_mismatch = A[31] ^ B[31];
initial result <= 0;
        assign zero = ~|result; //unary nor result to check for zero
        always@* case (control)
                //… your previous cases go here
                3'b111 : result <= A < B  ? 1-sign_mismatch:
                  0+sign_mismatch;
                default:;// $display("unknown ALU operation");
        endcase
```

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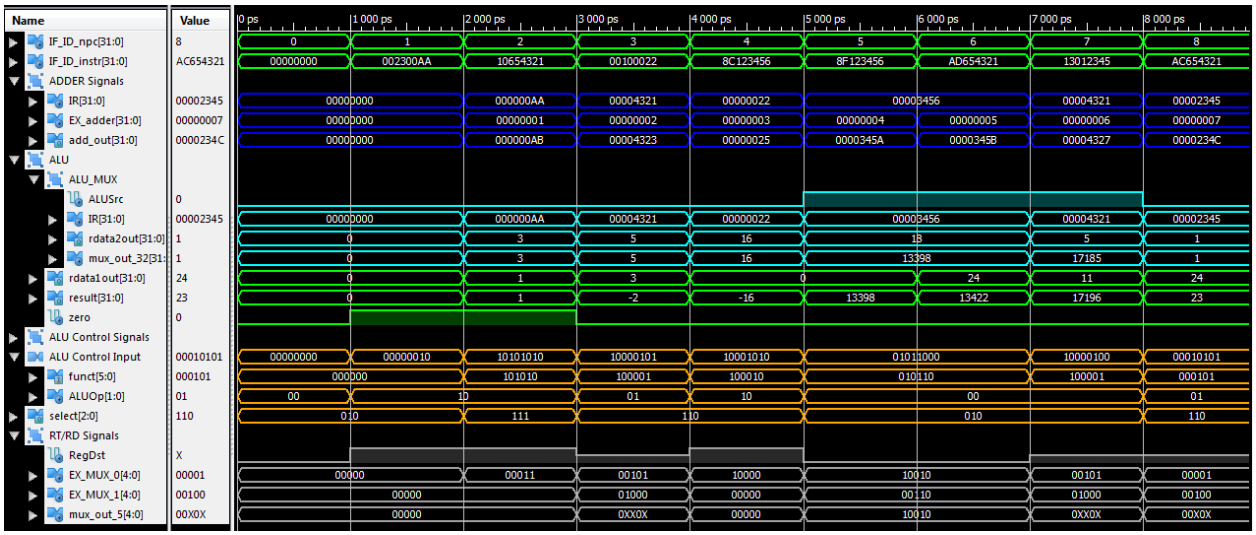
The required signals for full credit on the timing diagram are:

ALU Control Signals, ALU inputs and outputs, Adder signals, and the Instruction.

Your timing diagram should look something like the below reference:



Here are the instructions used

0000_0000_0010_0011_0000_0000_1010_1010 //0x002300AAh
0001_0000_0110_0101_0100_0011_0010_0001 //0x10654321h
0000_0000_0001_0000_0000_0000_0010_0010 //0x00100022h
1000_1100_0001_0010_0011_0100_0101_0110 //0x8C123456h
1000_1111_0001_0010_0011_0100_0101_0110 //0x8F123456h
1010_1101_0110_0101_0100_0011_0010_0001 //0xAD654321h
0001_0011_0000_0001_0010_0011_0100_0101 //0x13012345h
1010_1100_0110_0101_0100_0011_0010_0001 //0xAC654321h
0001_0010_0000_0001_0010_0011_0100_0101 //0x12012345h

Extra Credit: create a single parameterized multiplexer module that can be instantiated with a variable number of bits.