Lab Assistant: Jason Fredrick
jasondfredrick@gmail.com
909-996-5548 (SMS text only)

Notes

-The MUX signals 0 and 1 selection are flipped in the diagram for this lab. You should walk through your timing diagram and make sure you are using the right *a* and *b* for your Multiplexer. Use the control signal, *sel*, to determine what should be *a* and what should be *b*.

-If your instructions are still failing after a few cycles, you might have to go back and flip your *a* and *b* signals in your multiplexers if you are running into problems.

-Make sure that all of the control signals from lab2 are being correctly indexed (refer to the lab2 control chart). For example, if MemRead and MemBranch are flipped, then the machine will be trying to read memory when a branch is supposed to occur.

Lab 5 requirements

Lab due dates are posted on the calendar.

Pace yourself and if you have any questions, feel free to email or text me and I will try to reply as soon as possible. I will get back to you much faster if you text me saying you sent an email.

Write-up Requirements

You are far enough along in the labs that you shouldn't need a timing diagram reference to aid you. I would recommend creating a few R-Type instructions to test that your machine is working properly. A test of a few adds and subtracts will be sufficient. Since this lab is hooking up the Writeback portion of the pipeline; therefore, I want to see the writeback signals added to a timing digram.

I should see the ALU result, the instruction, the register that the instruction is writing to and the writedata signals for at least three instructions. This lab is very flexible, so use whatever instructions you think is suitable for a good test. In industry, you usually don't have someone holding your hand the whole time and you will have to test your code on your own so good luck.