Lab 8: Three Digit Decimal BCD Ripple Counter

Objective: To deisgn a 3 digit BCD counter in Verilog and synthesize it in FPGA Spartan 3.

8.1 Design a BCD counter

Write a behavioral modle of a decimal BCD counter in Verilog. The counter counts from 0, 1, $\cdots$, to 9, then goes back to 0, and repeat. The counter is reset when reset signal goes from 1 to 0.
Generate a testbench to simulate the counter. Show the simulation result to the instructor or TA.

8.2 Make a 3 digit decimal BCD counter

Refer to the block diagram on page 271 in textbook to build a 3-digit decimal BCD counter. The trhee counters share the same reset signal.

8.3 Make the counter with 7-seg display of each digit

Use the modules hex_to_sseg.v and disp_mux.v (provided in lab4 and posted on the class website) to make a top module that will count and also display the three digits of count.

8.4 Synthesize the ripple counter with Spartan3

To synthesize the ripple counter, use the debound button for reset and 7-seg for display. To use the clock signal on Spartan3, you need add a frequency dividor module to decrease the speed of count.

8.5 Questions

1. How to revise the module of BCD counter so that it has the function to pre-set a data to an individual BCD counter?
2. How to revise it and make it work as a digital clock?