Lab Assistant: Jason Fredrick
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909-996-5548 (SMS text only)

Lab1 Notes

Note: If you cannot zoom in on the older Xilinx 10.1 version, add `timescale 1ps/1ns to all of your modules. (There is a warning that shows up in the older version) The older version does not propagate the timescale directive to the child modules.

Note: Change $finish to $stop to see instances in the simulation so that you can add internal signals. The $finish compiler ends the simulation and closes the instances of objects whereas the $stop directive will make the simulation interactive and allow addition of waveform signals.

Note: If you receive an error while trying to run a simulation, check the windows task manager for a previously run simulation 'pipeline_isim_beh.exe' and terminate that process. Also, if you receiving issues with compiling, try cleaning up your source files under Project->Cleanup Source Files. MAKE A BACKUP OF YOUR FILES BEFORE RUNNING CLEANUP SOURCE FILES; I have been told that this can sometimes wipe out your project file on the older versions of Xilinx Webpack ISE.

Lab 1 requirements

Submit your Lab write-up (document preferably doc or rtf) along with your Verilog source code as a compressed file to jasondfredrick@gmail.com. You can RAR the package together using WinRAR (http://www.rarlabs.com). I would prefer that you send the document and source code in one RAR file.

You can work in teams of 2 or individually; however, make sure that both of your names are listed in the compressed file to receive credit.

I expect the file to have the following naming convention: lastname1[-lastname2]-labX.rar where lastname1 [and lastname2] are the surnames of the team members and X is the lab number.

Example: fredrick-lab1.rar

Document the source code by supplying your name(s) and any comments you have regarding your code. Use the extreme programming approach, because it is self-documenting.

Write-up Requirements

Introduction: 1 paragraph (5-7 sentences)

-Provide a description of the Lab and give a brief overview of what the function is of top level module.

Summary: 1 paragraph + Timing Diagram and/or Detailed Simulation Log

-Provide an explanation behind the signals on your timing diagram and make sure to remove the unnecessary signals.

-The explanation should be thorough enough so that I can tell that you understand the timing diagram or detailed simulation log.

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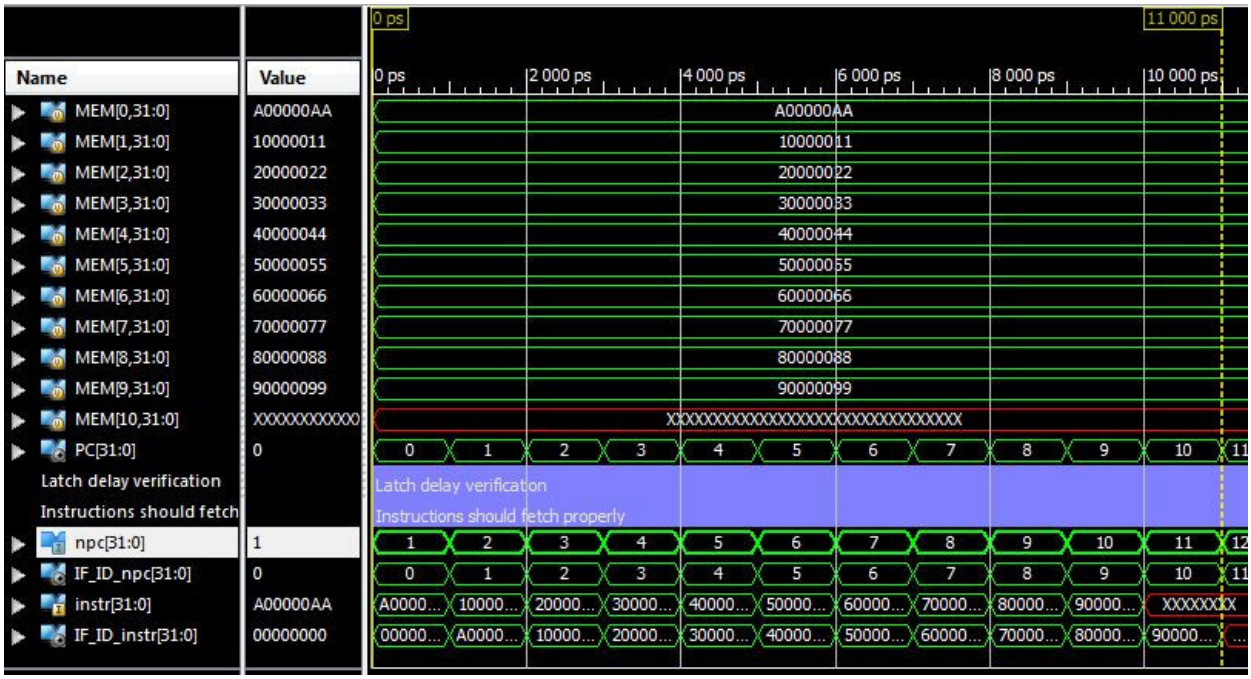

Your timing diagram should look something like this: DO NOT USE MY PICTURE PROVIDED. It is merely for your reference.