CSCI 401 Final

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1. (60 pts) You are given a 128-bit **asynchronous** bus with a time of flight of 10 ns. Your computer has the following equipment attached:

Hard Drive	RAM
Total Latency: 7.84 ms	Access Time: 40ns
Disk Transfer Rate: 100MB/s	No Burst Mode
Number of Disks: 4	

Showing all work calculate the following:

(a) the band width of the bus,

(b) the percent of the bus utilized by continuous paging of a virtual memory system with 32KB pages,

(c) the number of cache to RAM transfers that can occur if: The bus is continuously paging and 18% of the bandwidth must be left for other transactions (Hint: calculate the available bandwidth for the RAM transactions and use the size of the transactions).

The bandwidth of the bus is:

$$\begin{aligned} \text{BW} &= \frac{\text{Data Transfered}}{\text{Time to Transfer}} \\ &= \frac{\text{Bus Width}}{4T_{Hand} + \max 2T_{Hand}, T_{RAM}} \\ &= \frac{16B}{4(10ns) + \max 2(10ns), 40ns} \\ &= \frac{16B}{80ns} \\ &= 200MB/s \end{aligned}$$

The effective transfer rate of the pages from the disks is:

$$\begin{aligned} \text{Rate}_{\text{Disk}} &= \frac{\text{Data Transfered}}{\text{Time to Transfer}} \\ &= \frac{\text{Data Transfered}}{\text{Total Latency} + \frac{\text{Data Transfered}}{\text{Combined Disk Transfer Rate}}} \end{aligned}$$

$$
\begin{aligned}
&= \frac{32KB}{7.84ms + \frac{32KB}{min(4\times 100MB/s, 200MB/s)}} \\
&= \frac{32KB}{7.84ms + .16ms} \\
&= 4MB/s
\end{aligned}
$$

Thus the bandwidth available to RAM is $200-36-4 = 160$ MB/s. Since each transfer is 4 B, the transfers per second is 40×10^6 transfers/sec or 1 every 25ns.

2. (40 pts) Use the following chart to show the state of a 4 location, 2-Way associative cache, that uses LRU. If a location has a number printed in it, the address is valid, if no number appears the contents are invalid. For simplicity the computer only has 16 locations in memory. If the cache takes 5ns to access and RAM takes 60ns, what is the effective access time given the sequence?

Time	0	1	2	3	4	5	6	7	8	9	10
Lookup Address	-	2	5	6	B	5	2	2	B	C	5
Cache location 00	A										
Cache location 01	B										
Cache location 10											
Cache location 11											

Time	0	1	2	3	4	5	6	7	8	9	10
Lookup Address	-	2	5	6	B	5	2	2	B	C	5
Cache location 00	A	A	A	6	6	6	6	6	6	C	C
Cache location 01	B	B	B	B	B	B	B	B	B	B	B
Cache location 10		2	2	2	2	2	2	2	2	2	2
Cache location 11			5	5	5	5	5	5	5	5	5

MR=.4

$$
\begin{aligned}
T_{eff} &= T_{cache} + MR(T_{RAM}) \\
&= 5ns + .4(60ns) \\
&= 29ns
\end{aligned}
$$

3. (80 pts) A pipelined RISC computer has 8 stages, and runs at 2.5 GHz. The cache has a miss rate of 1% for data and instructions, and a miss penalty of 12 ns. The system has a dynamic branch predictor that is wrong only 10% of the time. Branch errors cost 5 cycles.

   (a) What is the ideal (no stalls) speedup over a non-pipelined machine?

   (b) What is the impact to the CPI due to cache misses on a non-memory operation?

(c) What is the impact to the CPI due to cache misses on a memory operation?

(d) What is the impact to the CPI due to branch errors on branching instructions?

(e) If memory operation make up 20% of the commands in a typical program and branching make up 15% of the commands, what is the average CPI?

(a) $n = \frac{\text{Time Without Pipeline}}{\text{Time With Pipeline}} = \frac{I \times 8}{I+8} \approx 8$ for large I (number of instructions).

(b) $\Delta CPI = \text{Miss Rate} \times \text{Miss Penalty} \times \text{Clock Frequency} = (.01)(12ns)(2.5GHz) = .3$

(c) Twice above or .6.

(d) $\Delta CPI = \text{Branch Error Rate} \times (BranchPenalty) = .1 \times 5 = .5$

(e) $CPI_{avg} = .2(1 + .6) + .15(1 + .3 + .5) + .65(1 + .3) = .32 + .27 + .845 = 1.435$

4. (20 pts) A 32-bit virtual memory system has a 64KB page size, and 1 GB of RAM. How large is the physical page number in bits? Assuming that the each entry in the table is word aligned, how large is the lookup table in bytes?

64KB = 2^16

1GB = 2^30

So the physical page number is 30-16=14 bits

The table size is $2^(32 - 16) \times 4B = 2^{18}B = 256KB$