

Notes

-There are two *LD* instructions in the code given for lab 6 where the binary values do not match the comments on the side. Correct these instructions in your code by changing the Source2 (*rt*) values.

-Note that the NOP (no operation) instructions are in place because there are data dependencies, which limits the efficiency of the pipeline.

Lab 6 requirements

Lab due dates are posted on the [calendar](#).

Pace yourself and if you have any questions, feel free to email or text me and I will try to reply as soon as possible. I will get back to you much faster if you text me saying you sent an email.

Write-up Requirements

You are far enough along in the labs that you shouldn't need a timing diagram reference to aid you. This last lab is short and allows you to play around with your final modules. The requirements of the lab are to fix the instructions given and make sure that they run properly in your pipeline. To receive full credit, your R1 register should be on your timing diagram and should have the sequence:

1, 3, 6, 12

as stated in the lab manual with a simulation length of 24 cycles. You should also be showing your instructions and your writedata signals.