Lab Assistant: Jason Fredrick
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Notes

-When connecting modules together, make sure to use wires. Leaving EX_MEM_PCSrc and EX_MEM_NPC will cause problems.

-If your instructions are failing after a few cycles, verify that PCSrc is connected properly and there are no typos. Realize that PCSrc is a one-bit wire and if it is named incorrectly (PCCrc or PCRrc), Verilog will instantiate this as a new one-bit wire.

Lab 4 requirements

Lab due dates are posted on the calendar.

Pace yourself and if you have any questions, feel free to email or text me and I will try to reply as soon as possible. I will get back to you much faster if you text me saying you sent an email.

Write-up Requirements

Introduction: 1 paragraph (5-7 sentences)

-Provide a description of the Lab and give a brief overview of what the top level module is intended to do. Also include any changes to the previous stages if required.

Summary: 1 paragraph + Timing Diagram and/or Detailed Simulation Log

-Provide an explanation behind the signals on your timing diagram and make sure to remove the unnecessary signals.

-The explanation should be thorough enough so that I can tell that you understand the timing diagram or detailed simulation log.

-Make sure you remove unconnected signals (I.E. high impedance ZZZZZZ…)

Here are the following instructions to test the module:

0x00221820h //000000_00001_00010_00011_00000_100000 add $3, $1, $2
0x8C220004h //100011_00001_00010_00000_00000_000100 lw $2, 4($1)
0xACC50008h //101011_00110_00101_00000_00000_001000 sw $5, 8($6)
0x10200000h //000100_10000_00000_00000_00000_000000 beq $16, $0, 0

The required signals for full credit on the timing diagram are:

Memread, Memwrite, read_data, writedata, and the Instructions (IF_ID_Instr).

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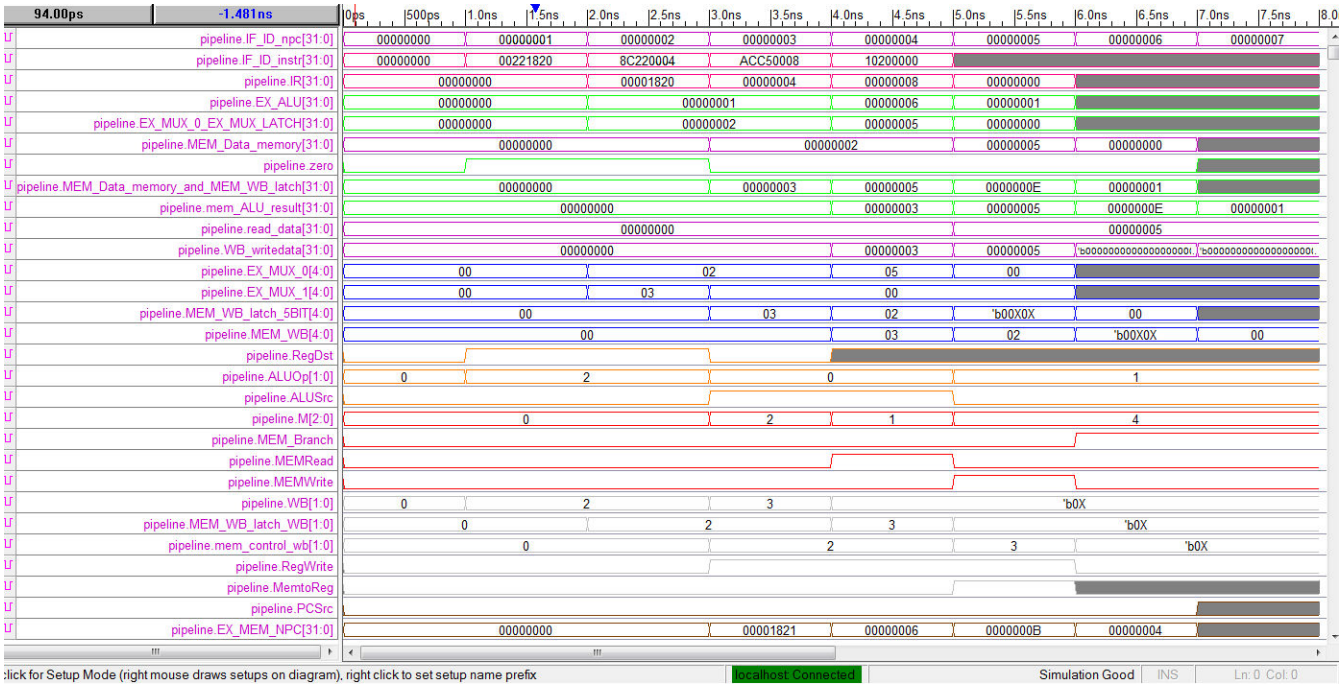
Your timing diagram should look something like the below reference:



If your read data signal is unknown (XXXXXX's) during non-read instructions that is ok.