Lab 6: Flip-flop and Counter

Objective: To implement a RS latch and a binary counter with D-type flip flops.

Provided: 74X374 (D flip-flops), 7400 (quad 2-input NAND), breadboard.

3.1 Experiment: RS Latch

Build an SR latch using 4 NAND gates (Figure 5-4(a), page 194, 5th Edition of Mano and Ciletti book). Demonstrate your circuit to the instructor. Do your observations agree with what you expect (Figure 5-4(b))?
Explain why the input S=0 R=0 should be forbidden.

3.2 Experiment: Binary Counter

Deisgn a binary counter that counts from 0 to 9 then back to 0 and repeat, display the count on 7 segment LED.

1. Examine the pin-out diagram of the 74X374.

```
74374
8-bit 3-state D flip-flop.
    +---+--+---+             +---+---+---*---+
/OE |1  +--+ 20| VCC         |/OE|CLK| D | Q |
 Q1 |2       19| Q8          +===+===+===*===+
 D1 |3       18| D8          | 1 | X | X | Z |
 D2 |4       17| D7          | 0 | / | 0 | 0 |
 Q2 |5   74  16| Q7          | 0 | / | 1 | 1 |
 Q3 |6  374  15| Q6          | 0 |!/ | X | - |
 D3 |7       14| D6          +---+---+---*---+
 D4 |8       13| D5
 Q4 |9       12| Q5
GND |10      11| CLK
    +----------+
```

2. Start by filling the following table:

$Q_3(t)$	$Q_2(t)$	$Q_1(t)$	$Q_0(t)$	D_3 $Q_3(t+1)$	D_2 $Q_2(t+1)$	D_1 $Q_1(t+1)$	D_0 $Q_0(t+1)$
0	0	0	0	0	0	0	1

3. Next, draw Karnaugh maps to find boolean expressions for each D input in terms of $Q_3(t)$, $Q_2(t)$, $Q_1(t)$, and $Q_0(t)$. Mark the inputs from 1010 to 1111 as don't care conditions in K-map. Try to use NAND gates in the resulting expressions.

4. Connect the 4-bit output of the counter to hex-to-7segment circuit (PLD) you made in last lab and display the count in hex.