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**Notes**

**-The forwarding unit is a controller that detects data dependencies in pipelined instructions and reduces the amount of stalling required by forwarding data from the past instructions execution and memory stages to the present execution stage. Therefore, an instruction can continue execution without waiting for the register file to be updated before it reads from it. The Forwarding Unit is actually not constrained to any specific stage of the pipeline. Its inputs are strictly five bit addresses because it uses register addresses (RS, RT, RD) and compares past and present instructions to detect dependencies between RS and RD or RT and RD. Your CSE 401 course book talks about it if you are interested in how to code it. It also shows the conditional checks and outputs; Google is also a great resource to aid in your understanding.**

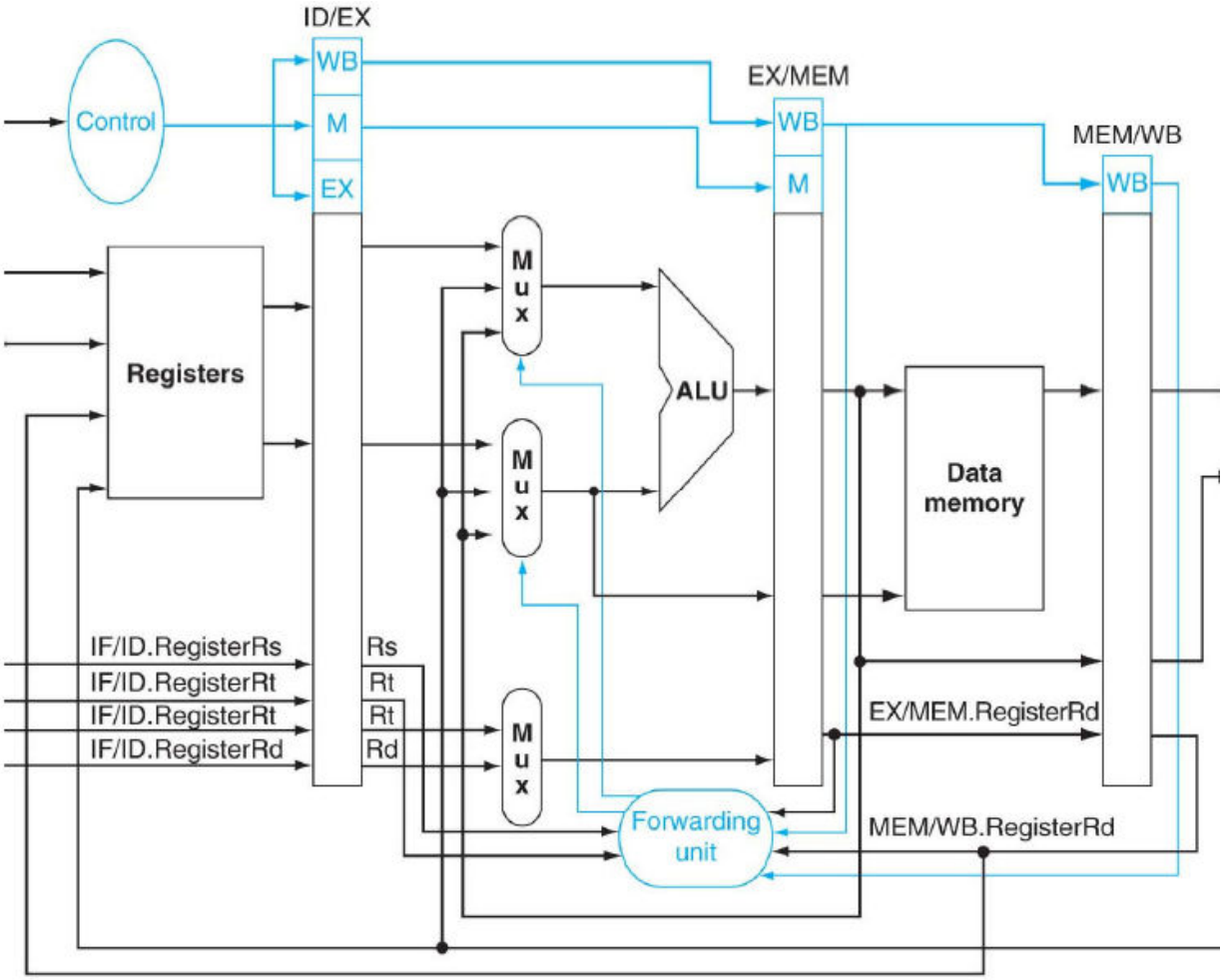


Image Source: Virginia Tech CS2504 Spring 2009 Course

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## Forwarding Unit Requirements

**The Forwarding Unit due date is posted on the calendar.**

**The easiest way to test the functionality of the Forwarding Unit is to introduce data dependences in your instruction block. Therefore, you can use the lab6 instructions, but you must remove some of the NOP instructions (stalls) between each data dependency. If all goes well, you should be able to remove two NOPs between each instruction and still produce the 1, 3, 6, 12 sequence in a shorter amount of cycles.**

## Write-up Requirements

**You are far enough along in the labs that you shouldn't need a timing diagram reference to aid you. Take your instructions from lab 6 to test your Forwarding Unit and make sure they run properly in your pipeline. To receive full credit, your R1 register should be on your timing diagram and should have the sequence:**

**1, 3, 6, 12**

**as stated in the lab manual with a simulation length of 24 cycles. You should also be showing your instructions and your writedata signals.**