chapter 7.22

The CPV C cay only perform floating-point add and substract operations, and Xand Y are floating point elements. The rector processor to usue 2 loads, 8 matrix elements in parallel from A and 8 matrix elements from B into a single rector register and they perform a rector subtract. The result put in memory. Since the rector processor does not have comparison instructions, we would have CPV A performy 2 parallel conditional Jumps hased on Haating point registers Suppose Increment two counts based on the conditional Compare and they Just add the two counts for the easine matrix

The problem is to show that it is difficult to perform operation on individual vector element. when utilizing a rector processor. What might be a nice instruction to add would be a rector compavisor that would allow for is to compare two rectors and produce scalar value of the number of elements where one rector was largorthe number of elements where one rector was largorthe ofter. This would reduce the computation to a single instruction for the compavisor of 8 Fp winder pairs, and they an integer computation of some pairs, and they an integer computation of some some pairs and they are integer computation of some some pairs and they are integer computation of some some pairs and they are integer computation of some some pairs and they are integer computation of some some pairs and they are integer computation.