# ELEG-5403 Control Systems Design Project

Aircraft Bank Angle Control

Andrew Cox

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## Background

The final design project explored for ELEG-5403 is Design Option 2 which consists of a bank angle control autopilot system. This report explores the various controller design methods required to reach the design specification goals using control theory as well as tools such as MATLAB and Simulink. This report includes the quantitative analysis and reference to block diagrams and scripting code; however, those models and programming files will be provided external of this report and as part of the submittal.

Aircrafts utilize autopilot systems to improve handling and provide pilots with relief for extended periods of flight. These systems need to be responsive, stable, and robust to counteract variations in weather as well as variations of the respective pilot. Systematic design techniques were deployed by the Wright Brothers which contributed to their success (Dorf & Bishop, 2010). Many things have changed since 1903 and the first powered takeoff with the Wright Flyer I, however these pioneers shaped the path for aviation and control systems today.

## Design Goals and Process

The design process was taken from Dorf and Bishop Modern Control Systems Twelfth Edition and used as a guide through the project shown in figure 1 (Dorf & Bishop, 2010). The following design specifications/goals were provided as customer requirements:

1. Add and additional 125ms delay in the system
2. DS1: Percent Overshoot < 20%
3. DS2: Rise Time < 2.1 Seconds (fast response time)
4. DS3: Settling Time < 4.5 Seconds

Various other analysis scenarios will be performed to understand the modified design compared to the original benchmark system as shown in Figure 2.

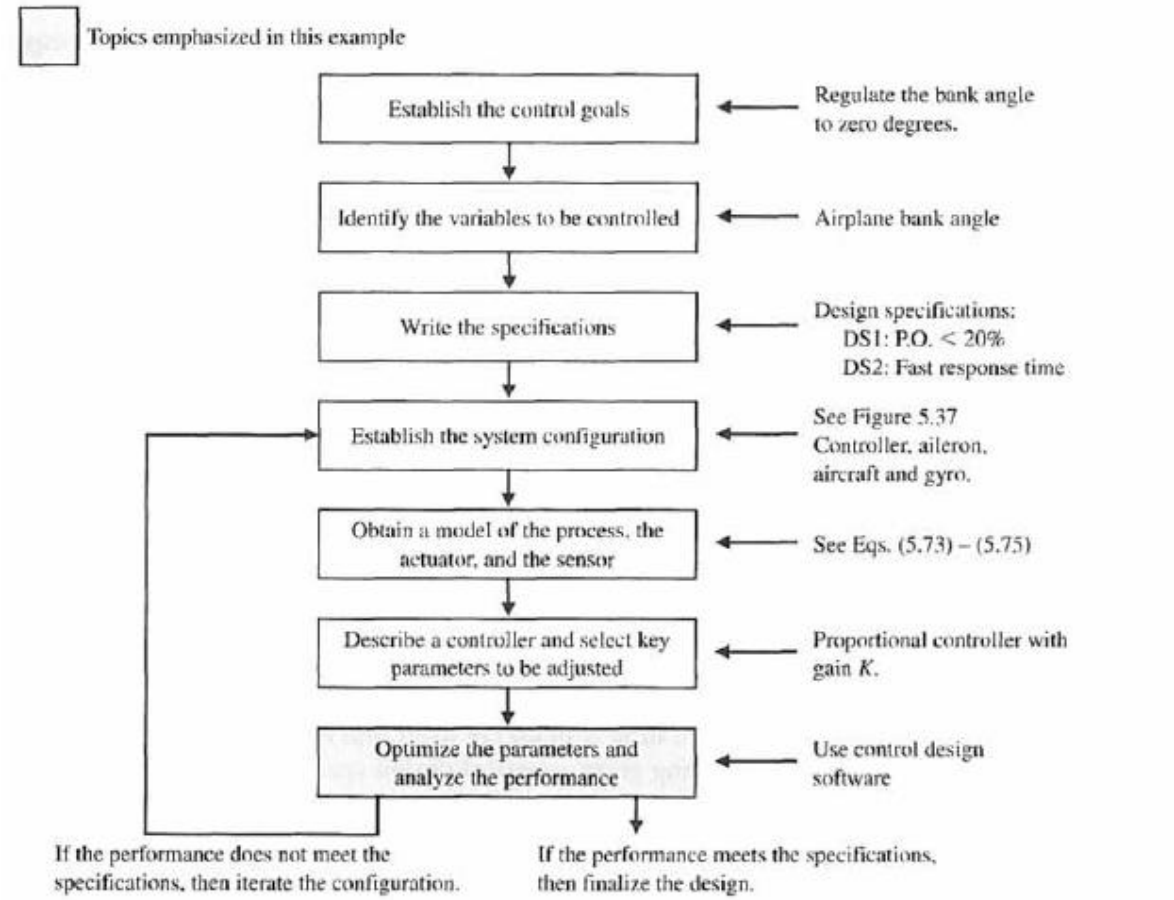


**FIGURE 5.36** Elements of the control system design process emphasized in the airplane attitude control example.

Figure 1: Design Process

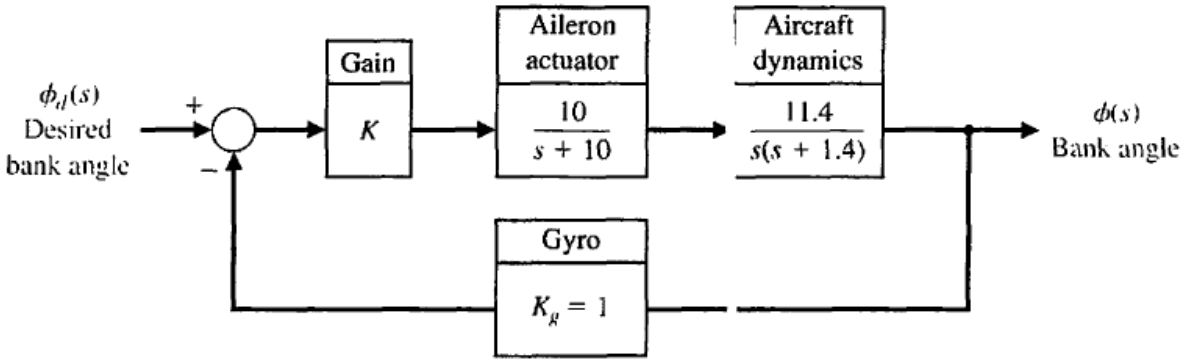


Figure 2: Bank Angle Control Autopilot

## Original System and PID Controller

The original system as shown in figure 2 does not contain the 125ms time delay which was the first step in the design process after writing system specifications and goals. With addition of the time delay, the step response is plotted in Figure 3, after a 10 second time range and a gain value of K=0.16 (specified in the textbook). The transfer function of the bank angle and aileron deflection can be seen in equation 1 below.

System *Rise Time* is calculated as 1.08 seconds, *Percent Overshoot* as 29.5%, and *Settling Time* as 8.51 seconds with the uncompensated system. We can see that these values do not meet the design requirements DS1-DS3. The time delay can be seen by the lag at the initial response on the X-axis. Additionally, the Bode plot is shown in Figure 4 with a *Gain Margin* of 8.67dB and *Phase Margin* of 43.5 degrees.

$$\frac{\phi(s)}{\delta_a(s)} = \frac{k(s - c_0)(s^2 + b_1 s + b_0)}{s(s + d_0)(s + e_0)(s^2 + f_1 s + f_0)}.$$

Equation 1 – Transfer Function of Bank Angle and Aileron Deflection Input

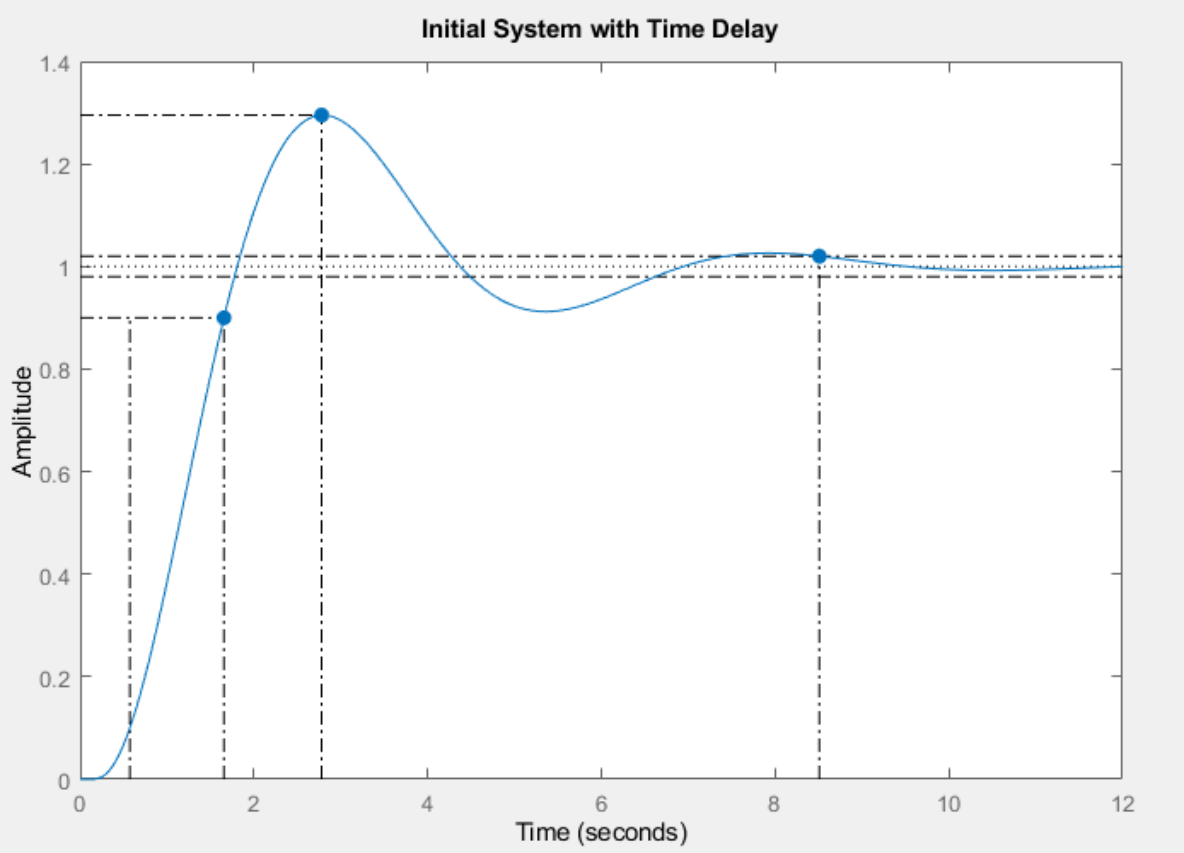


Figure 3 – System Step Response with Time Delay

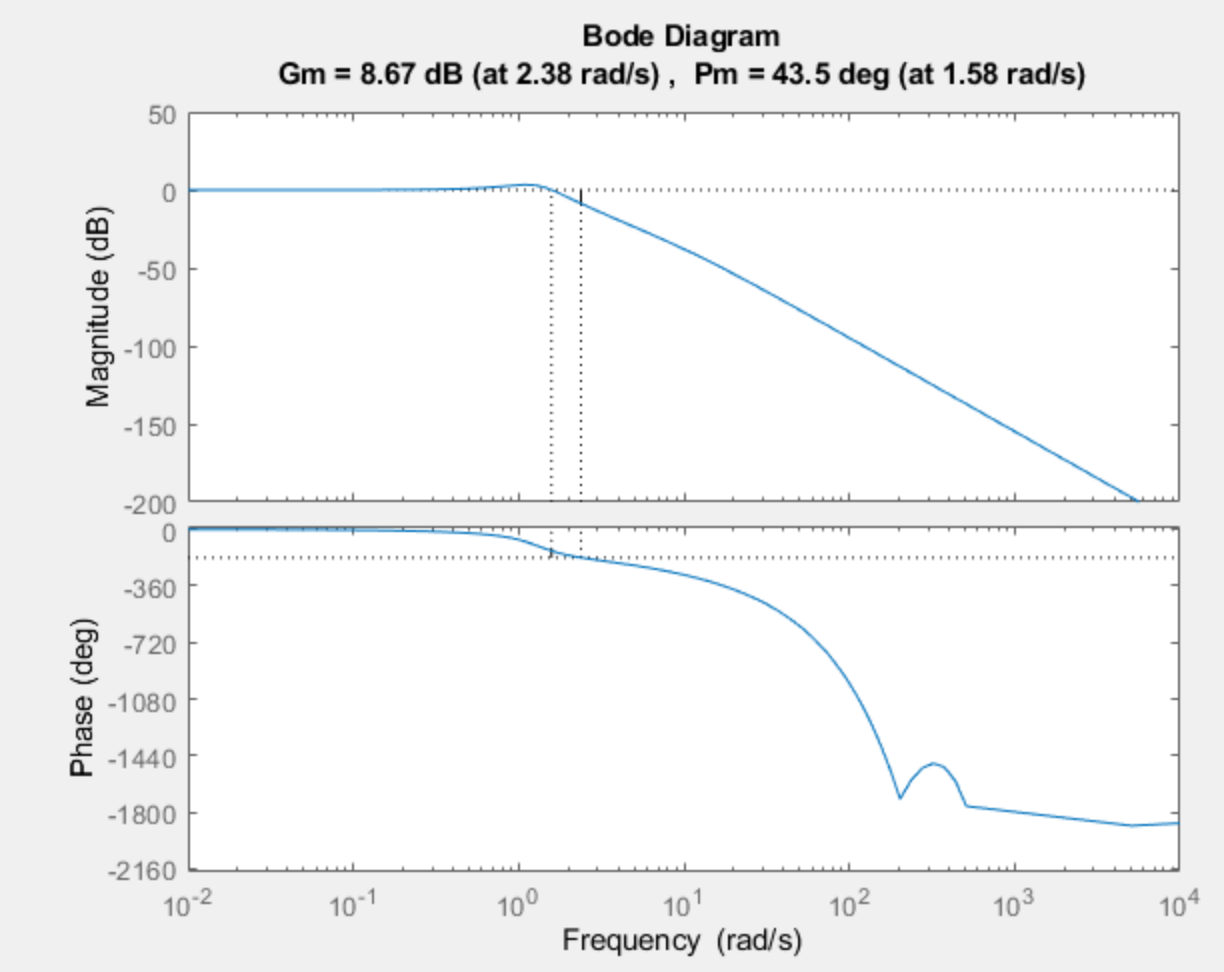


Figure 4 – Bode Diagram of Original System with Time Delay

By setting the Percent Overshoot to 20% we were able to solve for zeta with a value of Z=0.456 (equation 3) and phase margin of 45.6°. Plugging that into the settling time equation we were able to solve for Wn and get a value of 1.846 and Tp of 1.91sec for the third order system. The closed loop transfer function can be seen in equation 2 below with a 125ms time delay and excluding the gain value (K) of the system.

$$\exp(-0.125s) * \frac{114}{s^3 + 11.4\,s^2 + 14\,s}$$

Equation 2 – Matlab Transfer function with Time Delay

$$solve\ for\ z,\ 20\ =\ 100\cdot\ e^{\left(\frac{-z\cdot\pi}{\sqrt{1-z^2}}\right)}$$

Equation 3 – Percent Overshoot

$$T_p = \left(\frac{\pi}{w_n\sqrt{1-z^2}}\right) \quad T_s = \frac{4}{\zeta\omega_n}$$

Equation 4 - Peak Time Relationship and Settling Time

A mathematical relationship can be made using the values derived from the equations and analyzed but the use of control design software was permitted (Simulink and Matlab) which aided in deriving optimal PID parameters to meet the design goals of the system. The Simulink model and the step response can be seen in Figures 5 and 6. After PID tuning, the system step response showed a System *Rise Time* is calculated as 1.78 seconds, *Percent Overshoot* as 1.27%, and *Settling Time* as 4.39 seconds. Using these PID parameters Kp=0.9215, Ki=0.0166, Kd=1.3563, the system meets the original design requirements.

The Bode plot was updated based on the new values from the PID compensated system. The new system was observed as stable with increased stability in Gain and Phase margin, although the plot seemed the phase could be improved particularly in the frequency range of $11^2$ to $10^4$ rad/sec. This will be investigated in greater detail in the future.

Proportional analysis of the uncompensated system with varying gain values from 0.10 to 0.20 (0.02 step) is shown in figure 8. Typical system characteristics can be seen to shift “up and left” systematically as the gain values increase, therefore as gain values decrease the percent overshoot decreases.

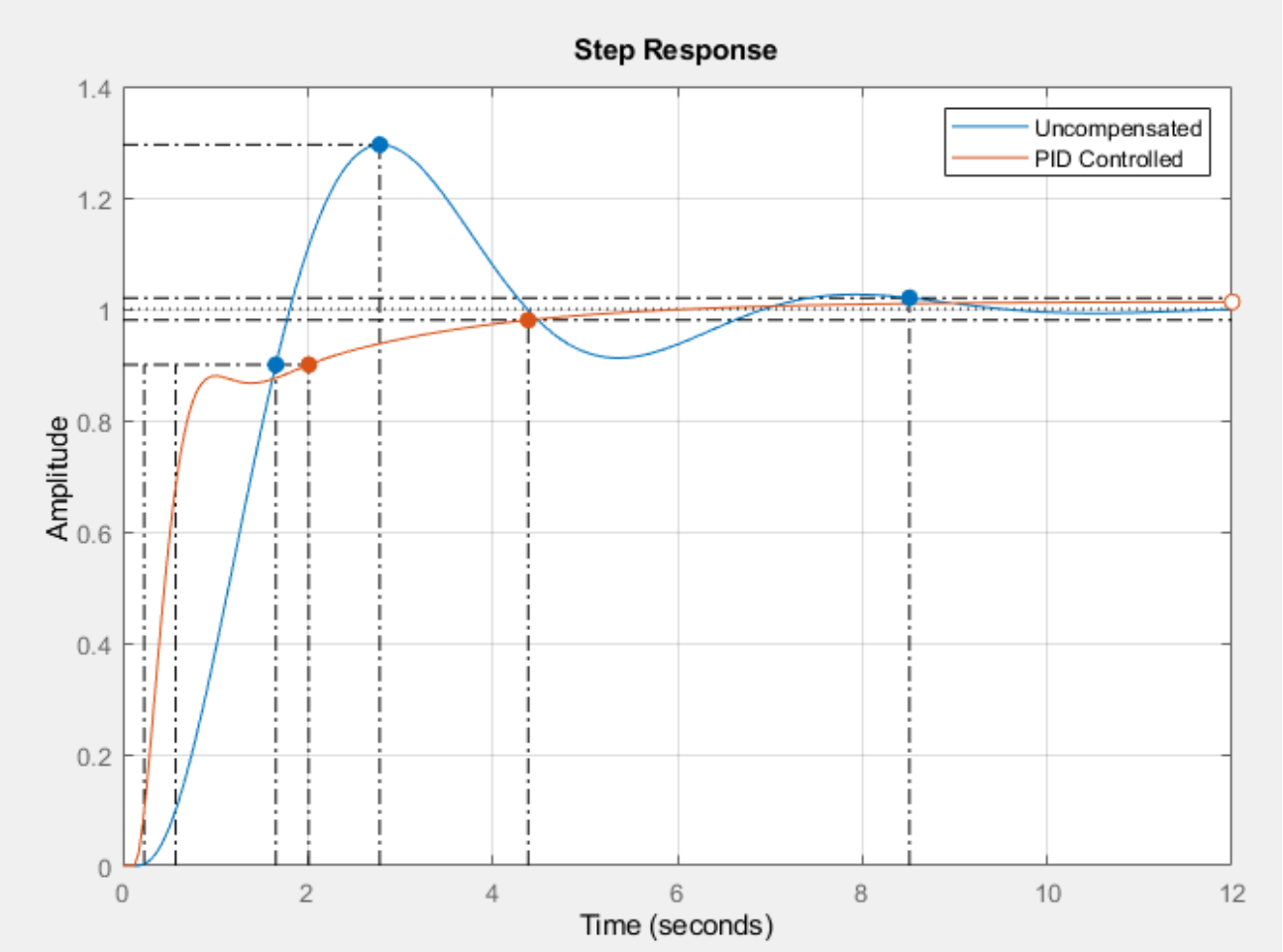


Figure 5 – System Step Response Uncompensated vs. Compensated

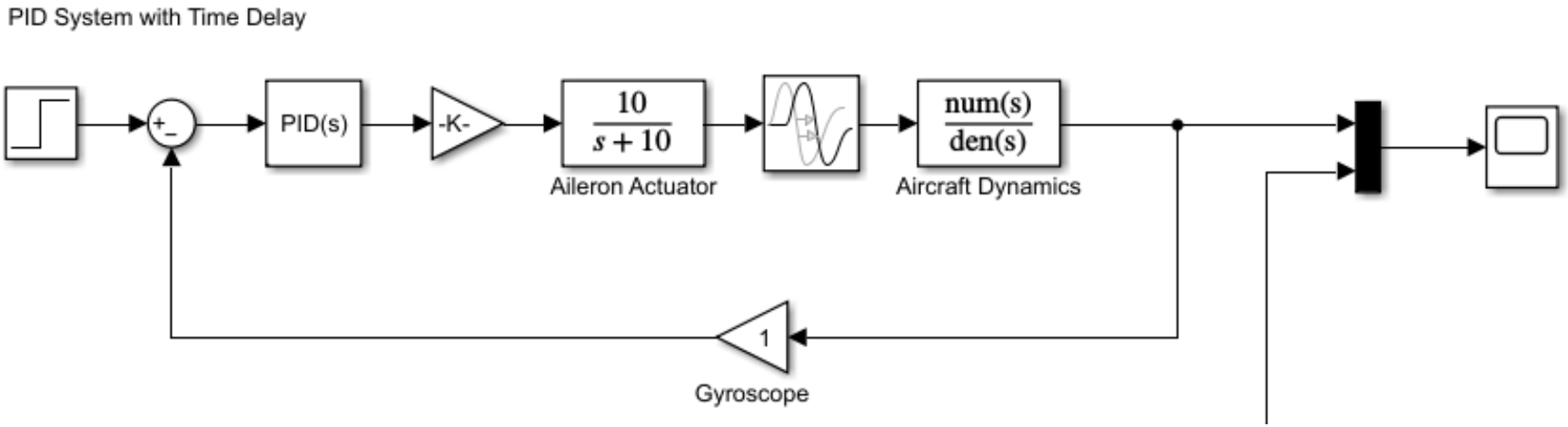


Figure 6 – Simulink model of System with PID Controller

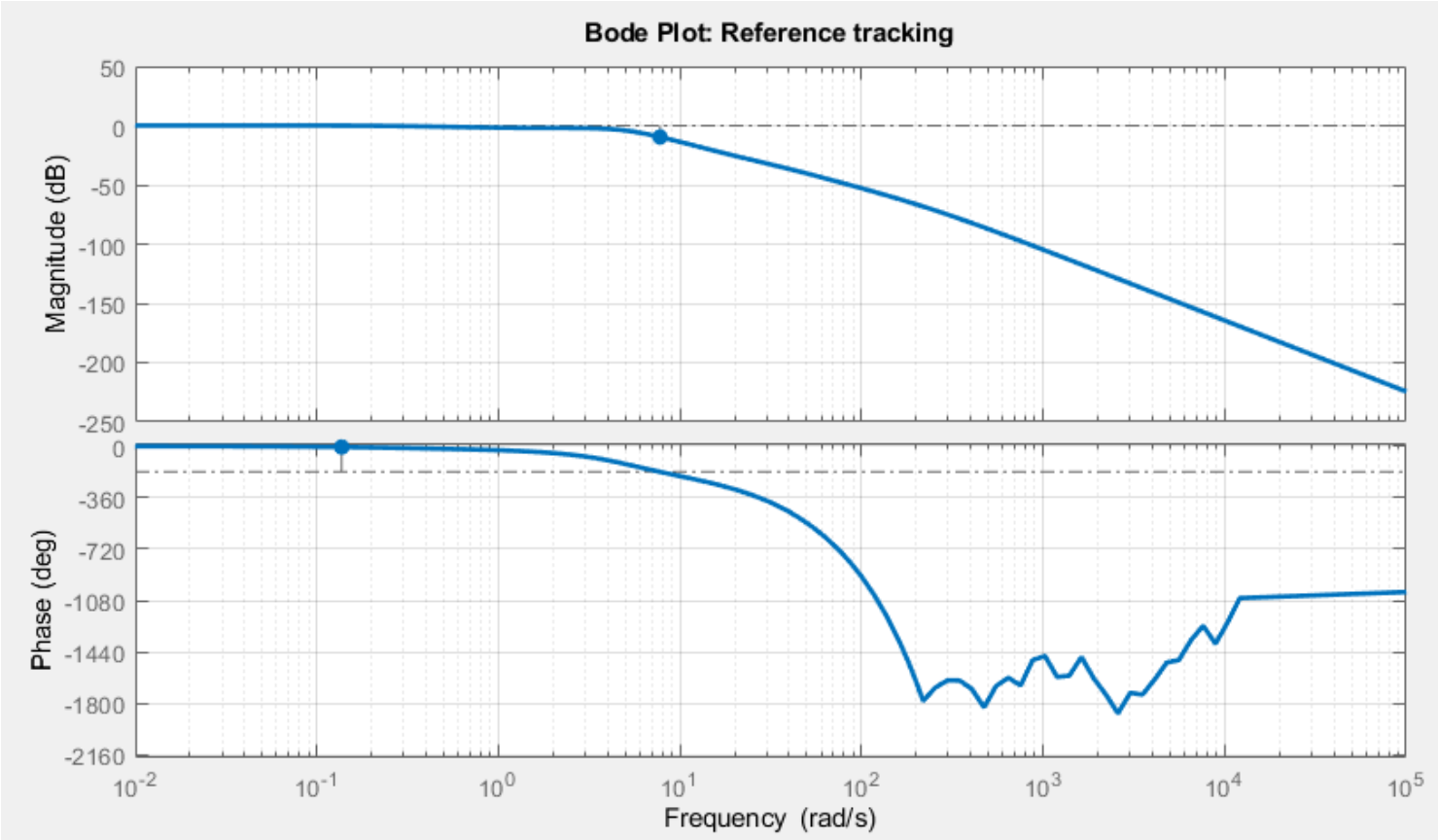


Figure 7 – PID Compensated System Bode Plot

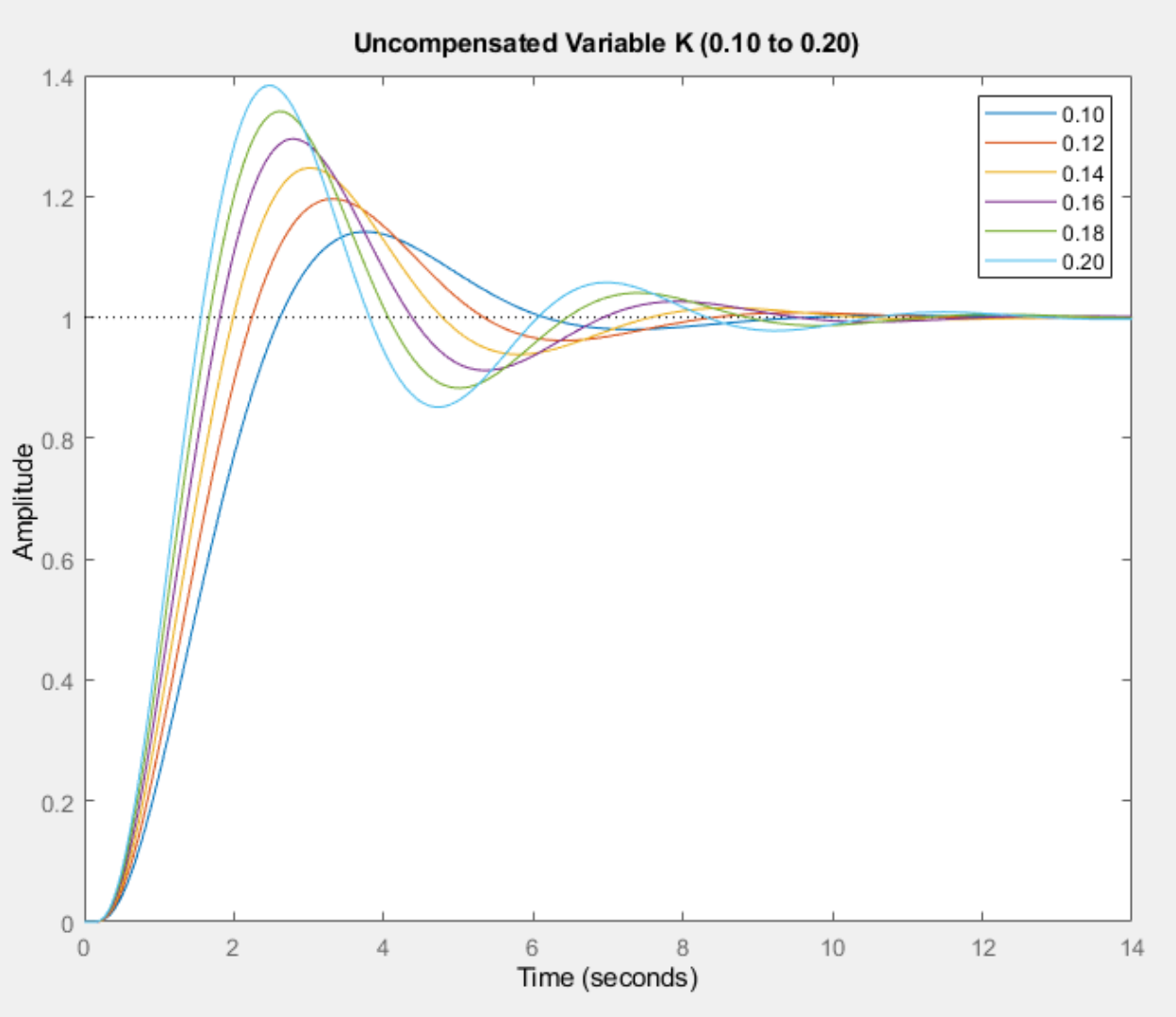


Figure 8 – Uncompensated Step Response with Gain (K) Varying

## Lead-Lag Compensator Design

With the same design requirements as specified in "Design Goals and Process" section, a lead-lag compensator design was requested. The analysis is essentially the same as the PID compensator although it was necessary to evaluate the system with and without the time delay and compare the various results in the frequency domain. In addition, the process taken for lead-lag design is different than when designing for a PID compensated system. To aid in preparation of designing a lead-lag compensator, the time delay was removed, and the root locus analyzed for poles and zero locations for the uncompensated system (Figure 9).

We can reuse the Bode plot (Figure 4) when developing ideal Kp, p, and z values for the system design. Analyzing the Bode plot will also allow us to understand the amount of additional phase margin that is needed. Here we can choose an arbitrarily high Kp value and start analyzing the systems poles and zero values. From the root locus we can see a pole at -10, -1.4, and 0.

In developing a single lead-lag compensator, we started to experiment with a high proportional gain (Kp) value of 20 and worked our way down using the equations provided. We found an alpha value of 0.677 and used that for developing a p and z value for simulation. The single stage lead lag compensator yielded the following results: *Rise Time* is calculated as 1.68 seconds, *Percent Overshoot* as 13.7%, and *Settling Time* as 5.89 seconds. The lead-lag compensator design does not meet the design requirements in terms of settling time, so a double lead stage was introduced. After adding a double lead stage, the system responded worse in regards to settling time and overshoot, however the system was more responsive. As provided in the "lead_lag_design.m" Matlab file, the system seemed to converge in respect to settling time at > 5.89 seconds and modifications made to the compensator did not yield optimal performance results (figure 11).

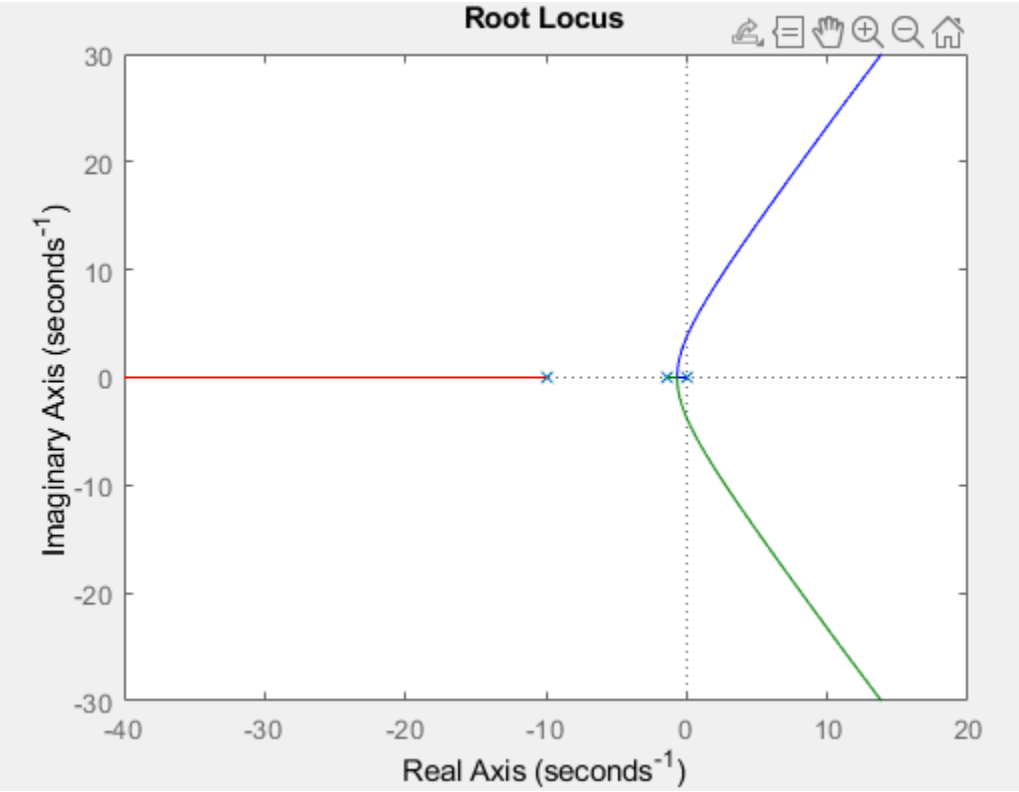

Figure 9 – Root Locus of Uncompensated System (without time delay)

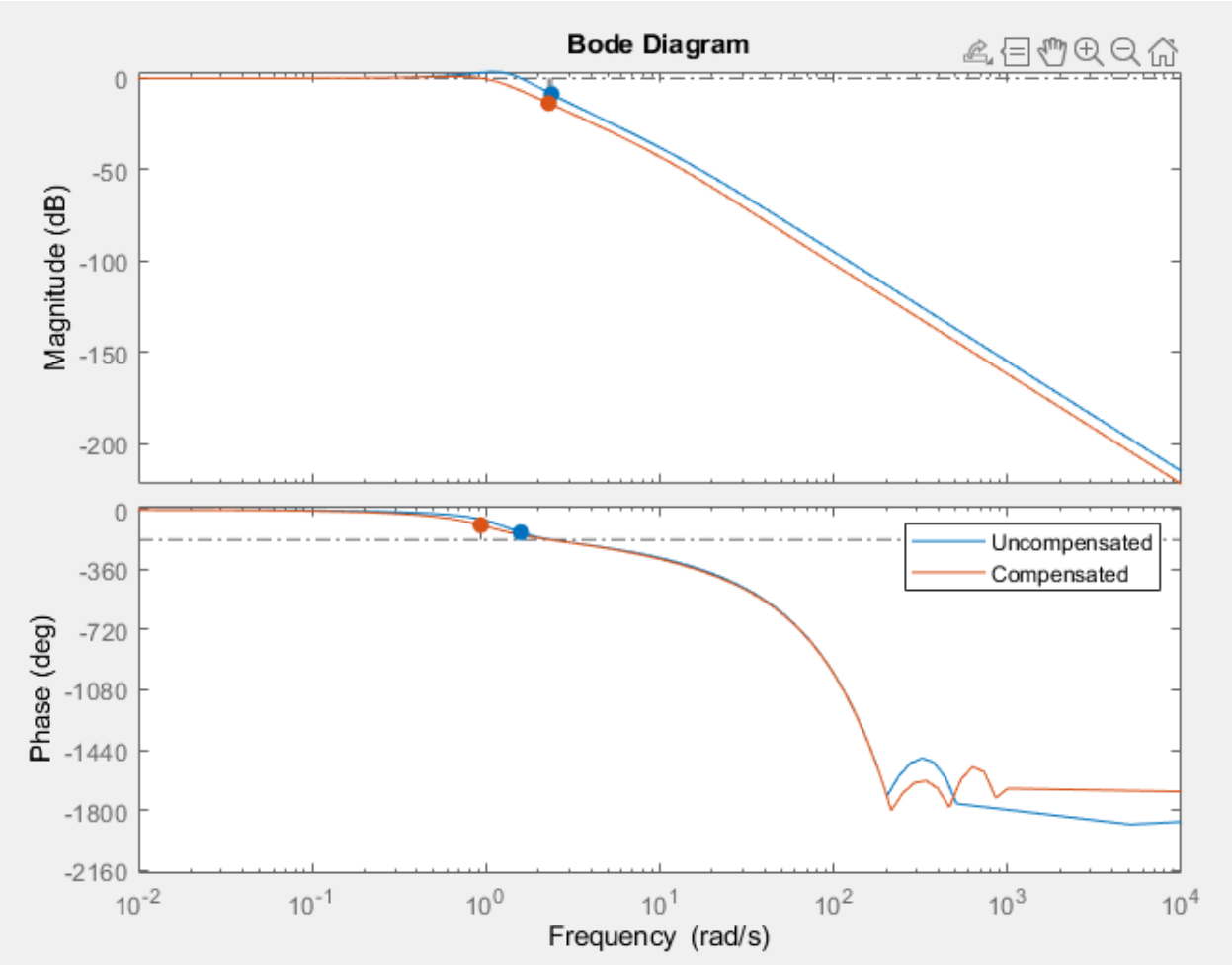


Figure 10 – Bode Plot of Lead-Lag Compensator and Uncompensated System

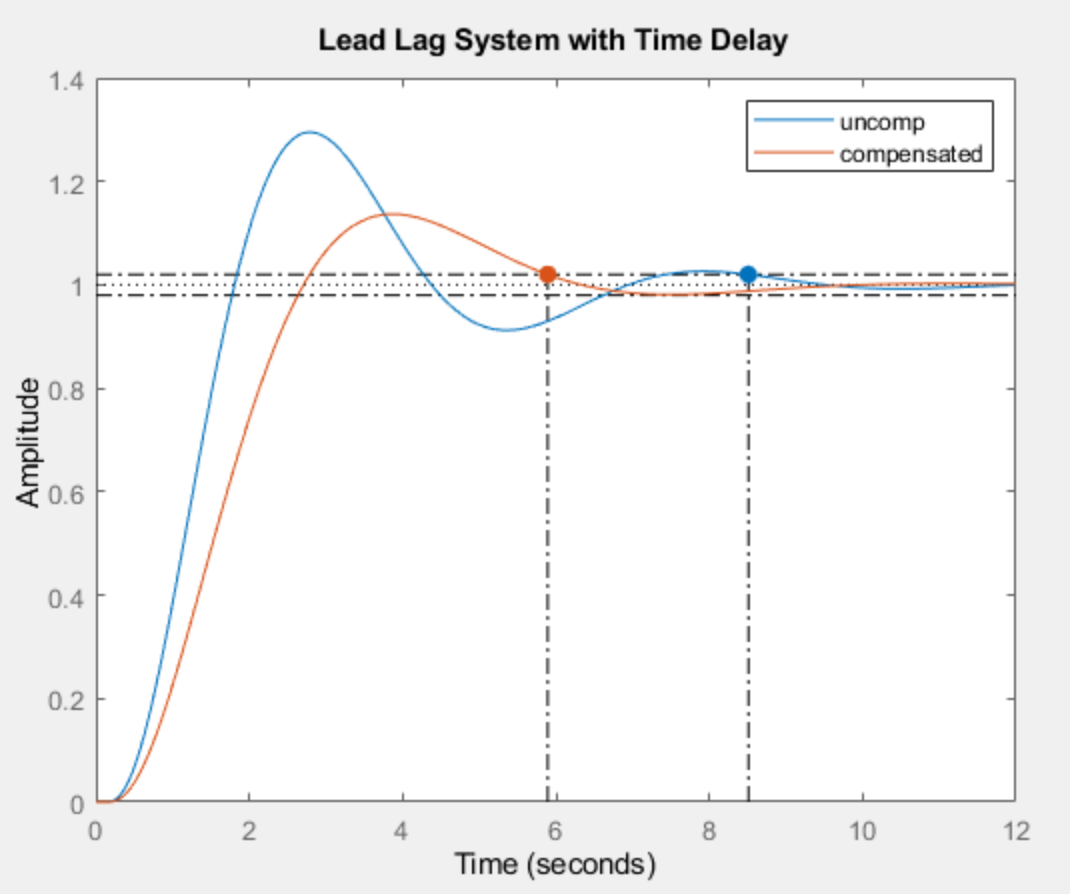


Figure 11 – System Step Response of Lead-Lag Compensator

There was a request to analyze the system without the time delay and compare the results without modification to the controller design. From Figure 12 below, we can observe that the peak response was the major difference in the compensated system. The system without the 125ms time delay showed a reduction in *percent overshoot* from 13.7% to 9.17%. Analyzing in the frequency domain we can see that the bode plot is much different in terms of phase as the phase is minimized at -270° for the system without a time delay.

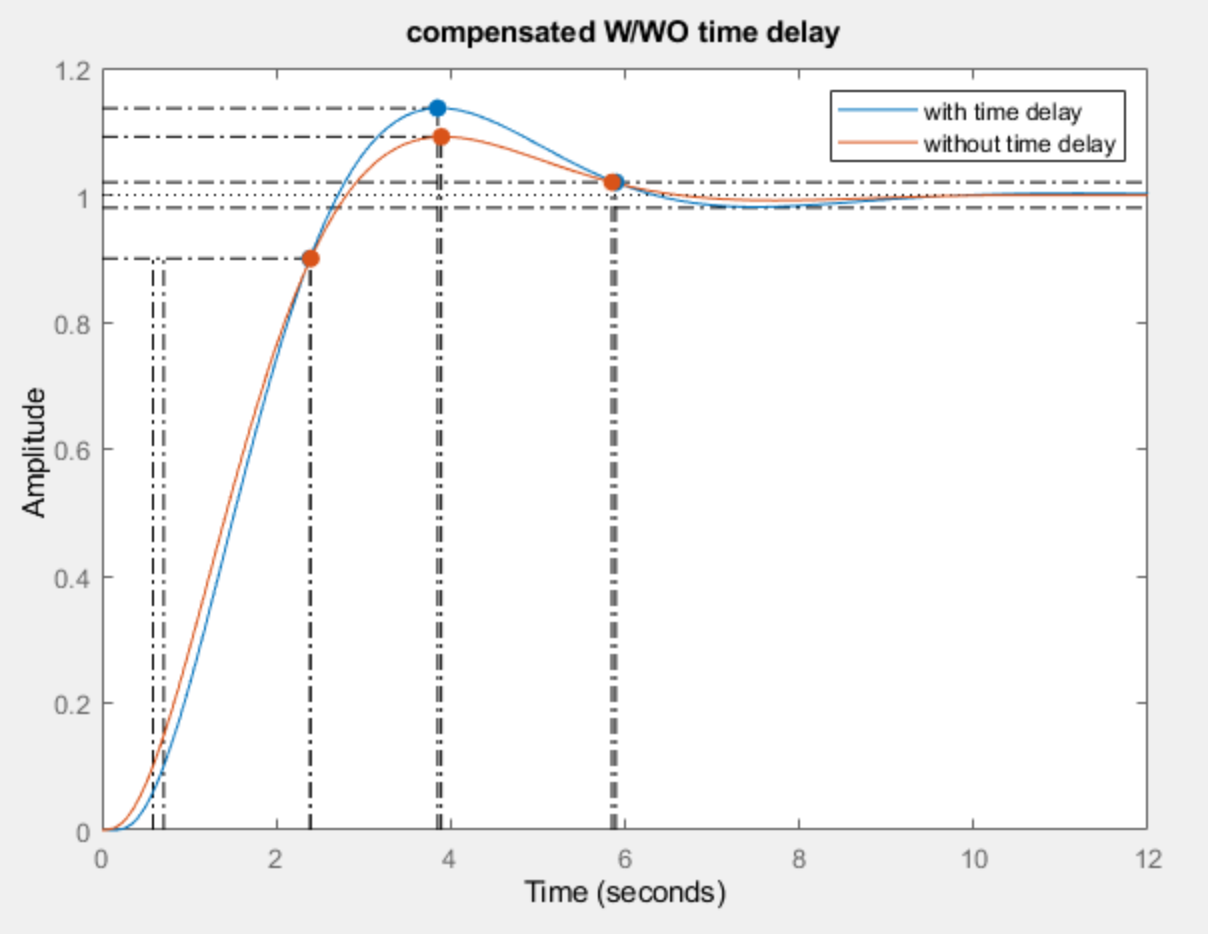


Figure 12 – Compensated with and without Time Delay

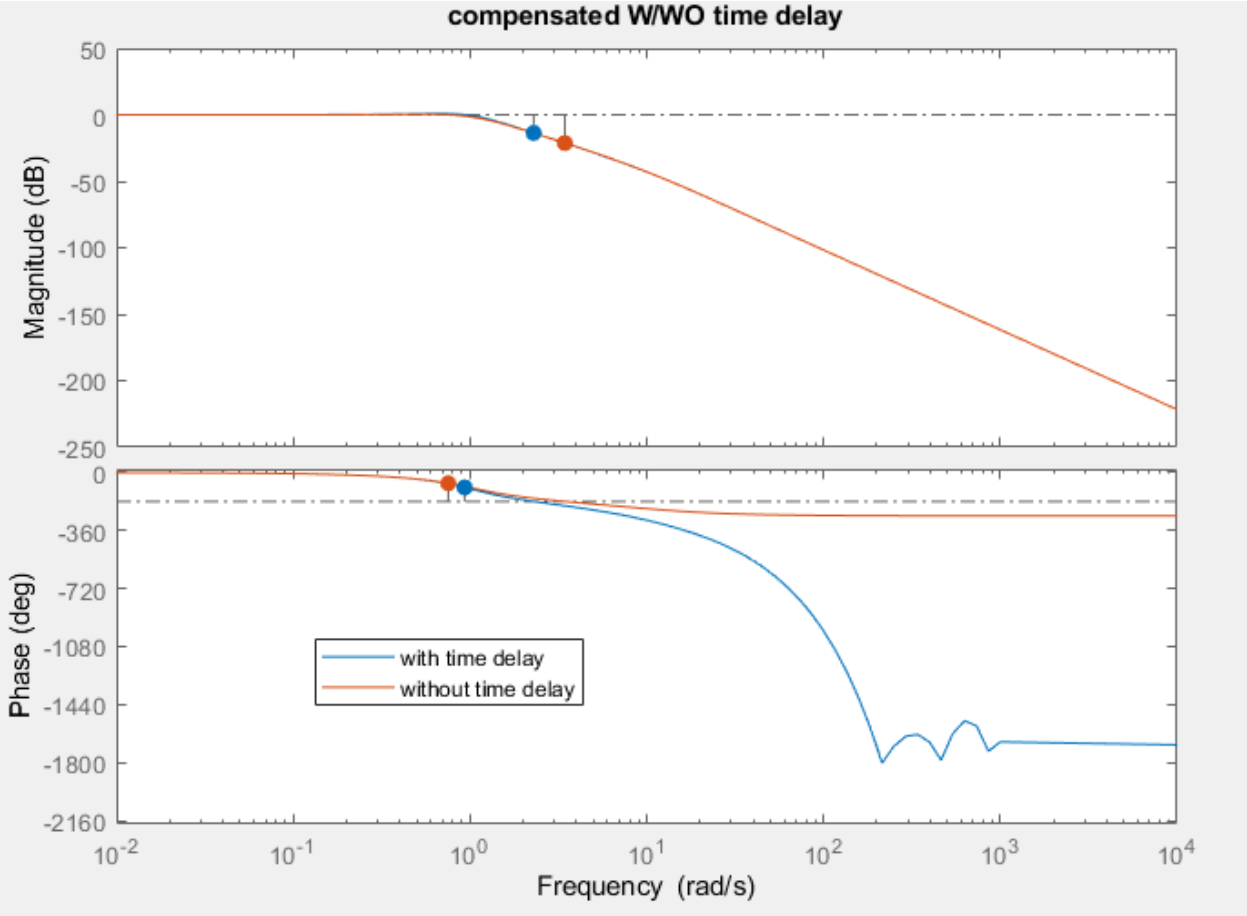


Figure 13 – Bode Compensated with and without Time Delay

# Digital Implementation

## PID Digital Implementation

A continuous implementation of the PID controller was created and verified during the PID controller design process as shown in the "PID Controller" section (Figure 6). A digital implementation was developed in Simulink to compare results and understand how sample time effects the performance of the system. An initial sample time was set for the PID controller and changed to a discrete implementation while modifying the step input to match the sample rate of 0.1 (10Hz). The PID parameters were kept the same as in the continuous model and plotted below. The blue trace on the scope shows the digital implementation compared to the continuous (yellow), along with the original uncompensated system in orange. The retuned digital implementation does not meet the settling time design requirements and seems to only increase as the sampling rate decreases/sample time increases.

When trying to re-tune at a slower sampling rate it is very difficult to meet any of the design requirements. The signal looks “binned” due to the slow sampling rate as shown in figure 15. Knowing the exact limit a controller can sample is rather difficult and application dependent although I found that anything over 0.1 or <10 Hz produced inaccurate results for this PID implementation.  A designer should consider the following when selecting a sample rate:

1. Make the sampling time T small enough to react to disturbances affecting the system.
2. Make the sampling time large enough to avoid numerical errors.
3. Make the sampling time large enough to avoid fast and expensive control hardware. (Bemporad, 2010)

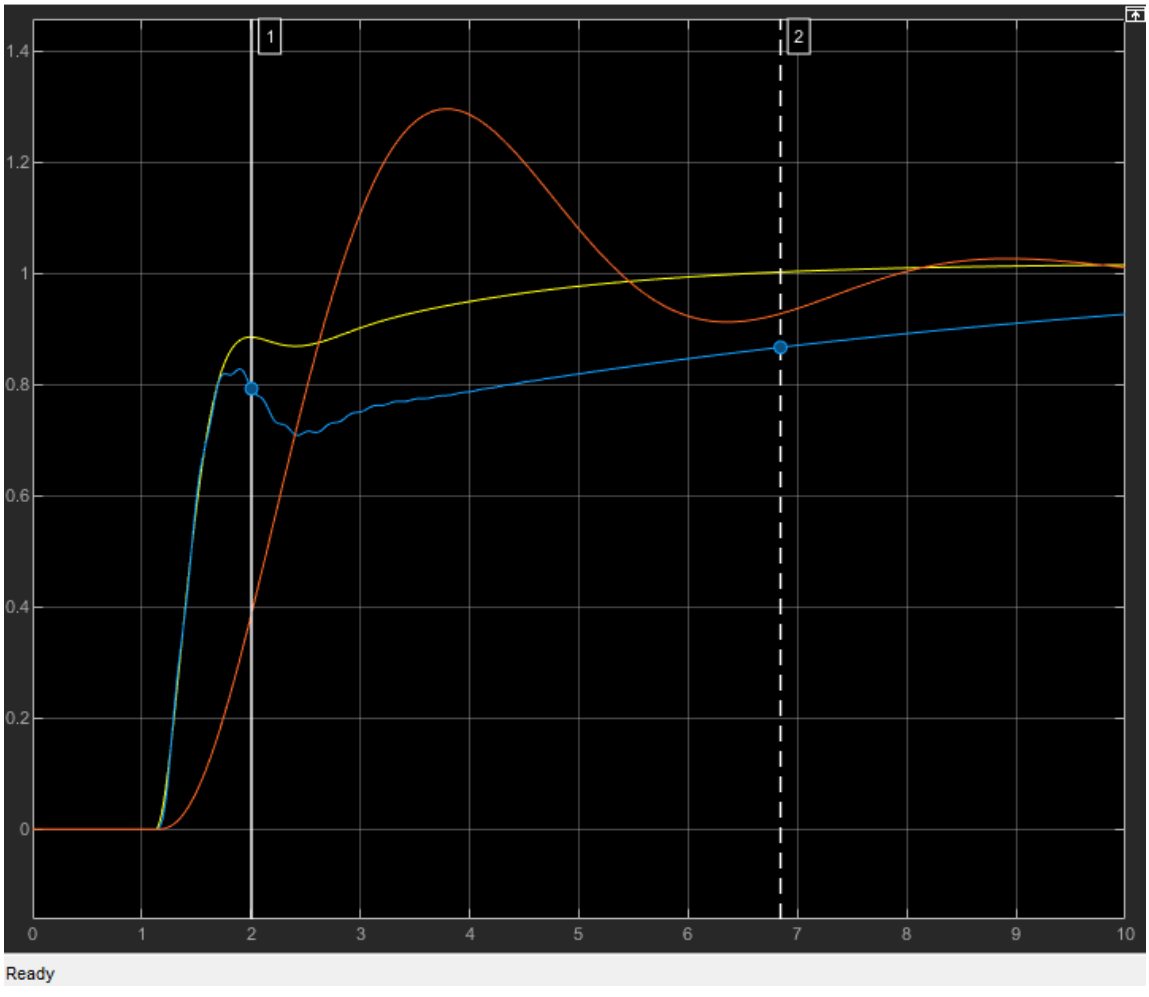


Figure 14 – Digital and Continuous Implementation Step Response

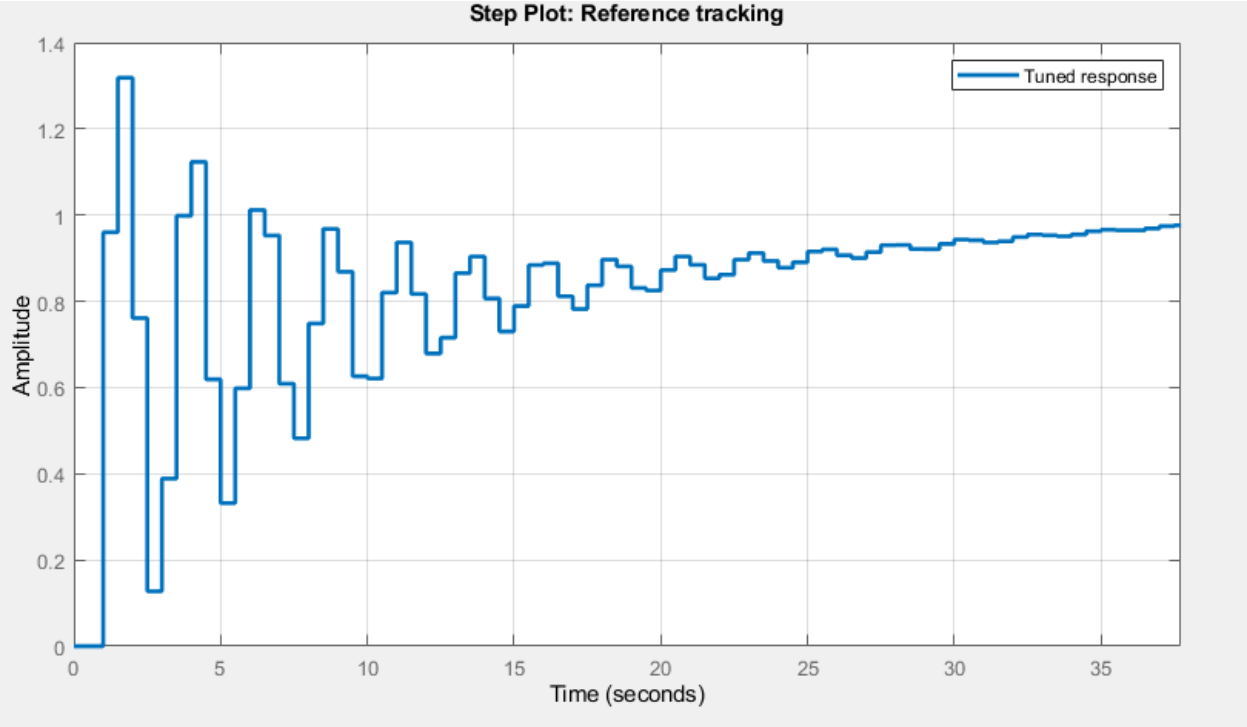


Figure 15 – Digital PID Step Response at 2 Hz sampling

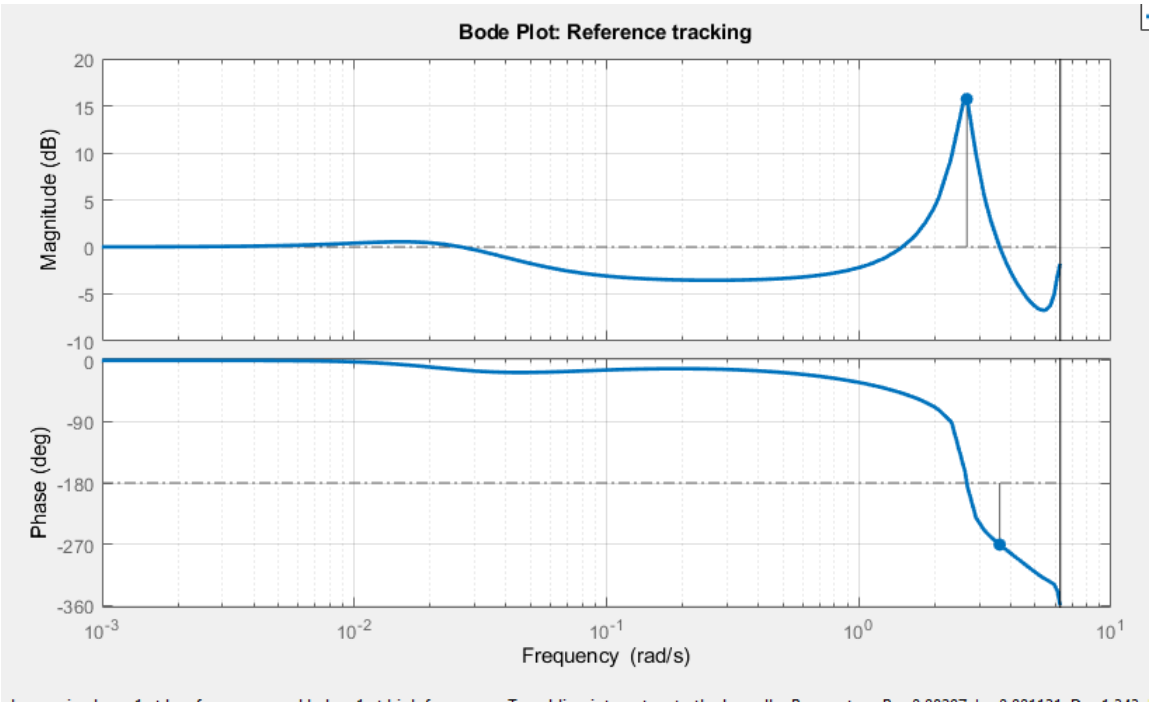


Figure 16 – Digital PID Bode Plot at 2 Hz sampling

When removing the time delay from the actuator transfer we can see that the percent overshoot was eliminated (green). All the signals for the PID implementation are compared and plotted in the step response signal in Figure 17.

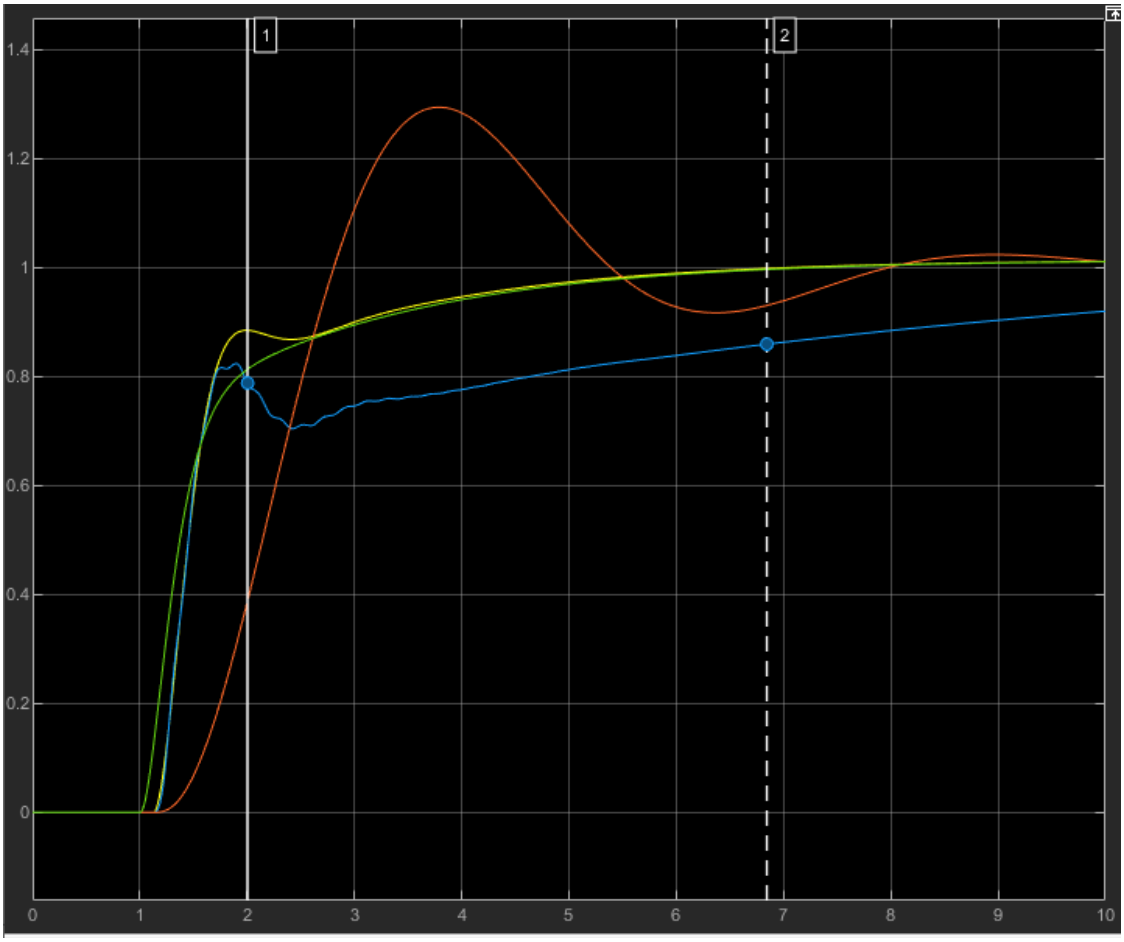


Figure 17 – All PID systems and Original Step Response

## Lead Lag Digital Implementation

The idea was to duplicate the analysis performed in the previous digital PID section with the lead lag controller design as a discrete implementation. This was accomplished by using the Matlab function "c2d" to convert the continuous to discrete form as shown in Figure 18 with a sample time of Ts=0.1sec. Both transfer functions include the proportional gain value (Kp=0.6). Figure 19 shows the scope differences of the discrete (blue) vs. continuous signal (yellow). The discrete signal matches very closely to the continuous signal.

Next, I have increased the sample time to T=0.5 then 0.1. What I noticed is that as the sample time increases the percent overshoot and settling time of the system increases. The signal starts to become oscillatory, and the time domain window needs to be extended to observe steady state (Figure 20). To understand how the time delay effects the digital system, the sample time was kept at T=1.5 while removing the time delay from the actuator signal. This is shown in Figure 21 which we can see that the system step is more responsive than with the delay.

Overall, it seems as if the lead-lag compensated system is an optimal design choice than the PID if handling a slower sample time is a requirement as it does so more gracefully. Similarly, to the PID, I believe if sample time is increased over 0.1-0.2sec, the system performance will start to degrade.

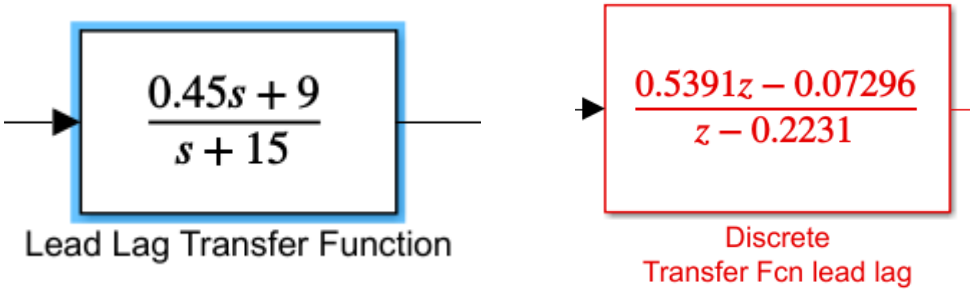


Figure 18 – Continuous Lead Lag converted to Discrete (with Kp)

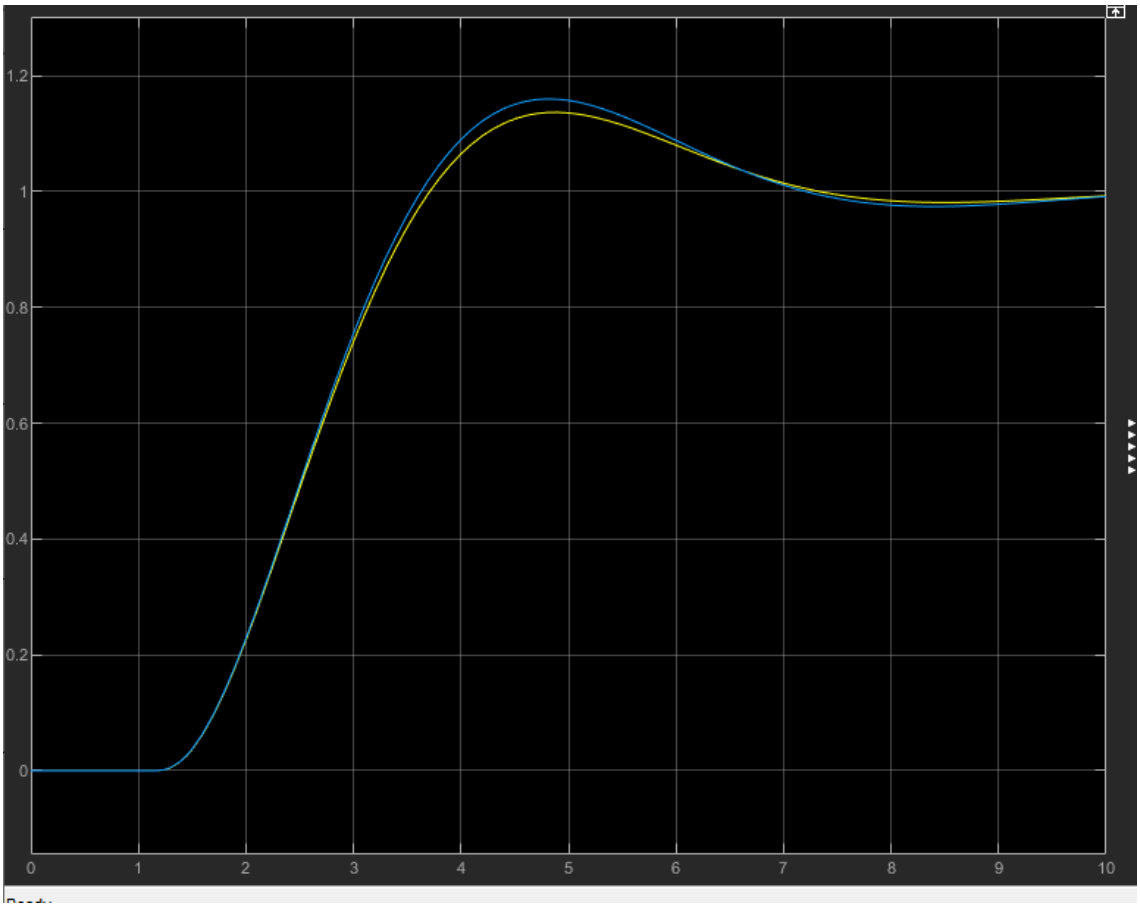


Figure 19 – Continuous Lead Lag converted to Discrete

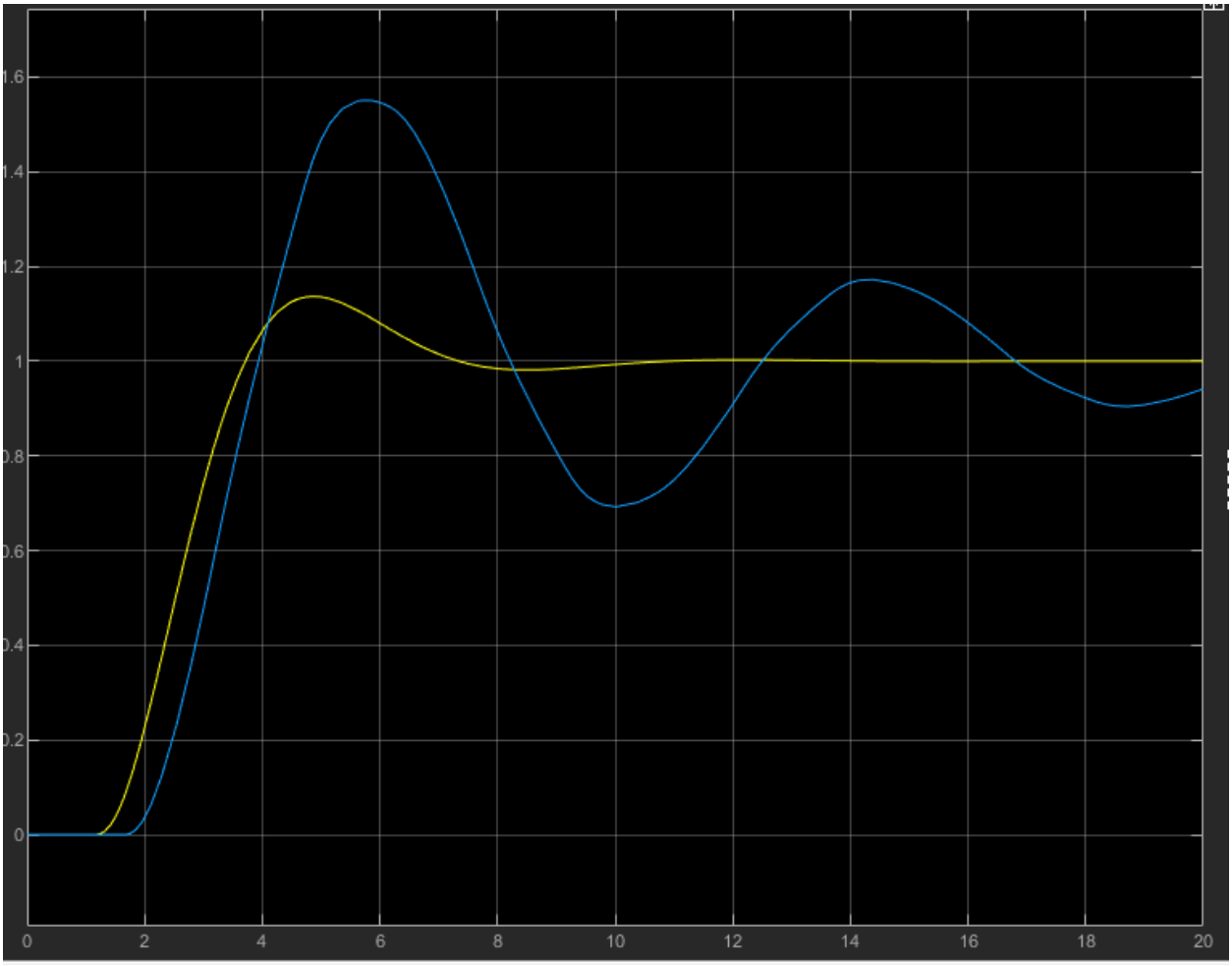


Figure 20 – Continuous Lead Lag converted to Discrete at T=1.5sec

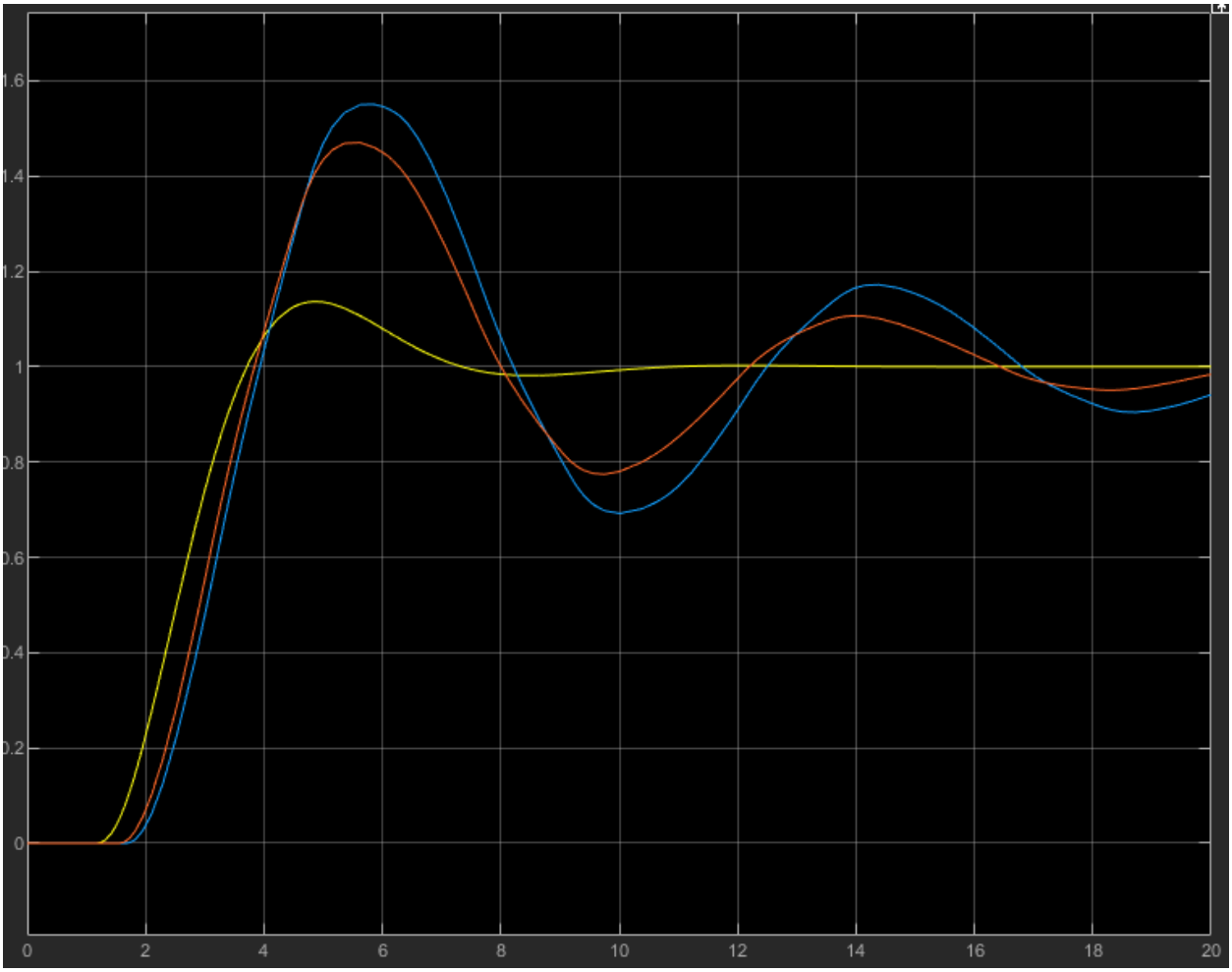


Figure 21 – Continuous Lead Lag without time delay

## References

Dorf, R. C., & Bishop, R. H. (2010). *Modern Control Systems (12th Edition)* (12th ed.). Pearson.

Bemporad, A. B. (2010). *Automatic Control 2 - Sampling* [Slides]. Research Gate. https://www.researchgate.net/profile/Hazim-Tahir/post/Why-is-proper-selection-of-sampling-important/attachment/59d61d9879197b8077978591/AS%3A271756365893632%401441803174401/download/AC2-03-Sampling.pdf