Includes MAX 7000E & MAX 7000S

MAX 7000

Programmable Logic Device Family

July 1999, ver. 6.01 | Data Sheet

Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation Multiple Array MatriX (MAX®) architecture
- 5.0-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface available in MAX 7000S devices
- Includes 5.0-V MAX 7000 devices and 5.0-V ISP-based MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see Tables 1 and 2)
- 5-ns pin-to-pin logic delays with up to 175.4-MHz counter frequencies (including interconnect)
- Peripheral component interconnect (PCI)-compliant devices available

For information on in-system programmable 3.3-V MAX 7000A or 2.5-V MAX 7000B devices, see the *MAX 7000A Programmable Logic Device Family Data Sheet* or the *MAX 7000B Programmable Logic Devices Advance Information Brief*.

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7064	EPM7096	EPM7128E	EPM7160E	EPM7192E	EPM7256E
Usable gates	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	64	96	128	160	192	256
Logic array blocks	2	4	6	8	10	12	16
Maximum user I/O pins	36	68	76	100	104	124	164
t_{PD} (ns)	6	6	7.5	7.5	10	12	12
t_{SU} (ns)	5	5	6	6	7	7	7
t_{FSU} (ns)	2.5	2.5	3	3	3	3	3
t_{CO1} (ns)	4	4	4.5	4.5	5	6	6
f_{CNT} (MHz)	151.5	151.5	125.0	125.0	100.0	90.9	90.9

Table 2. MAX 7000S Device Features

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t_{PD} (ns)	5	5	6	6	7.5	7.5
t_{SU} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f_{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations, and the Quartus™ development system for Windows-based PCs and Sun SPARCstation and HP 9000 Series 700 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 3 for available speed grades.

Table 3. MAX 7000 Speed Grades

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

Table 4. MAX 7000 Device Features

Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface *(2)*	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:
(1) Available in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 *(2)*	100				
EPM7160E					64	84		104				
EPM7160S					64		84 *(2)*	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 *(2)*		164		164
EPM7256S											164 *(2)*	164

Notes:
(1) When the JTAG interface in MAX 7000S devices is used, four I/O pins become JTAG pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See the *Operating Requirements for Altera Devices Data Sheet* for more information.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by the Quartus and MAX+PLUS II development systems, a single, integrated package that allows schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The Quartus and MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations. The Quartus software runs on Windows-based PCs, as well as Sun SPARCstation and HP 9000 Series 700 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram

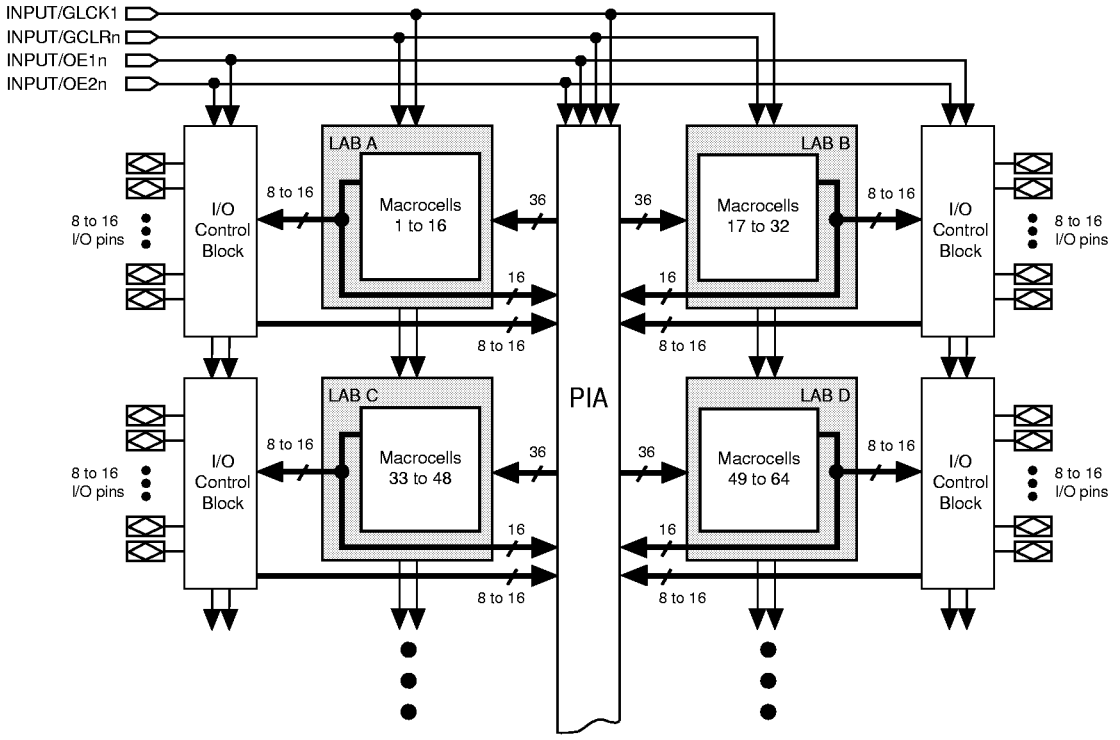
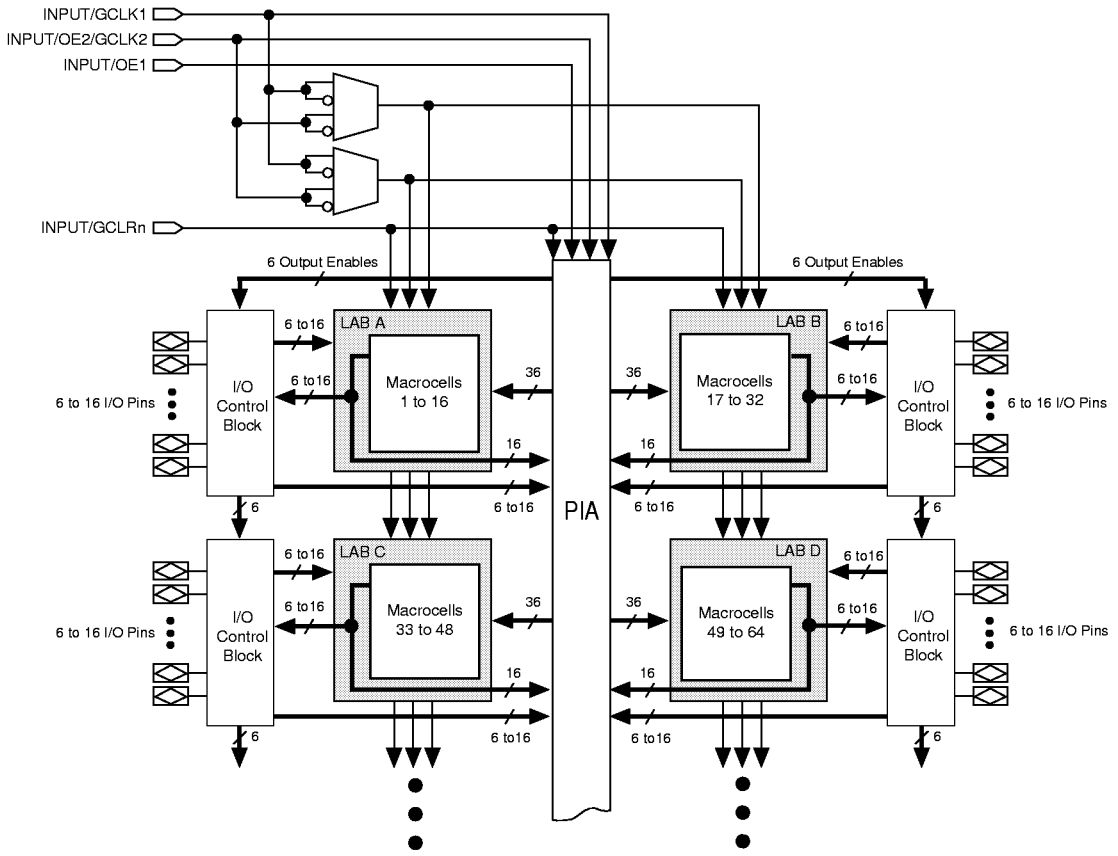


Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

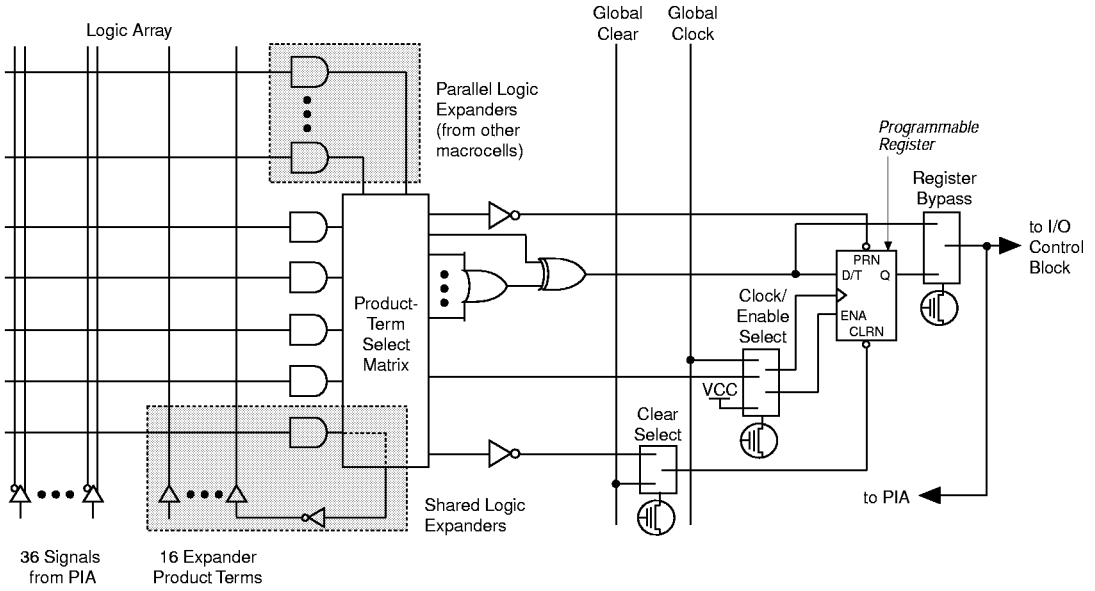
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

Macrocells

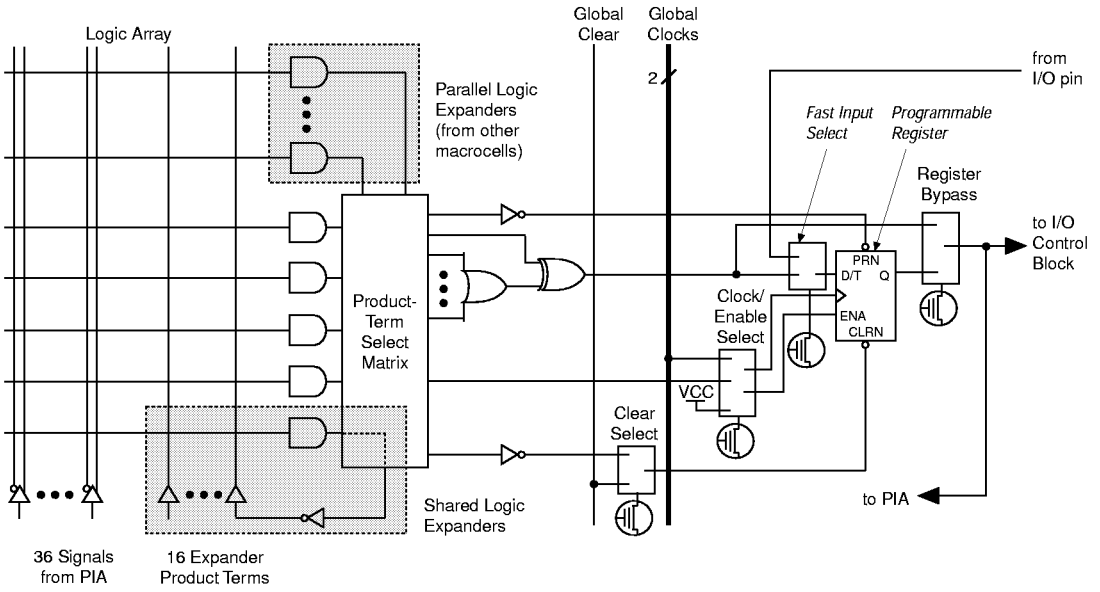
The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell



The macrocell of MAX 7000E and MAX 7000S devices is shown in Figure 4.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Quartus and MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Quartus and MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in Figure 1. In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figures 3 and 4, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5-ns) input setup time.

Expander Product Terms

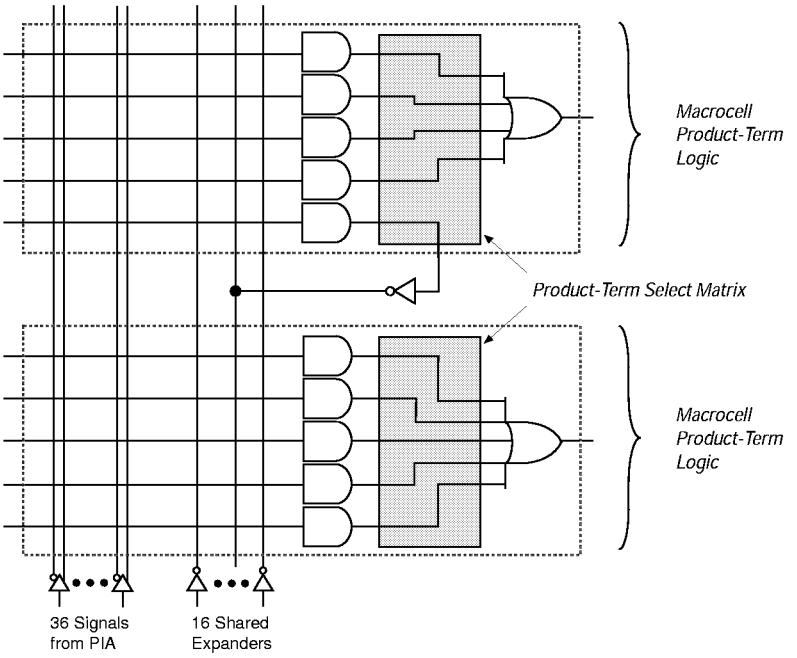
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

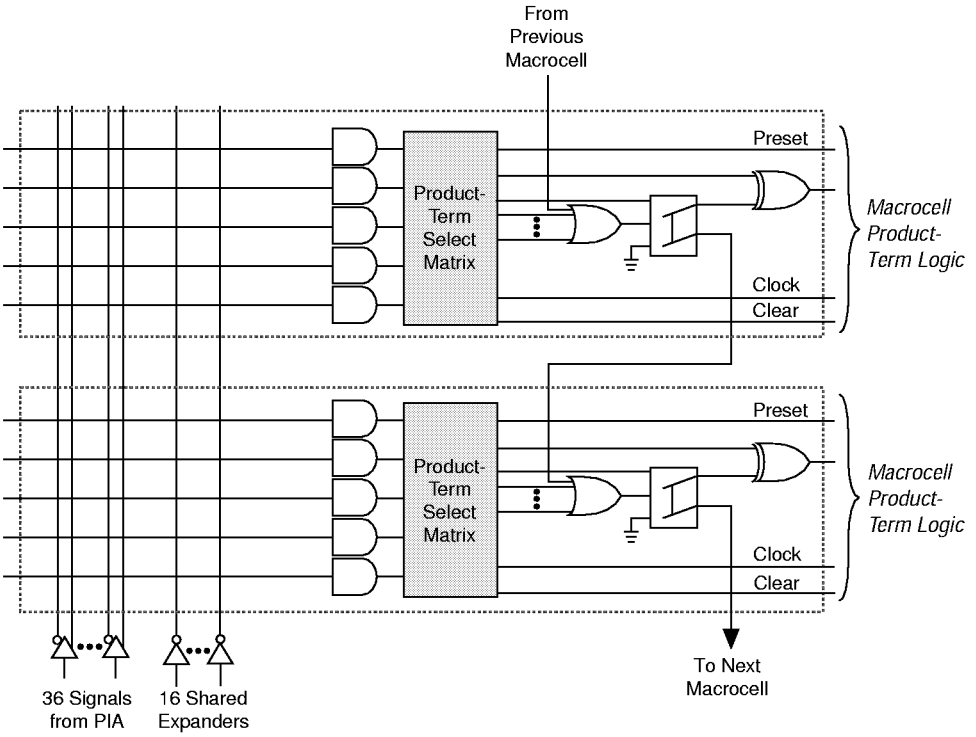
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Quartus and MAX+PLUS II Compilers can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

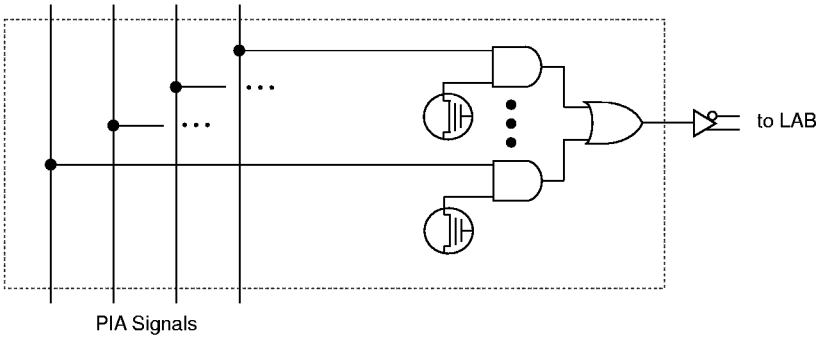
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



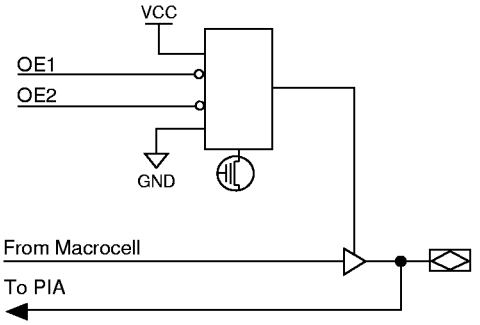
While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

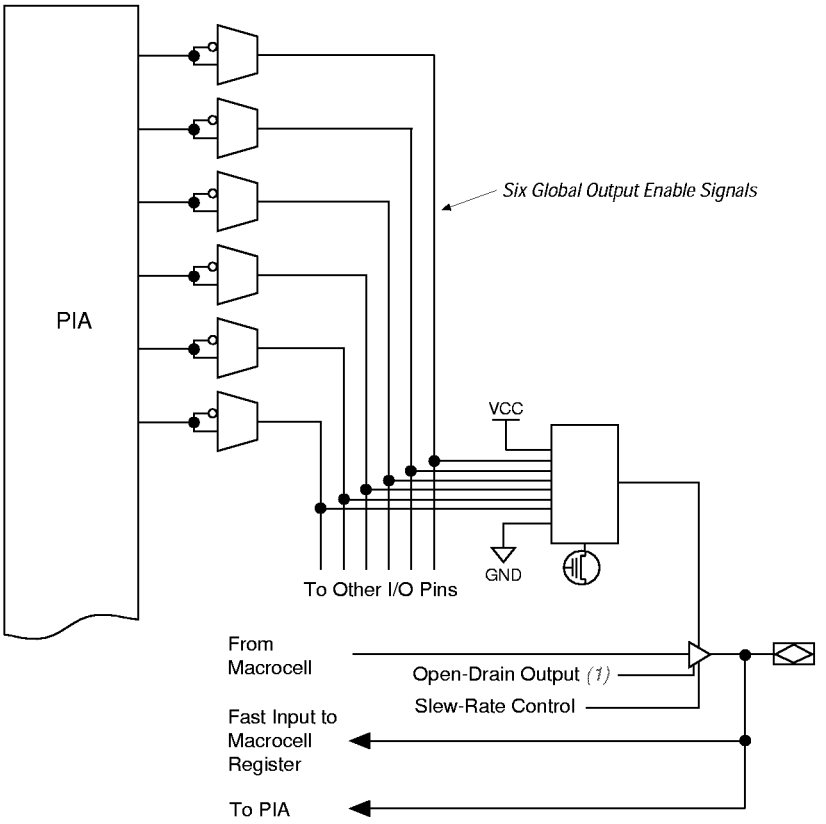
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7064 & EPM7096 Devices



MAX 7000E & MAX 7000S Devices



Note:
(1) The open-drain output option is available in MAX 7000S devices only.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera BitBlaster, ByteBlaster, ByteBlasterMV, or MasterBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers can not support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm are marked with an "F" suffix in the ordering code.

The Jam™ programming and test language can be used to program MAX 7000S devices with in-circuit test equipment (e.g., PC, embedded processor).

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor).*

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, and t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When V_{CCIO} is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Output pins on 5.0-V MAX 7000S devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the MAX+PLUS II Programmer, an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device. For more information, see the *Altera Programming Hardware Data Sheet*.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 6 describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables starting on page 55 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 6. MAX 7000 JTAG Instructions

JTAG Instruction	Devices	Description
SAMPLE/PRELOAD	EPM7128S EPM7160S EPM7192S EPM7256S	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	EPM7128S EPM7160S EPM7192S EPM7256S	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ISP Instructions	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	These instructions are used when programming MAX 7000S devices via the JTAG ports with the BitBlaster, ByteBlaster, ByteBlasterMV, or MasterBlaster download cable, or using a Jam File (**.jam**), Jam Byte-Code (**.jbc**), or Serial Vector Format (**.svf**) file via an embedded processor or test equipment.

The instruction register length of MAX 7000S devices is 10 bits. Tables 7 and 8 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

Table 7. MAX 7000S Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032S	1 *(1)*
EPM7064S	1 *(1)*
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

Note:
(1) This device does not support JTAG boundary-scan testing.

Table 8. 32-Bit MAX 7000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Figure 9 shows the timing requirements for the JTAG signals.

Figure 9. MAX 7000 JTAG Waveforms

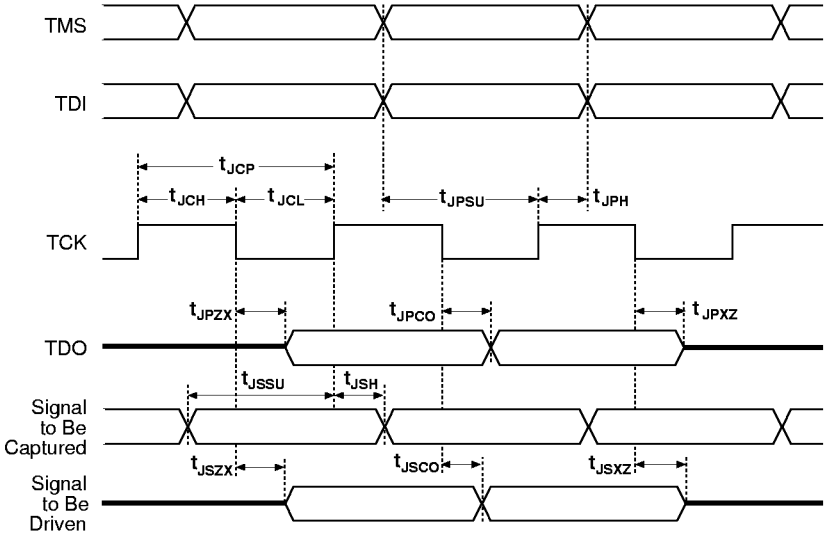


Table 9 shows the JTAG timing parameters and values for MAX 7000S devices.

Table 9. JTAG Timing Parameters & Values for MAX 7000S Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

For more information, see *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Design Security

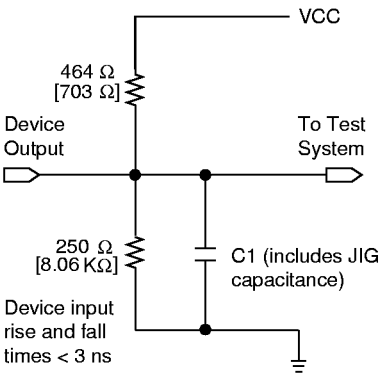
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 10. Test patterns can be used and then erased during early stages of the production flow.

Figure 10. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.

For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet*.

MAX 7000S devices are not shipped in carriers.

Operating Conditions

Tables 10 through 15 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

Table 10. MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Table 11. MAX 7000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3)*, *(4)*, *(5)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during ISP	*(6)*	4.75	5.25	V
V_I	Input voltage		–0.5 *(7)*	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 12. MAX 7000 5.0-V Device DC Operating Conditions *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5 *(7)*	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(9)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.0 V *(9)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(10)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V *(10)*		0.2	V
I_I	Leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	I/O pin tri-state output off-state current	V_O = V_{CC} or ground *(11)*	–40	40	µA

Table 13. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 14. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

Table 15. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (12)*

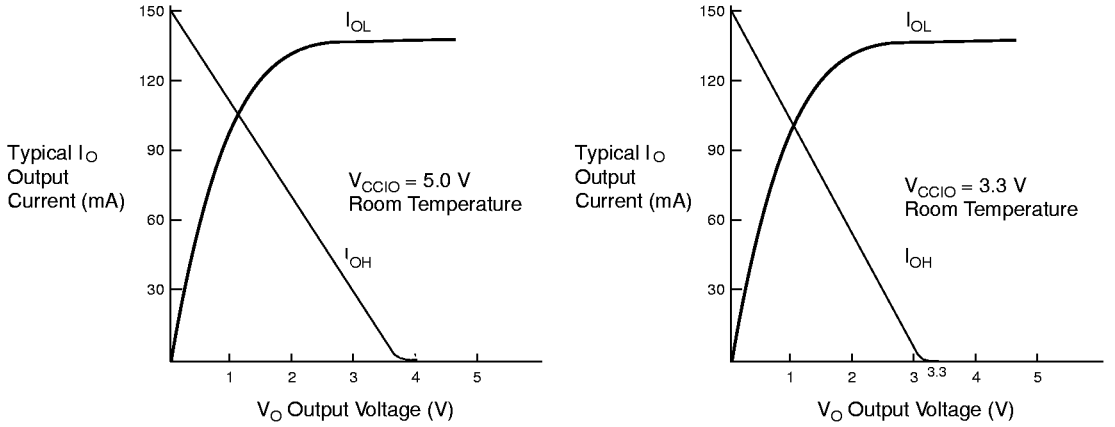
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage on I/O pins is –0.5 V and on 4 dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) V_{CC} must rise monotonically.
(5) 3.3-V I/O operation is not available for 44-pin packages.
(6) The V_{CCISP} parameter applies only to MAX 7000S devices.
(7) During in-system programming, the minimum DC input voltage is –0.3 V.
(8) These values are specified in Table 11 on page 23.
(9) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(10) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
(11) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically –60 µA.
(12) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

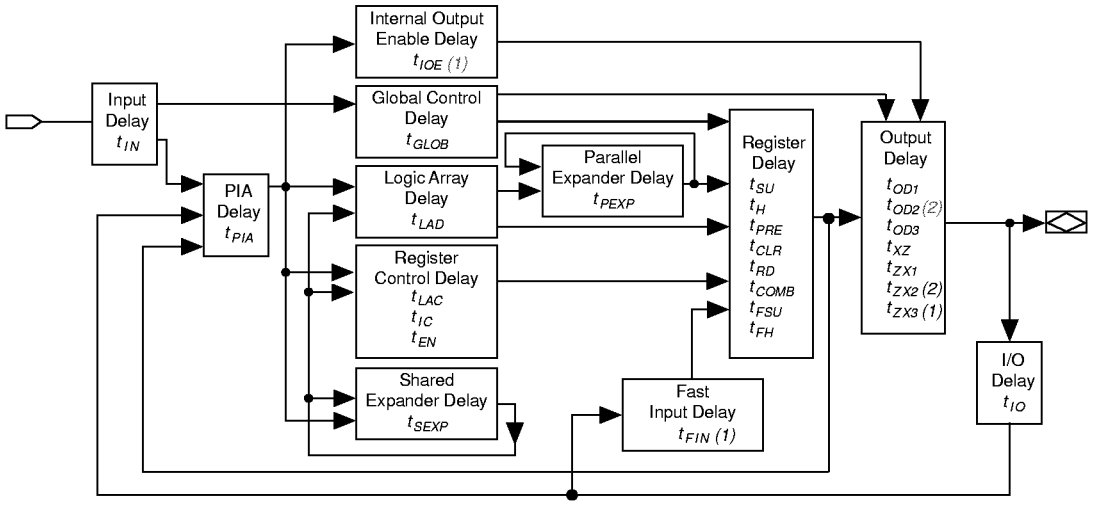
Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



Timing Model

MAX 7000 device timing can be analyzed with the Quartus or MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 12. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Quartus and MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Figure 12. MAX 7000 Timing Model



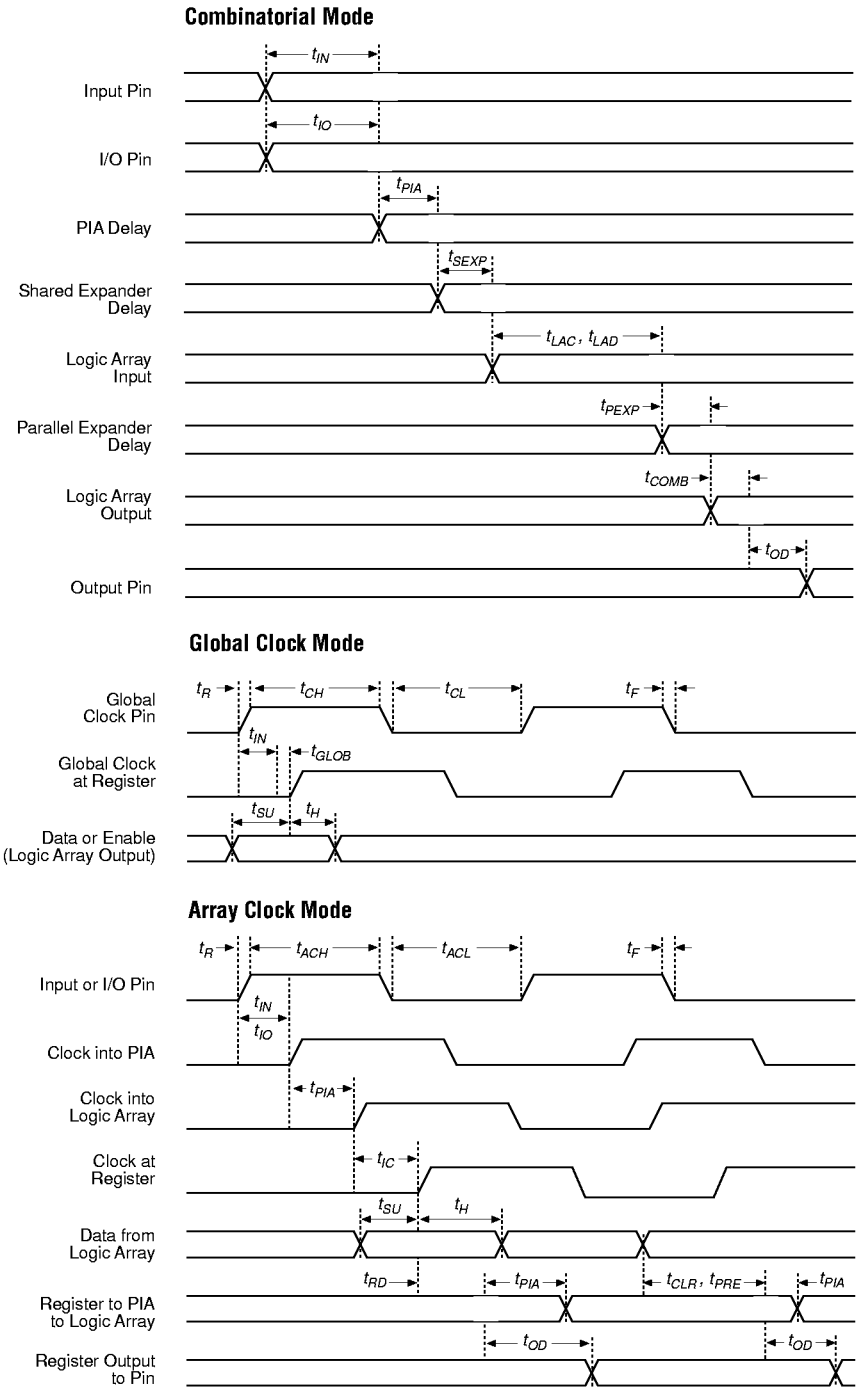
Notes:
(1) Only available in MAX 7000E and MAX 7000S devices.
(2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Figure 13. Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 16 through 23 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 16. MAX 7000 & MAX 7000E External Timing Parameters Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-6		-7		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_{H}	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	*(6)*	200		166.7		MHz

Table 17. MAX 7000 & MAX 7000E Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade				Unit
			-6		-7		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.5	ns
t_{FIN}	Fast input delay	*(2)*		0.8		1.0	ns
t_{SEXP}	Shared expander delay			3.5		4.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			2.0		3.0	ns
t_{LAC}	Logic control array delay			2.0		3.0	ns
t_{IOE}	Internal output enable delay	*(2)*				2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		2.0		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		7.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0	ns
t_{SU}	Register setup time		3.0		3.0		ns
t_{H}	Register hold time		1.5		2.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	2.5		3.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.5		0.5		ns
t_{RD}	Register delay			0.8		1.0	ns
t_{COMB}	Combinatorial delay			0.8		1.0	ns
t_{IC}	Array clock delay			2.5		3.0	ns
t_{EN}	Register enable time			2.0		3.0	ns
t_{GLOB}	Global control delay			0.8		1.0	ns
t_{PRE}	Register preset time			2.0		2.0	ns
t_{CLR}	Register clear time			2.0		2.0	ns
t_{PIA}	PIA delay			0.8		1.0	ns
t_{LPA}	Low-power adder	*(8)*		10.0		10.0	ns

Table 18. MAX 7000 & MAX 7000E External Timing Parameters

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t_{SU}	Global clock setup time		7.0		8.0		ns
t_{H}	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t_{CH}	Global clock high time		4.0		4.0		ns
t_{CL}	Global clock low time		4.0		4.0		ns
t_{ASU}	Array clock setup time		2.0		3.0		ns
t_{AH}	Array clock hold time		3.0		3.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t_{ACH}	Array clock high time		4.0		4.0		ns
t_{ACL}	Array clock low time		4.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	4.0		4.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		ns
t_{CNT}	Minimum global clock period			10.0		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	100.0		100.0		MHz
t_{ACNT}	Minimum array clock period			10.0		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	100.0		100.0		MHz
f_{MAX}	Maximum clock frequency	*(6)*	125.0		125.0		MHz

Table 19. MAX 7000 & MAX 7000E Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.5		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.5		1.0	ns
t_{FIN}	Fast input delay	*(2)*		1.0		1.0	ns
t_{SEXP}	Shared expander delay			5.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	*(2)*		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		1.5		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.0		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		5.5		6.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		5.0	ns
t_{SU}	Register setup time		2.0		3.0		ns
t_{H}	Register hold time		3.0		3.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.5		0.5		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			5.0		5.0	ns
t_{GLOB}	Global control delay			1.0		1.0	ns
t_{PRE}	Register preset time			3.0		3.0	ns
t_{CLR}	Register clear time			3.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	*(8)*		11.0		11.0	ns

Table 20. MAX 7000 & MAX 7000E External Timing Parameters

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t_{SU}	Global clock setup time		7.0		10.0		ns
t_{H}	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t_{CH}	Global clock high time		4.0		4.0		ns
t_{CL}	Global clock low time		4.0		4.0		ns
t_{ASU}	Array clock setup time		3.0		4.0		ns
t_{AH}	Array clock hold time		4.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t_{ACH}	Array clock high time		5.0		5.0		ns
t_{ACL}	Array clock low time		5.0		5.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	5.0		5.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		ns
t_{CNT}	Minimum global clock period			11.0		11.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	90.9		90.9		MHz
t_{ACNT}	Minimum array clock period			11.0		11.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	90.9		90.9		MHz
f_{MAX}	Maximum clock frequency	*(6)*	125.0		125.0		MHz

Table 21. MAX 7000 & MAX 7000E Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t_{FIN}	Fast input delay	*(2)*		1.0		1.0	ns
t_{SEXP}	Shared expander delay			7.0		7.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0	ns
t_{LAD}	Logic array delay			7.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	*(2)*		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		1.0		3.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.0		4.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		5.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		7.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0	ns
t_{SU}	Register setup time		1.0		4.0		ns
t_{H}	Register hold time		6.0		4.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	4.0		2.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.0		2.0		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			7.0		5.0	ns
t_{GLOB}	Global control delay			2.0		0.0	ns
t_{PRE}	Register preset time			4.0		3.0	ns
t_{CLR}	Register clear time			4.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	*(8)*		12.0		12.0	ns

Table 22. MAX 7000 & MAX 7000E External Timing Parameters

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{SU}	Global clock setup time		11.0		11.0		12.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		–		5.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.0		–		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t_{CH}	Global clock high time		5.0		6.0		6.0		ns
t_{CL}	Global clock low time		5.0		6.0		6.0		ns
t_{ASU}	Array clock setup time		4.0		4.0		5.0		ns
t_{AH}	Array clock hold time		4.0		4.0		5.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t_{ACH}	Array clock high time		6.0		6.5		8.0		ns
t_{ACL}	Array clock low time		6.0		6.5		8.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	6.0		6.5		8.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			13.0		13.0		16.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	76.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13.0		13.0		16.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	76.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*(6)*	100		83.3		83.3		MHz

Table 23. MAX 7000 & MAX 7000E Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	*(2)*		2.0		–		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	*(2)*		3.0		–		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.0		–		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		8.0		–		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		–		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		–		14.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_{H}	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	2.0		–		4.0		ns
t_{FH}	Register hold time of fast input	*(2)*	2.0		–		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	*(8)*		13.0		15.0		15.0	ns

Notes to tables:

(1) These values are specified in Table 11 on page 23.
(2) This parameter applies to MAX 7000E devices only.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(5) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 24 and 25 show the EPM7032S AC operating conditions.

Table 24. EPM7032S External Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time		2.9		4.0		5.0		7.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t_{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t_{ASU}	Array clock setup time		0.7		0.9		1.1		2.0		ns
t_{AH}	Array clock hold time		1.8		2.1		2.7		3.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t_{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t_{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	2.5		2.5		3.0		4.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	175.4		142.9		116.3		100.0		MHz
t_{ACNT}	Minimum array clock period			5.7		7.0		8.6		10.0	ns

Table 24. EPM7032S External Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(3)*	175.4		142.9		116.3		100.0		MHz
f_{MAX}	Maximum clock frequency	*(4)*	250.0		200.0		166.7		125.0		MHz

Table 25. EPM7032S Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		2.1		2.5		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.6		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		1.4		0.8	ns
t_{LAD}	Logic array delay			2.6		3.3		4.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.3		4.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		1.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		0.4		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		0.7		0.8		0.9		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		5.4		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		1.3		2.0		ns
t_{H}	Register hold time		1.7		2.0		2.5		3.0		ns
t_{FSU}	Register setup time of fast input		1.9		1.8		1.7		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.8		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.9		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.1		1.4		2.0	ns
t_{IC}	Array clock delay			2.7		3.4		4.2		5.0	ns
t_{EN}	Register enable time			2.6		3.3		4.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.4		1.7		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		3.0		3.0	ns

Table 25. EPM7032S Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLR}	Register clear time			2.0		2.4		3.0		3.0	ns
t_{PIA}	PIA delay	*(6)*		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	*(7)*		12.0		10.0		10.0		11.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The f_{MAX} values represent the highest frequency for pipelined data.

(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.

(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 26 and 27 show the EPM7064S AC operating conditions.

Table 26. EPM7064S External Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t_{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t_{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t_{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 26. EPM7064S External Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t_{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t_{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	2.5		2.5		3.0		4.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	175.4		140.8		125.0		100.0		MHz
t_{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	175.4		140.8		125.0		100.0		MHz
f_{MAX}	Maximum clock frequency	*(4)*	250.0		200.0		166.7		125.0		MHz

Table 27. EPM7064S Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns

Table 27. EPM7064S Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_H	Register hold time		1.7		2.0		2.0		3.0		ns
t_{FSU}	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.0		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.0		1.0		2.0	ns
t_{IC}	Array clock delay			2.7		3.3		3.0		5.0	ns
t_{EN}	Register enable time			2.6		3.2		3.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.9		1.0		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		2.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		2.0		3.0	ns
t_{PIA}	PIA delay	*(6)*		1.1		1.3		1.0		1.0	ns
t_{LPA}	Low-power adder	*(7)*		12.0		11.0		10.0		11.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.

(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 28 and 29 show the EPM7128S AC operating conditions.

Table 28. EPM7128S External Timing Parameters

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t_{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	3.0		3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	147.1		125.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	147.1		125.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(4)*	166.7		166.7		125.0		100.0		MHz

Table 29. EPM7128S Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		1.0		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.7		4.0		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.1		0.8		0.8		1.0	ns
t_{LAD}	Logic array delay			3.0		3.0		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.0		3.0		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		2.0		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		2.0		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		0.9		2.5		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		7.0		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		3.0		2.0		4.0		ns
t_{H}	Register hold time		1.7		2.0		5.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		3.0		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.5		0.5		1.0		ns
t_{RD}	Register delay			1.4		1.0		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		2.0		1.0	ns
t_{IC}	Array clock delay			3.1		3.0		5.0		6.0	ns
t_{EN}	Register enable time			3.0		3.0		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		1.0		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		2.0		3.0		4.0	ns
t_{CLR}	Register clear time			2.4		2.0		3.0		4.0	ns
t_{PIA}	PIA delay	*(6)*		1.4		1.0		1.0		2.0	ns
t_{LPA}	Low-power adder	*(7)*		11.0		10.0		11.0		13.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The f_{MAX} values represent the highest frequency for pipelined data.
(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 30 and 31 show the EPM7160S AC operating conditions.

Table 30. EPM7160S External Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		3.4		4.2		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.9		4.8		5		8	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.9		1.1		2.0		4.0		ns
t_{AH}	Array clock hold time		1.7		2.1		3.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.4		7.9		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	2.5		3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.7		8.2		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	149.3		122.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			6.7		8.2		10.0		13.0	ns

Table 30. EPM7160S External Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(3)*	149.3		122.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(4)*	166.7		166.7		125.0		100.0		MHz

Table 31. EPM7160S Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.6		4.3		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.3		0.8		1.0	ns
t_{LAD}	Logic array delay			2.8		3.4		5.0		6.0	ns
t_{LAC}	Logic control array delay			2.8		3.4		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		0.9		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		1.2		2.0		4.0		ns
t_{H}	Register hold time		1.6		2.0		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
t_{RD}	Register delay			1.3		1.6		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.3		2.0		1.0	ns
t_{IC}	Array clock delay			2.9		3.5		5.0		6.0	ns
t_{EN}	Register enable time			2.8		3.4		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		2.4		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		3.0		3.0		4.0	ns

Table 31. EPM7160S Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLR}	Register clear time			2.4		3.0		3.0		4.0	ns
t_{PIA}	PIA delay	(6)		1.6		2.0		1.0		2.0	ns
t_{LPA}	Low-power adder	(7)		11.0		10.0		11.0		13.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The f_{MAX} values represent the highest frequency for pipelined data.
(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, t_{ACL}, and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 32 and 33 show the EPM7192S AC operating conditions.

Table 32. EPM7192S External Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		4.1		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		1.0		2.0		4.0		ns
t_{AH}	Array clock hold time		1.8		3.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns

Table 32. EPM7192S External Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{ACH}	Array clock high time		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			8.0		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	125.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			8.0		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	125.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(4)*	166.7		125.0		100.0		MHz

Table 33. EPM7192S Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			4.2		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.2		0.8		1.0	ns
t_{LAD}	Logic array delay			3.1		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.1		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		7.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.1		2.0		4.0		ns
t_{H}	Register hold time		1.7		3.0		4.0		ns

Table 33. EPM7192S Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{FSU}	Register setup time of fast input		2.3		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.7		0.5		1.0		ns
t_{RD}	Register delay			1.4		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.2		2.0		1.0	ns
t_{IC}	Array clock delay			3.2		5.0		6.0	ns
t_{EN}	Register enable time			3.1		5.0		6.0	ns
t_{GLOB}	Global control delay			2.5		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	*(6)*		2.4		1.0		2.0	ns
t_{LPA}	Low-power adder	*(7)*		10.0		11.0		13.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.

(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 34 and 35 show the EPM7256S AC operating conditions.

Table 34. EPM7256S External Timing Parameters

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF	7.5		10.0			15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF	7.5		10.0			15.0	ns
t_{SU}	Global clock setup time		3.9		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	4.7		5.0			8.0	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t_{AH}	Array clock hold time		1.9		3.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF	7.8		10.0			15.0	ns
t_{ACH}	Array clock high time		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(1)*	3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(2)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period		7.8		10.0			13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*	128.2		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period		7.8		10.0			13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	128.2		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(4)*	166.7		125.0		100.0		MHz

Table 35. EPM7256S Internal Timing Parameters

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			3.4		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.9		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.1		0.8		1.0	ns
t_{LAD}	Logic array delay			2.6		5.0		6.0	ns
t_{LAC}	Logic control array delay			2.6		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.8		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(5)*		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(5)*		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.1		2.0		4.0		ns
t_{H}	Register hold time		1.6		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		2.4		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.5		1.0		ns
t_{RD}	Register delay			1.1		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.1		2.0		1.0	ns
t_{IC}	Array clock delay			2.9		5.0		6.0	ns
t_{EN}	Register enable time			2.6		5.0		6.0	ns
t_{GLOB}	Global control delay			2.8		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	*(6)*		3.0		1.0		2.0	ns
t_{LPA}	Low-power adder	*(7)*		10.0		11.0		13.0	ns

Notes to tables:

(1) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(5) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(6) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$ in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}}$$

The parameters in this equation are shown below:

MC_{TON}	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (**.rpt**)
$\mathbf{f_{MAX}}$	=	Highest clock frequency to the device
$\mathbf{tog_{LC}}$	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in Table 36

Table 36. MAX 7000 I_{CC} Equation Constants

Device	A	B	C
EPM7032	1.87	0.52	0.144
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S	0.93	0.40	0.040
EPM7064S	0.93	0.40	0.040
EPM7128S	0.93	0.40	0.040
EPM7160S	0.93	0.40	0.040
EPM7192S	0.93	0.40	0.040
EPM7256S	0.93	0.40	0.040

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

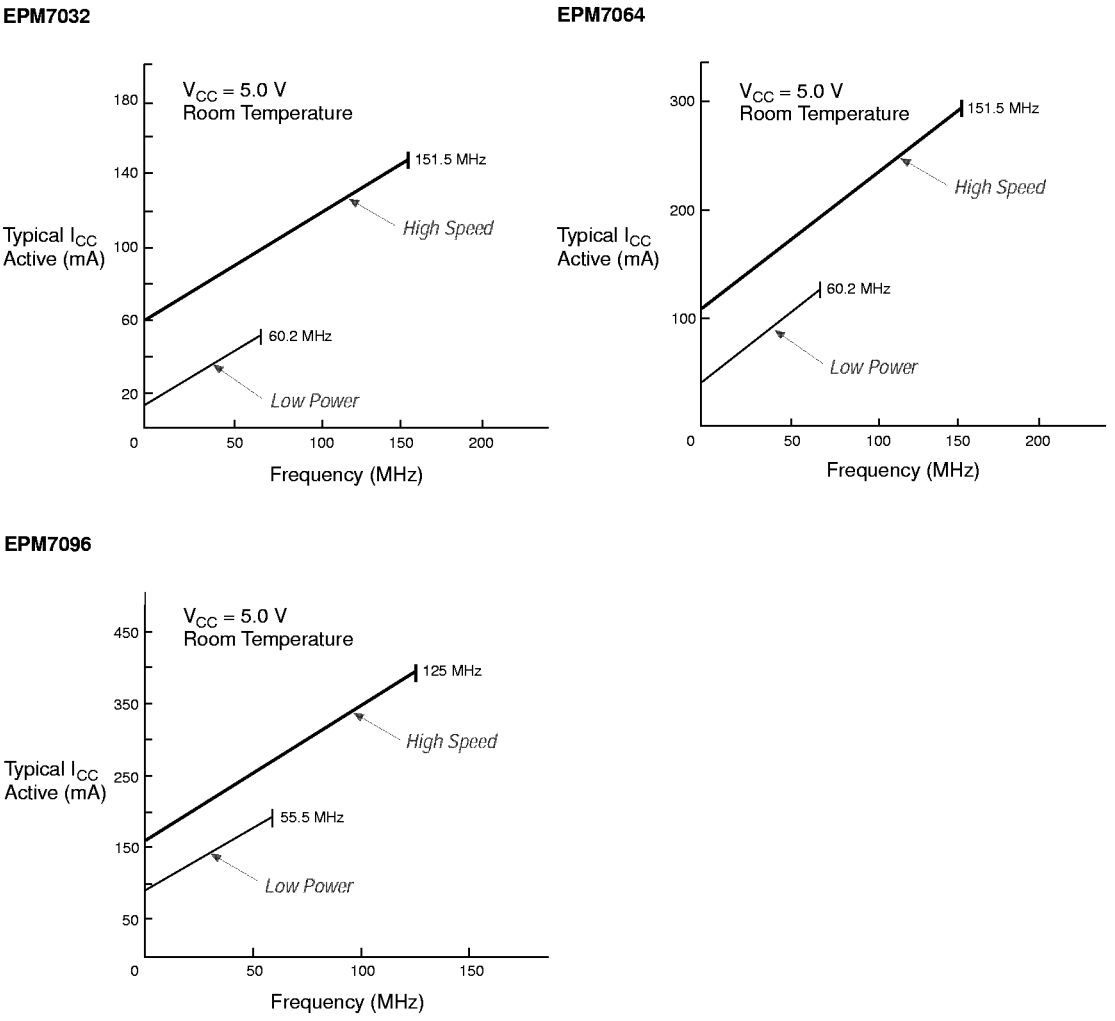
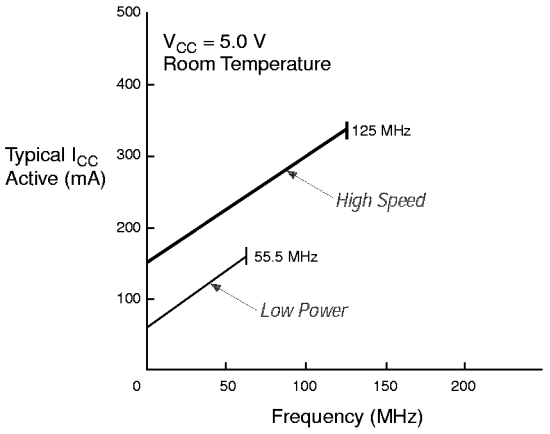
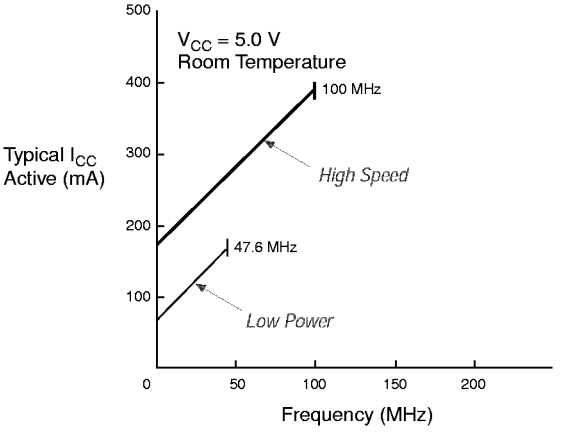


Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

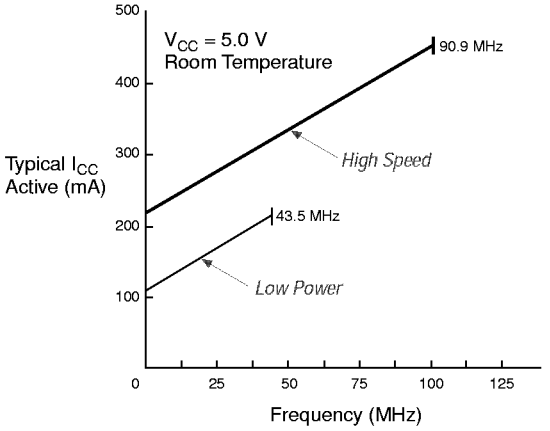
EPM7128E



EPM7160E



EPM7192E



EPM7256E

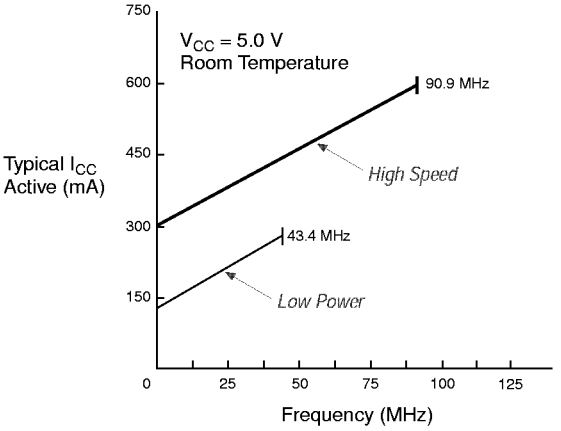


Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

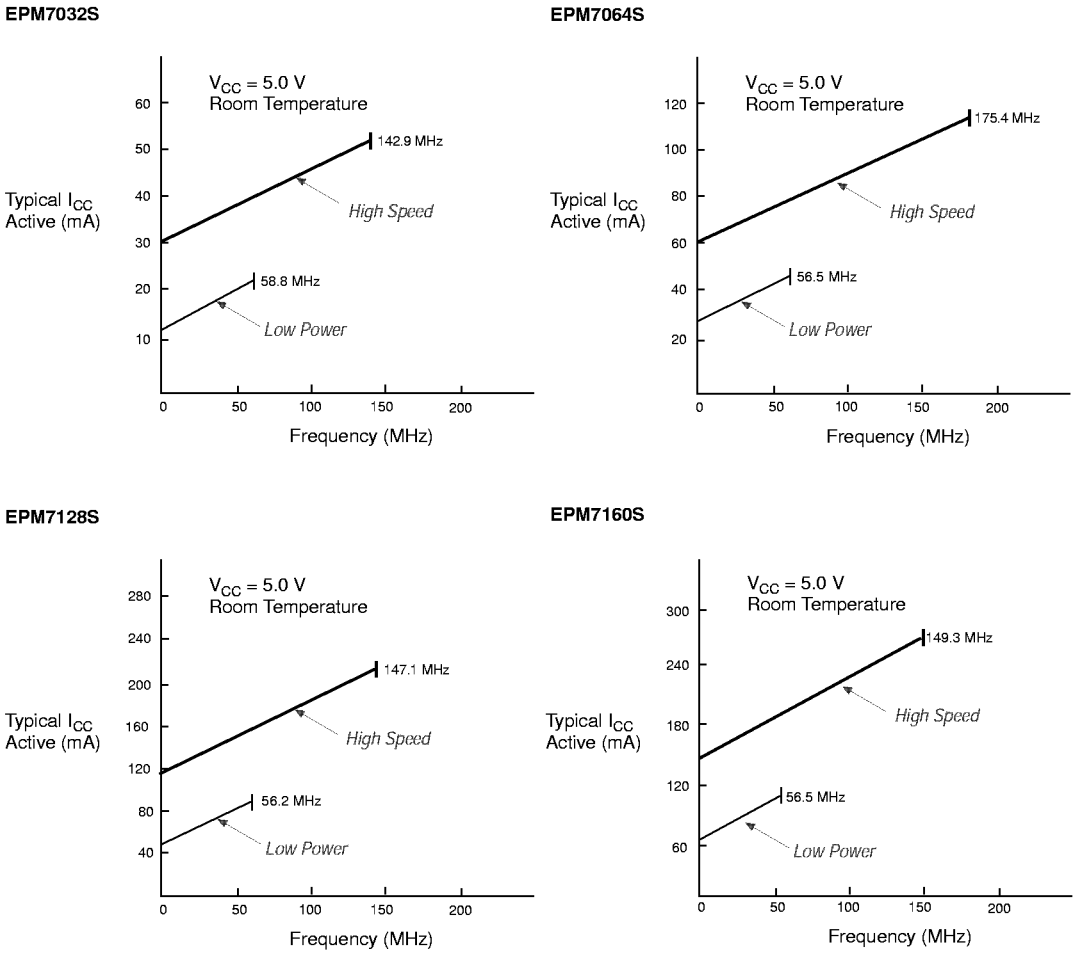
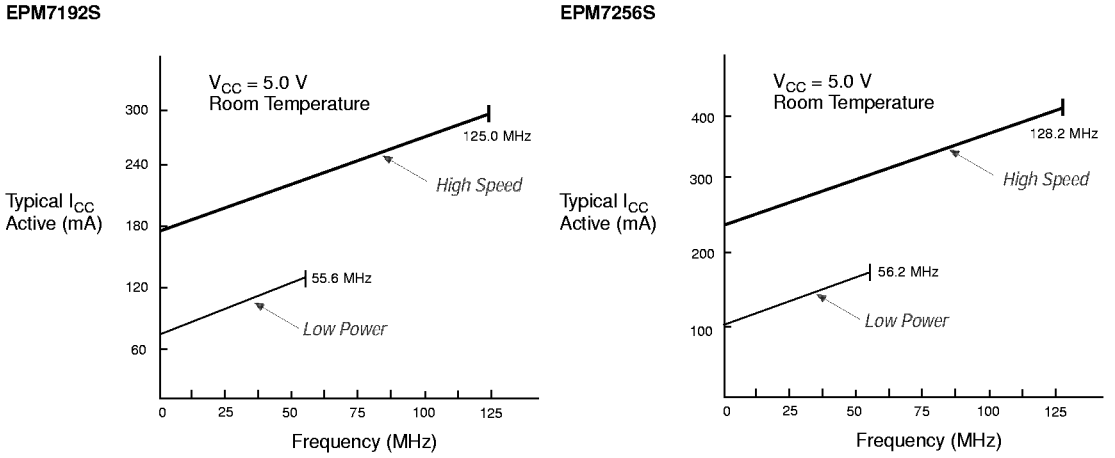


Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)



Device Pin-Outs

Tables 37 through 51 show the pin names and numbers for the pins in each MAX 7000 device package.

Table 37. EPM7032 & EPM7032S Dedicated Pin-Outs

Pin Name	44-Pin PLCC	44-Pin PQFP/TQFP *(1)*
INPUT/GCLK1	43	37
INPUT/GCLRn	1	39
INPUT/OE1	44	38
INPUT/OE2/GCLK2 *(2)*	2	40
TDI *(3)*	7	1
TMS *(3)*	13	7
TCK *(3)*	32	26
TDO *(3)*	38	32
PDn *(4)*	3	41
GND	10, 22, 30, 42	4, 16, 24, 36
VCC	3, 15, 23, 35	9, 17, 29, 41
No Connect (N.C.)	–	–
Total User I/O Pins *(5)*	36	36

Table 38. EPM7032 & EPM7032S I/O Pin-Outs

LAB	MC	44-Pin PLCC	44-Pin PQFP/TQFP *(1)*	LAB	MC	44-Pin PLCC	44-Pin PQFP/TQFP *(1)*
A	1	4	42	B	17	41	35
	2	5	43		18	40	34
	3	6	44		19	39	33
	4	7 *(3)*	1 *(3)*		20	38 *(3)*	32 *(3)*
	5	8	2		21	37	31
	6	9	3		22	36	30
	7	11	5		23	34	28
	8	12	6		24	33	27
	9	13 *(3)*	7 *(3)*		25	32 *(3)*	26 *(3)*
	10	14	8		26	31	25
	11	16	10		27	29	23
	12	17	11		28	28	22
	13	18	12		29	27	21
	14	19	13		30	26	20
	15	20	14		31	25	19
	16	21	15		32	24	18

Notes to tables:

(1) EPM7032S and EPM7032V devices are not available in the 44-pin PQFP package.
(2) The GCLK2 function is available in MAX 7000S and MAX 7000E devices only.
(3) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.
(4) The PDn pin is available in EPM7032V devices only.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 39. EPM7064 & EPM7064S Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	68-Pin PLCC *(1)*	84-Pin PLCC	100-Pin TQFP *(2)*	100-Pin PQFP *(1)*
INPUT/GCLK1	43	37	67	83	87	89
INPUT/GCLRn	1	39	1	1	89	91
INPUT/OE1	44	38	68	84	88	90
INPUT/OE2/GCLK2 *(3)*	2	40	2	2	90	92
TDI *(4)*	7	1	12	14	4	6
TMS *(4)*	13	7	19	23	15	17
TCK *(4)*	32	26	50	62	62	64
TDO *(4)*	38	32	57	71	73	75
GND	10, 22, 30, 42	4, 16, 24, 36	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	38, 86, 11, 26, 43, 59, 74, 95	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V only)	3, 15, 23, 35	9, 17, 29, 41	3, 35	3, 43	39, 91	41, 93
VCCIO (3.3 V or 5.0 V)	–	–	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	–	–	–	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80
Total User I/O Pins *(5)*	32	32	48	64	64	64

Table 40. EPM7064 & EPM7064S I/O Pin-Outs (44-Pin PLCC, 44-Pin TQFP & 68-Pin PLCC Packages)

LAB	MC	44-Pin PLCC	44-Pin TQFP	68-Pin PLCC *(1)*	LAB	MC	44-Pin PLCC	44-Pin TQFP	68-Pin PLCC *(1)*
A	1	12	6	18	C	33	24	18	36
	2	–	–	–		34	–	–	–
	3	11	5	17		35	25	19	37
	4	9	3	15		36	26	20	39
	5	8	2	14		37	27	21	40
	6	–	–	13		38	–	–	41
	7	–	–	–		39	–	–	–
	8	7 *(4)*	1 *(4)*	12 *(4)*		40	28	22	42
	9	–	–	10		41	29	23	44
	10	–	–	–		42	–	–	–
	11	6	44	9		43	–	–	45
	12	–	–	8		44	–	–	46
	13	–	–	7		45	–	–	47
	14	5	43	5		46	31	25	49
	15	–	–	–		47	–	–	–
	16	4	42	4		48	32 *(4)*	26 *(4)*	50 *(4)*
B	17	21	15	33	D	49	33	27	51
	18	–	–	–		50	–	–	–
	19	20	14	32		51	34	28	52
	20	19	13	30		52	36	30	54
	21	18	12	29		53	37	31	55
	22	–	–	28		54	–	–	56
	23	–	–	–		55	–	–	–
	24	17	11	27		56	38 *(4)*	32 *(4)*	57 *(4)*
	25	16	10	25		57	39	33	59
	26	–	–	–		58	–	–	–
	27	–	–	24		59	–	–	60
	28	–	–	23		60	–	–	61
	29	–	–	22		61	–	–	62
	30	14	8	20		62	40	34	64
	31	–	–	–		63	–	–	–
	32	13 *(4)*	7 *(4)*	19 *(4)*		64	41	35	65

Table 41. EPM7064 & EPM7064S I/O Pin-Outs (84-Pin PLCC, 100-Pin TQFP & 100-Pin PQFP Packages)

LAB	MC	84-Pin PLCC	100-Pin TQFP *(2)*	100-Pin PQFP *(1)*	LAB	MC	84-Pin PLCC	100-Pin TQFP *(2)*	100-Pin PQFP *(1)*
A	1	22	14	16	C	33	44	40	42
	2	21	13	15		34	45	41	43
	3	20	12	14		35	46	42	44
	4	18	10	12		36	48	44	46
	5	17	9	11		37	49	45	47
	6	16	8	10		38	50	46	48
	7	15	6	8		39	51	47	49
	8	14 *(4)*	4 *(4)*	6 *(4)*		40	52	48	50
	9	12	100	4		41	54	52	54
	10	11	99	3		42	55	54	56
	11	10	98	100		43	56	56	58
	12	9	97	99		44	57	57	59
	13	8	96	98		45	58	58	60
	14	6	94	96		46	60	60	62
	15	5	93	95		47	61	61	63
	16	4	92	94		48	62 *(4)*	62 *(4)*	64 *(4)*
B	17	41	37	39	D	49	63	63	65
	18	40	36	38		50	64	64	66
	19	39	35	37		51	65	65	67
	20	37	33	35		52	67	67	69
	21	36	32	34		53	68	68	70
	22	35	31	33		54	69	69	71
	23	34	30	32		55	70	71	73
	24	33	29	31		56	71 *(4)*	73 *(4)*	75 *(4)*
	25	31	25	27		57	73	75	77
	26	30	23	25		58	74	76	78
	27	29	21	23		59	75	79	81
	28	28	20	22		60	76	80	82
	29	27	19	21		61	77	81	83
	30	25	17	19		62	79	83	85
	31	24	16	18		63	80	84	86
	32	23 *(4)*	15 *(4)*	17 *(4)*		64	81	85	87

Notes to tables:
(1) EPM7064S devices are not available in the 100-pin PQFP package or 68-pin PLCC packages.
(2) EPM7064 devices are not available in the 100-pin TQFP package.
(3) The GCLK2 function is available in MAX 7000S and MAX 7000E devices only.
(4) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 42. EPM7096 Dedicated Pin-Outs

Dedicated Pin	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP
INPUT/GCLK1	67	83	89
INPUT/GCLRn	1	1	91
INPUT/OE1	68	84	90
INPUT/OE2	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V Only)	3, 35	3, 43	41, 93
VCCIO (3.3 V or 5.0 V)	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96
Total User I/O Pins *(1)*	48	60	72

Note:
(1) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 43. EPM7096 I/O Pin-Outs (Part 1 of 2)

LAB	MC	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	LAB	MC	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP
A	1	13	16	8	B	17	23	28	23
	2	–	–	–		18	–	–	–
	3	–	15	7		19	22	27	22
	4	12	14	6		20	–	–	21
	5	–	–	4		21	20	25	19
	6	10	12	3		22	–	24	18
	7	–	–	–		23	–	–	–
	8	9	11	2		24	19	23	17
	9	8	10	1		25	18	22	16
	10	–	–	–		26	–	–	–
	11	–	9	100		27	17	21	15
	12	7	8	99		28	–	20	14
	13	–	–	98		29	15	18	12
	14	5	5	95		30	–	–	11
	15	–	–	–		31	–	–	–
	16	4	4	94		32	14	17	10

Table 43. EPM7096 I/O Pin-Outs (Part 2 of 2)

LAB	MC	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	LAB	MC	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP
C	33	33	41	39	E	65	46	57	58
	34	–	–	–		66	–	–	–
	35	32	40	38		67	47	58	59
	36	–	–	35		68	–	–	60
	37	30	37	34		69	49	60	62
	38	–	36	33		70	–	61	63
	39	–	–	–		71	–	–	–
	40	29	35	32		72	50	62	64
	41	28	34	31		73	51	63	65
	42	–	–	–		74	–	–	–
	43	27	33	30		75	52	64	66
	44	–	–	29		76	–	65	67
	45	25	31	27		77	54	67	69
	46	–	30	26		78	–	–	70
	47	–	–	–		79	–	–	–
	48	24	29	25		80	55	68	71
D	49	36	44	42	F	81	56	69	73
	50	–	–	–		82	–	–	–
	51	37	45	43		83	–	70	74
	52	–	–	46		84	57	71	75
	53	39	48	47		85	–	–	77
	54	–	49	48		86	59	73	78
	55	–	–	–		87	–	–	–
	56	40	50	49		88	60	74	79
	57	41	51	50		89	61	75	80
	58	–	–	–		90	–	–	–
	59	42	52	51		91	–	76	81
	60	–	–	52		92	62	77	82
	61	44	54	54		93	–	–	83
	62	–	55	55		94	64	80	86
	63	–	–	–		95	–	–	–
	64	45	56	56		96	65	81	87

Table 44. EPM7128E & EPM7128S Dedicated Pin-Outs

Dedicated Pin	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP *(1), (2)*	160-Pin PQFP
INPUT/GCLK1	83	89	87	139
INPUT/GCLRn	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/OE2/GCLK2	2	92	90	142
TDI *(3)*	14	6	4	9
TMS *(3)*	23	17	15	22
TCK *(3)*	62	64	62	99
TDO *(3)*	71	75	73	112
GNDINT	42, 82	40, 88	38, 86	60, 138
GNDIO	7, 19, 32,47, 59, 72	13, 28, 45, 61, 76, 97	11, 26, 43, 59, 74, 95	17, 42, 66, 95, 113, 148
VCCINT (5.0 V only)	3, 43	41, 93	39, 91	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	3, 18, 34, 51, 66, 82	8, 26, 55, 79, 104, 133
No Connect (N.C.)	–	–	–	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins *(4)*	64	80	80	96

Table 45. EPM7128E & EPM7128S I/O Pin-Outs (Part 1 of 2)

LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP *(1), (2)*	160-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP *(1), (2)*	160-Pin PQFP
A	1	–	4	2	160	C	33	–	27	25	41
	2	–	–	–	–		34	–	–	–	–
	3	12	3	1	159		35	31	26	24	33
	4	–	–	–	158		36	–	–	–	32
	5	11	2	100	153		37	30	25	23	31
	6	10	1	99	152		38	29	24	22	30
	7	–	–	–	–		39	–	–	–	–
	8	9	100	98	151		40	28	23	21	29
	9	–	99	97	150		41	–	22	20	28
	10	–	–	–	–		42	–	–	–	–
	11	8	98	96	149		43	27	21	19	27
	12	–	–	–	147		44	–	–	–	25
	13	6	96	94	146		45	25	19	17	24
	14	5	95	93	145		46	24	18	16	23
	15	–	–	–	–		47	–	–	–	–
	16	4	94	92	144		48	23 *(3)*	17 *(3)*	15 *(3)*	22 *(3)*
B	17	22	16	14	21	D	49	41	39	37	59
	18	–	–	–	–		50	–	–	–	–
	19	21	15	13	20		51	40	38	36	58
	20	–	–	–	19		52	–	–	–	57
	21	20	14	12	18		53	39	37	35	56
	22	–	12	10	16		54	–	35	33	54
	23	–	–	–	–		55	–	–	–	–
	24	18	11	9	15		56	37	34	32	53
	25	17	10	8	14		57	36	33	31	52
	26	–	–	–	–		58	–	–	–	–
	27	16	9	7	13		59	35	32	30	51
	28	–	–	–	12		60	–	–	–	50
	29	15	8	6	11		61	34	31	29	49
	30	–	7	5	10		62	–	30	28	48
	31	–	–	–	–		63	–	–	–	–
	32	14 *(3)*	6 *(3)*	4 *(3)*	9 *(3)*		64	33	29	27	43

Table 45. EPM7128E & EPM7128S I/O Pin-Outs (Part 2 of 2)

LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP *(1), (2)*	160-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP *(1), (2)*	160-Pin PQFP
E	65	44	42	40	62	G	97	63	65	63	100
	66	–	–	–	–		98	–	–	–	–
	67	45	43	41	63		99	64	66	64	101
	68	–	–	–	64		100	–	–	–	102
	69	46	44	42	65		101	65	67	65	103
	70	–	46	44	67		102	–	69	67	105
	71	–	–	–	–		103	–	–	–	–
	72	48	47	45	68		104	67	70	68	106
	73	49	48	46	69		105	68	71	69	107
	74	–	–	–	–		106	–	–	–	–
	75	50	49	47	70		107	69	72	70	108
	76	–	–	–	71		108	–	–	–	109
	77	51	50	48	72		109	70	73	71	110
	78	–	51	49	73		110	–	74	72	111
	79	–	–	–	–		111	–	–	–	–
	80	52	52	50	78		112	71 *(3)*	75 *(3)*	73 *(3)*	112 *(3)*
F	81	–	54	52	80	H	113	–	77	75	121
	82	–	–	–	–		114	–	–	–	–
	83	54	55	53	88		115	73	78	76	122
	84	–	–	–	89		116	–	–	–	123
	85	55	56	54	90		117	74	79	77	128
	86	56	57	55	91		118	75	80	78	129
	87	–	–	–	–		119	–	–	–	–
	88	57	58	56	92		120	76	81	79	130
	89	–	59	57	93		121	–	82	80	131
	90	–	–	–	–		122	–	–	–	–
	91	58	60	58	94		123	77	83	81	132
	92	–	–	–	96		124	–	–	–	134
	93	60	62	60	97		125	79	85	83	135
	94	61	63	61	98		126	80	86	84	136
	95	–	–	–	–		127	–	–	–	–
	96	62 *(3)*	64 *(3)*	62 *(3)*	99 *(3)*		128	81	87	85	137

Notes to tables:

(1) A complete thermal analysis should be performed before committing a design to this device package.
(2) EPM7128E devices are not available in the 100-pin TQFP package.
(3) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or for ISP, this pin is not available as a user I/O pin.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 46. EPM7160E & EPM7160S Dedicated Pin-Outs

Dedicated Pin	84-Pin PLCC	100-Pin TQFP *(1), (2)*	100-Pin PQFP *(3)*	160-Pin PQFP
INPUT/GCLK1	83	87	89	139
INPUT/GCLRn	1	89	91	141
INPUT/OE1	84	88	90	140
INPUT/OE2/GCLK2	2	90	92	142
TDI *(4)*	14	4	6	9
TMS *(4)*	23	15	17	22
TCK *(4)*	62	62	64	99
TDO *(4)*	71	73	75	112
GND	7, 19, 32, 42, 47, 59, 72, 82	38, 86, 11, 26, 43, 59, 74, 95	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	39,91	41, 93	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	5, 20, 36, 53, 68, 84	8, 26, 55, 79, 104, 133
No Connect (N.C.)	6, 39, 46, 79	–	–	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins *(5)*	60	80	80	100

Table 47. EPM7160E & EPM7160S I/O Pin-Outs (Part 1 of 3)

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
A	1	11	100	2	158	C	33	–	19	21	27
	2	–	–	–	–		34	–	–	–	–
	3	10	99	1	153		35	25	17	19	25
	4	–	–	–	–		36	–	–	–	–
	5	–	–	–	152		37	–	–	–	24
	6	–	98	100	151		38	24	16	18	23
	7	–	–	–	–		39	–	–	–	–
	8	9	97	99	150		40	23 (4)	15 (4)	17 (4)	22 (4)
	9	8	96	98	149		41	–	10	12	16
	10	–	–	–	–		42	–	–	–	–
	11	5	94	96	147		43	20	12	14	18
	12	–	–	–	–		44	–	–	–	–
	13	–	–	–	146		45	–	–	–	19
	14	–	93	95	145		46	21	13	15	20
	15	–	–	–	–		47	–	–	–	–
	16	4	92	94	144		48	22	14	16	21
B	17	18	9	11	15	D	49	–	–	–	48
	18	–	–	–	–		50	–	–	–	–
	19	17	8	10	14		51	33	28	30	44
	20	–	–	–	–		52	–	–	–	–
	21	–	–	–	13		53	–	27	29	43
	22	–	7	9	12		54	31	25	27	41
	23	–	–	–	–		55	–	–	–	–
	24	16	6	8	11		56	30	24	26	33
	25	15	5	7	10		57	–	–	–	32
	26	–	–	–	–		58	–	–	–	–
	27	14 (4)	4 (4)	6 (4)	9 (4)		59	29	23	25	31
	28	–	–	–	–		60	–	–	–	–
	29	–	–	–	7		61	–	22	24	30
	30	–	2	4	160		62	28	21	23	29
	31	–	–	–	–		63	–	–	–	–
	32	12	1	3	159		64	27	20	22	28

Table 47. EPM7160E & EPM7160S I/O Pin-Outs (Part 2 of 3)

LAB	MC	84-Pin PLCC	100-Pin TQFP *(1), (2)*	100-Pin PQFP *(3)*	160-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin TQFP *(1), (2)*	100-Pin PQFP *(3)*	160-Pin PQFP
E	65	–	–	–	59	G	97	–	–	–	73
	66	–	–	–	–		98	–	–	–	–
	67	41	37	39	58		99	52	49	51	77
	68	–	–	–	–		100	–	–	–	–
	69	–	36	38	57		101	–	50	52	78
	70	40	35	37	56		102	54	52	54	80
	71	–	–	–	–		103	–	–	–	–
	72	37	33	35	54		104	55	53	55	88
	73	–	–	–	53		105	–	–	–	89
	74	–	–	–	–		106	–	–	–	–
	75	36	32	34	52		107	56	54	56	90
	76	–	–	–	–		108	–	–	–	–
	77	–	31	33	51		109	–	55	57	91
	78	35	30	32	50		110	57	56	58	92
	79	–	–	–	–		111	–	–	–	–
	80	34	29	31	49		112	58	57	59	93
F	81	–	–	–	62	H	113	–	58	60	94
	82	–	–	–	–		114	–	–	–	–
	83	44	40	42	63		115	60	60	62	96
	84	–	–	–	–		116	–	–	–	–
	85	–	41	43	64		117	–	–	–	97
	86	45	42	44	65		118	61	61	63	98
	87	–	–	–	–		119	–	–	–	–
	88	48	44	46	67		120	62 *(4)*	62 *(4)*	64 *(4)*	99 *(4)*
	89	–	–	–	68		121	–	67	69	105
	90	–	–	–	–		122	–	–	–	–
	91	49	45	47	69		123	65	65	67	103
	92	–	–	–	–		124	–	–	–	–
	93	–	46	48	70		125	–	–	–	102
	94	50	47	49	71		126	64	64	66	101
	95	–	–	–	–		127	–	–	–	–
	96	51	48	50	72		128	63	63	65	100

Table 47. EPM7160E & EPM7160S I/O Pin-Outs (Part 3 of 3)

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
I	129	67	68	70	106	J	145	74	77	79	123
	130	–	–	–	–		146	–	–	–	–
	131	68	69	71	107		147	75	78	80	128
	132	–	–	–	–		148	–	–	–	–
	133	–	–	–	108		149	–	–	–	129
	134	–	70	72	109		150	–	79	81	130
	135	–	–	–	–		151	–	–	–	–
	136	69	71	73	110		152	76	80	82	131
	137	70	72	74	111		153	77	81	83	132
	138	–	–	–	–		154	–	–	–	–
	139	71 (4)	73 (4)	75 (4)	112 (4)		155	80	83	85	134
	140	–	–	–	–		156	–	–	–	–
	141	–	–	–	114		157	–	–	–	135
	142	–	75	77	121		158	–	84	86	136
	143	–	–	–	–		159	–	–	–	–
	144	73	76	78	122		160	81	85	87	137

Notes to tables:

(1) EPM7160E devices are not available in the 100-pin TQFP package.
(2) A complete thermal analysis should be performed before committing a design to this device package.
(3) EPM7160S devices are not available in the 100-pin PQFP package.
(4) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or with ISP, this pin is not available as a user I/O pin.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 48. EPM7192E & EPM7192S Dedicated Pin-Outs

Dedicated Pin	160-Pin PGA *(1)*	160-Pin PQFP
INPUT/GCLK1	M8	139
INPUT/GCLRn	N8	141
INPUT/OE1	P8	140
INPUT/OE2/GCLK2	R8	142
TDI *(2)*	P9	146
TMS *(2)*	G15	23
TCK *(2)*	G2	98
TDO *(2)*	R7	135
GND	C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148
VCCINT (5.0 V Only)	C7, C9, N7, N9	56, 65, 137, 144
VCCIO (3.3 V or 5.0 V)	C5, C10, C12, D3, G12, H4, J12, M3, N5, N12	10, 25, 40, 55, 74, 89, 103, 118, 133, 155
No Connect (N.C.)	A1, A2, A14, A15, R1, R2, R14, R15	1, 11, 39,54, 67, 82, 110, 120
Total User I/O Pins *(3)*	120	120

Table 49. EPM7192E & EPM7192S I/O Pin-Outs (Part 1 of 3)

LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP
A	1	M12	156	B	17	L14	8	C	33	H14	21
	2	–	–		18	–	–		34	–	–
	3	P11	154		19	M14	7		35	J13	20
	4	–	–		20	–	–		36	–	–
	5	P12	153		21	M15	6		37	H15	19
	6	P10	152		22	N14	5		38	J15	17
	7	–	–		23	–	–		39	–	–
	8	R12	151		24	N15	4		40	J14	16
	9	N10	150		25	P15	2		41	K15	15
	10	–	–		26	–	–		42	–	–
	11	R11	149		27	N13	160		43	K13	14
	12	–	–		28	–	–		44	–	–
	13	R10	147		29	P14	159		45	L15	13
	14	P9 *(2)*	146 *(2)*		30	P13	158		46	K14	12
	15	–	–		31	–	–		47	–	–
	16	R9	145		32	R13	157		48	L13	9

Table 49. EPM7192E & EPM7192S I/O Pin-Outs (Part 2 of 3)

LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP
D	49	D15	33	F	81	D8	60	H	113	A3	76
	50	–	–		82	–	–		114	–	–
	51	E15	31		83	A9	59		115	B4	77
	52	–	–		84	–	–		116	–	–
	53	E14	30		85	C8	58		117	B3	78
	54	F15	29		86	B9	53		118	C3	79
	55	–	–		87	–	–		119	–	–
	56	F13	28		88	A10	52		120	B2	80
	57	G14	27		89	B10	51		121	B1	83
	58	–	–		90	–	–		122	–	–
	59	F14	26		91	A11	50		123	C2	84
	60	–	–		92	–	–		124	–	–
	61	G13	24		93	B11	49		125	C1	85
	62	G15 *(2)*	23 *(2)*		94	A12	48		126	D2	86
	63	–	–		95	–	–		127	–	–
	64	H13	22		96	A13	46		128	D1	87
E	65	B12	45	G	97	A8	61	I	129	E3	88
	66	–	–		98	–	–		130	–	–
	67	B13	44		99	B8	62		131	F3	90
	68	–	–		100	–	–		132	–	–
	69	C13	43		101	A7	63		133	E2	91
	70	B14	42		102	A6	68		134	F2	92
	71	–	–		103	–	–		135	–	–
	72	C14	41		104	B7	69		136	E1	93
	73	D12	38		105	A5	70		137	G3	94
	74	–	–		106	–	–		138	–	–
	75	B15	37		107	B6	71		139	F1	95
	76	–	–		108	–	–		140	–	–
	77	D14	36		109	A4	72		141	G1	97
	78	C15	35		110	B5	73		142	G2 *(2)*	98 *(2)*
	79	–	–		111	–	–		143	–	–
	80	E13	34		112	D4	75		144	H1	99

Table 49. EPM7192E & EPM7192S I/O Pin-Outs (Part 3 of 3)

LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP	LAB	MC	160-Pin PGA *(1)*	160-Pin PQFP
J	145	H2	100	K	161	L2	113	L	177	R3	125
	146	–	–		162	–	–		178	–	–
	147	J1	101		163	N1	114		179	R4	127
	148	–	–		164	–	–		180	–	–
	149	H3	102		165	L3	115		181	M4	128
	150	J3	104		166	P1	116		182	R5	129
	151	–	–		167	–	–		183	–	–
	152	K1	105		168	M2	117		184	P5	130
	153	J2	106		169	N2	119		185	R6	131
	154	–	–		170	–	–		186	–	–
	155	K2	107		171	P2	121		187	P6	132
	156	–	–		172	–	–		188	–	–
	157	K3	108		173	N3	122		189	N6	134
	158	L1	109		174	P3	123		190	R7 *(2)*	135 *(2)*
	159	–	–		175	–	–		191	–	–
	160	M1	112		176	P4	124		192	P7	136

Notes to tables:

(1) EPM7192S devices are not available in the 160-pin PGA package.

(2) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 50. EPM7256E & EPM7256S Dedicated Pin-Outs

Dedicated Pin	160-Pin PQFP *(1)*, *(2)*	192-Pin PGA *(2)*	208-Pin RQFP/PQFP *(3)*
INPUT/GCLK1	139	P9	184
INPUT/GCLRn	141	R9	182
INPUT/OE1	140	T9	183
INPUT/OE2/GCLK2	142	U9	181
TDI *(4)*	146	U10	176
TMS *(4)*	23	H15	127
TCK *(4)*	98	H3	30
TDO *(4)*	135	U8	189
GND	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCCINT (5.0 V only)	56, 65, 137, 144	D7, D11, P7, P11	74, 83, 179, 186
VCCIO (3.3 V or 5.0 V)	10, 25, 40, 55, 74, 89, 103, 118, 133, 155	C5, C11, D14, G4, H14, K4, L14, P3, R5, R14	5, 23, 41, 63, 85, 107, 125, 143, 165, 191
No Connect (N.C.)	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208.
Total User I/O Pins *(5)*	128	160	160

Table 51. EPM7256E & EPM7256S I/O Pin-Outs (Part 1 of 5)

LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP	LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP (3)
A	1	2	U17	153	C	33	39	B17	108
	2	–	–	–		34	–	–	–
	3	1	R16	154		35	38	C15	109
	4	–	–	–		36	–	–	–
	5	160	P14	159		37	37	C17	110
	6	–	U16	160		38	–	C16	111
	7	–	–	–		39	–	–	–
	8	159	R15	161		40	36	D17	112
	9	158	U15	162		41	35	D15	113
	10	–	–	–		42	–	–	–
	11	157	T15	163		43	34	E17	114
	12	–	–	–		44	–	–	–
	13	156	U14	164		45	33	D16	115
	14	–	U13	166		46	–	E15	117
	15	–	–	–		47	–	–	–
	16	154	T14	167		48	31	F16	118
B	17	12	N17	141	D	49	49	A14	92
	18	–	–	–		50	–	–	–
	19	11	M16	142		51	48	B12	93
	20	–	–	–		52	–	–	–
	21	9	M15	144		53	46	B13	95
	22	–	P17	145		54	–	A15	96
	23	–	–	–		55	–	–	–
	24	8	N16	146		56	45	B14	97
	25	7	R17	147		57	44	A16	98
	26	–	–	–		58	–	–	–
	27	6	P16	148		59	43	C14	99
	28	–	–	–		60	–	–	–
	29	5	T17	149		61	42	B16	100
	30	–	N15	150		62	–	B15	101
	31	–	–	–		63	–	–	–
	32	4	T16	151		64	41	A17	102

Table 51. EPM7256E & EPM7256S I/O Pin-Outs (Part 2 of 5)

LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP	LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP (3)
E	65	153	U12	168	G	97	30	E16	119
	66	–	–	–		98	–	–	–
	67	152	R13	169		99	29	F17	120
	68	–	–	–		100	–	–	–
	69	151	U11	170		101	28	F15	121
	70	–	T13	171		102	–	G16	122
	71	–	–	–		103	–	–	–
	72	150	T11	172		104	27	G15	123
	73	149	T12	173		105	26	G17	124
	74	–	–	–		106	–	–	–
	75	147	R12	175		107	24	H17	126
	76	–	–	–		108	–	–	–
	77	146 (4)	U10 (4)	176 (4)		109	23 (4)	H15 (4)	127 (4)
	78	–	R10	177		110	–	J17	128
	79	–	–	–		111	–	–	–
	80	145	T10	178		112	22	H16	129
F	81	21	J16	130	H	113	60	C9	79
	82	–	–	–		114	–	–	–
	83	20	J15	131		115	59	D9	80
	84	–	–	–		116	–	–	–
	85	19	K17	132		117	58	C10	81
	86	–	J14	133		118	–	A10	84
	87	–	–	–		119	–	–	–
	88	17	K16	135		120	54	A11	86
	89	16	K15	136		121	53	B10	87
	90	–	–	–		122	–	–	–
	91	15	L17	137		123	52	A12	88
	92	–	–	–		124	–	–	–
	93	14	L16	138		125	51	B11	89
	94	–	M17	139		126	–	A13	90
	95	–	–	–		127	–	–	–
	96	13	L15	140		128	50	C12	91

Table 51. EPM7256E & EPM7256S I/O Pin-Outs (Part 3 of 5)

LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP	LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP (3)
I	129	128	U6	197	J	145	100	J2	27
	130	–	–	–		146	–	–	–
	131	129	T5	196		147	101	J3	26
	132	–	–	–		148	–	–	–
	133	130	U7	195		149	102	K1	25
	134	–	T6	194		150	–	J4	24
	135	–	–	–		151	–	–	–
	136	131	T7	193		152	104	K2	22
	137	132	R6	192		153	105	K3	21
	138	–	–	–		154	–	–	–
	139	134	R7	190		155	106	L1	20
	140	–	–	–		156	–	–	–
	141	135 (4)	U8 (4)	189 (4)		157	107	L2	19
	142	–	R8	188		158	–	M1	18
	143	–	–	–		159	–	–	–
	144	136	T8	187		160	108	L3	17

Table 51. EPM7256E & EPM7256S I/O Pin-Outs (Part 4 of 5)

LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP	LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP (3)
K	161	91	F3	38	M	193	119	U1	4
	162	–	–	–		194	–	–	–
	163	92	F1	37		195	120	R2	3
	164	–	–	–		196	–	–	–
	165	93	E2	36		197	121	R3	206
	166	–	G2	35		198	–	U2	205
	167	–	–	–		199	–	–	–
	168	94	G3	34		200	122	P4	204
	169	95	G1	33		201	123	U3	203
	170	–	–	–		202	–	–	–
	171	97	H1	31		203	124	T3	202
	172	–	–	–		204	–	–	–
	173	98 (4)	H3 (4)	30 (4)		205	125	U4	201
	174	–	J1	29		206	–	U5	199
	175	–	–	–		207	–	–	–
	176	99	H2	28		208	127	T4	198
L	177	61	B9	78	N	209	109	N1	16
	178	–	–	–		210	–	–	–
	179	62	C8	77		211	110	M2	15
	180	–	–	–		212	–	–	–
	181	63	A9	76		213	112	M3	13
	182	–	A8	73		214	–	P1	12
	183	–	–	–		215	–	–	–
	184	67	A7	71		216	113	N2	11
	185	68	B8	70		217	114	R1	10
	186	–	–	–		218	–	–	–
	187	69	A6	69		219	115	P2	9
	188	–	–	–		220	–	–	–
	189	70	B7	68		221	116	T1	8
	190	–	A5	67		222	–	N3	7
	191	–	–	–		223	–	–	–
	192	71	C6	66		224	117	T2	6

Table 51. EPM7256E & EPM7256S I/O Pin-Outs (Part 5 of 5)

LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP	LAB	MC	160-Pin PQFP (1), (2)	192-Pin PGA (2)	208-Pin RQFP/PQFP (3)
O	225	82	B1	49	P	241	72	A4	65
	226	–	–	–		242	–	–	–
	227	83	C3	48		243	73	B6	64
	228	–	–	–		244	–	–	–
	229	84	C1	47		245	75	B5	62
	230	–	D3	46		246	–	A3	61
	231	–	–	–		247	–	–	–
	232	85	D1	45		248	76	B4	60
	233	86	C2	44		249	77	A2	59
	234	–	–	–		250	–	–	–
	235	87	E1	43		251	78	C4	58
	236	–	–	–		252	–	–	–
	237	88	E3	42		253	79	B2	57
	238	–	D2	40		254	–	B3	56
	239	–	–	–		255	–	–	–
	240	90	F2	39		256	80	A1	55

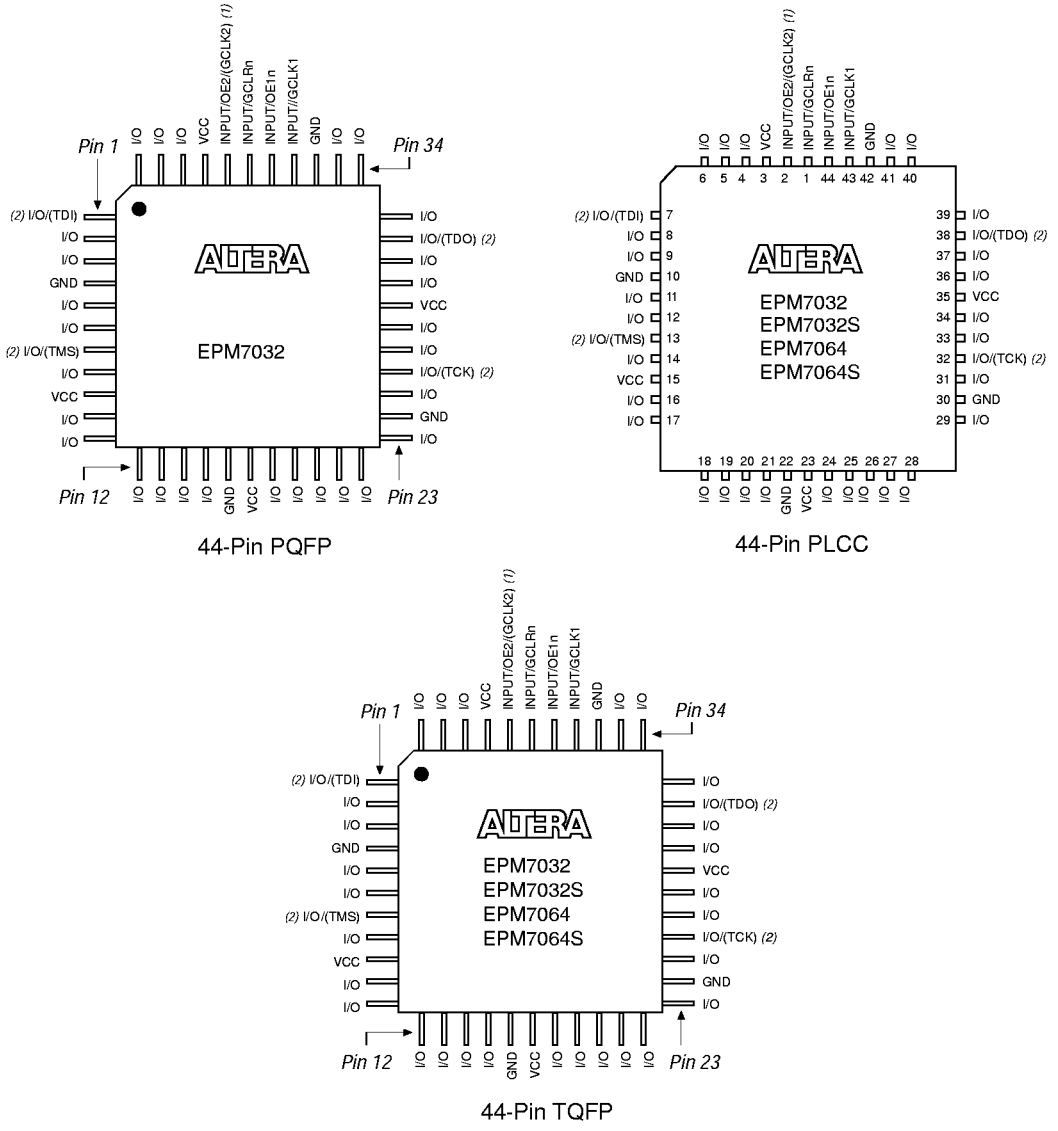
Notes to tables:

(1) A complete thermal analysis should be performed before committing a design to this device package. See the *Operating Requirements for Altera Devices Data Sheet* for more information.
(2) EPM7256S devices is not available in the 160-pin PQFP package.
(3) EPM7256E devices are not available in the 208-pin RQFP/PQFP packages.
(4) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for ISP, this pin is not available as a user I/O pin.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

Figure 16. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S or MAX 7000E devices only.



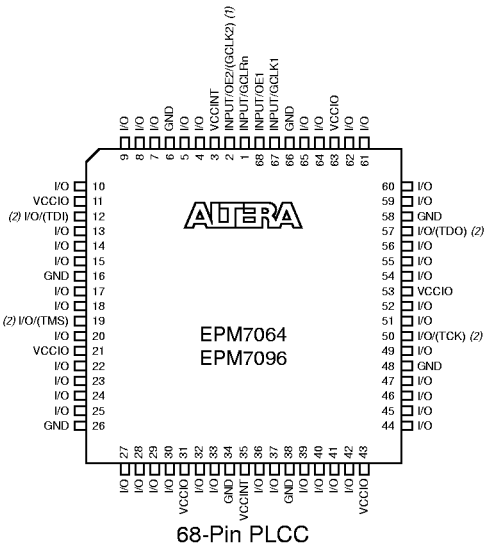
Notes:

(1) These pins are available in MAX 7000E and MAX 7000S devices only.

(2) JTAG ports are available in MAX 7000S devices only.

Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale. Pin functions shown in parentheses are for MAX 7000S or MAX 7000E devices only.



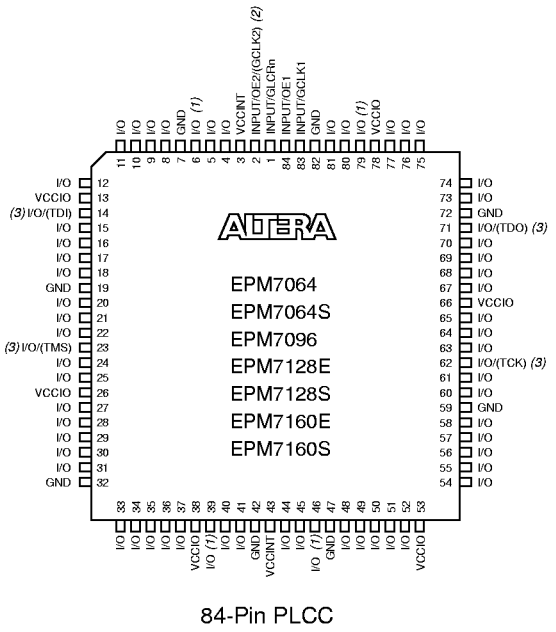
Notes:

(1) These pins are available in MAX 7000E and MAX 7000S devices only.

(2) JTAG ports are available in MAX 7000S devices only.

Figure 18. 84-Pin Package Pin-Out Diagram

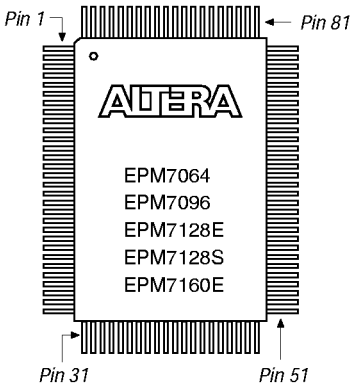
Package outline not drawn to scale. Pin functions in parentheses are for MAX 7000S or MAX 7000E devices only.



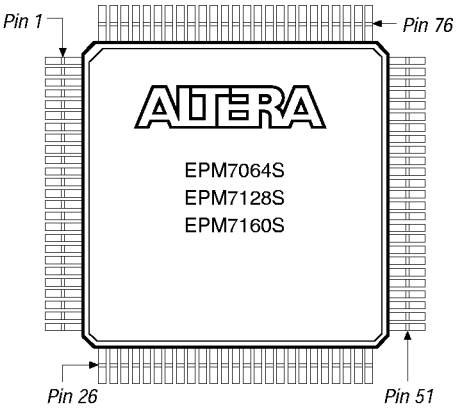
Notes:
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
(2) This pin is available in MAX 7000E and MAX 7000S devices only.
(3) JTAG ports are available in MAX 7000S devices only.

Figure 19. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



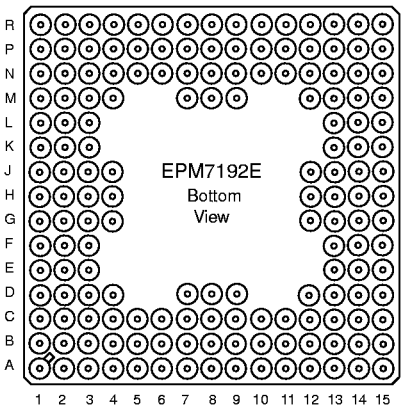
100-Pin PQFP



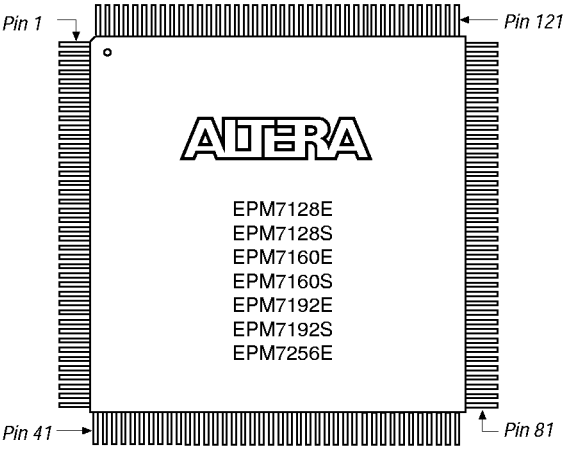
100-Pin TQFP

Figure 20. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



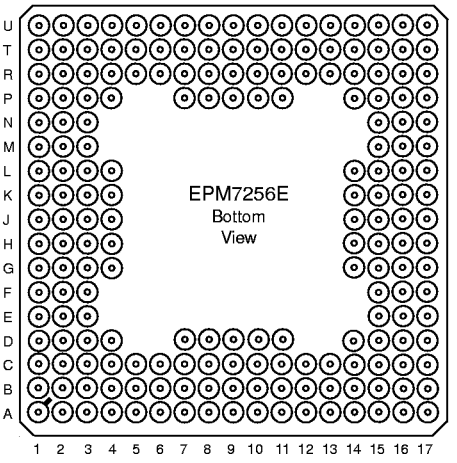
160-Pin PGA



160-Pin PQFP

Figure 21. 192-Pin Package Pin-Out Diagram

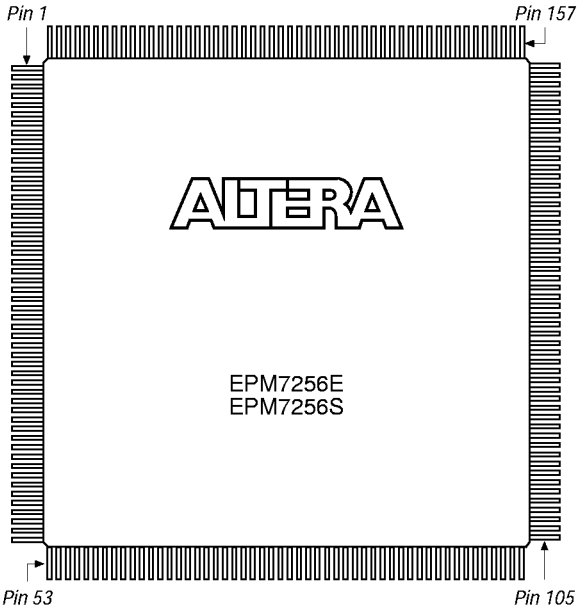
Package outline not drawn to scale.



192-Pin PGA

Figure 22. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



208-Pin PQFP/RQFP

Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.01 supersedes information published in previous version. The following changes were made to the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.01:

- The MasterBlaster serial/USB download cable was added to this document
- Figures 3 and 4 were updated.
- t_{CPPW} timing parameter information was clarified in the "Timing Model" section.