SIEMENS

SIMATIC

S7-1500, ET 200SP, ET 200pro

Cycle and response times

Function manual

Edition 09/2016

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This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

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⚠ WARNING
indicates that death or severe personal injury **may** result if proper precautions are not taken.

⚠ CAUTION
indicates that minor personal injury can result if proper precautions are not taken.

NOTICE
indicates that property damage can result if proper precautions are not taken.

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The product/system described in this documentation may be operated only by **personnel qualified** for the specific task in accordance with the relevant documentation, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products/systems.

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We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions.

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Preface

Purpose of the documentation

The controller offers various options for program execution with different run priorities. Cyclic-driven and time-driven program execution have the largest share. The response times of a controller are therefore significantly determined by the processing cycles.

There is also the possibility of event-driven program execution. The event-driven program execution is normally limited to a few selected events.

This manual provides information on the following topics:

- Types of program execution
- Run priorities
- Cycle and response times, and the influences to which they are subject
- Configuration options for the optimization of your user program

Basic knowledge required

The following knowledge is required in order to understand the documentation:

- General knowledge of automation technology
- Knowledge of the SIMATIC industrial automation system
- Knowledge of the use of Windows-based computers
- Knowledge of working with STEP 7

Conventions

STEP 7: In this documentation, "STEP 7" is used as a synonym for the configuration and programming software "STEP 7 as of V12 (TIA Portal)" and subsequent versions.

Please also observe notes marked as follows:

Note

A note contains important information on the product described in the documentation, on the handling of the product or on the section of the documentation to which particular attention should be paid.

Scope of the documentation

This documentation mainly describes the CPU components of the cycle and response times of the S7-1500 automation system, the CPUs of the ET 200SP distributed I/O system, and the CPU 1516pro-2 PN of the ET 200pro distributed I/O system. You can find links to more information on the ET 200MP, ET 200SP and ET 200pro distributed I/O systems at the corresponding points in this manual.

What's new compared to the previous version of the function manual (02/2014 edition)?

What's new?		What are the customer benefits?	Where can I find information?
Changed contents	Scope of the function manual expanded to include the CPUs of the ET 200SP distributed I/O system and CPU 1516pro-2 PN of the ET 200pro distributed I/O system	Functions that you will be familiar with from the SIMATIC S7-1500 CPUs are implemented in CPUs in other designs (ET 200SP) and in the CPU 1516pro-2 PN (degree of protection IP 65, IP 66 and IP 67).	Starting from section Program execution (Page 12)

See also

SIMATIC Portal (http://www.siemens.com/simatic-tech-doku-portal)

Catalog (http://mall.automation.siemens.com)

Security information

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- **Application examples**

  Tools and examples to solve your automation tasks – as well as function blocks, performance information and videos.

- **Services**

  Information about Industry Services, Field Services, Technical Support, spare parts and training offers.

- **Forums**

  For answers and solutions concerning automation technology.

- **mySupport**

  Your personal working area in Industry Online Support for messages, support queries, and configurable documents.

This information is provided by the Siemens Industry Online Support in the Internet (http://www.siemens.com/automation/service&support).

Industry Mall

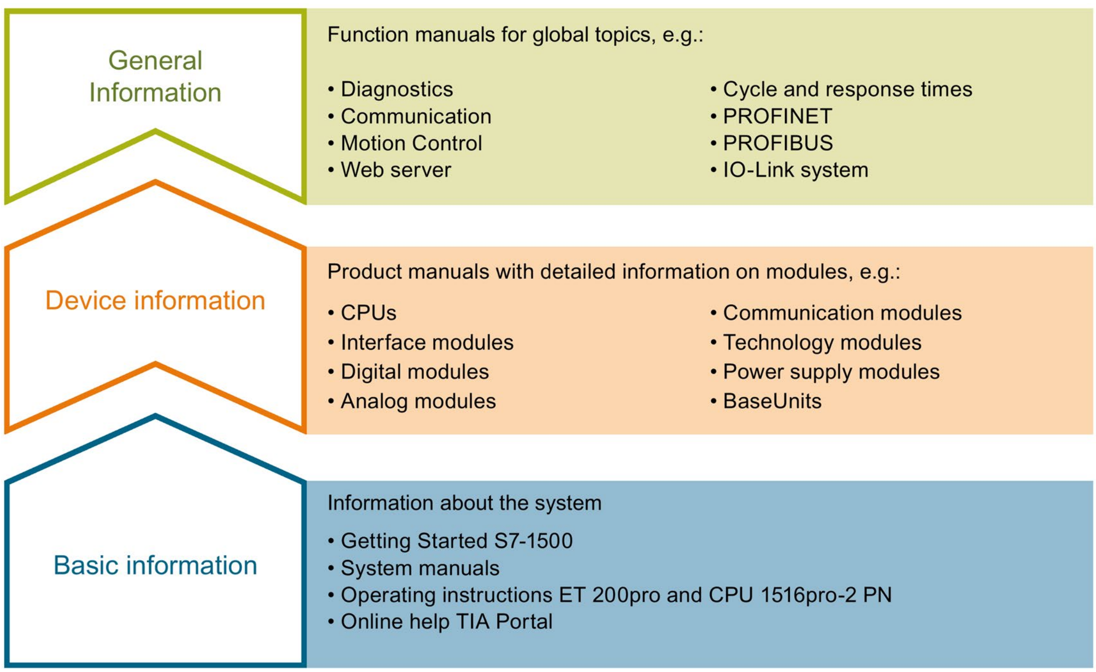
The Industry Mall is the catalog and order system of Siemens AG for automation and drive solutions on the basis of Totally Integrated Automation (TIA) and Totally Integrated Power (TIP).

Catalogs for all the products in automation and drives are available on the Internet (https://mall.industry.siemens.com).

Table of contents

1 Documentation guide

The documentation for the SIMATIC S7-1500 automation system, for CPU 1516pro-2 PN based on SIMATIC S7-1500, and for the distributed I/O systems SIMATIC ET 200MP, ET 200SP and ET 200AL is divided into three areas.
This division allows you easier access to the specific information you require.



Basic information

System manuals and Getting Started manuals describe in detail the configuration, installation, wiring and commissioning of the SIMATIC S7-1500, ET 200MP, ET 200SP and ET 200AL systems; use the corresponding operating instructions for CPU 1516pro-2 PN. The STEP 7 online help supports you in configuration and programming.

Device information

Product manuals contain a compact description of the module-specific information, such as properties, terminal diagrams, characteristics and technical specifications.

General information

The function manuals contain detailed descriptions on general topics such as diagnostics, communication, Motion Control, Web server, OPC UA.

You can download the documentation free of charge from the Internet (http://w3.siemens.com/mcms/industrial-automation-systems-simatic/en/manual-overview/Pages/Default.aspx).

Changes and additions to the manuals are documented in product information sheets.

You will find the product information on the Internet:

- S7-1500/ET 200MP (https://support.industry.siemens.com/cs/us/en/view/68052815)
- ET 200SP (https://support.industry.siemens.com/cs/us/en/view/73021864)
- ET 200AL (https://support.industry.siemens.com/cs/us/en/view/99494757)

Manual Collections

The Manual Collections contain the complete documentation of the systems put together in one file.

You will find the Manual Collections on the Internet:

- S7-1500/ET 200MP (https://support.industry.siemens.com/cs/ww/en/view/86140384)
- ET 200SP (https://support.industry.siemens.com/cs/ww/en/view/84133942)
- ET 200AL (https://support.industry.siemens.com/cs/ww/en/view/95242965)

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In the Documentation area in "mySupport" you can combine entire manuals or only parts of these to your own manual.
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You can find "mySupport" - Documentation on the Internet (http://support.industry.siemens.com/My/ww/en/documentation).

"mySupport" - CAx data

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You configure your own download package with a few clicks.

In doing so you can select:

- Product images, 2D dimension drawings, 3D models, internal circuit diagrams, EPLAN macro files
- Manuals, characteristics, operating manuals, certificates
- Product master data

You can find "mySupport" - CAx data on the Internet (http://support.industry.siemens.com/my/ww/en/CAxOnline).

Application examples

The application examples support you with various tools and examples for solving your automation tasks. Solutions are shown in interplay with multiple components in the system - separated from the focus on individual products.

You will find the application examples on the Internet (https://support.industry.siemens.com/sc/ww/en/sc/2054).

TIA Selection Tool

With the TIA Selection Tool, you can select, configure and order devices for Totally Integrated Automation (TIA).
This tool is the successor of the SIMATIC Selection Tool and combines the known configurators for automation technology into one tool.
With the TIA Selection Tool, you can generate a complete order list from your product selection or product configuration.

You can find the TIA Selection Tool on the Internet (http://w3.siemens.com/mcms/topics/en/simatic/tia-selection-tool).

SIMATIC Automation Tool

You can use the SIMATIC Automation Tool to run commissioning and maintenance activities simultaneously on different SIMATIC S7 stations as a bulk operation, independently of the TIA Portal.

The SIMATIC automation tool provides a variety of functions:

- Scanning of a PROFINET/Ethernet plant network and identification of all connected CPUs
- Address assignment (IP, subnet, gateway) and station name (PROFINET device) to a CPU
- Transfer of the date and programming device/PC time converted to UTC time to the module
- Program download to CPU
- Operating mode switchover RUN/STOP
- CPU localization by means of LED flashing
- Reading out CPU error information
- Reading of CPU diagnostic buffer
- Reset to factory settings
- Updating the firmware of the CPU and connected modules

You can find the SIMATIC Automation Tool on the Internet (https://support.industry.siemens.com/cs/ww/en/view/98161300).

PRONETA

With SIEMENS PRONETA (PROFINET network analysis), you analyze the plant network during commissioning. PRONETA features two core functions:

- The topology overview independently scans PROFINET and all connected components.
- The IO check is a fast test of the wiring and the module configuration of a plant.

You can find SIEMENS PRONETA on the Internet (https://support.industry.siemens.com/cs/ww/en/view/67460624).

Program execution 2

2.1 Principle of operation

Introduction

You often program your user program with a cyclic OB, usually in OB 1. With complex applications, problems are often encountered in complying with the response times required by the application. You can often meet the response time requirements by splitting the user program up into several parts with different response time requirements. The CPU offers a number of different OB types for this purpose, the properties (priority, frequency, etc.) of which can be adapted to meet your requirements.

Program organization

You can choose from the following types of program execution for running your user program:

Program execution in the cyclic program of the CPU:

The CPU executes the user program cyclically. When the execution has reached the end of a cycle, the program execution starts again in the next cycle. In the simplest case, you execute the entire user program in the cyclic program of the CPU. All tasks in the user program are then processed with equal rank. This also results in the same response times for all tasks.

In addition to program execution in the cyclic program, there is time-driven and event-driven program execution.

Time-driven execution:

In a complex user program, there are frequently portions with different response time requirements. You can optimize the response times by taking advantage of these differences in the requirements. To do so, you can move the program parts with higher response time requirements to higher-priority OBs with shorter cycles, for example cyclic interrupt OBs.

The execution of these parts can thus occur with different frequencies and priorities.

Event-driven execution:

Depending on the I/O modules used, you can configure hardware interrupts for specific process events (such as an edge change of a digital input) that result in the call of the assigned hardware interrupt OB. The hardware interrupts have a higher priority and interrupt the cyclic program of the CPU. You can achieve very short response time in the CPU with hardware interrupts by directly triggering program execution.

Keep in mind that the time characteristics of your application becomes less predictable with intense use of hardware interrupts. The reason for this is that the time at which the triggering events occur can result in drastically different response times.

Tip: Use hardware interrupts only for a few selected events.

Special consideration for hardware interrupts: If you have assigned an OB to an event (hardware interrupt), the OB then has the priority of the event.

Using process image partitions

If a program is distributed over various OBs, for example, due to differing response time requirements, it is advisable and often necessary to assign the update of the used I/O data directly to these OBs. You can use process image partitions for this purpose.

You group the input and output data in a process image partition according to their use in the program and assign the data to the OB.

A process image partition of the inputs (PIPI) permits the associated input data for an OB program to be updated immediately before the OB program starts.

A process image partition of the outputs (PIPQ) permits the output data associated with an OB program to become effective on the outputs immediately after the OB program runs.

You have 32 (0 … 31) process image partitions at your disposal. The I/O is assigned to the process image partition 0 by default (setting: "Automatic update"). Process image partition 0 is permanently assigned to cyclic execution.

You have to configure the "system-side update of process image partitions". You can find additional information on configuration of process image partitions in the online help for STEP 7 under the keyword "Assign process image/process image partition".

Interruptibility of program execution

Each organization block is processed according to the priority it has been assigned. You can adapt the priority according to the response time requirements for most organization blocks.

All cycle OBs always have the lowest priority of 1. The highest priority is 26.

Communication tasks always have priority 15. If necessary, you can change the priority of your blocks and select a higher priority than the communication.

Organization blocks or system activities with higher priority interrupt those with lower priority, and thus extend the runtime of the interrupted organization blocks or system activities. If two pending tasks have the same priority, these tasks are processed in the order in which the tasks occurred.

Note

Higher priority OBs

Communication functionality is strongly influenced by too many or runtime-intensive OBs with a priority > 15.

When using OBs with a priority > 15, you should consider the runtime load that they cause in order to keep communication functionality at a reasonable level.

Reference

You can find additional information on the subject of "priorities" in the section Events and OBs of the system manual S7-1500 Automation system (http://support.automation.siemens.com/WW/view/en/59191792), the system manual ET 200SP distributed I/O system (http://support.automation.siemens.com/WW/view/en/58649293) and the operating instructions for CPU 1516pro-2 PN (https://support.industry.siemens.com/cs/ww/en/view/109482416).

You can find additional information on organization blocks and their priorities for Motion Control in the function manual S7-1500T Motion Control V3.0 in the TIA Portal V14 (https://support.industry.siemens.com/cs/ww/en/view/109481326).

2.2 CPU overload behavior

Principle of CPU overload behavior

An occurring event triggers the execution of the associated OB. Depending on the OB priority and the current processor load, a time delay may occur before the OB is executed when there is an overload. The same event can therefore occur once or several times before the user program processes the OB belonging to the preceding event. The CPU handles such a situation as follows: The operating system queues the events in the queue associated with their priority in the order of their occurrence.

To control temporary overload situations, you can limit the number of queued events that originate from the same source. The next event is discarded as soon as the maximum number of pending triggers of a specific cyclic interrupt OB, for example, is reached.

An overload occurs when events which originate from the same source occur faster than they can be processed by the CPU.

Configuration of the overload response

In the properties of an organization block in which an overload can occur, you can select the response to an overload occurrence under "Attributes" and "Event queuing".

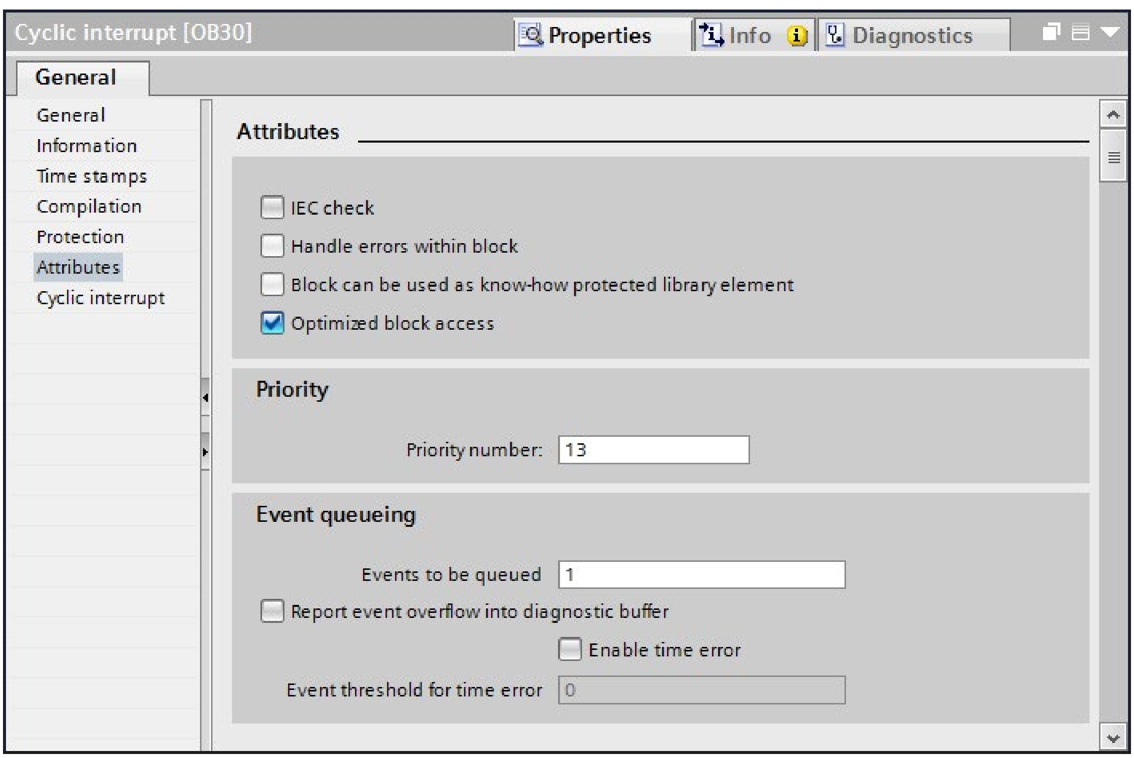


Figure 2-1 Configuration of the overload response in the block properties

Below, the term "similar events" refers to events from a single source, such as triggers for a specific cyclic interrupt OB.

The OB parameter "Events to be queued" is used to specify how many similar events the operating system places in the associated queue and therefore post-processes. If this parameter has the value 1, for example, exactly one event is stored temporarily.

Note

Post-processing of cyclic events is often not desirable, as this can lead to an overload with OBs of the same or lower priority. Therefore, it is generally advantageous to discard similar events and to react to the overload situation during the next scheduled OB execution. If the value of the "Events to be queued" parameter is low, this ensures that an overload situation is mitigated rather than aggravated.

If the maximum number of triggers is reached in the queue for a cyclic interrupt OB (Cyclic interrupt), for example, each additional trigger is only counted and subsequently discarded. During the next scheduled execution of the OB, the CPU provides the number of discarded triggers in the "Event_Count" input parameter (in the start information). You can then react appropriately to the overload situation. The CPU then sets the counter for lost events to zero.

If the CPU first discards a trigger for a cyclic interrupt OB, for example, its further behavior depends on the OB parameter "Report event overflow into diagnostic buffer": If the check box is selected, the CPU enters the event DW#16#0002:3507 once in the diagnostics buffer for the overload situation at this event source. The CPU suppresses additional diagnostics buffer entries of the event DW#16#0002:3507 until all events from this source have been post-processed.

The cyclic interrupt OB parameter "Enable time error" is used to specify whether the time error OB should be called when a specific overload level is reached for similar events. You can find the OB parameter "Enable time error" in the properties of the OB in the "Attributes" category.

When you enable the time error OB (check box selected), use the OB parameter "Event threshold for time error" to specify the number of similar events in the queue as of which the time error OB is called. If this parameter has the value 1, for example, the CPU enters the event DW#16#0002:3502 once in the diagnostics buffer and requests the time error OB when the second event occurs. The CPU suppresses additional diagnostics buffer entries of the event DW#16#0002:3502 until all events from this source have been post-processed.

Note

The "Enable time error" parameter is not enabled in the default setting. If a time error occurs due to a cyclic interrupt OB, for example, the CPU does not change to STOP mode.

In the event of an overload, you therefore have the option of programming a reaction well before the limit is reached for similar events and thus before events are discarded.

The following value range applies to the "Event threshold for time error" parameter:
1 ≤ "Event threshold for time error" ≤ "Events to be queued".

3 Cyclic program execution

3.1 Cycle

Definition of cycle

A cycle includes the following sections:

- Automatic update of the process image partition 0 of the inputs (PIPI 0)
- Execution of the cyclic program
- Update of process image partition 0 of the outputs (PIPQ 0)

The process image partition 0 is automatically updated in the cycle. You assign the I/O addresses to these process image partitions (PIPI 0 / PIPQ 0) when you configure the I/O modules via the "Automatic update" setting (default).

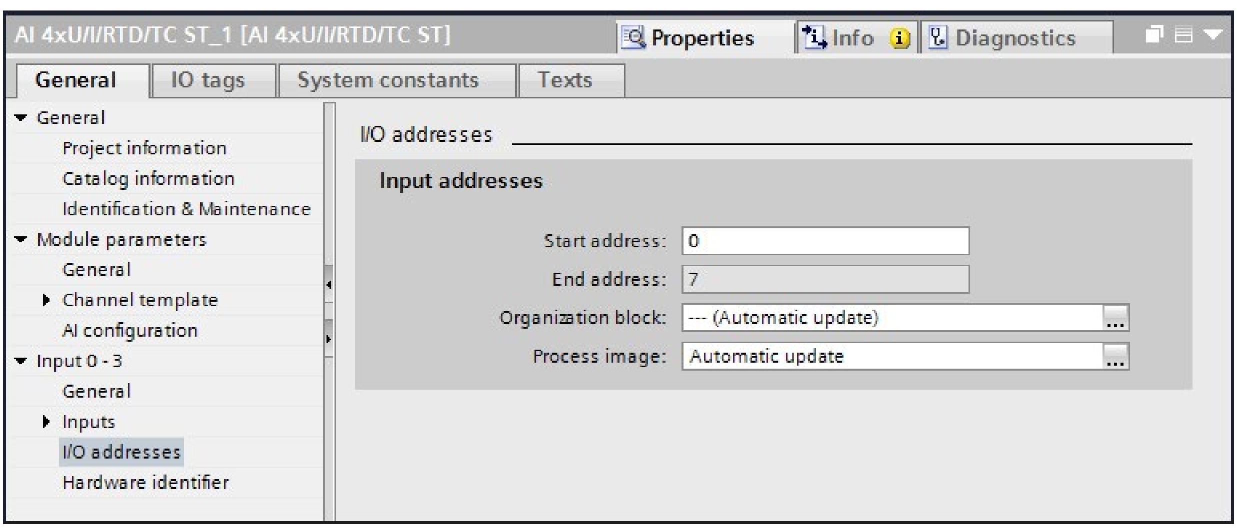
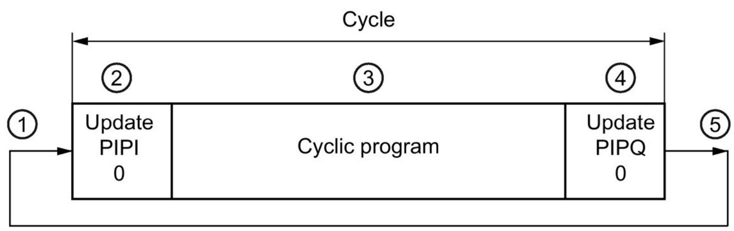


Figure 3-1 Assigning I/O addresses to process image partitions

The figure below illustrates the phases that are passed through during a cycle.



① The operating system starts measurement of the cycle time.
② The CPU reads the status of the inputs at the input module and writes the input data to the process image input.
③ The CPU processes the user program and executes the instructions specified in the program.
④ The CPU writes the states from the process image output to the output modules.
⑤ The operating system evaluates the determined cycle time and starts the measurement again.

Figure 3-2 Cycle

3.2 Cycle time

Definition of cycle time

The cycle time is the time the CPU needs to execute the cyclic program and to update the process image input and output as well as for all program parts and system activities that interrupt this cycle.

3.2.1 Different cycle times

Introduction

The cycle time (T_{cyc}) is not the same length in each cycle because the execution times may vary. Causes of this include:

- Different program runtimes

  (e.g. program loops, conditional commands, conditional block calls, or different program paths)
- Lengthening due to interruptions

  (e.g. time-driven interrupt execution, execution of hardware interrupts or communication)

Causes of different cycle times

The cycle time T_{cyc2} is longer than T_{cyc1}, because the cyclic program is interrupted by a cyclic interrupt OB in this example (e.g. OB 30) The cyclic interrupt OB in turn is interrupted by Motion Control functions and communication.

The figure below shows the different cycle times T_{cyc1} and T_{cyc2}.

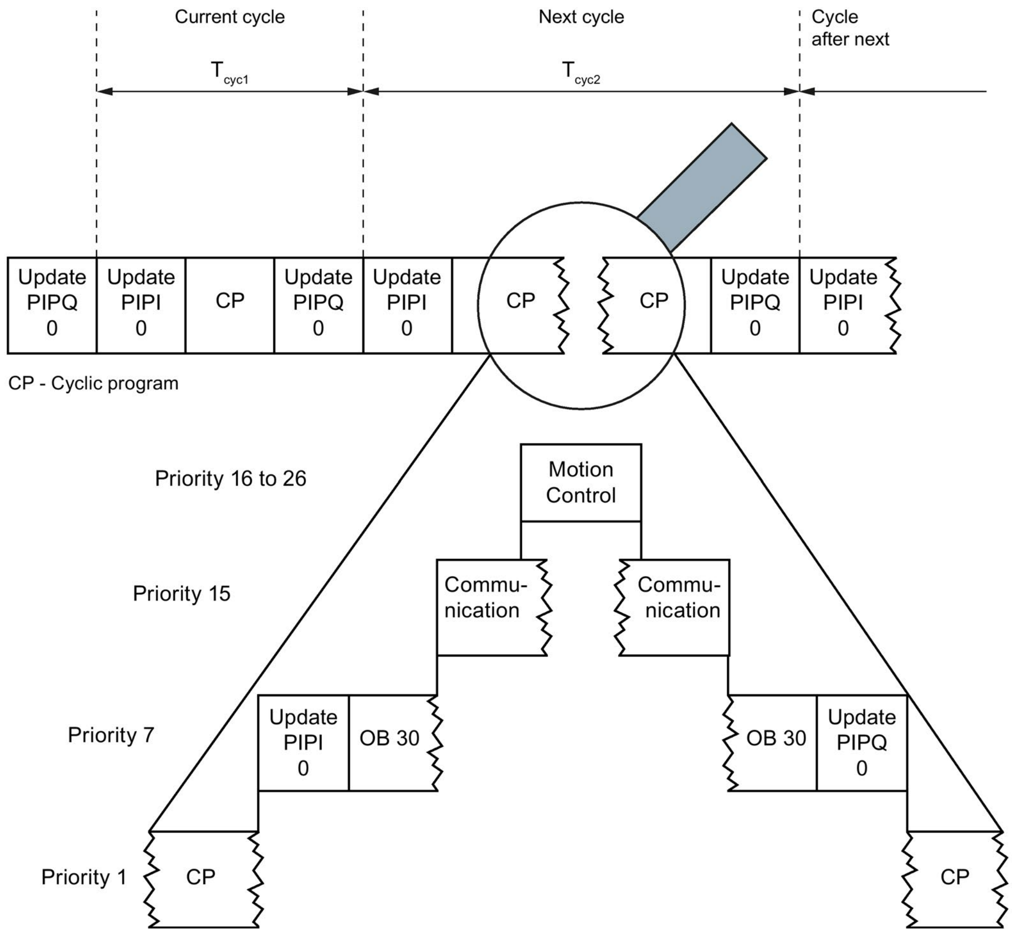


Figure 3-3 Possible causes of differing cycle times

Minimum cycle time

In STEP 7, you can set a minimum cycle time for a CPU. The default for the minimum cycle time is one millisecond. It may be advisable to increase this setting in the following cases:

- To reduce the cycle time's fluctuation range.
- To make remaining computing time available for communication tasks that the CPU can process until the expiry of the minimum cycle time, for example, when
  - The CPU is mainly used for communication purposes
  - The processing power of the communication is not enough because many organization blocks are set with a priority > 15 (e.g. for Motion Control functions)

Maximum cycle time

The cycle time is monitored by the CPU. By default, the maximum cycle time is 150 ms. You can set this value from 1 ms to 6000 ms when assigning parameters to the CPU. When the cycle time is longer than the maximum cycle time, the time error OB (OB 80) is called.

You have the option of restarting the maximum cycle time using the "RE_TRIGR" instruction, and thus extending it.

With the user program in OB 80 you specify how the CPU responds to the time error. The CPU goes to STOP under the following conditions.

- If you have not loaded an OB 80.
- If the cycle is still not completed after an additional maximum cycle time

Keep in mind that the cycle time is extended by interruptions as shown in the previous figure.

Cycle time statistics

You can read the cycle time statistics either directly from STEP 7 (Online tools task card) or with the "RT_INFO" instruction.

You can use the "RT_INFO" instruction to generate statistics in STEP 7 on the runtime of specific organization blocks, communication or the user program. For example, this includes

- The minimum and maximum cycle time
- The portions of runtime used for communication and the user program

---

Note

Showing the cycle time statistics on the display and Web server

With the S7-1500 CPUs, you also have the option of calling the cycle time statistics via the display of the CPU. As of firmware version 2.0 of the CPUs, the cycle time statistics are also displayed in the Web server.

To view the cycle time statistics directly in STEP 7, follow these steps:

1. Establish an online connection to the CPU with STEP 7.
2. Select the Online tools task card on the very right.

Result: The diagram of the cycle time statistics is displayed in the cycle time section.

The following figure shows an extract from STEP 7 with the cycle time statistics. In this example, the cycle time fluctuates between 7 ms and 12 ms. The current cycle time is 10 ms. The maximum cycle time that can be set in this example is 40 ms.

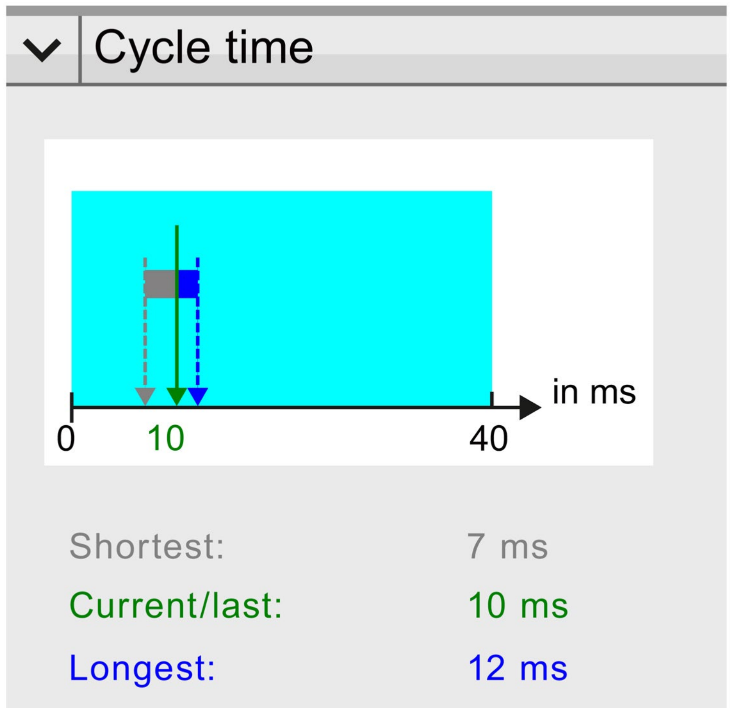


Figure 3-4 Cycle time statistics

You can find additional information on the runtime characteristics of the CPU with the "RT_INFO" instruction in the user program. You can read the utilization of the CPU by the user program and communication in percentage, and you can also read the runtime statistics of individual OBs.

Reference

You can find additional information on the "RT_INFO" instruction in the STEP 7 online help.

3.2.2 Influences on the cycle time

3.2.2.1 Update time for process image partitions

Estimating update time for process image partitions

The update time of the process image partitions depends on the volume of assigned central and distributed I/O module data.

You can estimate the update time using the following formula:

  Base load for process image update
+ Number of words in the process image x copy time for central I/O
+ Number of words in the process image via DP x copy time for PROFIBUS I/O
+ Number of words in the process image via PROFINET x copy time for PROFINET I/O

= **Update time of the process image partition**

Update times of the process image partitions

The following table contains the times for estimating the typical update times of the process image partitions.

Table 3- 1 Data for estimating the typical update time of the process image partition

Components	**Update time of the CPU**			
	S7-1500			
	1511(F)-1 PN **1511T-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T-2 PN** **1516(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP ODK**
Base load for process image partition update	35 μs	30 μs	7 μs	5 μs
Copy time for central I/O	9 μs/word	8 μs/word	5 μs/word	4 μs/word
Copy time for distributed I/O via PROFIBUS	0.5 μs/word	0.5 μs/word	0.4 μs/word	0.3 μs/word
Copy time for distributed I/O via PROFINET	0.5 μs/word	0.5 μs/word	0.4 μs/word	0.3 μs/word

Components	Update time of the CPU		
	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Base load for process image partition update	60 µs	60 µs	30 µs
Copy time for central I/O	0.5 µs/word	0.5 µs/word	0.5 µs/word
Copy time for distributed I/O via PROFIBUS	0.5 µs/word	0.5 µs/word	0.5 µs/word
Copy time for distributed I/O via PROFINET	0.5 µs/word	0.5 µs/word	0.5 µs/word

Components	Update time of the CPU
	ET 200pro
	1516pro(F)-2 PN
Base load for process image partition update	30 µs
Copy time for central I/O	120 µs/word
Copy time for distributed I/O via PROFIBUS	0.5 µs/word
Copy time for distributed I/O via PROFINET	0.5 µs/word

Note

Update time of the backplane bus for ET 200SP CPUs

For the update time of the ET 200SP CPUs, observe also the information in table "Update time of the ET 200SP CPUs" in the section Response time for cyclic and time-driven program execution (Page 33).

3.2.2.2 User program execution time

Introduction

Organization blocks or system activities with higher priority interrupt those with lower priority, and thus extend the runtime of the lower-priority organization blocks or system activities.

Program execution time without interruptions

The user program has a certain runtime without interruptions. The length of the runtime depends on the number of operations that are executed in the user program.

The following table contains the typical durations of operations.

Table 3- 2 Duration of an operation

	S7-1500						
CPU	1511(F)-1 PN 1511T-1 PN 1511C-1 PN	1512C-1 PN	1513(F)-1 PN	1515(F)-2 PN 1515T-2 PN	1516(F)-3 PN/DP	1517(F)-3 PN/DP 1517T(F)-3 PN/DP	1518(F)-4 PN/DP 1518(F)-4 PN/DP ODK
Bit operations, typ.	60 ns	48 ns	40 ns	30 ns	10 ns	2 ns	1 ns
Word operations, typ.	72 ns	58 ns	48 ns	36 ns	12 ns	3 ns	2 ns
Fixed-point arithmetic, typ.	96 ns	77 ns	64 ns	48 ns	16 ns	3 ns	2 ns
Floating-point arithmetic, typ.	384 ns	307 ns	256 ns	192 ns	64 ns	12 ns	6 ns

	ET 200SP		
CPU	**1510SP(F)-1 PN**	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Bit operations, typ.	72 ns	48 ns	30 ns
Word operations, typ.	86 ns	58 ns	36 ns
Fixed-point arithmetic, typ.	115 ns	77 ns	48 ns
Floating-point arithmetic, typ.	461 ns	307 ns	192 ns

	ET 200pro
CPU	**1516pro(F)-2 PN**
Bit operations, typ.	10 ns
Word operations, typ.	12 ns
Fixed-point arithmetic, typ.	16 ns
Floating-point arithmetic, typ.	64 ns

Note

Instruction "RUNTIME"

You can measure the runtimes of program sequences with the instruction "RUNTIME".

Extension due to nesting of higher-priority OBs and/or interrupts

The interruption of a user program at the end of an instruction by a higher-priority OB causes a certain basic time expenditure. Take account of this basic time expenditure in addition to the update time of the assigned process image partitions and the execution time of the contained user program. The following tables contain the typical times for the various interrupts and error events.

Table 3- 3 Basic time expenditure for an interrupt

	S7-1500			
CPU	**1511(F)-1 PN** **1511T-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T-2 PN** **1516(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP ODK**
Hardware interrupt	90 µs	80 µs	20 µs	12 µs
Time-of-day interrupt	90 µs	80 µs	20 µs	12 µs
Time-delay interrupt	90 µs	80 µs	20 µs	12 µs
Cyclic interrupt	90 µs	80 µs	20 µs	12 µs

	ET 200SP		
CPU	**1510SP(F)-1 PN**	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Hardware interrupt	90 µs	90 µs	80 µs
Time-of-day interrupt	90 µs	90 µs	80 µs
Time-delay interrupt	90 µs	90 µs	80 µs
Cyclic interrupt	90 µs	90 µs	80 µs

	ET 200pro
CPU	**1516pro(F)-2 PN**
Hardware interrupt	80 µs
Time-of-day interrupt	80 µs
Time-delay interrupt	80 µs
Cyclic interrupt	80 µs

Table 3- 4 Basic time expenditure for an error OB

	S7-1500			
CPU	**1511(F)-1 PN** **1511T-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T-2 PN** **1516(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP ODK**
Programming error	90 µs	80 µs	20 µs	12 µs
I/O access error	90 µs	80 µs	20 µs	12 µs
Time error	90 µs	80 µs	20 µs	12 µs
Diagnostic interrupt	90 µs	80 µs	20 µs	12 µs
Module failure/recovery	90 µs	80 µs	20 µs	12 µs
Station failure/recovery	90 µs	80 µs	20 µs	12 µs

	ET 200SP		
CPU	**1510SP(F)-1 PN**	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Programming error	90 µs	90 µs	80 µs
I/O access error	90 µs	90 µs	80 µs
Time error	90 µs	90 µs	80 µs
Diagnostic interrupt	90 µs	90 µs	80 µs
Module failure/recovery	90 µs	90 µs	80 µs
Station failure/recovery	90 µs	90 µs	80 µs

	ET 200pro
CPU	**1516pro(F)-2 PN**
Programming error	80 µs
I/O access error	80 µs
Time error	80 µs
Diagnostic interrupt	80 µs
Module failure/recovery	80 µs
Station failure/recovery	80 µs

Reference

You can find additional information on the topic of error handling in the Events and OBs section of the

- System manual S7-1500 Automation system (http://support.automation.siemens.com/WW/view/en/59191792)
- System manual ET 200SP distributed I/O system (http://support.automation.siemens.com/WW/view/en/58649293)
- Operating instructions CPU 1516pro-2 PN (https://support.industry.siemens.com/cs/ww/en/view/109482416)

You can find additional information on the topic of the complete cycle time of a program in an FAQ on the Internet (https://support.industry.siemens.com/cs/ww/en/view/87668055).

3.2.2.3 Extension of cycle time due to communication load

Impact of communication on the cycle time

In the sequence model of the CPU, communication tasks are processed with priority 15. All program parts with priority > 15 (e.g. for Motion Control functions) are unaffected by communication.

Configured communication load

The CPU operating system provides the maximum specified percentage of total CPU processing power for communication tasks. The communication load is preset in STEP 7 at 50%, for example, for the CPUs of the S7 series. If the processing power is not needed for communication, then the processing power is available to the operating system and the user program.

Communication is allocated the requisite computing time in 1 ms increments, with priority 15. At 50% communication load, 500 µs of each 1 millisecond are used for communication.

The following formula may be used to estimate the extension of the cycle time by communication.

$$\text{Actual cycle time} = \text{Cycle time without communication} \times \frac{100}{100 - \text{"configured communication load in \%"}}$$

Figure 3-5 Formula: Impact of communication load

With a complete use of the communication load of 50% (default), the following value results:

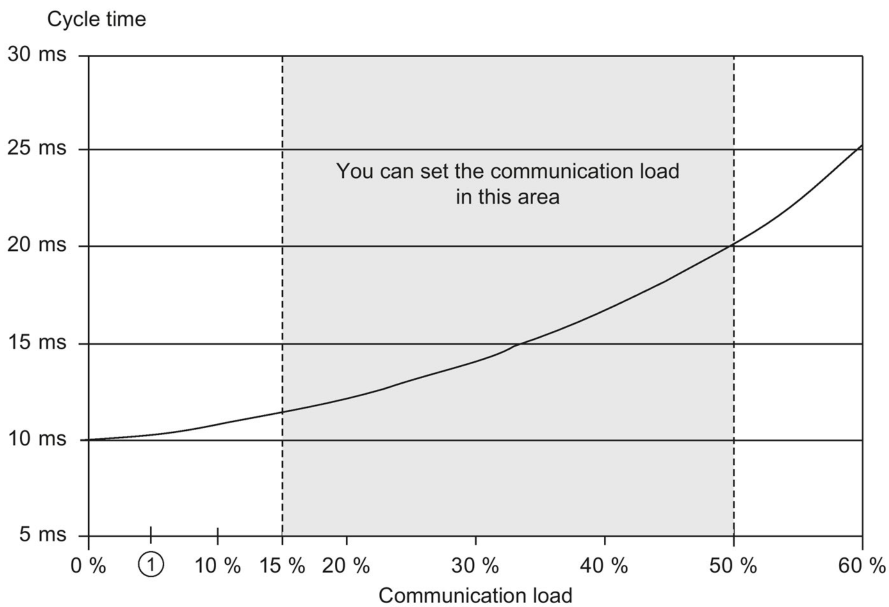
$$\text{Actual cycle time} = \text{Cycle time without communication} \times 2$$

Figure 3-6 Extension of cycle time due to communication load

The actual cycle time is up to twice as long as the cycle time without communication when you use the default communication load.

Dependency of maximum cycle time on the configured communication load

The diagram shows the nonlinear relationship between maximum cycle time and configured communication load with a pure cycle time of 10 ms, which means without interruptions.



① CPUs 1517(F)-3 PN/DP, CPU 1517T(F)-3 PN/DP, CPU 1518(F)-4 PN/DP, CPU 1518(F)-4 PN/DP ODK: The (minimum) communication load that can be set is 5%.

Figure 3-7 Maximum cycle time depending on the configured communication load

The shown influence of the communication load on the execution time applies to all OBs with a priority ≤ 15.

Reducing the cycle time with a lower communication load

You can reduce the setting for the communication load in the hardware configuration. If you set a communication load of 20% instead of the default 50%, for example, the cycle time extension due to the communication is reduced from a factor of 2 to 1.25.

Effect on the actual cycle time

Communication is only one cause of extension of the cycle time. All events that extend the cycle time (e.g. hardware interrupts) mean that more asynchronous events can occur within a cycle which additionally extend the cyclic program. This extension depends on the number of events that occur in the cyclic program and the time required to process these events.

Note

Checking parameter changes

- Check the effects of a value change on the "Cycle load due to communication" parameter during system operation. You can use the "RT_INFO" instruction to determine the portions of runtime used for communication and the user program.
- Take the communication load into consideration when setting the maximum cycle time to prevent time errors (for example, exceeding the cycle time within a cycle) from occurring.

Tips

Whenever possible, use the default setting for the configured communication load.

If you reduce the value of the communication load, keep in mind that communication tasks are interrupted by higher-priority OBs. This means it will also take longer to process the communication.

See also

Different cycle times (Page 18)

3.2.2.4 Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2)

Introduction

If you configure the PROFINET IO communication on the 2nd PROFINET interface (X2) (operated as IO controller or IO device) of the CPUs 1515(F)-2 PN, 1515T-2 PN, 1516(F)-3 PN/DP and 1516(F)pro-2 PN (as of firmware version 2.0), additional system load occurs.

This additional system load has priority 26 and extends the runtime of the program. The execution of synchronous cycle interrupts or hardware interrupts, for example, can be delayed as a result.

The additional system load depends on:

- The communication load on the 2nd PROFINET interface (X2)
- The number of IO devices that the CPU on the 2nd PROFINET interface (X2) updated within a millisecond

You determine the additional system load with the RT_INFO (read RUNTIME statistics) instruction at the Mode parameter with mode 10 or mode 20.

Reducing additional system load

Reduce the communication load on the 2nd PROFINET interface, e.g. with:

- Fewer HMI devices or slower update cycles of the HMI devices
- Less or slower communication with other CPUs

Increase the update times in STEP 7 for all IO devices that are assigned to the 2nd PROFINET interface (X2):

1. Select the "I/O communication" in the "Network view" of STEP 7.
2. Set the "Update mode" parameter to "Adjustable".
3. Select a higher value for the "Update time [ms]" parameter in the drop-down list.
4. Repeat this setting for the other IO devices.

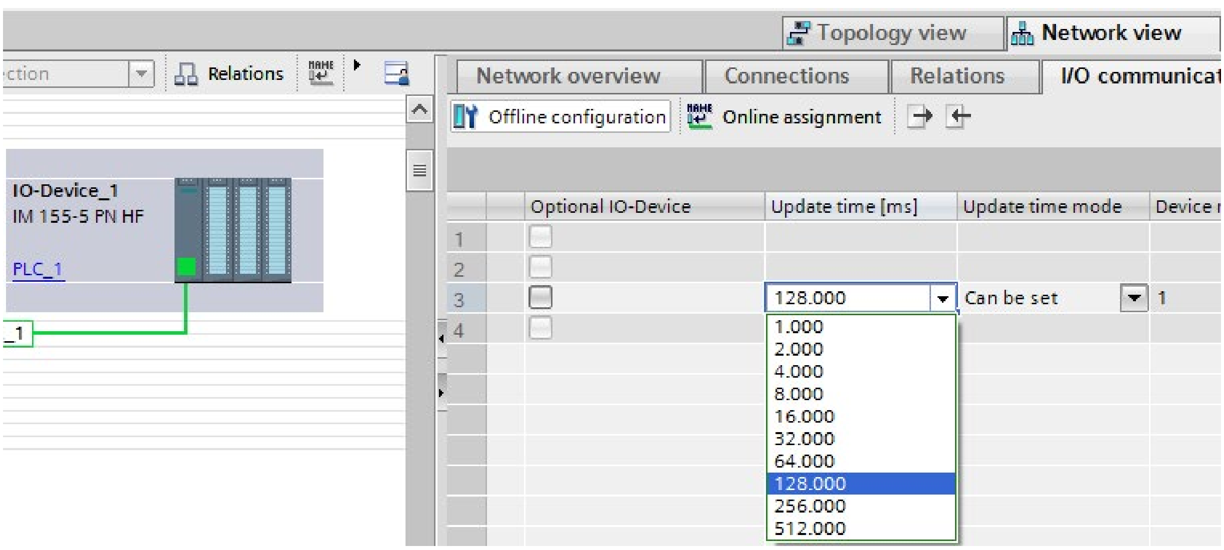


Figure 3-8 Increasing update times

3.3 Time-driven program execution in cyclic interrupts

With a cyclic interrupt, you can have a particular program processed in a defined cycle. A priority from 2 to 24 can be set for the cyclic interrupt. This makes the priority of cyclic interrupts higher than the priority of the cyclic program. A cyclic interrupt increases the execution time of the cyclic program.

Tip: By shifting program sections to cyclic interrupts, you can reduce the response times or better adapt them to your requirements.

In STEP 7, the organization blocks OB 30 to OB 38 are provided for the execution of cyclic interrupts. You can create additional cyclic interrupts starting with organization block OB 123. The number of available organization blocks depends on the CPU used.

Definition

A cyclic interrupt is an interrupt initiated according to a defined cycle that causes a cyclic interrupt OB to be processed.

Cycle of a cyclic interrupt

The cycle of a cyclic interrupt is defined as the time from the call of a cyclic interrupt OB to the next call of a cyclic interrupt OB.

The following figure shows an example of the cycle of a cyclic interrupt.

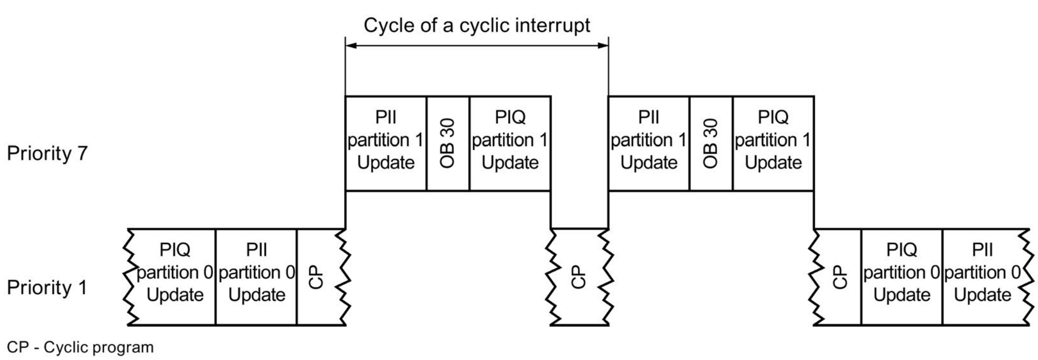


Figure 3-9 Call interval of a cyclic interrupt

Accuracy of a cyclic interrupt

If a cyclic interrupt is not delayed by a higher-priority OB or communication activities, the accuracy with which it is started is nevertheless subject to system-dependent fluctuations.

The following table shows the accuracy (typical times) with which a cyclic interrupt is triggered:

Table 3- 5 Accuracy of cyclic interrupts

	S7-1500			
CPU	**1511(F)-1 PN** **1511T-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T-2 PN** **1516(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP ODK**
Cyclic interrupt	±90 µs	±80 µs	±30 µs	±25 µs

	ET 200SP		
CPU	**1510SP(F)-1 PN**	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Cyclic interrupt	±90 µs	±90 µs	±80 µs

	ET 200pro
CPU	**1516pro(F)-2 PN**
Cyclic interrupt	±80 µs

3.4 Response time for cyclic and time-driven program execution

Introduction

In this section you will learn about the concept of "response time", and how to calculate the response time.

Definition

The response time in the case of cyclic or time-controlled program execution is the time between the detection of an input signal and the change of a connected output signal.

Fluctuation in the response time of the CPU

The actual response time of the CPU fluctuates between one and two cycles for cyclic program execution and between one and two cyclic interrupt cycles for time-controlled program execution.

You should always assume the longest response time when configuring your system.

The following figure shows the shortest and longest response times of the CPU to an event.

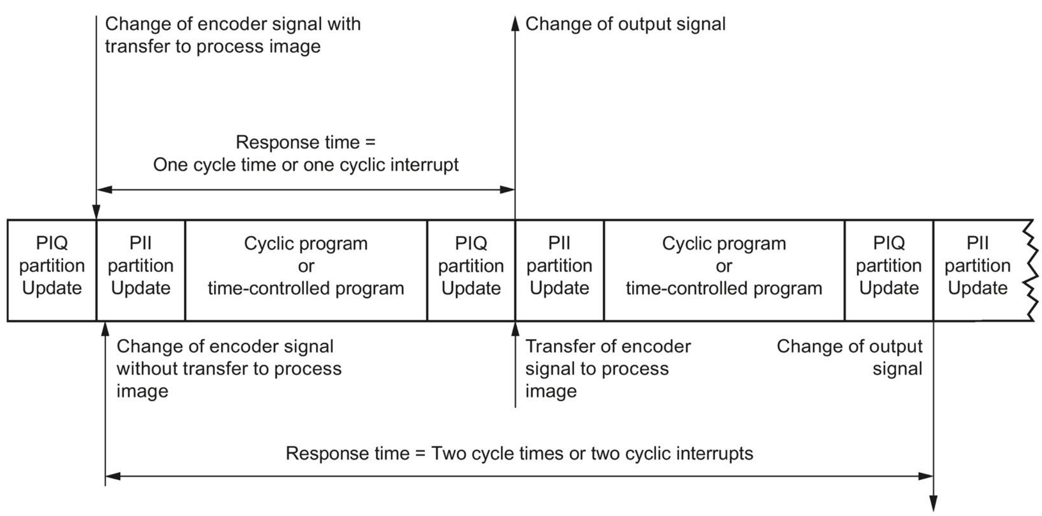


Figure 3-10 Shortest and longest response times of the CPU

Factors

To determine the process response time, you must take account of the following factors in addition to the CPU response time described above:

- Delay of the inputs and outputs on the input/output module
- Switching times of the sensors and actuators used
- Update times for PROFINET IO or DP cycle times on PROFIBUS DP, update time of the backplane bus for ET 200SP CPUs

Delay at the inputs and outputs of the modules

The delay and cycle times can be found in the technical specifications for the input/output modules.

Update times for PROFINET IO and DP cycle times on PROFIBUS DP

When distributed I/O is used, the maximum response time is additionally extended by the bus transmission times of PROFIBUS or PROFINET. These bus transmission times occur during both the reading and output of the process image partitions. The bus transmission times correspond to the bus update cycle of the distributed device.

PROFINET IO

If you use STEP 7 to configure your PROFINET IO system, STEP 7 calculates the update time. To display the update time, follow these steps:

- Select the PROFINET interface of the I/O module.
- In the General tab, select "Advanced options > Real time settings > IO cycle".

The update time is displayed in the "Update time" field and can be set for each IO device.

PROFIBUS DP

If you use STEP 7 to configure your PROFIBUS DP master system, STEP 7 calculates the DP cycle time. To display the DP cycle time, follow these steps:

- Select the PROFIBUS subnet in the network view.
- In the General tab of the Inspector window, navigate to the Bus parameters.

The DP cycle time is displayed in the "Parameters" field at "Typical Ttr".

The following figure illustrates the additional bus runtimes using distributed I/O.

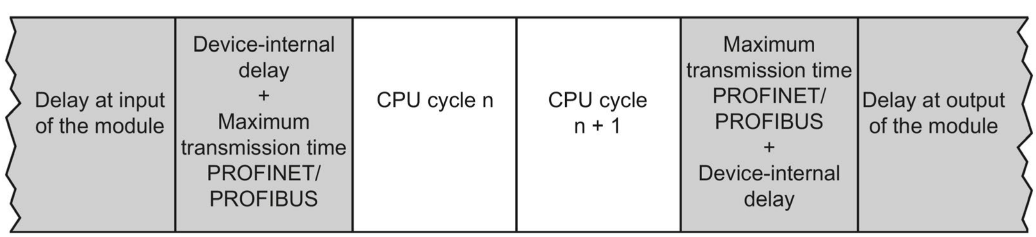


Figure 3-11 Additional bus runtimes with distributed I/O

You can achieve a further optimization of the response times using isochronous mode.

Update time of the backplane bus for ET 200SP CPUs

The following table shows the central (typical) update times of the backplane bus in the ET 200SP CPUs.

Table 3- 6 Update time of the ET 200SP CPUs

Components	Update time of the CPU		
	ET 200SP		
	1510SP(F)-1 PN	1512SP(F)-1 PN	1515SP(F)-PC
Update time for central I/O	250 µs to 1 ms, depending on number and type of central I/O modules[1]		

[1] The duration of the update time depends on the number of the I/O modules and their type (ST, HF, HS). The update time is set at 1 ms for a max. central I/O configuration with standard I/O modules. By using HF I/O modules, for example, and by reducing the number of modules, the update time can be reduced down to 250 µs.

Reference

The following links provide additional information:

- Application example for determining the response time for PROFINET (http://support.automation.siemens.com/WW/view/en/21869080)
- Transmission times and isochronous mode in function manual PROFINET with STEP 7 V13 (http://support.automation.siemens.com/WW/view/en/49948856); see also the section "Tips on assembly"
- Transmission times and isochronous mode in function manual PROFIBUS with STEP 7 V13 (http://support.automation.siemens.com/WW/view/en/59193579); see also the section "Network settings"
- Delays at the input or output of the modules can be found in the manual for the respective device.
- Information on device-internal delays can be found in the manuals for the ET 200MP and ET 200SP distributed I/O systems.

3.5 Summary of response time with cyclic and time-controlled program execution

Estimation of the shortest and longest response time

The following formulas may be used to estimate the shortest and longest response time:

Estimation of the shortest response time

The shortest response time is the sum of:

1 x delay of the input/output module for inputs
+ 1 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for ET 200SP CPUs)
+ 1 x transfer time of the process image input
+ 1 x execution of the user program
+ 1 x transfer time of the process image output
+ 1 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for ET 200SP CPUs)
+ 1 x delay of the input/output module for outputs

= **Shortest response time**

* Time is dependent on the configuration and the extent of the network.

The shortest response time is equivalent to the sum of the cycle time plus the input and output delay times.

Estimation of the longest response time

The longest response time is the sum of:

1 x delay of the input/output module for inputs
+ 2 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for ET 200SP CPUs)
+ 2 x transfer time of the process image input
+ 2 x execution of the user program
+ 2 x transfer time of the process image output
+ 2 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for ET 200SP CPUs)
+ 1 x delay of the input/output module for outputs

= **Longest response time**

* Time is dependent on the configuration and the extent of the network.

The longest response time is equivalent to the sum of twice the cycle time plus the delay times of the inputs and outputs. The longest reaction time includes twice the update time for PROFINET IO or twice the DP cycle time on PROFIBUS DP.

4 Event-driven program execution

4.1 Response time of the CPUs when program execution is event-controlled

Introduction

In order to detect events in the process immediately in the user program and to react to them with an appropriate program, you use hardware interrupts. In STEP 7, organization blocks OB 40 to OB 47 are provided for processing a hardware interrupt. You can create additional hardware interrupts starting with organization block OB 123. The number of available organization blocks depends on the CPU used.

Definition

A hardware interrupt is an interrupt that occurs during the running program execution, due to an interrupt-triggering process event. The operating system calls the assigned interrupt OB; as a result, the execution of the program cycle or of lower priority program parts is interrupted.

Interrupt response times of the CPUs for hardware interrupts

The interrupt response times of the CPUs start with the occurrence of a hardware interrupt event in the CPU and end with the start of the assigned hardware interrupt OB.

This time is subject to system-inherent fluctuations, and this is expressed using a minimum and maximum interrupt response time.

The following table contains the length of the typical response times of the CPUs for hardware interrupts.

Table 4- 1 Response times of the CPUs for hardware interrupts

		S7-1500			
CPU		**1511(F)-1 PN** **1511T-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T-2 PN** **1516(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP ODK**
Interrupt response times	Min.	100 µs	90 µs	30 µs	20 µs
	Max.	400 µs	360 µs	120 µs	90 µs

		ET 200SP		
CPU		1510SP(F)-1 PN	1512SP(F)-1 PN	1515SP(F)-PC
Interrupt response times	Min.	100 µs	100 µs	90 µs
	Max.	400 µs	400 µs	360 µs

		ET 200pro
CPU		1516pro(F)-2 PN
Interrupt response times	Min.	90 µs
	Max.	360 µs

Note that the times are extended if higher-priority interrupts are queued up for execution, and if the hardware interrupt OB is assigned to a process image partition. You can find these times in the 'Extension due to nesting of higher-priority OBs and/or interrupts' table in the section User program execution time (Page 23)

If you need fast interrupt response times, do not assign a process image partition to the hardware interrupt OB and use direct access in the hardware interrupt OB.

You can find additional information on determining response times for PROFINET in the application example with the entry ID 21869080 on the Service&Support (http://support.automation.siemens.com/WW/view/en/21869080) Internet page.

Influence of input modules on the interrupt response times of hardware interrupts

Digital input modules:

Interrupt response time of hardware interrupts = internal interrupt processing time + input delay (see section Technical specifications in the manual)

Analog input modules:

Interrupt response time of hardware interrupts = internal interrupt processing time + conversion time (see section Technical specifications in the manual)

Impact of communication on interrupts

Communication tasks are always processed by the CPU with priority 15. If you do not want the interrupt execution to be delayed or interrupted by communication, configure the interrupt execution with priority > 15. The default setting for interrupt execution is priority 16.

Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2)

You can find information in the section Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2) (Page 29).

4.2 Process response time when program execution is event-driven

When program execution is event-driven, the process response time is determined by the following:

- Delay times of the input and output modules used
- Update times for PROFIBUS/PROFINET for distributed modules; update time of the backplane bus for ET 200SP CPUs
- Interrupt response time of CPU
- Runtimes of the interrupt OB including update of the process image partition

The following figure shows the individual execution steps for event-driven program execution.

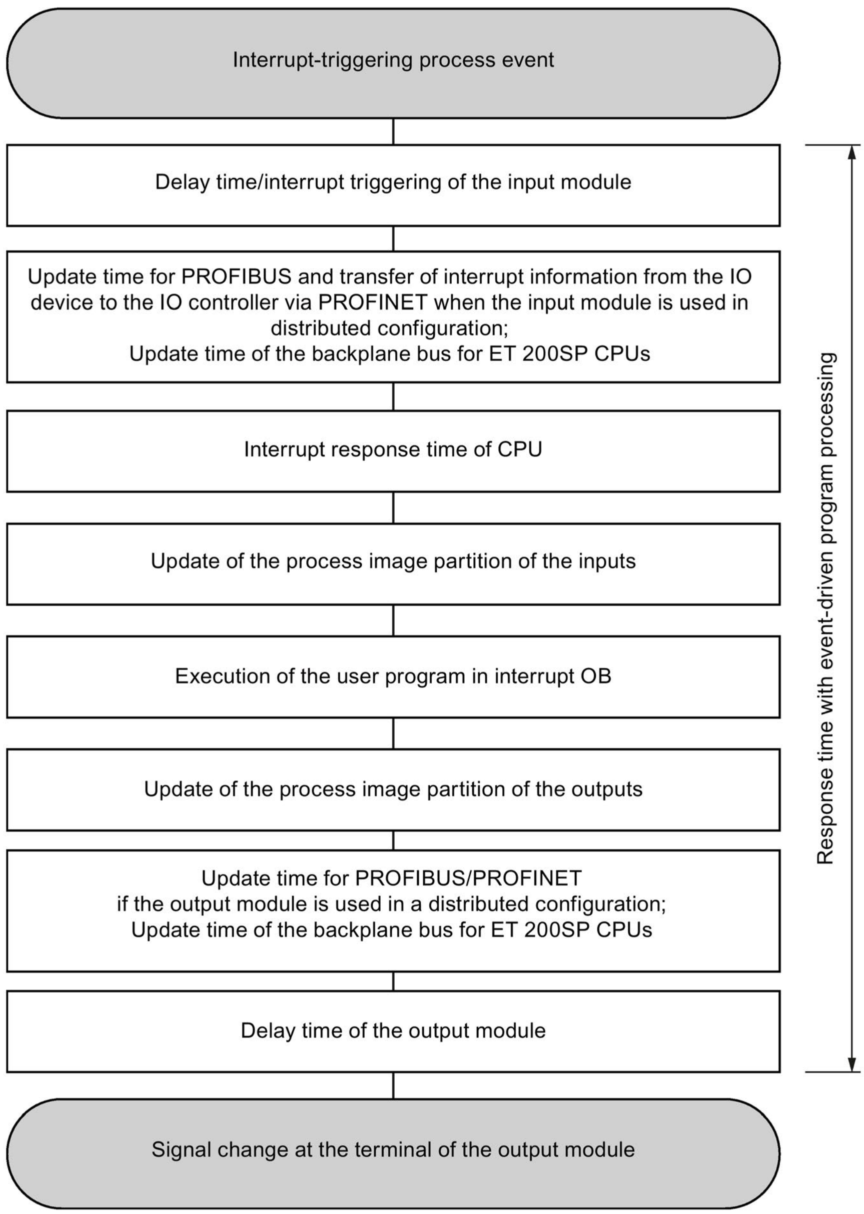


Figure 4-1 Schematic representation of event-driven program execution

Glossary

Automation system

An automation system in the context of SIMATIC S7 is a programmable logic controller.

Cyclic interrupt

A cyclic interrupt is generated periodically by the CPU in a configurable time pattern. At this point in time the corresponding organization block is processed.

Diagnostic interrupt

Diagnostics-capable modules signal detected system errors to the CPU using diagnostic interrupts.

Hardware interrupt

A hardware interrupt is started by interrupt-triggering modules when a specific event occurs in the process. The hardware interrupt is reported to the CPU. The assigned organization block is then processed according to the interrupt priority.

Interrupt

The CPU's operating system distinguishes between various priority classes that control the execution of the user program. These priority classes include interrupts, such as hardware interrupts. When an interrupt occurs, the operating system automatically calls an assigned organization block, in which the user programs the desired response.

Process image

The process image is part of the CPU system memory. At the start of the cyclic program, the signal states of the input modules are transmitted to the process image input. At the end of the cyclic program, the process image output is transmitted as signal state to the output modules.

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