University of Balamand

Keypad Experiment

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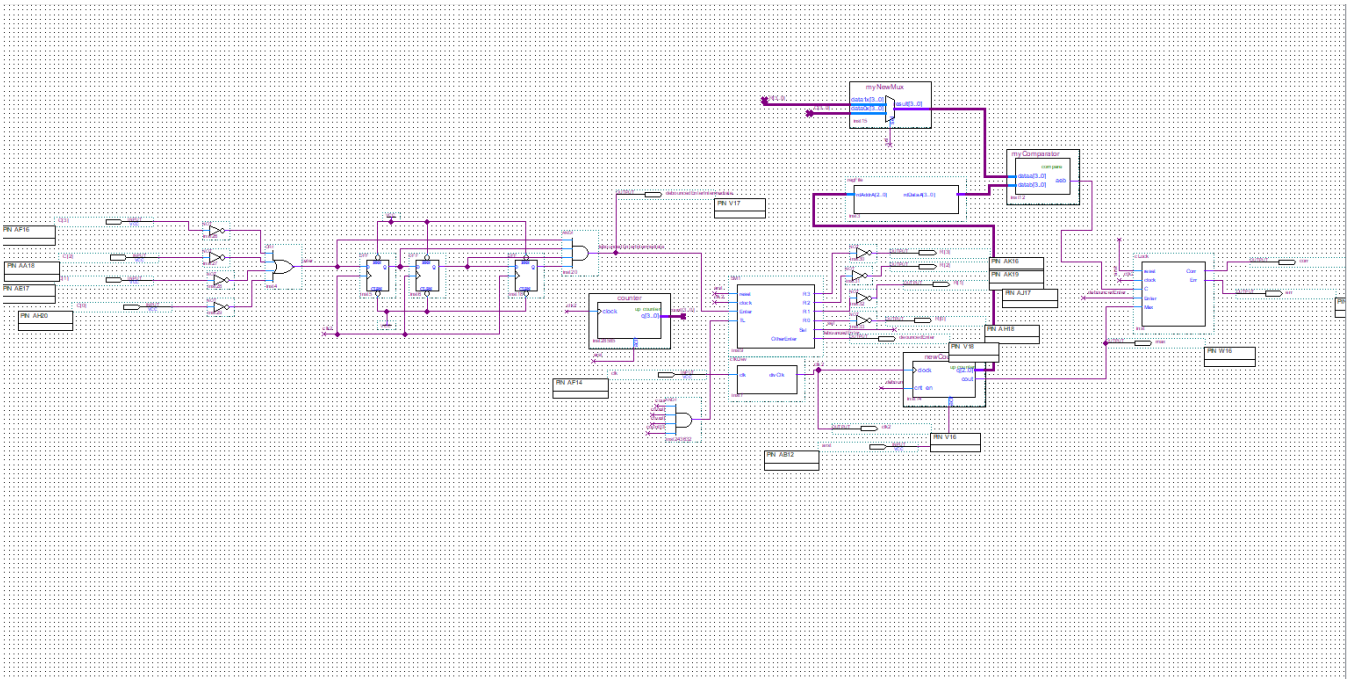
Presented to

Mr. Nassif Daoud

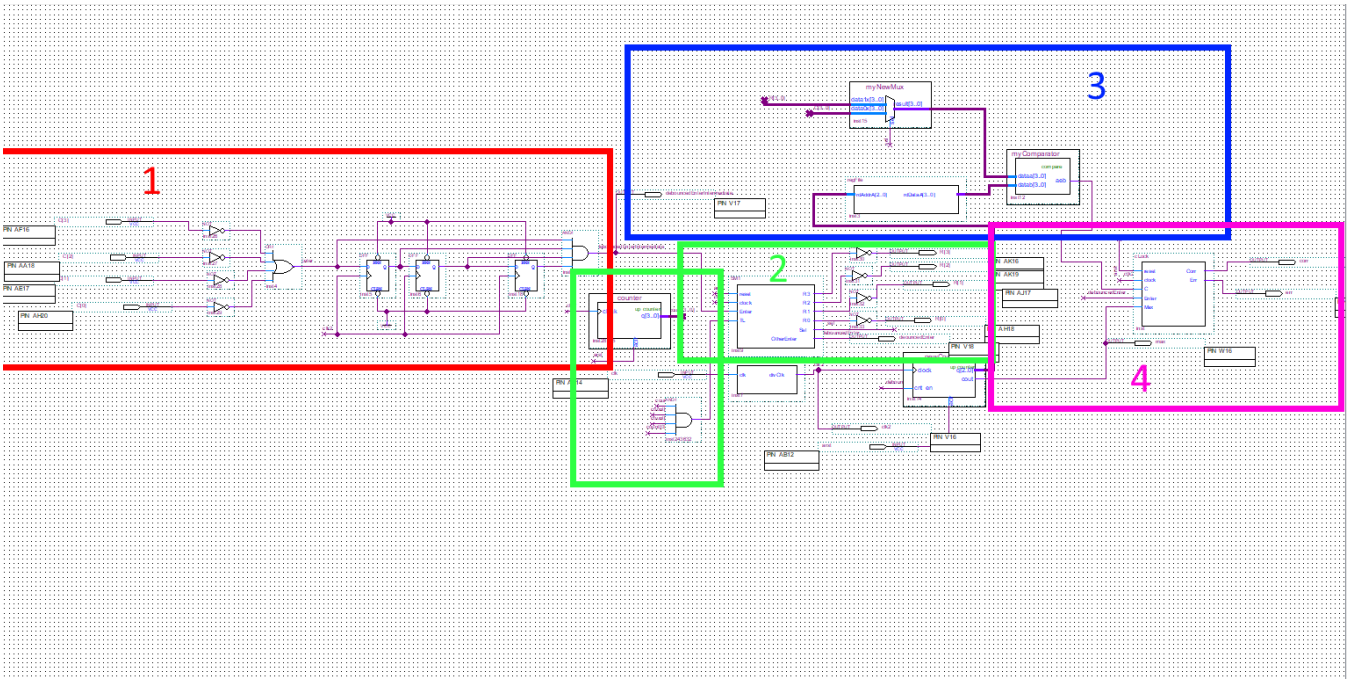
A lab report for the CPEN 202: Logic Lab

Faculty of Engineering

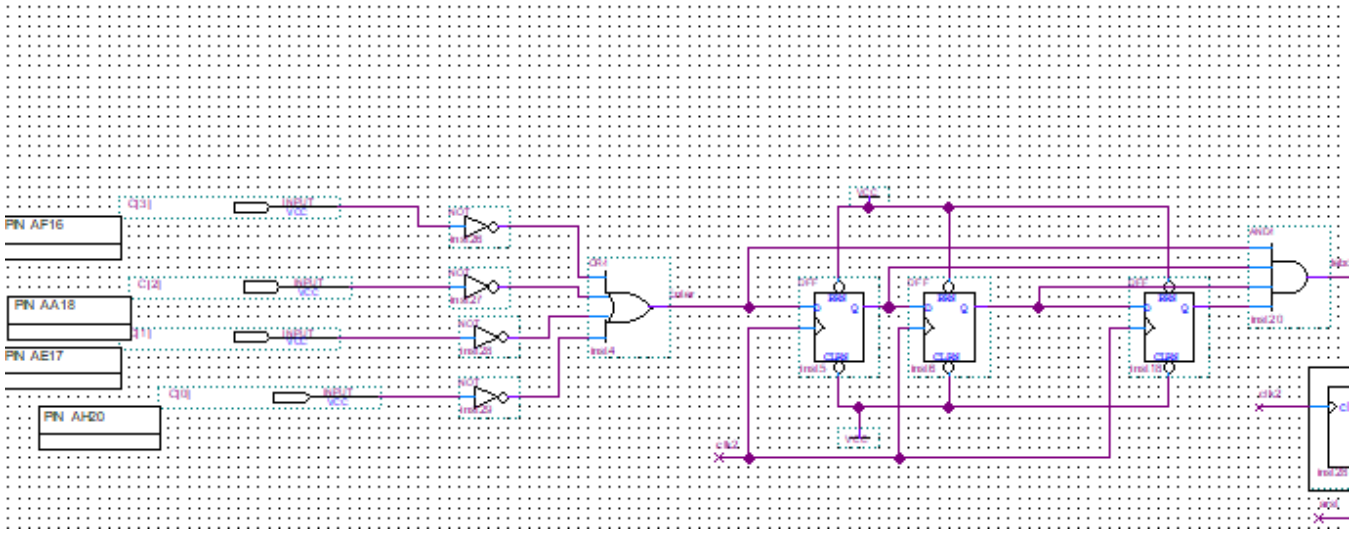


This is the highest level schematic file, it connects all the components we built together. In the next few pages we'll explore them one by one

Parts division:

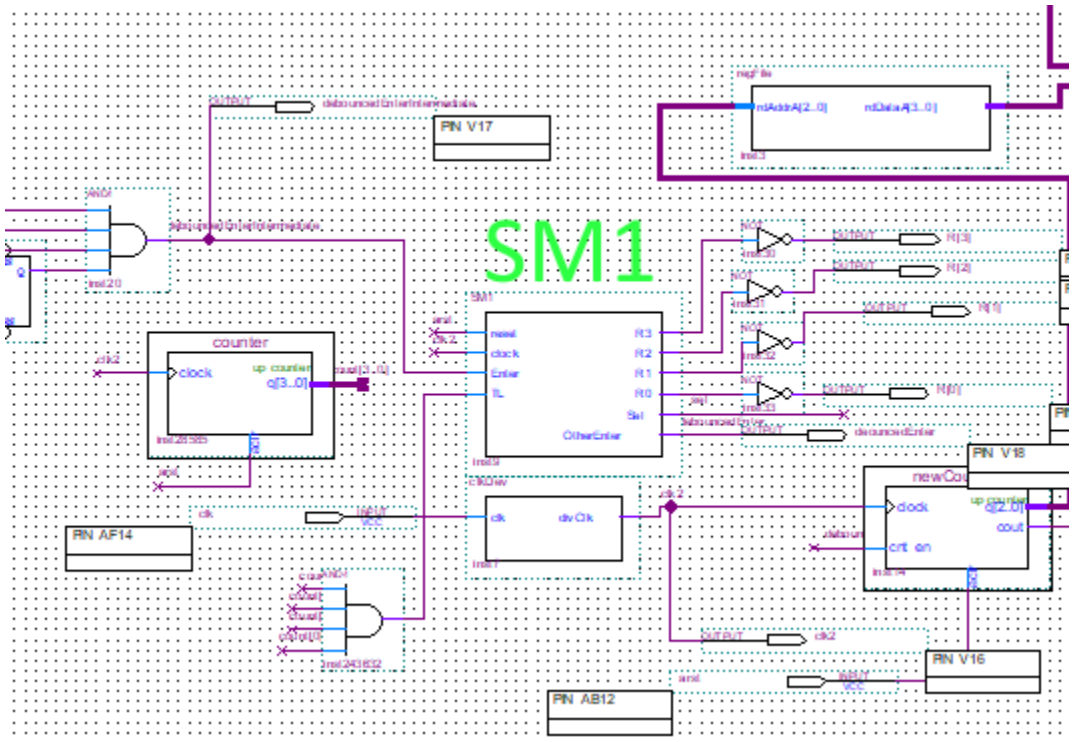


Part 1:

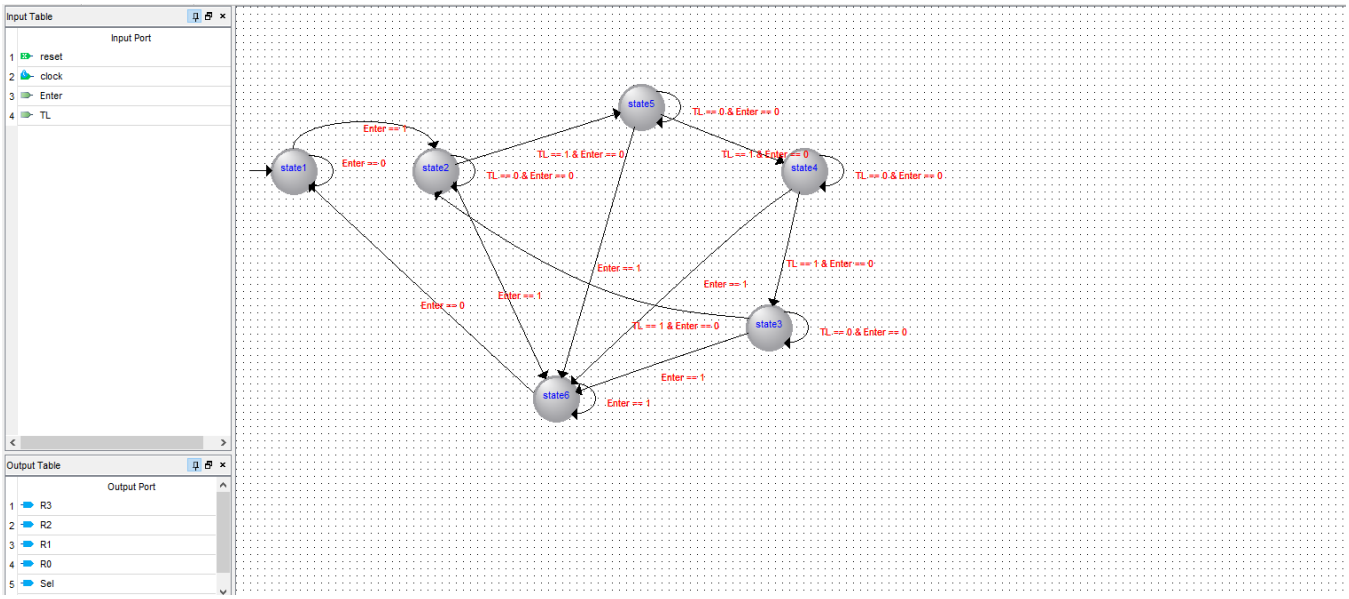


This part detects button presses and denounces them.

Part 2

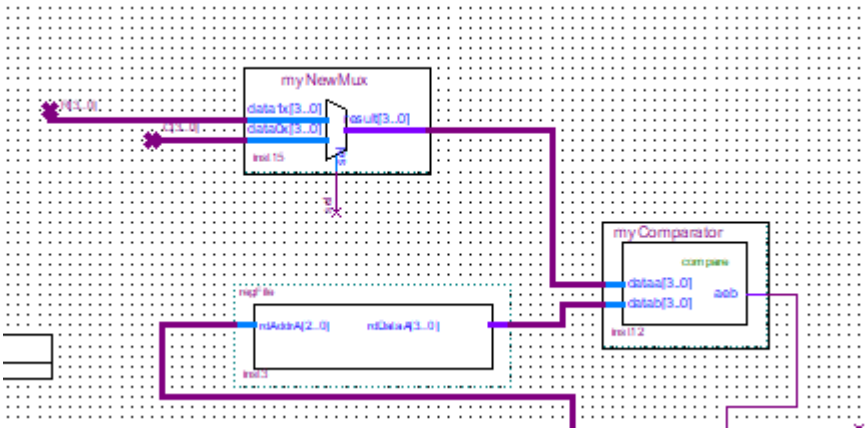


This part takes the debounced enter and TL of a counter that counts up to TL to generate the output columns, and a one-pulse enter for every button press for the rest of the circuit. SM1 internally looks like this:



In state 1, all row outputs are 1. After that, it rotates between states 2-3-4-5, sending a one only to one row at a time, until it sees an enter = 1 again(correct row is found), then it sits in state 6 until that button is released so as not to treat a long button press as multiple button presses. In each state it waits at least one TL(generated by a simple LPM counter) to make sure that the enter has the time to be debounced.

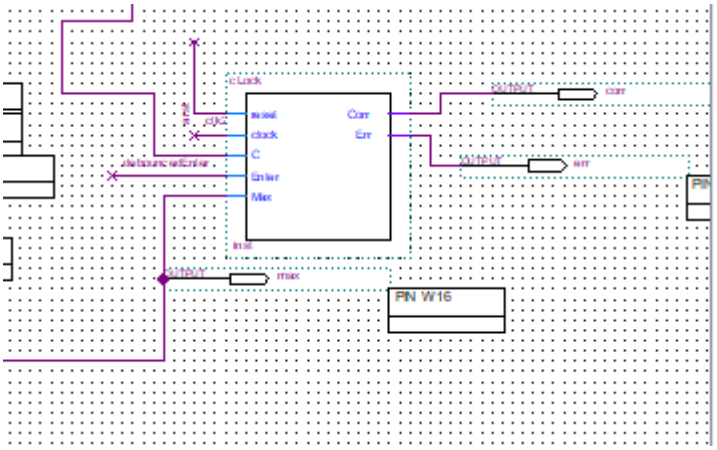
Part 3



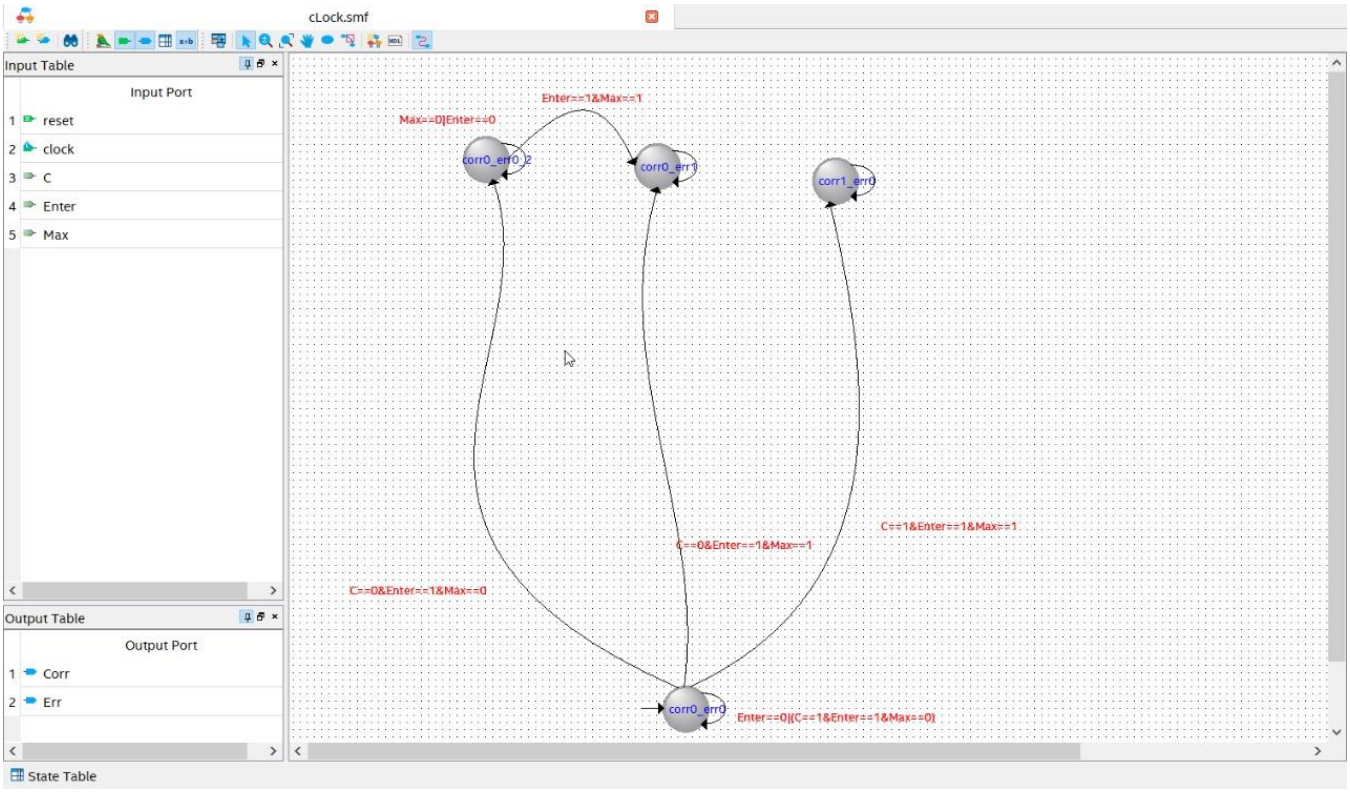
The password(rows and columns) is stored in the register file. It sends data to the comparator to be compared to the input data(row/col) chosen by a mux, with a select line determined by SM1. The register file's read address is given by counter that increments by 1 every detected enter. The mux is the default one found in altera, the register file is custom built/written in system verilog.

```
1   module regFile ( input logic [2:0] rdAddrA,
2                    output logic [3:0] rdDataA );
3
4     logic [3:0] regFile[0:7];
5
6     always_comb
7     begin
8     regFile[0] = 4'b0111;
9     regFile[1] = 4'b0111;
10    regFile[2] = 4'b0111;
11    regFile[3] = 4'b1011;
12    regFile[4] = 4'b0111;
13    regFile[5] = 4'b1101;
14    regFile[6] = 4'b0111;
15    regFile[7] = 4'b1110;
16    end
17
18    assign rdDataA = regFile[rdAddrA];
19
20  endmodule
```

Part 4



Part 4 is unchanged from the last experiment (combinational lock). It is the same state machine.


cLock.smf
Input Table
Input Port
1 reset
2 clock
3 C
4 Enter
5 Max
Output Table
Output Port
1 Corr
2 Err
State Table
Enter==1&Max==1
Max==0|Enter==0
corr0_err0_2
corr0_err1
corr1_err0
C==1&Enter==1&Max==1
C==0&Enter==1&Max==1
C==0&Enter==1&Max==0
corr0_err0
Enter==0||(C==1&Enter==1&Max==0)