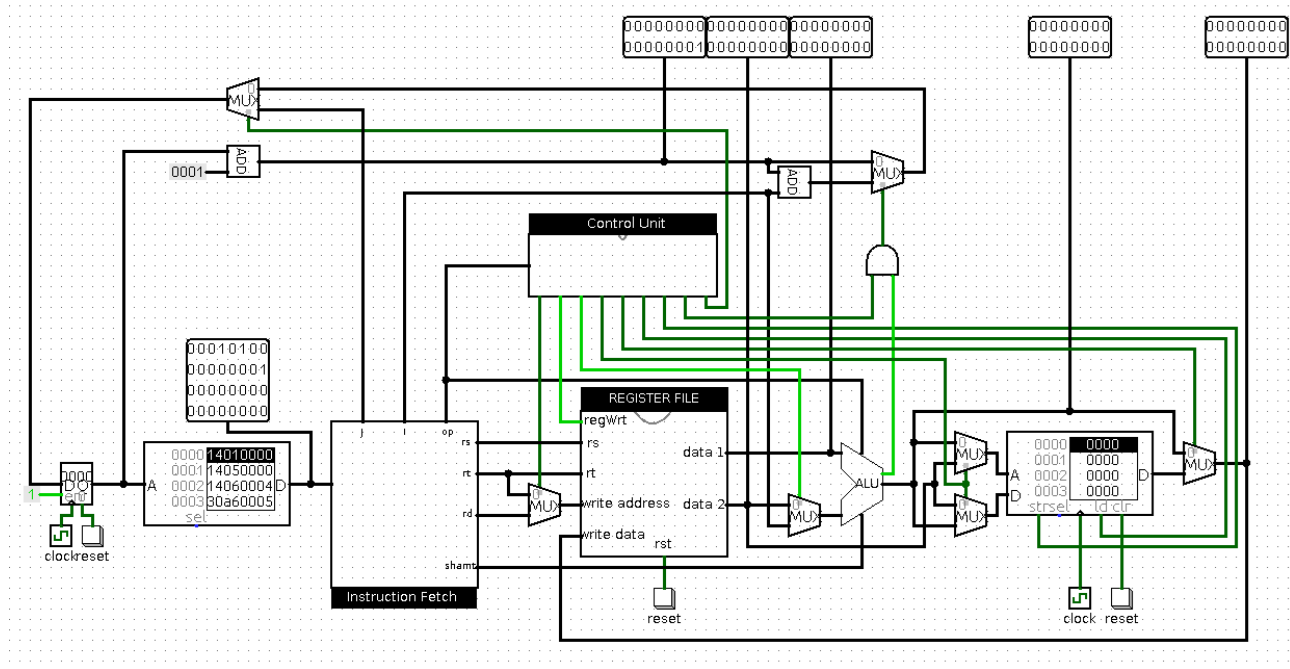# COMP 303 TERM PROJECT REPORT

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Figure: 16-Bit Single Cycle Processor Schematic

Instruction Memory & Instruction Fetch

In this project, we designed a single cycle 16-bit processor. Initially, we used ROM Block of "Logisim" to represent "Instruction Memory". As it can be seen above, "Instruction Fetch" block is placed right of the "Instruction Memory". "Instruction Fetch" ensures that 32 bit instruction is split into "op", "rs", "rt", "rd", "shamt", "func", "Immediate", and "Jump Address". After an instruction is fetched, "rs", "rt" and "rd" parts goes into "Register File".
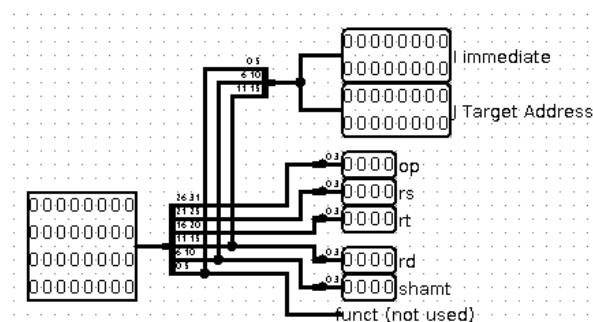
Figure: Instruction Fetch
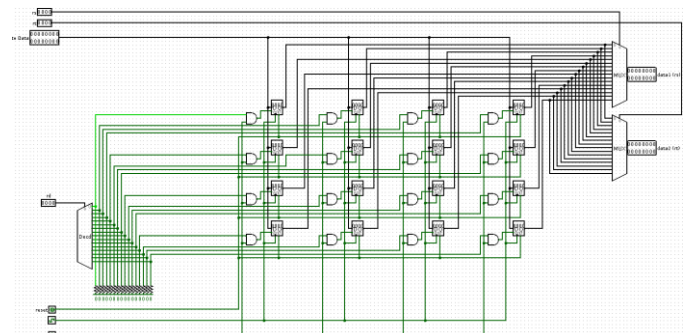
Figure: Register File

Register File

In "Register File", there are 16 registers to hold data in CPU and they are open to write or read operation for only specific "rs" and "rt". "rs" and "rt" represents address bits of register. Since there are 16 registers, we have only used least significant 4 bits of "rs", "rt" and "rd". "rd" works to determine where to write calculated data in register file. "Write data" collects data to be written in registers from ALU or memory(we used RAM Block). "Data 1" and "Data 2" pins represent the data which come from registers that are selected by "rs" and "rt". "regWrite" is a control signal to control whether a data is to be written in register file or not.
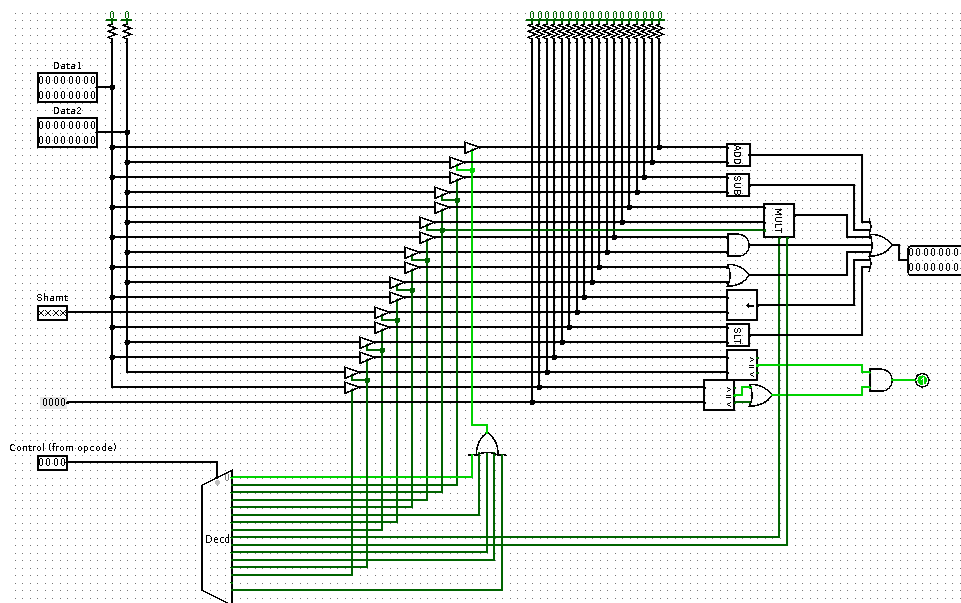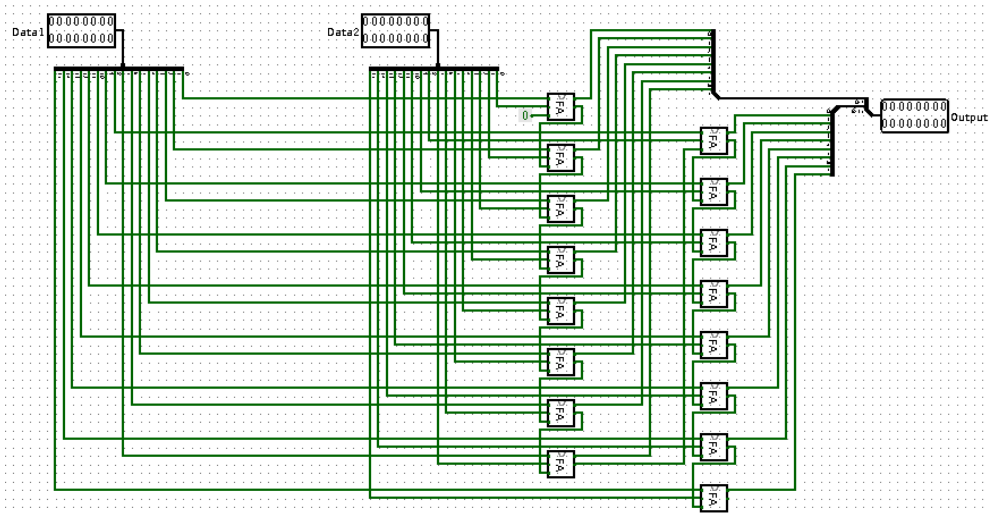

Figure: Arithmetic Logic Unit

ALU

ALU (Arithmetic Logic Unit) takes 4 input signals which are "Data1", "Data2", "shamt" and "op". In ALU there are several arithmetic operations (i.e. addition, multiplication, …). "op" code selects which operation will be done by using a decoder. "Data1" and "Data2" are 16-bits data coming from register file or one of them from "Immediate" and they are will be entered into operation by ALU. On "Data2" branch, there is a multiplexer which is controlled by Control Unit to determine if it is a R-Type or I-Type operation. According to the type of operation "shamt" represents shift amount. Since ALU has a shift operation, "shamt" is used to shift "rs". There is also "zero" output from ALU to indicate whether "Data1" and "Data2" are equal or not or "less than".

Memory

Memory is designed by placing RAM into circuit. That is because RAM have read and write option which we desired for memory. Computed data in ALU enters Address pin of RAM to determine which word will be read or written in memory. "rt" enters "data" pin of RAM to determine which data will be written in memory. At the output of memory, read data is placed, but

there is a multiplexer at the end of memory in order to determine if ALU result or RAM result will be written into register file.

Figure: Control Unit

Control Unit

Control unit is used to determine select bits of all multiplexers in the circuit to achieve correct operation. Operation can be arithmetic, load, read, branch or unconditional branch.

Figure: 16 Bit Adder (Consists of 16 Full Adder Blocks)

PC (Program Counter)

Except Jump and branch operations, PC is incremented by 1 byte in each cycle. For conditional branch operations, a control unit signal and "zero" is "ANDed" and controls a multiplexer to select PC + 1 or branch. After this selection, a multiplexer is placed to select whether it is a unconditional branch operation or not.

Custom Instruction

adds rt, rs, Immediate

We need two instructions when we wish add a constant to a register's value, then store it into memory. By using new custom instruction "adds", user will be able to do this operation by one instruction. To do this, We placed two multiplexers between ALU and RAM to determine Address and Data ports of RAM. Operation can be simply described by addition of "rs" and "Immediate" will be written in memory's "rt"th slot.