Design Rules Verification Report

Filename : C:\Users\Hitech95\Documents\Altium\Projects\diyBMS\board.PcbDoc

Warnings 0
Rule Violations 4

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.229mm) (InNet('VCC')),(InNet('GND'))	0
Clearance Constraint (Gap=0.203mm) (All),(All)	0
Clearance Constraint (Gap=0.229mm) (InNet('BAT_POS')),(InNet('GND'))	0
Clearance Constraint (Gap=0.254mm) ((InNet('NetJ1_3') OR InNet('NetJ1_4'))),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=5.08mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.076mm) (All)	0
Hole Size Constraint (Min=0.2mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.152mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.152mm) (IsPad),(All)	2
Silk to Silk (Clearance=0.152mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	4

Silk To Solder Mask (Clearance=0.152mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.152mm) Between Pad Free-M2(2.75mm,47.25mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.152mm) Between Pad Free-M2(2.75mm,47.25mm) on Multi-Layer And Track

Silk to Silk (Clearance=0.152mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.152mm) Between Text "HOT" (25.8mm,0.5mm) on Top Overlay And Text "SURFACE!"
Silk To Silk Clearance Constraint: (Collision < 0.152mm) Between Text "U2" (20.5mm,45.7mm) on Top Overlay And Track