YijieBai

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Education Experience:

Northwestern University (NU), Evanston **09/2012-Present**

- Teaching Assistant for Advanced Digital Logic Design(EECS303) **09/2013-Present**
- Candidate for 2014 *Master of Science* in *Computer Engineering (March),* GPA: 3.87/4.0
- *Coursework:* Advanced Digital Logic Design, Computer Architecture, VLSI systems design, Intro to parallel computing, ASIC and FPGA Design, Parallel Architecture, Embedded system design, Concurrent programming

BeiHang University (BUAA), Beijing **08/2008-06/2012**

- *Bachelor of* Engineering in Software Engineering
- *Coursework:* Operating System 89, Embedded System 92, Computer Network 86, Algorithm 81

Technical Skills:

- Programming Language: *C(with MPI and LPT library)(preferred language)/C++ ,Python(daily use when doing data processing), VHDL(preferred Hardware Description Language), JAVA, Verilog.*
- Software environment: *Cadence, MGC(Mentor Graphics), Linux/Unix environment, Mac OSX, Altera FPGA, Modelsim simulator. Familiar with Gem5 simulator and SingleScalar Simulator.*
- Embedded System: Experienced in MCU51 Series, Familiar with ARM Architecture
- Language: Native in *Mandarin*; Fluent in *English*

Awards:

Creative Extracurricular Science and Technology Scholarship, *College of Software,BUAA* **Dec, 2011**
Third Prize, *Scholarship Award for outstanding science and technology competition, BUAA* **Nov, 2011**
Second Prize, *"Fengru Cup"Academic Science and Technology Competition***,** *BUAA* **Apr, 2011**
Best Volunteer Award*, Volunteer Division of College of Software, BUAA* **Nov, 2009**

Research & Professional Experience:

Individual project, *Android power model analysis,* **NU** microarchitecture lab **03/2013-09/2013**

- Continue Jamlogger project. Modify the old data sampling app in the new android platform and collect data from power monitor, which is a platform used to record the cell phone power consumption. Sink the data from both side together and create a new power model for newest version of Android platform.

Group leader, *8bit full functional calculator using Cadence Virtuoso,* NU **01/2013-03/2013**

- It is a team final project with one another student for course VLSI design and analysis (EECS391). In this project, we are asked to design an 8bit calculator that can do addition, subtraction, multiplication and division. After using Cadence Virtuoso for a quarter, finishing other smaller component, we finish this project successfully and I am also been graded A in this course.

Group Leader*, Dual-Tank Video Game Using Altera Quartus FPGA,* NU **01/2013-03.2013**

- It is a Team final Project for Course EECS355 ASIC and FPGA Design. In that class, I have learned a lot about VHDL and how to use VHDL properly and efficiently on selected FPGA board. The final project is a team project that require us to implement a dual tank game using several models in FPGA, including VGA part, keyboard input part etc. I take responsible to main control part associate with keyboard input part. And also help my teammate accommodate the VGA part. After four weeks' hard work, we finally fulfill all the requirements for this project.

Group leader, *32bit single-cycle processor using MIPS instruction set,* NU **09/2012-12/2012**

- It is a team final project with two other students for course Computer Architecture (EECS361). In this project, we are asked to design a single-cycle processor using MIPS ISA that can process 32-bit number shift-left-logic, logic AND, OR, Addition, Subtraction, conditional branch, from the instruction fetch phase till the end (data write phase). The CAD tool is MGC from Mentor Graphics.

Extracurricular Activities and others:

Vice President, *Student Union ofCollege of Software,* BUAA **07/2010-07/2011**

- *Sports Meeting*, **College of Software, BUAA**, Organizer, Field Management for Closing ceremony

Chairman, Volunteer Division of *College of Software,* BUAA **09/2008-09/2010**