AR0833 Register Reference, Rev. C

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

AR0833 Register Reference

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Introduction

This reference document describes the AR0833 registers. Summary and detailed information are presented in separate sections:

- "Register Summary" on page 5
- "Register Descriptions" on page 33

Note: Throughout this document, Green1 to corresponds to greenR; green2 corresponds to greenB.

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the AR0833 data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to "1."

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Register Summary

SMIA Configuration Register List and Default Values

Table 1: SMIA Configuration Register List and Default Values
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R0 (R0x0000)	chip_version_reg	dddd dddd dddd dddd	19203 (0x4B03)
R2 (R0x0002)	revision_number	???? ????	0 (0x00)
R3 (R0x0003)	manufacturer_id	???? ????	6 (0x06)
R4 (R0x0004)	smia_version	???? ????	10 (0x0A)
R5 (R0x0005)	frame_count	???? ????	255 (0xFF)
R6 (R0x0006)	pixel_order	0000 00??	1 (0x01)
R8 (R0x0008)	data_pedestal	0000 00dd dddd dddd	42 (0x002A)
R128 (R0x0080)	analogue_gain_capability	???? ???? ???? ????	1 (0x0001)
R132 (R0x0084)	analogue_gain_code_min	???? ???? ???? ????	1 (0x0001)
R134 (R0x0086)	analogue_gain_code_max	???? ???? ???? ????	32 (0x0020)
R136 (R0x0088)	analogue_gain_code_step	???? ???? ???? ????	1 (0x0001)
R138 (R0x008A)	analogue_gain_type	???? ???? ???? ????	0 (0x0000)
R140 (R0x008C)	analogue_gain_m0	???? ???? ???? ????	1 (0x0001)
R142 (R0x008E)	analogue_gain_c0	???? ???? ???? ????	0 (0x0000)
R144 (R0x0090)	analogue_gain_m1	???? ???? ???? ????	0 (0x0000)
R146 (R0x0092)	analogue_gain_c1	???? ???? ???? ????	1 (0x0001)
R192 (R0x00C0)	data_format_model_type	???? ????	1 (0x01)
R193 (R0x00C1)	data_format_model_subtype	???? ????	5 (0x05)
R194 (R0x00C2)	data_format_descriptor_0	???? ???? ???? ????	2570 (0x0A0A)
R196 (R0x00C4)	data_format_descriptor_1	???? ???? ???? ????	2056 (0x0808)
R198 (R0x00C6)	data_format_descriptor_2	???? ???? ???? ????	2568 (0x0A08)
R200 (R0x00C8)	data_format_descriptor_3	???? ???? ???? ????	2566 (0x0A06)

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Table 1: SMIA Configuration Register List and Default Values (continued)
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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R202 (R0x00CA)	data_format_descriptor_4	???? ???? ???? ????	0 (0x0000)
R204 (R0x00CC)	data_format_descriptor_5	???? ???? ???? ????	0 (0x0000)
R206 (R0x00CE)	data_format_descriptor_6	???? ???? ???? ????	0 (0x0000)
R256 (R0x0100)	mode_select	0000 000d	0 (0x00)
R257 (R0x0101)	image_orientation	0000 00dd	1 (0x01)
R259 (R0x0103)	software_reset	0000 000d	0 (0x00)
R260 (R0x0104)	grouped_parameter_hold	0000 000d	0 (0x00)
R261 (R0x0105)	mask_corrupted_frames	0000 000d	0 (0x00)
R272 (R0x0110)	ccp2_channel_mode	0000 0ddd	0 (0x00)
R273 (R0x0111)	ccp2_signalling_mode	0000 000d	1 (0x01)
R274 (R0x0112)	ccp_data_format	0000 dddd 0000 dddd	2570 (0x0A0A)
R288 (R0x0120)	gain_mode	0000 000d	0 (0x00)
R514 (R0x0202)	coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
R516 (R0x0204)	analogue_gain_code_global	0000 0000 00dd dddd	2 (0x0002)
R518 (R0x0206)	analogue_gain_code_greenr	0000 0000 00dd dddd	2 (0x0002)
R520 (R0x0208)	analogue_gain_code_red	0000 0000 00dd dddd	2 (0x0002)
R522 (R0x020A)	analogue_gain_code_blue	0000 0000 00dd dddd	2 (0x0002)
R524 (R0x020C)	analogue_gain_code_greenb	0000 0000 00dd dddd	2 (0x0002)
R526 (R0x020E)	digital_gain_greenr	0000 dddd dddd ddd0	256 (0x0100)
R528 (R0x0210)	digital_gain_red	0000 dddd dddd ddd0	256 (0x0100)
R530 (R0x0212)	digital_gain_blue	0000 dddd dddd ddd0	256 (0x0100)
R532 (R0x0214)	digital_gain_greenb	0000 dddd dddd ddd0	256 (0x0100)
R768 (R0x0300)	vt_pix_clk_div	0000 0000 000d dddd	5 (0x0005)
R770 (R0x0302)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)

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Table 1: SMIA Configuration Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R772 (R0x0304)	pre_pll_clk_div	0000 0000 00dd dddd	2 (0x0002)
R774 (R0x0306)	pll_multiplier	0000 0000 dddd dddd	64 (0x0040)
R776 (R0x0308)	op_pix_clk_div	0000 0000 000d dddd	10 (0x000A)
R778 (R0x030A)	op_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R832 (R0x0340)	frame_length_lines	dddd dddd dddd dddd	2561 (0x0A01)
R834 (R0x0342)	line_length_pck	dddd dddd dddd dddd	3944 (0x0F68)
R836 (R0x0344)	x_addr_start	0000 dddd dddd dddd	8 (0x0008)
R838 (R0x0346)	y_addr_start	0000 dddd dddd dddd	8 (0x0008)
R840 (R0x0348)	x_addr_end	0000 dddd dddd dddd	3271 (0x0CC7)
R842 (R0x034A)	y_addr_end	0000 dddd dddd dddd	2455 (0x0997)
R844 (R0x034C)	x_output_size	0000 dddd dddd dddd	3264 (0x0CC0)
R846 (R0x034E)	y_output_size	0000 dddd dddd dddd	2448 (0x0990)
R896 (R0x0380)	x_even_inc	???? ???? ???? ????	1 (0x0001)
R898 (R0x0382)	x_odd_inc	dddd dddd dddd dddd	1 (0x0001)
R900 (R0x0384)	y_even_inc	???? ???? ???? ????	1 (0x0001)
R902 (R0x0386)	y_odd_inc	dddd dddd dddd dddd	1 (0x0001)
R1024 (R0x0400)	scaling_mode	0000 0000 0000 00dd	0 (0x0000)
R1026 (R0x0402)	spatial_sampling	0000 0000 0000 000d	0 (0x0000)
R1028 (R0x0404)	scale_m	0000 0000 0ddd dddd	16 (0x0010)
R1030 (R0x0406)	scale_n	0000 0000 0??? ????	16 (0x0010)
R1280 (R0x0500)	compression_mode	0000 0000 0000 000?	1 (0x0001)
R1536 (R0x0600)	test_pattern_mode	0000 00dd 0000 0ddd	0 (0x0000)
R1538 (R0x0602)	test_data_red	0000 00dd dddd dddd	0 (0x0000)
R1540 (R0x0604)	test_data_greenr	0000 00dd dddd dddd	0 (0x0000)

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Table 1: SMIA Configuration Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R1542 (R0x0606)	test_data_blue	0000 00dd dddd dddd	0 (0x0000)
R1544 (R0x0608)	test_data_greenb	0000 00dd dddd dddd	0 (0x0000)

SMIA Parameter Limits Register List and Default Values

Table 2: SMIA Parameter Limits Register List and Default Values
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R4096 (R0x1000)	integration_time_capability	0000 0000 0000 000?	1 (0x0001)
R4100 (R0x1004)	coarse_integration_time_min	dddd dddd dddd dddd	0 (0x0000)
R4102 (R0x1006)	coarse_integration_time_max_margin	dddd dddd dddd dddd	1 (0x0001)
R4224 (R0x1080)	digital_gain_capability	0000 0000 0000 000?	1 (0x0001)
R4228 (R0x1084)	digital_gain_min	???? ???? ???? ????	2 (0x0002)
R4230 (R0x1086)	digital_gain_max	???? ???? ???? ????	4094 (0x0FFE)
R4232 (R0x1088)	digital_gain_step_size	???? ???? ???? ????	2 (0x0002)
R4352 (R0x1100)	min_ext_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1073741824 (0x40000000)
R4356 (R0x1104)	max_ext_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1115684864 (0x42800000)
R4360 (R0x1108)	min_pre_pll_clk_div	???? ???? ???? ????	1 (0x0001)
R4362 (R0x110A)	max_pre_pll_clk_div	???? ???? ???? ????	64 (0x0040)
R4364 (R0x110C)	min_pll_ip_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1073741824 (0x40000000)
R4368 (R0x1110)	max_pll_ip_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1103101952 (0x41C00000)
R4372 (R0x1114)	min_pll_multiplier	???? ???? ???? ????	32 (0x0020)
R4374 (R0x1116)	max_pll_multiplier	???? ???? ???? ????	384 (0x0180)
R4376 (R0x1118)	min_pll_op_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1136656384 (0x43C00000)
R4380 (R0x111C)	max_pll_op_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1145044992 (0x44400000)
R4384 (R0x1120)	min_vt_sys_clk_div	???? ???? ???? ????	1 (0x0001)

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Table 2: SMIA Parameter Limits Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R4386 (R0x1122)	max_vt_sys_clk_div	???? ???? ???? ????	16 (0x0010)
R4388 (R0x1124)	min_vt_sys_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1103101952 (0x41C00000)
R4392 (R0x1128)	max_vt_sys_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1103101952 (0x41C00000)
R4396 (R0x112C)	min_vt_pix_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1083808154 (0x4099999A)
R4400 (R0x1130)	max_vt_pix_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1130102784 (0x435C0000)
R4404 (R0x1134)	min_vt_pix_clk_div	???? ???? ???? ????	4 (0x0004)
R4406 (R0x1136)	max_vt_pix_clk_div	???? ???? ???? ????	16 (0x0010)
R4416 (R0x1140)	min_frame_length_lines	dddd dddd dddd dddd	115 (0x0073)
R4418 (R0x1142)	max_frame_length_lines	dddd dddd dddd dddd	65535 (0xFFFF)
R4420 (R0x1144)	min_line_length_pck	dddd dddd dddd dddd	3736 (0x0E98)
R4422 (R0x1146)	max_line_length_pck	dddd dddd dddd dddd	65532 (0xFFFC)
R4424 (R0x1148)	min_line_blanking_pck	dddd dddd dddd dddd	252 (0x00FC)
R4426 (R0x114A)	min_frame_blanking_lines	dddd dddd dddd dddd	113 (0x0071)
R4448 (R0x1160)	min_op_sys_clk_div	???? ???? ???? ????	1 (0x0001)
R4450 (R0x1162)	max_op_sys_clk_div	???? ???? ???? ????	16 (0x0010)
R4452 (R0x1164)	min_op_sys_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1103101952 (0x41C00000)
R4456 (R0x1168)	max_op_sys_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1148846080 (0x447A0000)
R4460 (R0x116C)	min_op_pix_clk_div	???? ???? ???? ????	8 (0x0008)
R4462 (R0x116E)	max_op_pix_clk_div	???? ???? ???? ????	10 (0x000A)
R4464 (R0x1170)	min_op_pix_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1075419546 (0x4019999A)
R4468 (R0x1174)	max_op_pix_clk_freq_mhz	???? ???? ???? ???? ???? ???? ???? ????	1120403456 (0x42C80000)
R4480 (R0x1180)	x_addr_min	???? ???? ???? ????	0 (0x0000)
R4482 (R0x1182)	y_addr_min	???? ???? ???? ????	0 (0x0000)
R4484 (R0x1184)	x_addr_max	???? ???? ???? ????	3279 (0x0CCF)

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Table 2: SMIA Parameter Limits Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R4486 (R0x1186)	y_addr_max	???? ???? ???? ????	2463 (0x099F)
R4544 (R0x11C0)	min_even_inc	???? ???? ???? ????	1 (0x0001)
R4546 (R0x11C2)	max_even_inc	???? ???? ???? ????	1 (0x0001)
R4548 (R0x11C4)	min_odd_inc	???? ???? ???? ????	1 (0x0001)
R4550 (R0x11C6)	max_odd_inc	???? ???? ???? ????	7 (0x0007)
R4608 (R0x1200)	scaling_capability	0000 0000 0000 00??	2 (0x0002)
R4612 (R0x1204)	scaler_m_min	???? ???? ???? ????	16 (0x0010)
R4614 (R0x1206)	scaler_m_max	???? ???? ???? ????	100 (0x0064)
R4616 (R0x1208)	scaler_n_min	???? ???? ???? ????	16 (0x0010)
R4618 (R0x120A)	scaler_n_max	???? ???? ???? ????	16 (0x0010)
R4864 (R0x1300)	compression_capability	0000 0000 0000 000?	1 (0x0001)
R5120 (R0x1400)	matrix_element_redinred	dddd dddd dddd dddd	578 (0x0242)
R5122 (R0x1402)	matrix_element_greeninred	dddd dddd dddd dddd	65280 (0xFF00)
R5124 (R0x1404)	matrix_element_blueinred	dddd dddd dddd dddd	65470 (0xFFBE)
R5126 (R0x1406)	matrix_element_redingreen	dddd dddd dddd dddd	65460 (0xFFB4)
R5128 (R0x1408)	matrix_element_greeningreen	dddd dddd dddd dddd	512 (0x0200)
R5130 (R0x140A)	matrix_element_blueingreen	dddd dddd dddd dddd	65357 (0xFF4D)
R5132 (R0x140C)	matrix_element_redinblue	dddd dddd dddd dddd	65521 (0xFFF1)
R5134 (R0x140E)	matrix_element_greeninblue	dddd dddd dddd dddd	65332 (0xFF34)
R5136 (R0x1410)	matrix_element_blueinblue	dddd dddd dddd dddd	476 (0x01DC)

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Manufacturer Specific Register List and Default Values

Table 3: Manufacturer Specific Register List and Default Values
1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	model_id_	dddd dddd dddd dddd	19203 (0x4B03)
R12290 (R0x3002)	y_addr_start_	0000 dddd dddd dddd	8 (0x0008)
R12292 (R0x3004)	x_addr_start_	0000 dddd dddd dddd	8 (0x0008)
R12294 (R0x3006)	y_addr_end_	0000 dddd dddd dddd	2455 (0x0997)
R12296 (R0x3008)	x_addr_end_	0000 dddd dddd dddd	3271 (0x0CC7)
R12298 (R0x300A)	frame_length_line_	dddd dddd dddd dddd	2561 (0x0A01)
R12300 (R0x300C)	line_length_pck_	dddd dddd dddd dddd	3736 (0x0E98)
R12306 (R0x3012)	coarse_integration_time_	dddd dddd dddd dddd	16 (0x0010)
R12310 (R0x3016)	row_speed	0000 0ddd 0ddd 0ddd	273 (0x0111)
R12312 (R0x3018)	extra_delay	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	dddd dddd dddd dddd	24 (0x0018)
R12316 (R0x301C)	mode_select_	0000 000d	0 (0x00)
R12317 (R0x301D)	image_orientation_	0000 00dd	1 (0x01)
R12318 (R0x301E)	data_pedestal_	0000 00dd dddd dddd	42 (0x002A)
R12321 (R0x3021)	software_reset_	0000 000d	0 (0x00)
R12322 (R0x3022)	grouped_parameter_hold_	0000 000d	0 (0x00)
R12323 (R0x3023)	mask_corrupted_frames_	0000 000d	0 (0x00)
R12324 (R0x3024)	pixel_order_	0000 00??	1 (0x01)
R12326 (R0x3026)	gpi_status	dddd dddd dddd dddd	65535 (0xFFFF)
R12328 (R0x3028)	global_analog_gain_	00dd dddd	2 (0x02)
R12330 (R0x302A)	analog_gain_greenr_	0000 0000 00dd dddd	2 (0x0002)
R12332 (R0x302C)	analog_gain_red_	0000 0000 00dd dddd	2 (0x0002)
R12334 (R0x302E)	analog_gain_blue_	0000 0000 00dd dddd	2 (0x0002)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12336 (R0x3030)	analog_gain_greenb_	0000 0000 00dd dddd	2 (0x0002)
R12338 (R0x3032)	digital_gain_greenr_	0000 dddd dddd ddd0	256 (0x0100)
R12340 (R0x3034)	digital_gain_red_	0000 dddd dddd ddd0	256 (0x0100)
R12342 (R0x3036)	digital_gain_blue_	0000 dddd dddd ddd0	256 (0x0100)
R12344 (R0x3038)	digital_gain_greenb_	0000 dddd dddd ddd0	256 (0x0100)
R12346 (R0x303A)	smia_version_	???? ????	10 (0x0A)
R12347 (R0x303B)	frame_count_	???? ????	255 (0xFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	2 (0x0002)
R12350 (R0x303E)	read_style	0000 0000 000d 00dd	0 (0x0000)
R12352 (R0x3040)	read_mode	dddd dddd dddd dddd	16449 (0x4041)
R12358 (R0x3046)	flash	??dd dddd dd0d dddd	1544 (0x0608)
R12360 (R0x3048)	flash_count	dddd dddd dddd dddd	8 (0x0008)
R12362 (R0x304A)	otpm_control	0000 0ddd 0??d d??d	0 (0x0000)
R12364 (R0x304C)	otpm_record	dddd dddd dddd dddd	512 (0x0200)
R12366 (R0x304E)	otpm_status	0000 ???? ???? ????	0 (0x0000)
R12368 (R0x3050)	otpm_manual_control	0000 0000 0??d 0??d	0 (0x0000)
R12370 (R0x3052)	otpm_manual_address	000d dddd dddd dddd	0 (0x0000)
R12372 (R0x3054)	otpm_expr	0000 dddd 0000 0000	0 (0x0000)
R12374 (R0x3056)	green1_gain	dddd dddd dddd dddd	4096 (0x1000)
R12376 (R0x3058)	blue_gain	dddd dddd dddd dddd	4096 (0x1000)
R12378 (R0x305A)	red_gain	dddd dddd dddd dddd	4096 (0x1000)
R12380 (R0x305C)	green2_gain	dddd dddd dddd dddd	4096 (0x1000)
R12382 (R0x305E)	global_gain	dddd dddd dddd dddd	4096 (0x1000)
R12394 (R0x306A)	odp_status	0000 0000 00?? 0000	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12398 (R0x306E)	data_path_select	dddd dd00 ?ddd 00dd	36992 (0x9080)
R12400 (R0x3070)	test_pattern_mode_	0000 00dd 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red_	0000 00dd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr_	0000 00dd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue_	0000 00dd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb_	0000 00dd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12448 (R0x30A0)	x_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc_	0000 0000 0000 0ddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc_	0000 0000 00dd dddd	1 (0x0001)
R12466 (R0x30B2)	tempsens_data	0000 00?? ???? ????	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	0000 0000 00dd dddd	0 (0x0000)
R12476 (R0x30BC)	y_output_offset	0000 dddd dddd dddd	0 (0x0000)
R12478 (R0x30BE)	x_output_offset	0000 dddd dddd dddd	0 (0x0000)
R12524 (R0x30EC)	ctx_rd_data	dddd dddd dddd dddd	0 (0x0000)
R12528 (R0x30F0)	vcm_control	d000 dddd 0000 dddd	0 (0x0000)
R12530 (R0x30F2)	vcm_new_code	0000 0000 dddd dddd	0 (0x0000)
R12532 (R0x30F4)	vcm_step_time	dddd dddd dddd dddd	0 (0x0000)
R12536 (R0x30F8)	gpio_ctrl	0000 0000 0000 00dd	3 (0x0003)
R12592 (R0x3130)	otpm_tcfg_write_01	dddd dddd dddd dddd	30721 (0x7801)
R12594 (R0x3132)	otpm_tcfg_write_23	dddd dddd dddd dddd	33 (0x0021)
R12596 (R0x3134)	otpm_tcfg_read_01	dddd dddd dddd dddd	3477 (0x0D95)
R12598 (R0x3136)	otpm_tcfg_read_23	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12602 (R0x313A)	otpm_manual_l	dddd dddd dddd dddd	0 (0x0000)
R12604 (R0x313C)	otpm_manual_h	dddd dddd dddd dddd	0 (0x0000)
R12606 (R0x313E)	otpm_manual_extra	dddd dddd dddd dddd	0 (0x0000)
R12632 (R0x3158)	slave_mode_control	ddd0 0000 0000 0000	0 (0x0000)
R12634 (R0x315A)	global_flash_start	dddd dddd dddd dddd	0 (0x0000)
R12636 (R0x315C)	global_bulb_trigger_count	dddd dddd dddd dddd	0 (0x0000)
R12638 (R0x315E)	global_seq_trigger	dddd 0d00 dddd 0ddd	0 (0x0000)
R12640 (R0x3160)	global_rst_end	dddd dddd dddd dddd	236 (0x00EC)
R12642 (R0x3162)	global_shutter_start	dddd dddd dddd dddd	791 (0x0317)
R12644 (R0x3164)	global_shutter_start2	0000 0000 dddd dddd	0 (0x0000)
R12646 (R0x3166)	global_read_start	dddd dddd dddd dddd	807 (0x0327)
R12648 (R0x3168)	global_read_start2	0000 0000 dddd dddd	0 (0x0000)
R12658 (R0x3172)	analog_control2	00dd 00dd dddd dddd	646 (0x0286)
R12704 (R0x31A0)	serial_format_descriptor_0	???? ???? ???? ????	513 (0x0201)
R12706 (R0x31A2)	serial_format_descriptor_1	???? ???? ???? ????	514 (0x0202)
R12708 (R0x31A4)	serial_format_descriptor_2	???? ???? ???? ????	516 (0x0204)
R12710 (R0x31A6)	serial_format_descriptor_3	???? ???? ???? ????	769 (0x0301)
R12712 (R0x31A8)	serial_format_descriptor_4	???? ???? ???? ????	770 (0x0302)
R12714 (R0x31AA)	serial_format_descriptor_5	???? ???? ???? ????	772 (0x0304)
R12716 (R0x31AC)	serial_format_descriptor_6	???? ???? ???? ????	0 (0x0000)
R12718 (R0x31AE)	serial_format	0000 00dd 0000 0ddd	516 (0x0204)
R12720 (R0x31B0)	frame_preamble	0000 0000 dddd dddd	113 (0x0071)
R12722 (R0x31B2)	line_preamble	0000 0000 dddd dddd	66 (0x0042)
R12724 (R0x31B4)	mipi_timing_0	dddd dddd dddd dddd	11896 (0x2E78)

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Table 3: Manufacturer Specific Register List and Default Values

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12726 (R0x31B6)	mipi_timing_1	dddd dddd dddd dddd	4765 (0x129D)
R12728 (R0x31B8)	mipi_timing_2	dddd dddd dddd dddd	16460 (0x404C)
R12730 (R0x31BA)	mipi_timing_3	dddd dddd dddd dddd	653 (0x028D)
R12732 (R0x31BC)	mipi_timing_4	dd00 0000 0ddd dddd	10 (0x000A)
R12734 (R0x31BE)	mipi_config	???0 0dd0 0000 dddd	49155 (0xC003)
R12736 (R0x31C0)	hispi_timing	dddd dddd dddd dddd	32768 (0x8000)
R12738 (R0x31C2)	hispi_blanking	dddd dddd dddd dddd	65535 (0xFFFF)
R12740 (R0x31C4)	hispi_sync_patt	dddd dddd dddd dddd	62805 (0xF555)
R12742 (R0x31C6)	hispi_control_status	??dd dddd dddd dddd	32768 (0x8000)
R12744 (R0x31C8)	hispi_ckecksum0	???? ???? ???? ????	0 (0x0000)
R12746 (R0x31CA)	hispi_ckecksum1	???? ???? ???? ????	0 (0x0000)
R12748 (R0x31CC)	hispi_ckecksum2	???? ???? ???? ????	0 (0x0000)
R12750 (R0x31CE)	hispi_ckecksum3	???? ???? ???? ????	0 (0x0000)
R12752 (R0x31D0)	mipi_compress_8_data_type	00dd dddd 00dd dddd	12849 (0x3231)
R12754 (R0x31D2)	mipi_compress_7_data_type	00dd dddd 00dd dddd	13620 (0x3534)
R12756 (R0x31D4)	mipi_compress_6_data_type	00dd dddd 00dd dddd	14134 (0x3736)
R12758 (R0x31D6)	mipi_jpeg_pn9_data_type	00dd dddd 00dd dddd	13104 (0x3330)
R12788 (R0x31F4)	fuse_id1	dddd dddd dddd dddd	0 (0x0000)
R12790 (R0x31F6)	fuse_id2	dddd dddd dddd dddd	0 (0x0000)
R12792 (R0x31F8)	fuse_id3	dddd dddd dddd dddd	0 (0x0000)
R12794 (R0x31FA)	fuse_id4	dddd dddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	28268 (0x6E6C)
R12798 (R0x31FE)	customer_rev	0000 0000 0??? ????	0 (0x0000)
R14336 (R0x3800)	otpm_data_000	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14338 (R0x3802)	otpm_data_001	dddd dddd dddd dddd	0 (0x0000)
R14340 (R0x3804)	otpm_data_002	dddd dddd dddd dddd	0 (0x0000)
R14342 (R0x3806)	otpm_data_003	dddd dddd dddd dddd	0 (0x0000)
R14344 (R0x3808)	otpm_data_004	dddd dddd dddd dddd	0 (0x0000)
R14346 (R0x380A)	otpm_data_005	dddd dddd dddd dddd	0 (0x0000)
R14348 (R0x380C)	otpm_data_006	dddd dddd dddd dddd	0 (0x0000)
R14350 (R0x380E)	otpm_data_007	dddd dddd dddd dddd	0 (0x0000)
R14352 (R0x3810)	otpm_data_008	dddd dddd dddd dddd	0 (0x0000)
R14354 (R0x3812)	otpm_data_009	dddd dddd dddd dddd	0 (0x0000)
R14356 (R0x3814)	otpm_data_010	dddd dddd dddd dddd	0 (0x0000)
R14358 (R0x3816)	otpm_data_011	dddd dddd dddd dddd	0 (0x0000)
R14360 (R0x3818)	otpm_data_012	dddd dddd dddd dddd	0 (0x0000)
R14362 (R0x381A)	otpm_data_013	dddd dddd dddd dddd	0 (0x0000)
R14364 (R0x381C)	otpm_data_014	dddd dddd dddd dddd	0 (0x0000)
R14366 (R0x381E)	otpm_data_015	dddd dddd dddd dddd	0 (0x0000)
R14368 (R0x3820)	otpm_data_016	dddd dddd dddd dddd	0 (0x0000)
R14370 (R0x3822)	otpm_data_017	dddd dddd dddd dddd	0 (0x0000)
R14372 (R0x3824)	otpm_data_018	dddd dddd dddd dddd	0 (0x0000)
R14374 (R0x3826)	otpm_data_019	dddd dddd dddd dddd	0 (0x0000)
R14376 (R0x3828)	otpm_data_020	dddd dddd dddd dddd	0 (0x0000)
R14378 (R0x382A)	otpm_data_021	dddd dddd dddd dddd	0 (0x0000)
R14380 (R0x382C)	otpm_data_022	dddd dddd dddd dddd	0 (0x0000)
R14382 (R0x382E)	otpm_data_023	dddd dddd dddd dddd	0 (0x0000)
R14384 (R0x3830)	otpm_data_024	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14386 (R0x3832)	otpm_data_025	dddd dddd dddd dddd	0 (0x0000)
R14388 (R0x3834)	otpm_data_026	dddd dddd dddd dddd	0 (0x0000)
R14390 (R0x3836)	otpm_data_027	dddd dddd dddd dddd	0 (0x0000)
R14392 (R0x3838)	otpm_data_028	dddd dddd dddd dddd	0 (0x0000)
R14394 (R0x383A)	otpm_data_029	dddd dddd dddd dddd	0 (0x0000)
R14396 (R0x383C)	otpm_data_030	dddd dddd dddd dddd	0 (0x0000)
R14398 (R0x383E)	otpm_data_031	dddd dddd dddd dddd	0 (0x0000)
R14400 (R0x3840)	otpm_data_032	dddd dddd dddd dddd	0 (0x0000)
R14402 (R0x3842)	otpm_data_033	dddd dddd dddd dddd	0 (0x0000)
R14404 (R0x3844)	otpm_data_034	dddd dddd dddd dddd	0 (0x0000)
R14406 (R0x3846)	otpm_data_035	dddd dddd dddd dddd	0 (0x0000)
R14408 (R0x3848)	otpm_data_036	dddd dddd dddd dddd	0 (0x0000)
R14410 (R0x384A)	otpm_data_037	dddd dddd dddd dddd	0 (0x0000)
R14412 (R0x384C)	otpm_data_038	dddd dddd dddd dddd	0 (0x0000)
R14414 (R0x384E)	otpm_data_039	dddd dddd dddd dddd	0 (0x0000)
R14416 (R0x3850)	otpm_data_040	dddd dddd dddd dddd	0 (0x0000)
R14418 (R0x3852)	otpm_data_041	dddd dddd dddd dddd	0 (0x0000)
R14420 (R0x3854)	otpm_data_042	dddd dddd dddd dddd	0 (0x0000)
R14422 (R0x3856)	otpm_data_043	dddd dddd dddd dddd	0 (0x0000)
R14424 (R0x3858)	otpm_data_044	dddd dddd dddd dddd	0 (0x0000)
R14426 (R0x385A)	otpm_data_045	dddd dddd dddd dddd	0 (0x0000)
R14428 (R0x385C)	otpm_data_046	dddd dddd dddd dddd	0 (0x0000)
R14430 (R0x385E)	otpm_data_047	dddd dddd dddd dddd	0 (0x0000)
R14432 (R0x3860)	otpm_data_048	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14434 (R0x3862)	otpm_data_049	dddd dddd dddd dddd	0 (0x0000)
R14436 (R0x3864)	otpm_data_050	dddd dddd dddd dddd	0 (0x0000)
R14438 (R0x3866)	otpm_data_051	dddd dddd dddd dddd	0 (0x0000)
R14440 (R0x3868)	otpm_data_052	dddd dddd dddd dddd	0 (0x0000)
R14442 (R0x386A)	otpm_data_053	dddd dddd dddd dddd	0 (0x0000)
R14444 (R0x386C)	otpm_data_054	dddd dddd dddd dddd	0 (0x0000)
R14446 (R0x386E)	otpm_data_055	dddd dddd dddd dddd	0 (0x0000)
R14448 (R0x3870)	otpm_data_056	dddd dddd dddd dddd	0 (0x0000)
R14450 (R0x3872)	otpm_data_057	dddd dddd dddd dddd	0 (0x0000)
R14452 (R0x3874)	otpm_data_058	dddd dddd dddd dddd	0 (0x0000)
R14454 (R0x3876)	otpm_data_059	dddd dddd dddd dddd	0 (0x0000)
R14456 (R0x3878)	otpm_data_060	dddd dddd dddd dddd	0 (0x0000)
R14458 (R0x387A)	otpm_data_061	dddd dddd dddd dddd	0 (0x0000)
R14460 (R0x387C)	otpm_data_062	dddd dddd dddd dddd	0 (0x0000)
R14462 (R0x387E)	otpm_data_063	dddd dddd dddd dddd	0 (0x0000)
R14464 (R0x3880)	otpm_data_064	dddd dddd dddd dddd	0 (0x0000)
R14466 (R0x3882)	otpm_data_065	dddd dddd dddd dddd	0 (0x0000)
R14468 (R0x3884)	otpm_data_066	dddd dddd dddd dddd	0 (0x0000)
R14470 (R0x3886)	otpm_data_067	dddd dddd dddd dddd	0 (0x0000)
R14472 (R0x3888)	otpm_data_068	dddd dddd dddd dddd	0 (0x0000)
R14474 (R0x388A)	otpm_data_069	dddd dddd dddd dddd	0 (0x0000)
R14476 (R0x388C)	otpm_data_070	dddd dddd dddd dddd	0 (0x0000)
R14478 (R0x388E)	otpm_data_071	dddd dddd dddd dddd	0 (0x0000)
R14480 (R0x3890)	otpm_data_072	dddd dddd dddd dddd	0 (0x0000)

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14482 (R0x3892)	otpm_data_073	dddd dddd dddd dddd	0 (0x0000)
R14484 (R0x3894)	otpm_data_074	dddd dddd dddd dddd	0 (0x0000)
R14486 (R0x3896)	otpm_data_075	dddd dddd dddd dddd	0 (0x0000)
R14488 (R0x3898)	otpm_data_076	dddd dddd dddd dddd	0 (0x0000)
R14490 (R0x389A)	otpm_data_077	dddd dddd dddd dddd	0 (0x0000)
R14492 (R0x389C)	otpm_data_078	dddd dddd dddd dddd	0 (0x0000)
R14494 (R0x389E)	otpm_data_079	dddd dddd dddd dddd	0 (0x0000)
R14496 (R0x38A0)	otpm_data_080	dddd dddd dddd dddd	0 (0x0000)
R14498 (R0x38A2)	otpm_data_081	dddd dddd dddd dddd	0 (0x0000)
R14500 (R0x38A4)	otpm_data_082	dddd dddd dddd dddd	0 (0x0000)
R14502 (R0x38A6)	otpm_data_083	dddd dddd dddd dddd	0 (0x0000)
R14504 (R0x38A8)	otpm_data_084	dddd dddd dddd dddd	0 (0x0000)
R14506 (R0x38AA)	otpm_data_085	dddd dddd dddd dddd	0 (0x0000)
R14508 (R0x38AC)	otpm_data_086	dddd dddd dddd dddd	0 (0x0000)
R14510 (R0x38AE)	otpm_data_087	dddd dddd dddd dddd	0 (0x0000)
R14512 (R0x38B0)	otpm_data_088	dddd dddd dddd dddd	0 (0x0000)
R14514 (R0x38B2)	otpm_data_089	dddd dddd dddd dddd	0 (0x0000)
R14516 (R0x38B4)	otpm_data_090	dddd dddd dddd dddd	0 (0x0000)
R14518 (R0x38B6)	otpm_data_091	dddd dddd dddd dddd	0 (0x0000)
R14520 (R0x38B8)	otpm_data_092	dddd dddd dddd dddd	0 (0x0000)
R14522 (R0x38BA)	otpm_data_093	dddd dddd dddd dddd	0 (0x0000)
R14524 (R0x38BC)	otpm_data_094	dddd dddd dddd dddd	0 (0x0000)
R14526 (R0x38BE)	otpm_data_095	dddd dddd dddd dddd	0 (0x0000)
R14528 (R0x38C0)	otpm_data_096	dddd dddd dddd dddd	0 (0x0000)

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14530 (R0x38C2)	otpm_data_097	dddd dddd dddd dddd	0 (0x0000)
R14532 (R0x38C4)	otpm_data_098	dddd dddd dddd dddd	0 (0x0000)
R14534 (R0x38C6)	otpm_data_099	dddd dddd dddd dddd	0 (0x0000)
R14536 (R0x38C8)	otpm_data_100	dddd dddd dddd dddd	0 (0x0000)
R14538 (R0x38CA)	otpm_data_101	dddd dddd dddd dddd	0 (0x0000)
R14540 (R0x38CC)	otpm_data_102	dddd dddd dddd dddd	0 (0x0000)
R14542 (R0x38CE)	otpm_data_103	dddd dddd dddd dddd	0 (0x0000)
R14544 (R0x38D0)	otpm_data_104	dddd dddd dddd dddd	0 (0x0000)
R14546 (R0x38D2)	otpm_data_105	dddd dddd dddd dddd	0 (0x0000)
R14548 (R0x38D4)	otpm_data_106	dddd dddd dddd dddd	0 (0x0000)
R14550 (R0x38D6)	otpm_data_107	dddd dddd dddd dddd	0 (0x0000)
R14552 (R0x38D8)	otpm_data_108	dddd dddd dddd dddd	0 (0x0000)
R14554 (R0x38DA)	otpm_data_109	dddd dddd dddd dddd	0 (0x0000)
R14556 (R0x38DC)	otpm_data_110	dddd dddd dddd dddd	0 (0x0000)
R14558 (R0x38DE)	otpm_data_111	dddd dddd dddd dddd	0 (0x0000)
R14560 (R0x38E0)	otpm_data_112	dddd dddd dddd dddd	0 (0x0000)
R14562 (R0x38E2)	otpm_data_113	dddd dddd dddd dddd	0 (0x0000)
R14564 (R0x38E4)	otpm_data_114	dddd dddd dddd dddd	0 (0x0000)
R14566 (R0x38E6)	otpm_data_115	dddd dddd dddd dddd	0 (0x0000)
R14568 (R0x38E8)	otpm_data_116	dddd dddd dddd dddd	0 (0x0000)
R14570 (R0x38EA)	otpm_data_117	dddd dddd dddd dddd	0 (0x0000)
R14572 (R0x38EC)	otpm_data_118	dddd dddd dddd dddd	0 (0x0000)
R14574 (R0x38EE)	otpm_data_119	dddd dddd dddd dddd	0 (0x0000)
R14576 (R0x38F0)	otpm_data_120	dddd dddd dddd dddd	0 (0x0000)

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Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14578 (R0x38F2)	otpm_data_121	dddd dddd dddd dddd	0 (0x0000)
R14580 (R0x38F4)	otpm_data_122	dddd dddd dddd dddd	0 (0x0000)
R14582 (R0x38F6)	otpm_data_123	dddd dddd dddd dddd	0 (0x0000)
R14584 (R0x38F8)	otpm_data_124	dddd dddd dddd dddd	0 (0x0000)
R14586 (R0x38FA)	otpm_data_125	dddd dddd dddd dddd	0 (0x0000)
R14588 (R0x38FC)	otpm_data_126	dddd dddd dddd dddd	0 (0x0000)
R14590 (R0x38FE)	otpm_data_127	dddd dddd dddd dddd	0 (0x0000)
R14592 (R0x3900)	otpm_data_128	dddd dddd dddd dddd	0 (0x0000)
R14594 (R0x3902)	otpm_data_129	dddd dddd dddd dddd	0 (0x0000)
R14596 (R0x3904)	otpm_data_130	dddd dddd dddd dddd	0 (0x0000)
R14598 (R0x3906)	otpm_data_131	dddd dddd dddd dddd	0 (0x0000)
R14600 (R0x3908)	otpm_data_132	dddd dddd dddd dddd	0 (0x0000)
R14602 (R0x390A)	otpm_data_133	dddd dddd dddd dddd	0 (0x0000)
R14604 (R0x390C)	otpm_data_134	dddd dddd dddd dddd	0 (0x0000)
R14606 (R0x390E)	otpm_data_135	dddd dddd dddd dddd	0 (0x0000)
R14608 (R0x3910)	otpm_data_136	dddd dddd dddd dddd	0 (0x0000)
R14610 (R0x3912)	otpm_data_137	dddd dddd dddd dddd	0 (0x0000)
R14612 (R0x3914)	otpm_data_138	dddd dddd dddd dddd	0 (0x0000)
R14614 (R0x3916)	otpm_data_139	dddd dddd dddd dddd	0 (0x0000)
R14616 (R0x3918)	otpm_data_140	dddd dddd dddd dddd	0 (0x0000)
R14618 (R0x391A)	otpm_data_141	dddd dddd dddd dddd	0 (0x0000)
R14620 (R0x391C)	otpm_data_142	dddd dddd dddd dddd	0 (0x0000)
R14622 (R0x391E)	otpm_data_143	dddd dddd dddd dddd	0 (0x0000)
R14624 (R0x3920)	otpm_data_144	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14626 (R0x3922)	otpm_data_145	dddd dddd dddd dddd	0 (0x0000)
R14628 (R0x3924)	otpm_data_146	dddd dddd dddd dddd	0 (0x0000)
R14630 (R0x3926)	otpm_data_147	dddd dddd dddd dddd	0 (0x0000)
R14632 (R0x3928)	otpm_data_148	dddd dddd dddd dddd	0 (0x0000)
R14634 (R0x392A)	otpm_data_149	dddd dddd dddd dddd	0 (0x0000)
R14636 (R0x392C)	otpm_data_150	dddd dddd dddd dddd	0 (0x0000)
R14638 (R0x392E)	otpm_data_151	dddd dddd dddd dddd	0 (0x0000)
R14640 (R0x3930)	otpm_data_152	dddd dddd dddd dddd	0 (0x0000)
R14642 (R0x3932)	otpm_data_153	dddd dddd dddd dddd	0 (0x0000)
R14644 (R0x3934)	otpm_data_154	dddd dddd dddd dddd	0 (0x0000)
R14646 (R0x3936)	otpm_data_155	dddd dddd dddd dddd	0 (0x0000)
R14648 (R0x3938)	otpm_data_156	dddd dddd dddd dddd	0 (0x0000)
R14650 (R0x393A)	otpm_data_157	dddd dddd dddd dddd	0 (0x0000)
R14652 (R0x393C)	otpm_data_158	dddd dddd dddd dddd	0 (0x0000)
R14654 (R0x393E)	otpm_data_159	dddd dddd dddd dddd	0 (0x0000)
R14656 (R0x3940)	otpm_data_160	dddd dddd dddd dddd	0 (0x0000)
R14658 (R0x3942)	otpm_data_161	dddd dddd dddd dddd	0 (0x0000)
R14660 (R0x3944)	otpm_data_162	dddd dddd dddd dddd	0 (0x0000)
R14662 (R0x3946)	otpm_data_163	dddd dddd dddd dddd	0 (0x0000)
R14664 (R0x3948)	otpm_data_164	dddd dddd dddd dddd	0 (0x0000)
R14666 (R0x394A)	otpm_data_165	dddd dddd dddd dddd	0 (0x0000)
R14668 (R0x394C)	otpm_data_166	dddd dddd dddd dddd	0 (0x0000)
R14670 (R0x394E)	otpm_data_167	dddd dddd dddd dddd	0 (0x0000)
R14672 (R0x3950)	otpm_data_168	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14674 (R0x3952)	otpm_data_169	dddd dddd dddd dddd	0 (0x0000)
R14676 (R0x3954)	otpm_data_170	dddd dddd dddd dddd	0 (0x0000)
R14678 (R0x3956)	otpm_data_171	dddd dddd dddd dddd	0 (0x0000)
R14680 (R0x3958)	otpm_data_172	dddd dddd dddd dddd	0 (0x0000)
R14682 (R0x395A)	otpm_data_173	dddd dddd dddd dddd	0 (0x0000)
R14684 (R0x395C)	otpm_data_174	dddd dddd dddd dddd	0 (0x0000)
R14686 (R0x395E)	otpm_data_175	dddd dddd dddd dddd	0 (0x0000)
R14688 (R0x3960)	otpm_data_176	dddd dddd dddd dddd	0 (0x0000)
R14690 (R0x3962)	otpm_data_177	dddd dddd dddd dddd	0 (0x0000)
R14692 (R0x3964)	otpm_data_178	dddd dddd dddd dddd	0 (0x0000)
R14694 (R0x3966)	otpm_data_179	dddd dddd dddd dddd	0 (0x0000)
R14696 (R0x3968)	otpm_data_180	dddd dddd dddd dddd	0 (0x0000)
R14698 (R0x396A)	otpm_data_181	dddd dddd dddd dddd	0 (0x0000)
R14700 (R0x396C)	otpm_data_182	dddd dddd dddd dddd	0 (0x0000)
R14702 (R0x396E)	otpm_data_183	dddd dddd dddd dddd	0 (0x0000)
R14704 (R0x3970)	otpm_data_184	dddd dddd dddd dddd	0 (0x0000)
R14706 (R0x3972)	otpm_data_185	dddd dddd dddd dddd	0 (0x0000)
R14708 (R0x3974)	otpm_data_186	dddd dddd dddd dddd	0 (0x0000)
R14710 (R0x3976)	otpm_data_187	dddd dddd dddd dddd	0 (0x0000)
R14712 (R0x3978)	otpm_data_188	dddd dddd dddd dddd	0 (0x0000)
R14714 (R0x397A)	otpm_data_189	dddd dddd dddd dddd	0 (0x0000)
R14716 (R0x397C)	otpm_data_190	dddd dddd dddd dddd	0 (0x0000)
R14718 (R0x397E)	otpm_data_191	dddd dddd dddd dddd	0 (0x0000)
R14720 (R0x3980)	otpm_data_192	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14722 (R0x3982)	otpm_data_193	dddd dddd dddd dddd	0 (0x0000)
R14724 (R0x3984)	otpm_data_194	dddd dddd dddd dddd	0 (0x0000)
R14726 (R0x3986)	otpm_data_195	dddd dddd dddd dddd	0 (0x0000)
R14728 (R0x3988)	otpm_data_196	dddd dddd dddd dddd	0 (0x0000)
R14730 (R0x398A)	otpm_data_197	dddd dddd dddd dddd	0 (0x0000)
R14732 (R0x398C)	otpm_data_198	dddd dddd dddd dddd	0 (0x0000)
R14734 (R0x398E)	otpm_data_199	dddd dddd dddd dddd	0 (0x0000)
R14736 (R0x3990)	otpm_data_200	dddd dddd dddd dddd	0 (0x0000)
R14738 (R0x3992)	otpm_data_201	dddd dddd dddd dddd	0 (0x0000)
R14740 (R0x3994)	otpm_data_202	dddd dddd dddd dddd	0 (0x0000)
R14742 (R0x3996)	otpm_data_203	dddd dddd dddd dddd	0 (0x0000)
R14744 (R0x3998)	otpm_data_204	dddd dddd dddd dddd	0 (0x0000)
R14746 (R0x399A)	otpm_data_205	dddd dddd dddd dddd	0 (0x0000)
R14748 (R0x399C)	otpm_data_206	dddd dddd dddd dddd	0 (0x0000)
R14750 (R0x399E)	otpm_data_207	dddd dddd dddd dddd	0 (0x0000)
R14752 (R0x39A0)	otpm_data_208	dddd dddd dddd dddd	0 (0x0000)
R14754 (R0x39A2)	otpm_data_209	dddd dddd dddd dddd	0 (0x0000)
R14756 (R0x39A4)	otpm_data_210	dddd dddd dddd dddd	0 (0x0000)
R14758 (R0x39A6)	otpm_data_211	dddd dddd dddd dddd	0 (0x0000)
R14760 (R0x39A8)	otpm_data_212	dddd dddd dddd dddd	0 (0x0000)
R14762 (R0x39AA)	otpm_data_213	dddd dddd dddd dddd	0 (0x0000)
R14764 (R0x39AC)	otpm_data_214	dddd dddd dddd dddd	0 (0x0000)
R14766 (R0x39AE)	otpm_data_215	dddd dddd dddd dddd	0 (0x0000)
R14768 (R0x39B0)	otpm_data_216	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14770 (R0x39B2)	otpm_data_217	dddd dddd dddd dddd	0 (0x0000)
R14772 (R0x39B4)	otpm_data_218	dddd dddd dddd dddd	0 (0x0000)
R14774 (R0x39B6)	otpm_data_219	dddd dddd dddd dddd	0 (0x0000)
R14776 (R0x39B8)	otpm_data_220	dddd dddd dddd dddd	0 (0x0000)
R14778 (R0x39BA)	otpm_data_221	dddd dddd dddd dddd	0 (0x0000)
R14780 (R0x39BC)	otpm_data_222	dddd dddd dddd dddd	0 (0x0000)
R14782 (R0x39BE)	otpm_data_223	dddd dddd dddd dddd	0 (0x0000)
R14784 (R0x39C0)	otpm_data_224	dddd dddd dddd dddd	0 (0x0000)
R14786 (R0x39C2)	otpm_data_225	dddd dddd dddd dddd	0 (0x0000)
R14788 (R0x39C4)	otpm_data_226	dddd dddd dddd dddd	0 (0x0000)
R14790 (R0x39C6)	otpm_data_227	dddd dddd dddd dddd	0 (0x0000)
R14792 (R0x39C8)	otpm_data_228	dddd dddd dddd dddd	0 (0x0000)
R14794 (R0x39CA)	otpm_data_229	dddd dddd dddd dddd	0 (0x0000)
R14796 (R0x39CC)	otpm_data_230	dddd dddd dddd dddd	0 (0x0000)
R14798 (R0x39CE)	otpm_data_231	dddd dddd dddd dddd	0 (0x0000)
R14800 (R0x39D0)	otpm_data_232	dddd dddd dddd dddd	0 (0x0000)
R14802 (R0x39D2)	otpm_data_233	dddd dddd dddd dddd	0 (0x0000)
R14804 (R0x39D4)	otpm_data_234	dddd dddd dddd dddd	0 (0x0000)
R14806 (R0x39D6)	otpm_data_235	dddd dddd dddd dddd	0 (0x0000)
R14808 (R0x39D8)	otpm_data_236	dddd dddd dddd dddd	0 (0x0000)
R14810 (R0x39DA)	otpm_data_237	dddd dddd dddd dddd	0 (0x0000)
R14812 (R0x39DC)	otpm_data_238	dddd dddd dddd dddd	0 (0x0000)
R14814 (R0x39DE)	otpm_data_239	dddd dddd dddd dddd	0 (0x0000)
R14816 (R0x39E0)	otpm_data_240	dddd dddd dddd dddd	0 (0x0000)

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Table 3: Manufacturer Specific Register List and Default Values

1 = read-only, always 1; 0 = read-only, always 0; d = programmable;? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14818 (R0x39E2)	otpm_data_241	dddd dddd dddd dddd	0 (0x0000)
R14820 (R0x39E4)	otpm_data_242	dddd dddd dddd dddd	0 (0x0000)
R14822 (R0x39E6)	otpm_data_243	dddd dddd dddd dddd	0 (0x0000)
R14824 (R0x39E8)	otpm_data_244	dddd dddd dddd dddd	0 (0x0000)
R14826 (R0x39EA)	otpm_data_245	dddd dddd dddd dddd	0 (0x0000)
R14828 (R0x39EC)	otpm_data_246	dddd dddd dddd dddd	0 (0x0000)
R14830 (R0x39EE)	otpm_data_247	dddd dddd dddd dddd	0 (0x0000)
R14832 (R0x39F0)	otpm_data_248	dddd dddd dddd dddd	0 (0x0000)
R14834 (R0x39F2)	otpm_data_249	dddd dddd dddd dddd	0 (0x0000)
R14836 (R0x39F4)	otpm_data_250	dddd dddd dddd dddd	0 (0x0000)
R14838 (R0x39F6)	otpm_data_251	dddd dddd dddd dddd	0 (0x0000)
R14840 (R0x39F8)	otpm_data_252	dddd dddd dddd dddd	0 (0x0000)
R14842 (R0x39FA)	otpm_data_253	dddd dddd dddd dddd	0 (0x0000)
R14844 (R0x39FC)	otpm_data_254	dddd dddd dddd dddd	0 (0x0000)
R14846 (R0x39FE)	otpm_data_255	dddd dddd dddd dddd	0 (0x0000)
R16326 (R0x3FC6)	tempsens_calib1	dddd dddd dddd dddd	291 (0x0123)
R16328 (R0x3FC8)	tempsens_calib2	dddd dddd dddd dddd	17767 (0x4567)
R16330 (R0x3FCA)	tempsens_calib3	dddd dddd dddd dddd	35243 (0x89AB)
R16332 (R0x3FCC)	tempsens_calib4	dddd dddd dddd dddd	52719 (0xCDEF)

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Register Descriptions

SMIA Configuration Register Descriptions

Table 4: SMIA Configuration Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
0 R0x0000	15:0	0x4B03	chip_version_reg (R/W)	N	N
	This register is an alias of R0x3000-1. Read-only. Can be made read/write by clearing R0x301A-B[3]. Legal values: [0, 65535].				
2 R0x0002	7:0	0x00	revision_number (RO)	N	N
	Aptina assigned revision number. Read-only. Can be made read/write by clearing R0x301A-B[3]. Read-only. Legal values: [0, 255].				
3 R0x0003	7:0	0x06	manufacturer_id (RO)	N	N
	Manufacturer ID assigned to Aptina. Read-only. Can be made read/write by clearing R0x301A-B[3]. Read-only. Legal values: [0, 255].				
4 R0x0004	7:0	0x0A	smia_version (RO)	N	N
	This register is an alias of R0x303A. Read-only. Read-only. Legal values: [0, 255].				
5 R0x0005	7:0	0xFF	frame_count (RO)	Y	N
	This register is an alias of R0x303B. Read-only. Read-only. Legal values: [0, 255].				
6 R0x0006	7:0	0x01	pixel_order (RO)	N	N
	The value in this register changes as a function of R0x3040[1:0]. 00 = First row is GreenR/Red, first pixel is GreenR 01 = First row is GreenR/Red, first pixel is Red 02 = First row is Blue/GreenB, first pixel is Blue 03 = First row is Blue/GreenB, first pixel is GreenB Read-only. Legal values: [0, 3].				
8 R0x0008	15:0	0x002A	data_pedestal (R/W)	N	Y
	This register is an alias of R0x301E-F. Read-only. Can be made read/write by clearing R0x301A-B[3]. Legal values: [0, 1023].				
128 R0x0080	15:0	0x0001	analogue_gain_capability (RO)	N	N
	Indicates the provision of separate (per-color) analog gain control. The sensor supports both global and separate (per-color) analog gain control. Read-only. Read-only. Legal values: [0, 65535].				
132 R0x0084	15:0	0x0001	analogue_gain_code_min (RO)	N	N
	Minimum gain code. Read-only. Read-only. Legal values: [0, 65535].				
134 R0x0086	15:0	0x0020	analogue_gain_code_max (RO)	N	N
	Maximum gain code. Read-only. Read-only. Legal values: [0, 65535].				
136 R0x0088	15:0	0x0001	analogue_gain_code_step (RO)	N	N
	Gain code step size. Read-only. Read-only. Legal values: [0, 65535].				
138 R0x008A	15:0	0x0000	analogue_gain_type (RO)	N	N
	Indicates support for analog gain coding type 0 (baseline SMIA). Read-only. Read-only. Legal values: [0, 65535].				

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
140 R0x008C	15:0	0x0001	analogue_gain_m0 (RO)	N	N
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 65535].				
142 R0x008E	15:0	0x0000	analogue_gain_c0 (RO)	N	N
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 65535].				
144 R0x0090	15:0	0x0000	analogue_gain_m1 (RO)	N	N
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 65535].				
146 R0x0092	15:0	0x0001	analogue_gain_c1 (RO)	N	N
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 255].				
192 R0x00C0	7:0	0x01	data_format_model_type (RO)	N	N
	Indicates the use of 2-byte data format. Read-only. Read-only. Legal values: [0, 255].				
193 R0x00C1	7:0	0x05	data_format_model_subtype (RO)	N	N
	Indicates the provision of 3 data format descriptors. Read-only. Read-only. Legal values: [0, 255].				
194 R0x00C2	15:0	0x0A0A	data_format_descriptor_0 (RO)	N	N
	Indicates support for RAW10, uncompressed data format. Read-only. Read-only. Legal values: [0, 65535].				
196 R0x00C4	15:0	0x0808	data_format_descriptor_1 (RO)	N	N
	Indicates support for RAW8 data format in which the two LSB of each 10-bit pixel data value are discarded. Read-only. Read-only. Legal values: [0, 65535].				
198 R0x00C6	15:0	0x0A08	data_format_descriptor_2 (RO)	N	N
	Indicates support for RAW8 data format in which each 10-bit pixel data value is compressed to an 8-bit value. Read-only. Read-only. Legal values: [0, 65535].				
200 R0x00C8	15:0	0x0A06	data_format_descriptor_3 (RO)	N	N
	Read-only. Read-only. Legal values: [0, 65535].				
202 R0x00CA	15:0	0x0000	data_format_descriptor_4 (RO)	N	N
	Read-only. Read-only. Legal values: [0, 65535].				
204 R0x00CC	15:0	0x0000	data_format_descriptor_5 (RO)	N	N
	Read-only. Read-only. Legal values: [0, 65535].				
206 R0x00CE	15:0	0x0000	data_format_descriptor_6 (RO)	N	N
	Read-only. Read-only. Legal values: [0, 65535].				
256 R0x0100	7:0	0x00	mode_select (R/W)	Y	N
	This bit is an alias of R0x301A-B[2].				

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
257 R0x0101	7:0	0x01	image_orientation (R/W)		
	7:2	X	Reserved		
	1	0x00	vert_flip This register field is an alias of R0x3040[15]	Y	YM
	0	0x01	horiz_mirror This register field is an alias of R0x3040[14]	Y	YM
259 R0x0103	7:0	0x00	software_reset (R/W)	N	y
	This register field is an alias of R0x301A-B[0].				
260 R0x0104	7:0	0x00	grouped_parameter_hold (R/W)	N	N
	This register field is an alias of R0x301A-B[15].				
261 R0x0105	7:0	0x00	mask_corrupted_frames (R/W)	N	Y
	This register field is an alias of R0x301A-B[9].				
272 R0x0110	7:0	0x00	ccp2_channel_mode (R/W)		
	7:3	X	Reserved		
	2:0	0x00	ccp2_channel_identifier ccp2_channel_identifier Legal values: [0, 7].	Y	N
273 R0x0111	7:0	0x01	ccp2_signalling_mode (R/W)	Y	N
	0: Use Data/Clock signaling on the CCP2 serial interface. 1: Use Data/Strobe signaling on the CCP2 serial interface.				
274 R0x0112	15:0	0x0A0A	ccp_data_format (R/W)		
	15:12	X	Reserved		
	11:8	0x000A	raw_data_format The bit-width of the uncompressed pixel data Legal values: [0, 15].	Y	N
	7:4	X	Reserved		
	3:0	0x000A	compressed_data_format The bit-width of the compressed pixel data Legal values: [0, 15].	Y	N
288 R0x0120	7:0	0x00	gain_mode (R/W)	N	N
	gain_mode				
514 R0x0202	15:0	0x0010	coarse_integration_time (R/W)	Y	N
	Integration time programmed in units of line_length_pck. This register is an alias of R0x3012-3. Legal values: [0, 65535].				
516 R0x0204	15:0	0x0002	analogue_gain_code_global (R/W)	Y	N
	global analog gain. Available analog gains : 0.5x through 16x, with step of 0.5 Legal values: [0,32].				
518 R0x0206	15:0	0x0002	analogue_gain_code_greenr (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenr analog gain for green R. Legal values: [0,32].	Y	N

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
520 R0x0208	15:0	0x0002	analogue_gain_code_red (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_red analog gain for red. Legal values: [0,32].	Y	N
522 R0x020A	15:0	0x0002	analogue_gain_code_blue (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_blue analog gain for blue. Legal values: [0,32].	Y	N
524 R0x020C	15:0	0x0002	analogue_gain_code_greenb (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenb analog gain for green B. Legal values: [0,32].	Y	N
526 R0x020E	15:0	0x0100	digital_gain_greenr (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_greenr global digital gain, gain = register value/128. Legal values: [0,2047].	Y	N
	0	X	Reserved		
528 R0x0210	15:0	0x0100	digital_gain_red (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_red global digital gain, gain = register value/128. Legal values: [0,2047].	Y	N
	0	X	Reserved		
530 R0x0212	15:0	0x0100	digital_gain_blue (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_blue global digital gain, gain = register value/128. Legal values: [0,2047].	Y	N
	0	X	Reserved		
532 R0x0214	15:0	0x0100	digital_gain_greenb (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_greenb global digital gain, gain = register value/128. Legal values: [0,2047].	Y	N
	0	X	Reserved		
768 R0x0300	15:0	0x0005	vt_pix_clk_div (R/W)	N	Y
	Clock divisor applied to video timing system clock to generate video timing pixel clock. Legal values: [0, 31].				

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
770 R0x0302	15:0	0x0001	vt_sys_clk_div (R/W)	N	N
	Clock divisor applied to PLL output clock to generate video timing system clock. Legal values: [0, 31].				
772 R0x0304	15:0	0x0002	pre_pll_clk_div (R/W)	N	Y
	Clock divisor applied to EXTCLK to generate PLL input clock. Legal values: [1, 63].				
774 R0x0306	15:0	0x0040	pll_multiplier (R/W)	N	Y
	Clock multiplier applied to PLL input clock. Legal values: [32, 254].				
776 R0x0308	15:0	0x000A	op_pix_clk_div (R/W)	N	Y
	Clock divisor applied to the output system clock to generate the output pixel clock. Legal values: [0, 31].				
778 R0x030A	15:0	0x0001	op_sys_clk_div (R/W)	N	Y
	Clock divisor applied to PLL output clock to generate output system clock. Legal values: [0, 31].				
832 R0x0340	15:0	0x0A01	frame_length_lines (R/W)	Y	YM
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Legal values: [0, 65535].				
834 R0x0342	15:0	0x0F68	line_length_pck (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Legal values: [0, 65535].				
836 R0x0344	15:0	0x0008	x_addr_start (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. Legal values: [0, 3279].				
838 R0x0346	15:0	0x0008	y_addr_start (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. Legal values: [0, 2463].				
840 R0x0348	15:0	0x0CC7	x_addr_end (R/W)	Y	N
	The last column of visible pixels to read out. Legal values: [0, 3279].				
842 R0x034A	15:0	0x0997	y_addr_end (R/W)	Y	YM
	The last row of visible pixels to be read out. Legal values: [0, 2463].				
844 R0x034C	15:0	0x0CC0	x_output_size (R/W)	YN	N
	Set X output size of displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of x_addr_end and x_addr_start. Legal values: [0, 4095].				
846 R0x034E	15:0	0x0990	y_output_size (R/W)	Y	N
	Set Y output size of the displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of y_addr_end and y_addr_start. Legal values: [0, 4095].				

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
896 R0x0380	15:0	0x0001	x_even_inc (RO)	N	N
	Read-only. Read-only.				
898 R0x0382	15:0	0x0001	x_odd_inc (R/W)	Y	YM
	This register field is an alias of R0x3040[8:6] Legal values: [0, 15].				
900 R0x0384	15:0	0x0001	y_even_inc (RO)	N	N
	Read-only. Read-only.				
902 R0x0386	15:0	0x0001	y_odd_inc (R/W)	Y	YM
	This register field is an alias of R0x3040[5:0] Legal values: [0, 63].				
1024 R0x0400	15:0	0x0000	scaling_mode (R/W)	Y	N
	0: Disable scaler 1: Enable horizontal scaling 2: Enable horizontal and vertical scaling 3: Reserved Legal values: [0, 2].				
1026 R0x0402	15:0	0x0000	spatial_sampling (R/W)	Y	N
	0: Bayer sampling 1: Co-sited sampling				
1028 R0x0404	15:0	0x0010	scale_m (R/W)	Y	N
	scale factor M(horizontal scale factor) Legal values: [16, 127].				
1030 R0x0406	15:0	0x0010	scale_n (RO)	N	N
	scale factor N(vertical scale factor) Read-only. Legal values: [16, 127].				
1280 R0x0500	15:0	0x0001	compression_mode (RO)	N	Y
	Read-only. 0x0001 = 10-bit to 8-bit compression uses the DPCM/PCM Simple Predictor algorithm. This register controls the algorithm that is to be used for compression. The sensor only supports a single algorithm and therefore this register is read-only. This register does not control whether data compression is enabled; that is controlled by the ccp_data_format register (R0x0012-3). Read-only.				
1536 R0x0600	15:0	0x0000	test_pattern_mode (R/W)		
	15:10	X	Reserved		
	9:8	0x0000	walking_one_pattern_enable Walking one pattern 256: Walking 1's test pattern (10-bit) 257: Walking 1's test pattern (8-bit) other = Reserved. Legal values: [0, 1].	N	Y
	7:3	X	Reserved		
	2:0	0x0000	test_pattern_select select test pattern 0: Normal operation, Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to gray color bar test pattern 4: PN9 Link integrity test pattern Legal values: [0, 7].	N	Y

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Table 4: SMIA Configuration Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
1538 R0x0602	15:0	0x0000	test_data_red (R/W)	N	Y
	red test data for solid test pattern. Legal values: [0, 1023].				
1540 R0x0604	15:0	0x0000	test_data_greenr (R/W)	N	Y
	greenR test data for solid test pattern. Legal values: [0, 1023].				
1542 R0x0606	15:0	0x0000	test_data_blue (R/W)	N	Y
	blue test data for solid test pattern. Legal values: [0, 1023].				
1544 R0x0608	15:0	0x0000	test_data_greenb (R/W)	N	Y
	greenB test data for solid test pattern. Legal values: [0, 1023].				

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SMIA Parameter Limits Register Descriptions

Table 5: SMIA Parameter Limits Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
4096 R0x1000	15:0	0x0001	integration_time_capability (RO)	N	N
	Indicates the provision of coarse and fine integration time control. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4100 R0x1004	15:0	0x0000	coarse_integration_time_min (R/W)	N	N
	The minimum coarse integration time. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4102 R0x1006	15:0	0x0001	coarse_integration_time_max_margin (R/W)	N	N
	The maximum coarse integration time is (frame_length_lines - coarse_integration_time_max_margin). Read-only. Can be made read/write by clearing R0x301A-B[3]. In the sensor, this limit can be broken. The result will be a graceful degradation of frame rate, like pre-mi3120 products.				
4224 R0x1080	15:0	0x0001	digital_gain_capability (RO)	N	N
	Indicates the provision of separate (per-color) digital gain control. Read-only.				
4228 R0x1084	15:0	0x0002	digital_gain_min (RO)	N	N
	UFIX16. Minimum value of digital gain is 1.0. Read-only.				
4230 R0x1086	15:0	0x0FFE	digital_gain_max (RO)	N	N
	UFIX16. Maximum value of digital gain is 7.0. Read-only.				
4232 R0x1088	15:0	0x0002	digital_gain_step_size (RO)	N	N
	UFIX16. Step size for digital gain is 1.0. Read-only.				
4352 R0x1100	31:0	0x40000000	min_ext_clk_freq_mhz (RO)	N	N
	FLP32. Minimum external clock frequency into PLL is 2.0 MHz. Read-only.				
4356 R0x1104	31:0	0x42800000	max_ext_clk_freq_mhz (RO)	N	N
	FLP32. Maximum external clock frequency into PLL is 64.0 MHz. Read-only.				
4360 R0x1108	15:0	0x0001	min_pre_pll_clk_div (RO)	N	N
	Minimum clock divisor applied to PLL input clock. Read-only.				
4362 R0x110A	15:0	0x0040	max_pre_pll_clk_div (RO)	N	N
	Maximum clock divisor applied to PLL input clock. Read-only.				
4364 R0x110C	31:0	0x40000000	min_pll_ip_freq_mhz (RO)	N	N
	FLP32. Minimum clock frequency into the PFD of the PLL is 4.0 MHz. Read-only.				
4368 R0x1110	31:0	0x41C00000	max_pll_ip_freq_mhz (RO)	N	N
	FLP32. Maximum clock frequency into the PFD of the PLL is 24 MHz. Read-only.				
4372 R0x1114	15:0	0x0020	min_pll_multiplier (RO)	N	N
	Minimum multiplier applied by PLL. Read-only.				
4374 R0x1116	15:0	0x0180	max_pll_multiplier (RO)	N	N
	Maximum multiplier applied by PLL. Read-only.				
4376 R0x1118	31:0	0x43C00000	min_pll_op_freq_mhz (RO)	N	N
	FLP32. Minimum output frequency supported by the PLL is 384.0 MHz. Read-only.				
4380 R0x111C	31:0	0x44400000	max_pll_op_freq_mhz (RO)	N	N
	FLP32. Maximum output frequency supported by the PLL is 1000.0 MHz. Read-only.				
4384 R0x1120	15:0	0x0001	min_vt_sys_clk_div (RO)	N	N
	Minimum divisor for the video timing sys_clk. Read-only.				
4386 R0x1122	15:0	0x0010	max_vt_sys_clk_div (RO)	N	N
	Maximum divisor for the video timing sys_clk. Read-only.				

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Table 5: SMIA Parameter Limits Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
4388 R0x1124	31:0	0x41C00000	min_vt_sys_clk_freq_mhz (RO)	N	N
	FLP32. Minimum frequency for the video timing sys_clk is 24.0 MHz.				
4392 R0x1128	31:0	0x41C00000	max_vt_sys_clk_freq_mhz (RO)	N	N
	FLP32. Maximum frequency for the video timing sys_clk is 1000.0 MHz. Read-only.				
4396 R0x112C	31:0	0x4099999A	min_vt_pix_clk_freq_mhz (RO)	N	N
	FLP32. Minimum frequency for video timing pix_clk is 4.8 MHz. Read-only.				
4400 R0x1130	31:0	0x435C0000	max_vt_pix_clk_freq_mhz (RO)	N	N
	FLP32. Maximum frequency for video timing pix_clk is 200.0 MHz. Read-only.				
4404 R0x1134	15:0	0x0004	min_vt_pix_clk_div (RO)	N	N
	Minimum divisor for the video timing pix_clk. Read-only.				
4406 R0x1136	15:0	0x0010	max_vt_pix_clk_div (RO)	N	N
	Maximum divisor for the video timing pix_clk. Read-only.				
4416 R0x1140	15:0	0x0073	min_frame_length_lines (R/W)	N	N
	Minimum frame length. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4418 R0x1142	15:0	0xFFFF	max_frame_length_lines (R/W)	N	N
	Maximum frame length. The maximum frame length is only constrained by the size of the read/write field in the frame_length_lines register (16-bits). Read-only. Can be made read/write by clearing R0x301A-B[3].				
4420 R0x1144	15:0	0x0E98	min_line_length_pck (R/W)	N	N
	Minimum line length. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4422 R0x1146	15:0	0xFFFC	max_line_length_pck (R/W)	N	N
	Maximum line length. The maximum line length is only constrained by the size of the read/write field in the line_length_pck register (16 bits). Read-only. Can be made read/write by clearing R0x301A-B[3].				
4424 R0x1148	15:0	0x00FC	min_line_blanking_pck (R/W)	N	N
	Minimum line blanking time. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4426 R0x114A	15:0	0x0071	min_frame_blanking_lines (R/W)	N	N
	Minimum frame blanking time. Read-only. Can be made read/write by clearing R0x301A-B[3].				
4448 R0x1160	15:0	0x0001	min_op_sys_clk_div (RO)	N	N
	Minimum divisor for the output sys_clk. Read-only.				
4450 R0x1162	15:0	0x0010	max_op_sys_clk_div (RO)	N	N
	Maximum divisor for the output sys_clk. Read-only.				
4452 R0x1164	31:0	0x41C00000	min_op_sys_clk_freq_mhz (RO)	N	N
	FLP32. Minimum frequency for output sys_clk is 24.0 MHz. Read-only.				
4456 R0x1168	31:0	0x447A0000	max_op_sys_clk_freq_mhz (RO)	N	N
	FLP32. Maximum frequency for output sys_clk is 1000.0 MHz. Read-only.				
4460 R0x116C	15:0	0x0008	min_op_pix_clk_div (RO)	N	N
	Minimum divisor for output pix_clk. Read-only.				
4462 R0x116E	15:0	0x000A	max_op_pix_clk_div (RO)	N	N
	Maximum divisor for output pix_clk. Read-only.				
4464 R0x1170	31:0	0x4019999A	min_op_pix_clk_freq_mhz (RO)	N	N
	FLP32. Minimum frequency for output pix_clk is 2.4 MHz. Read-only.				
4468 R0x1174	31:0	0x42C80000	max_op_pix_clk_freq_mhz (RO)	N	N
	FLP32. Maximum frequency for output pix_clk is 100.0 MHz. Read-only.				
4480 R0x1180	15:0	0x0000	x_addr_min (RO)	N	N
	Minimum value for x_addr_start, x_addr_end. Read-only.				

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Table 5: SMIA Parameter Limits Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
4482 R0x1182	15:0	0x0000	y_addr_min (RO)	N	N
	Minimum value for y_addr_start, y_addr_end. Read-only.				
4484 R0x1184	15:0	0x0CCF	x_addr_max (RO)	N	N
	Maximum value for x_addr_start, x_addr_end. Read-only.				
4486 R0x1186	15:0	0x099F	y_addr_max (RO)	N	N
	Maximum value for y_addr_start, y_addr_end. Read-only.				
4544 R0x11C0	15:0	0x0001	min_even_inc (RO)	N	N
	Minimum value for increment of even X/Y addresses when subsampling is enabled. Read-only.				
4546 R0x11C2	15:0	0x0001	max_even_inc (RO)	N	N
	Maximum value for increment of even X/Y addresses when subsampling is enabled. Read-only.				
4548 R0x11C4	15:0	0x0001	min_odd_inc (RO)	N	N
	Minimum value for increment of odd X/Y addresses when subsampling is enabled. Read-only.				
4550 R0x11C6	15:0	0x0007	max_odd_inc (RO)	N	N
	Maximum value for increment of odd X/Y addresses when subsampling is enabled. Read-only. Higher increment values are supported by the sensor, but only the values 1, 3 and 7 for x_odd_inc and 1, 3, 7, 15 and 31 for y_odd_inc. A value of 3 gives 2x subsampling and a value of 7 gives 4x subsampling.				
4608 R0x1200	15:0	0x0002	scaling_capability (RO)	N	N
	Indicates the provision of a full (horizontal and vertical) scaler. Read-only.				
4612 R0x1204	15:0	0x0010	scaler_m_min (RO)	N	N
	Indicates the minimum M value for the scaler. Read-only.				
4614 R0x1206	15:0	0x0064	scaler_m_max (RO)	N	N
	Indicates the maximum M value for the scaler. Read-only.				
4616 R0x1208	15:0	0x0010	scaler_n_min (RO)	N	N
	Indicates the minimum N value for the scaler. Read-only.				
4618 R0x120A	15:0	0x0010	scaler_n_max (RO)	N	N
	Indicates the maximum N value for the scaler. Read-only.				
4864 R0x1300	15:0	0x0001	compression_capability (RO)	N	N
	Indicates the capability for performing 10-bit to 8-bit pixel data compression. Read-only.				
5120 R0x1400	15:0	0x0242	matrix_element_redinred (R/W)	N	N
	Read-only. Can be made read/write by clearing R0x301A-B[3].				
5122 R0x1402	15:0	0xFF00	matrix_element_greeninred (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5124 R0x1404	15:0	0xFFBE	matrix_element_blueinred (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5126 R0x1406	15:0	0xFFB4	matrix_element_redingreen (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5128 R0x1408	15:0	0x0200	matrix_element_greeningreen (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5130 R0x140A	15:0	0xFF4D	matrix_element_blueingreen (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5132 R0x140C	15:0	0xFFF1	matrix_element_redinblue (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				
5134 R0x140E	15:0	0xFF34	matrix_element_greeninblue (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				

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Table 5: SMIA Parameter Limits Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
5136 R0x1410	15:0	0x01DC	matrix_element_blueinblue (R/W)	N	N
	Color-correction matrix. Read-only. Can be made read/write by clearing R0x301A-B[3].				

Manufacturer Specific Register Descriptions

Table 6: Manufacturer-Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12288 R0x3000	15:0	0x4B03	model_id_ (R/W)	N	N
	This register is an alias of R0x3000-1. Read-only. Can be made read/write by clearing R0x301A-B[3]. Legal values: [0, 65535].				
12290 R0x3002	15:0	0x0008	y_addr_start_ (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. Legal values: [0, 2463].				
12292 R0x3004	15:0	0x0008	x_addr_start_ (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. Legal values: [0, 3279].				
12294 R0x3006	15:0	0x0997	y_addr_end_ (R/W)	Y	YM
	The last row of visible pixels to be read out. Legal values: [0, 2463].				
12296 R0x3008	15:0	0x0CC7	x_addr_end_ (R/W)	Y	N
	The last column of visible pixels to read out. Legal values: [0, 3279].				
12298 R0x300A	15:0	0x0A01	frame_length_line_ (R/W)	Y	YM
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Legal values: [0, 65535].				
12300 R0x300C	15:0	0x0E98	line_length_pck_ (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Legal values: [0, 65535].				
12306 R0x3012	15:0	0x0010	coarse_integration_time_ (R/W)	Y	N
	Integration time 1 specified in multiples of line_length_pck_. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12310 R0x3016	15:0	0x0111	row_speed (R/W)	N	N
	15:11	X	Reserved		
	10:8	0x0001	op_speed Slows down the output pixel clock frequency relative to the system clock frequency. A programmed value of N gives a output pixel clock period of N system clocks. Only values 1, 2 and 4 are supported. A value of 0 is illegal: it causes the clock to stop.	N	N
	7	X	Reserved		
	6:4	0x0001	Reserved		
	3	X	Reserved		
	2:0	0x0001	pc_speed Slows down the internal pixel clock frequency relative to the system clock frequency. A programmed value of N gives a pixel clock period of N system clocks. Only values 1, 2 and 4 are supported. A value of 0 is illegal: it causes the clock to stop.	Y	YM
12312 R0x3018	15:0	0x0000	extra_delay (R/W)	Y	N
	extra delay Extra blanking inserted between frames. A programmed value of N increases the vertical blanking time by N pixel clock periods. Can be used to get a more exact frame rate. May affect the integration times of parts of the image when the integration time is less than 1 frame Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12314 R0x301A	15:0	0x0018	reset_register (R/W)		
	15	0x0000	grouped_parameter_hold_ctl Group parameter hold 0: Synchronizes insert of many of the registers to frame start. 1: Inhibits register inserts; register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register inserts will be made on the next frame start.	N	N
	14	0x0000	gain_update_all_frame With this bit set, gain is updated at next frame regardless integration time update. With this bit reset, gain is synced with integration time update.	N	Y
	13	0x0000	fast_integration_time_update 0= integration time update is done conventionally 1= integration time could be updated right next frame	N	N
	12	0x0000	smia_dis This bit disables the SMIA high-speed serializer and differential output buffers.	N	N
	11	0x0000	pll_always_on set to 1, to make PLL always on to shorten the state transaction from standby to streaming. This is used in 3D support mode	N	N
	10	0x0000	restart_bad Restart at bad frame 0: A bad frame will be detected at the end of the frame. 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	gpi_en 0: the primary input buffers associated with the GPI0, GPI1, GPI2, GPI3 inputs are powered down and the GPI cannot be used. 1: the input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0000	Reserved		
	6	0x0000	Reserved		
	5	0x0000	reg_rd_en This bit set to 1 enables signal to allow read from fuse ID registers.	N	N
	4	0x0001	Reserved		
	3	0x0001	lock_reg Many SMIA registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	stream Setting this bit (=1) places the sensor in streaming mode. Clearing this bit (=0) places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N
	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	N
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	N
12316 R0x301C	7:0	0x00	mode_select_ (R/W)	Y	N
	This bit is an alias of R0x301A-B[2].				
12317 R0x301D	7:0	0x01	image_orientation_ (R/W)		
	7:2	X	Reserved		
	1	0x00	image_orientation_vert_flip_ This register field is an alias of R0x3040[15]	Y	YM
	0	0x01	image_orientation_horiz_mirror_ This register field is an alias of R0x3040[14]	Y	YM
12318 R0x301E	15:0	0x002A	data_pedestal_ (R/W)	N	Y
	Constant offset that is added to the ADC output for all visible pixels in order to set the black level to a value greater than 0. Read-only. Can be made read/write by clearing R0x301A-B[3]. Legal values: [0, 1023].				
12321 R0x3021	7:0	0x00	software_reset_ (R/W)	N	Y
	This bit is an alias of R0x301A-B[0].				
12322 R0x3022	7:0	0x00	grouped_parameter_hold_ (R/W)	N	N
	This bit is an alias of R0x301A-B[15].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12323 R0x3023	7:0	0x00	mask_corrupted_frames_ (R/W)	N	N
	This bit is an alias of R0x301A-B[9].				
12324 R0x3024	7:0	0x01	pixel_order_ (RO)	N	N
	Pixel Order 00 = First row is GreenR/Red, first pixel is GreenR 01 = First row is GreenR/Red, first pixel is Red 02 = First row is Blue/GreenB, first pixel is Blue 03 = First row is Blue/GreenB, first pixel is GreenB The value in this register changes as a function of R0x3040[1:0]. Read-only. Legal values: [0, 3].				
12326 R0x3026	15:0	0xFFFF	gpi_status (R/W)	N	N
	15:13	0x0007	standby_pin_select Associate the standby function with an active-high input pin 0: associate with GPI0 1: associate with GPI1 2: associate with GPI2 3: associate with GPI3 4-6: RESERVED 7: standby function cannot be controlled by any pin Must be set to 7 if reset[8]=0. Legal values: [0, 7].	N	N
	12:10	0x0007	oe_n_pin_selct Associate the output-enable function with an active-low input pin 0: associate with GPI0 1: associate with GPI1 2: associate with GPI2 3: associate with GPI3 4-6: RESERVED 7: output-enable function is not controlled by any pin Must be set to 7 if reset[8]=0. Legal values: [0, 7].	N	N
	9:7	0x0007	trigger_pin_select Associate the trigger function with an active-high input pin 0: associate with GPI0 1: associate with GPI1 2: associate with GPI2 3: associate with GPI3 4-6: RESERVED 7: trigger function is not controlled by any pin Must be set to 7 if R0x301A-B[8]=0. Legal values: [0, 7].	N	N
	6:4	0x0007	saddr_pin_select Associate the SADDR function with an active-high input pin 0: associate with GPI0 1: associate with GPI1 2: associate with GPI2 3: associate with GPI3 4-6: RESERVED 7: SADDR function is not controlled by any pin Must be set to 7 if R0x301A-B[8]=0. Legal values: [0, 7].	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	3	0x0001	gpi3 Read-only. Return the current state of the GPI3 input pin. Invalid if R0x301A-B[8]=0.	N	N
	2	0x0001	gpi2 Read-only. Return the current state of the GPI2 input pin. Invalid if R0x301A-B[8]=0.	N	N
	1	0x0001	gpi1 Read-only. Return the current state of the GPI1 input pin. Invalid if R0x301A-B[8]=0.	N	N
	0	0x0001	gpi0 Read-only. Return the current state of the GPI0 input pin. Invalid if R0x301A-B[8]=0.	N	N
12328 R0x3028	7:0	0x02	global_analog_gain_ (R/W)	N	N
	global analog gain. Available analog gains: 0.5x, 0.67x, 1x, 1.34x, 1.5x, 2x, 3, 4x, 6x and 8x Legal values: [0, 32].				
12330 R0x302A	15:0	0x0002	analog_gain_greenr_ (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenr_ analog gain for green R. Legal values: [0, 32].	Y	N
12332 R0x302C	15:0	0x0002	analog_gain_red_ (R/W)	Y	N
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_red_ analog gain for red. Legal values: [0, 32].	Y	N
12334 R0x302E	15:0	0x0002	analog_gain_blue_ (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_blue_ analog gain for blue. Legal values: [0, 32].	Y	N
12336 R0x3030	15:0	0x0002	analog_gain_greenb_ (R/W)		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenb_ analog gain for green B. Legal values: [0, 32].	Y	N
12338 R0x3032	15:0	0x0100	digital_gain_greenr_ (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_greenr_ same as digital_gain_for_greenr_data, gain = register value/128. Legal values: [0, 2047].	Y	N
	0	X	Reserved		

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12340 R0x3034	15:0	0x0100	digital_gain_red_ (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_red_ same as digital_gain_for_blue_data, gain = register value/128. Legal values: [0, 2047].	Y	N
	0	X	Reserved		
12342 R0x3036	15:0	0x0100	digital_gain_blue_ (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_blue_ same as digital_gain_for_red_data, gain = register value/128. Legal values: [0, 2047].	Y	N
	0	X	Reserved		
12344 R0x3038	15:0	0x0100	digital_gain_greenb_ (R/W)		
	15:12	X	Reserved		
	11:1	0x0080	digital_gain_for_greenb_ same as digital_gain_for_greenb_data, gain = register value/128. Legal values: [0, 2047].	Y	N
	0	X	Reserved	N	N
12346 R0x303A	7:0	0x0A	smia_version_ (RO)		
	SMIA version Return the value 10 to indicate an implementation of revision 1.0 of the SMIA specification. Read-only. Read-only. Legal values: [0, 255].				
12347 R0x303B	7:0	0xFF	frame_count_ (RO)	Y	N
	frame count In the soft standby state this counter is set to 0xFF. In streaming state this counter increments by 1 (modulo 255) at the start of each frame. The counter is incremented for both good frames and bad (corrupted) frames - its behavior is not affected by the state of R0x301A-B[9] (mask_corrupted_frames). After entry to the streaming state, the first frame will show a frame count of 0x01 in its embedded data. Read-only. Read-only. Legal values: [0, 255].				
12348 R0x303C	15:0	0x0002	frame_status (RO)	N	N
	15:2	X	Reserved		
	1	RO	frame_status_standby frame status standby This bit tells you whether the sensor is in standby state. Can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit 0x301A[4]. Read-only.	N	N
	0	RO	frame_status_framesync frame status frame synced Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization. Read-only.	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12350 R0x303E	15:0	0x0000	read_style (R/W)	N	N
	15:5	X	Reserved		
	4	0x0000	hdr_dark_row_ignore_t2 When set, dark rows are integrated with only T1 integration when hdr_enable is set.	N	N
	3:2	X	Reserved		
	1	0x0000	hdr_first_field 0: The first two rows readout and every subsequent alternate two rows are with exposure time T1	N	N
	0	0x0000	hdr_enable Enable iHDR 0: disable 1: enable	N	N
12352 R0x3040	15:0	0x4041	read_mode (R/W)		
	15	0x0000	vert_flip 0 = Normal readout 1 = Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order (see R0x3024).	Y	YM
	14	0x0001	horiz_mirror 0 = Normal readout 1 = Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order (see R0x3024).	Y	YM
	13	0x0000	row_sum Enable analog summing in Y (row) direction. When set, y_odd_inc must be set to 3 for row summing along with other register changes	Y	N
	12	0x0000	eis_mode when eis_mode is 1, to disable the bad frame generation when y_start/_end is changed within the window	Y	N
	11	0x0000	x_bin_en Enable analog binning in X (column) direction. When set, additionally x_odd_inc must be set to 3 for column binning along with other register changes.	Y	N
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8:6	0x0001	x_odd_inc Increment applied in X (column) direction. Read out 1= Normal 3= 1 out of 2 pixels 7= 1 out of 4 pixels	Y	YM
	5:0	0x0001	y_odd_inc Increment applied in Y (row) direction. Read out 1= Normal 3= 1 out of 2 pixels 7= 1 out of 4 pixels 15= 1 out of 8 pixels 31= 1 out of 16 pixels, not supported for AR0833 63= 1 out of 32 pixels; not supported for AR0833	Y	YM

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12358 R0x3046	15:0	0x0608	flash (R/W)		
	15	RO	flash_strobe Reflects the current state of the FLASH output signal. Read-only. Read-only.	N	N
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only. Read-only.	N	N
	13	0x0000	xenon_flash When set, the FLASH output signal will assert for the programmed period (bits [7:0]) during vertical blanking. This is achieved by keeping the integration time equal to one frame, and the pulse width less than the vertical blanking time.	Y	N
	12:11	0x0000	flash_frame_delay Flash pulse delay measured in frames. 00: no delay. 01: one frame delay 10: two frames delay 11: three frames delay Legal values: [0, 3].	N	N
	10	0x0001	flash_end_of_reset 1 = In Xenon mode, the flash is triggered after resetting a frame. 0 = In Xenon mode, the flash is triggered after a frame readout.	N	N
	9	0x0001	every_frame 0 = Flash should be enabled for 1 frame only. 1 = Flash should be enabled every frame.	N	N
	8	0x0000	led_flash Enable LED flash. When set, the FLASH output signal will assert prior to the start of the resetting of a frame and will remain asserted until the end of the frame readout.	Y	Y
	7	0x0000	flash_invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	6	0x0000	flash_xenon_no_delay 1: At the start of streaming, no frame delay will occur before the xenon flash pulse is triggered.	N	N
	5	X	Reserved		
	4	0x0000	flash_trigger_timed 1 = Enable Flash Count	N	N
	3:0	0x0008	flash_scale scale the flash count down counter with 2^(flash_scale+1) Legal values: [0, 15].	N	N
12360 R0x3048	15:0	0x0008	flash_count (R/W)		
	Length of flash pulse when Xenon flash is enabled. The value specifies the length in units of 256 x system_clock. When the Xenon count is set to its maximum value (0x3FF), the flash pulse will automatically be truncated prior to the readout of the first row, giving the longest pulse possible. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12362 R0x304A	15:0	0x0000	otpm_control (R/W)		
	15:11	X	Reserved		
	10	0x0000	otpm_control_enable_standby OTPM control enable standby When this bit is 0, the standby signal will never be asserted to the HV switch. When this bit is 1, the standby signal will be controlled automatically to the HV switch: negated when an OTPM read or write operation is being performed, and asserted otherwise. Asserting the standby signal to the HV switch connects the internal vcmn signal to gndio preventing leakage though any programmed anti-fuses.	N	N
	9	0x0000	otpm_control_single_record_only When set, automatic read sequence will end after one record is read out	N	N
	8	0x0000	otpm_control_auto_rd_start_next To be used when otpm_control_single_record_only = 1 and otpm_expr_bypass_record = 0. Triggers automatic OTPM read sequence to read the next record; bit 6 and bit 9 should both be set to 1.	N	N
	7	X	Reserved		
	6	RO	otpm_control_auto_rd_success Indicates whether the automatic read sequence was successful. Read-only.	N	N
	5	RO	otpm_control_auto_rd_end Indicates whether the automatic read sequence is finished. Read-only.	N	N
	4	0x0000	otpm_control_auto_rd_start Triggers automatic OTPM read sequence. When otpm_expr_bypass_record = 1, the OTPM address to start will be taken from OTPM manual control register bits [15:8]. The length of the data to read is taken from OTPM (0x304C) record control register bits [7:0]. The data taken from OTPM will appear in otpm_data* registers. When otpm_expr_bypass_record =0, record(s) may be read out by record type (OTPM record (0x304C) [15:8]) or by OTPM address 0x3050 (OTPM manual control [6:0]). The payload of the record(s) will appear in otpm_data* registers.	N	N
	3	0x0000	disable_auto_read When register bit is set to 1, disable automatic OTPM read sequence.	N	N
	2	RO	otpm_control_auto_wr_success 1: Indicates whether the automatic write sequence was successful. Read-only.	N	N
	1	RO	otpm_control_auto_wr_end 1: Indicates whether the automatic write sequence is finished. Read-only.	N	N
	0	0x0000	otpm_control_auto_wr_start Trigger automatic OTPM write sequence The high voltage must be available on the high voltage pad before this sequence is triggered. The OTPM address to start will be taken from OTPM manual control register bits [15:8]. The length of the data to program is taken from OTPM record control register bits [6:0]. The data is taken from otpm_data* (beginning at R0x3800) registers.	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12364 R0x304C	15:0	0x0200	otpm_record (R/W)		
	15:8	0x0002	otpm_record_record_type Type of record Currently supported types are 0x02: Default registers loaded before software standby 0x1n: Default registers loaded after software standby 0x2n: Register sets Other types are only available for read-back from the OTPM RAM through the otpm_data_* (beginning at 0x3800) registers Legal values: [0, 255].	N	N
	7:0	0x0000	otpm_record_record_length Length of record payload in 16-bit words (between 1 and 255) Legal values: [0, 255].	N	N
12366 R0x304E	15:0	0x0000	otpm_status (RO)		
	15:12	X	Reserved		
	11	RO	otpm_status_op_busy OTPM busy status bit. When bit is high, the OTPM state machine is not idle. Read-only.	N	N
	10	RO	otpm_status_otpm_insufficient 1: Insufficient OTPM space to include a record Read-only.	N	N
	9	RO	otpm_status_otpm_full 1: OTPM is full Read-only.	N	N
	8	RO	otpm_status_ded_parity_failure 1: Double error-detect parity failure, data bad Read-only.	N	N
	7	RO	otpm_status_sec_used 1: ECC single bit error correction activated Read-only.	N	N
	6:1	RO	otpm_status_ecc_check_bits Check bits produced by ECC Read-only. Legal values: [0, 64].	N	N
	0	RO	otpm_status_op_done 1: Read/Write Operation complete Read-only.	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12368 R0x3050	15:0	0x0000	otpm_manual_control (R/W)	N	N
	15:7	X	Reserved		
	6	RO	otpm_manual_control_single_rd_success 1: Indicates whether the single read sequence was successful. Read-only.	N	N
	5	RO	otpm_manual_control_single_rd_end 1: Indicates whether the single read sequence is finished. Read-only.	N	N
	4	0x0000	otpm_manual_control_single_rd_start 1: Trigger single OTPM read sequence from the memory address programmed in otpm_manual_control[14:8].	N	N
	3	X	Reserved		
	2	RO	otpm_manual_control_single_wr_success 1: Indicates whether the single write sequence was successful. Read-only.	N	N
	1	RO	otpm_manual_control_single_wr_end Indicates whether the single write sequence is finished. Read-only.	N	N
	0	0x0000	otpm_manual_control_single_wr_start 1: Triggers single OTPM write sequence The high voltage must be available on the high voltage pad before this sequence is triggered. otpm_manual_control[14:8] is the address of the memory cell that will be programmed to 1. A single read sequence will automatically be triggered for the same address. This can be used to determine whether the program was successful.	N	N
12370 R0x3052	15:0	0x0000	otpm_manual_address (R/W)		
	15:13	X	Reserved		
	12:0	0x0000	otpm_manual_address_otpm_address Address of the OTPM used for single writes/reads as well as auto writes/reads. Legal values: [0, 8191].	N	N
12372 R0x3054	15:0	0x0000	otpm_expr (R/W)		
	15:12	X	Reserved		
	11	0x0000	otpm_expr_trigger_auto_ram_load Load current content of the OTPM RAM to registers.	N	N
	10	0x0000	otpm_expr_disable_auto_ram_load Disable automatic RAM load for record types supporting RAM load.	N	N
	9	0x0000	otpm_expr_ecc_bypass When set the ECC logic will be bypassed.	N	N
	8	0x0000	otpm_expr_bypass_record When enabled the record structure will be bypassed. Data in otpm_data* will be written directly to the OTPM.	N	N
	7:0	X	Reserved		

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12374 R0x3056	15:0	0x1000	green1_gain (R/W)	Y	N
	15:5	0x0080	digital_gain_for_greenr_data digital gain for greenR pixel gain = register value/128. Legal values: [0, 2047].	Y	N
	4:2	0x0000	adc_gain_for_greenr adc gain, only global gain is available for analog gain. Legal values: [0, 7].	Y	N
	1:0	0x0000	column_amp_gain_for_greenr column amp gain, only global gain is available for analog gain. Legal values: [0, 3].	Y	N
12376 R0x3058	15:0	0x1000	blue_gain (R/W)		
	15:5	0x0080	digital_gain_for_blue_data digital gain for red pixel gain = register value/128. Legal values: [0, 2047].	Y	N
	4:2	0x0000	adc_gain_for_blue adc gain, only global gain is available for analog gain. Legal values: [0, 7].	Y	N
	1:0	0x0000	column_amp_gain_for_blue column amp gain, only global gain is available for analog gain. Legal values: [0, 3].	Y	N
12378 R0x305A	15:0	0x1000	red_gain (R/W)		
	15:5	0x0080	digital_gain_for_red_data digital gain for blue pixel gain = register value/128. Legal values: [0, 2047].	Y	N
	4:2	0x0000	adc_gain_for_red adc gain, only global gain is available for analog gain. Legal values: [0, 7].	Y	N
	1:0	0x0000	column_amp_gain_for_red column amp gain, only global gain is available for analog gain. Legal values: [0, 3].	Y	N
12380 R0x305C	15:0	0x1000	green2_gain (R/W)		
	15:5	0x0080	digital_gain_for_greenb_data digital gain for greenB pixel gain = register value/128. Legal values: [0, 2047].	Y	N
	4:2	0x0000	adc_gain_for_greenb adc gain, only global gain is available for analog gain. Legal values: [0, 7].	Y	N
	1:0	0x0000	column_amp_gain_for_greenb column amp gain, only global gain is available for analog gain. Legal values: [0, 3].	Y	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12382 R0x305E	15:0	0x1000	global_gain (R/W)		
	15:5	0x0080	global_digital_gain global digital gain, gain = register value/128. Legal values: [0, 2047].	Y	N
	4:2	0x0000	global_adc_gain global adc gain. set global_adc_gain[2]=1, enable 0.5x gain Legal values: [0, 7].	Y	N
	1:0	0x0000	global_column_amp_gain global column amp gain. Legal values: [0, 3].	Y	N
12394 R0x306A	15:0	0x0000	odp_status (RO)		
	15:6	X	Reserved		
	5	RO	mipi_preamble_err MIPI preamble error 1: A fatal error occurred because frame pixel data arrived at the MIPI data framer before the MIPI wake-up sequence and start-of-frame short packet had completed. Probable cause is that the value programmed for FRAME_PREAMBLE is too small. Read-only.	N	N
	4	RO	mipi_line_byte_err MIPI line byte error 1: A fatal error occurred because the line length of the pixel data that the MIPI serializer expected to transmit did not match the line length set by X_OUTPUT_SIZE. Read-only.	N	N
	3:0	X	Reserved		
12398 R0x306E	15:0	0x9080	data_path_select (R/W)		
	15:13	0x0004	slew_a slew rate control for all pins Legal values: [0, 7].	N	N
	12:10	0x0004	Reserved		
	9:8	X	Reserved		
	7	RO	profile12 SMIA profile mode Read-only. Legal values: [1, 1].	N	N
	6	0x0000	sum_2x2 1: Selects sum 2x2 mode	N	N
	5	0x0000	true_bin 1: Selects true bin mode	N	N
	4	0x0000	true_bayer 1: Selects true bayer mode	N	N
	3:2	X	Reserved		
	1	0x0000	xor_lv XOR LV	N	N
	0	0x0000	cont_lv cont LV	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12400 R0x3070	15:0	0x0000	test_pattern_mode_ (R/W)		
	15:10	X	Reserved		
	9:8	0x0000	walking_one_pattern_enable_ Walking one pattern 256: Walking 1s test pattern (10-bit) 257: Walking 1s test pattern (8-bit) Other = Reserved. Legal values: [0, 1].	N	N
	7:3	X	Reserved		
	2:0	0x0000	test_pattern_select_ select test pattern 0: Normal operation, Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to gray color bar test pattern 4: PN9 Link integrity test pattern	N	N
12402 R0x3072	15:0	0x0000	test_data_red_ (R/W)		
	red test data for solid test pattern. Legal values: [0, 1023].				
12404 R0x3074	15:0	0x0000	test_data_greenr_ (R/W)		
	greenR test data for solid test pattern. Legal values: [0, 1023].				
12406 R0x3076	15:0	0x0000	test_data_blue_ (R/W)		
	blue test data for solid test pattern. Legal values: [0, 1023].				
12408 R0x3078	15:0	0x0000	test_data_greenb_ (R/W)	N	Y
	greenB test data for solid test pattern. Legal values: [0, 1023].				
12410 R0x307A	15:0	0x0000	test_raw_mode (R/W)		
	15:2	X	Reserved		
	1	0x0000	test_pat_override 1: Prevents test_pattern from turning off corrections	N	N
	0	0x0000	raw_data Enable this bit to turn off all corrections	N	N
12448 R0x30A0	15:0	0x0001	x_even_inc_ (RO)		
	Read-only.				
12450 R0x30A2	15:0	0x0001	x_odd_inc_ (R/W)	Y	YM
	This register field is an alias of R0x3040[8:6] Legal values: [0, 7].				
12452 R0x30A4	15:0	0x0001	y_even_inc_ (RO)	Y	YM
	Read-only.				
12454 R0x30A6	15:0	0x0001	y_odd_inc_ (R/W)	Y	YM
	This register field is an alias of R0x3040[5:0] Legal values: [0, 63].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12466 R0x30B2	15:0	0x0000	tempsens_data (RO)	N	N
	15:10	X	Reserved		
	9:0	RO	tempsense_data Data from temperature sensor Read-only. Legal values: [0,1023].	N	N
12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)		
	15:6	X	Reserved		
	5	0x0000	temp_clear_value 1: Clears value in tempsens_data (R0x30B2[9:0]).	N	N
	4	0x0000	temp_start_conversion tempsens start conversion when set	N	N
	3:1	0x0000	tempsens_test_ctrl tempsens test ctrl Legal values: [0, 7].	N	N
	0	0x0000	tempsens_power_on 1: Turns on temperature sensor 0: Turns off temperature sensor	N	N
	control register for temp sensor				
12476 R0x30BC	15:0	0x0000	y_output_offset (R/W)	N	Y
	Number of rows offset to start of the displayed image (Y output size) Legal values: [0, 4095].				
12478 R0x30BE	15:0	0x0000	x_output_offset (R/W)	N	Y
	Number of columns offset to start of the displayed image (X output size) Legal values: [0,4095].				
12524 R0x30EC	15:0	0x0000	ctx_rd_data (R/W)	N	N
	context read data Legal values: [0, 65535].				
12528 R0x30F0	15:0	0x0000	vcm_control (R/W)	N	N
	15	0x0000	vcm_en 1: Disables VCM driver.	N	N
	14:12	X	Reserved		
	11:8	0x0000	Reserved		
	7:4	X	Reserved		
	3	0x0000	vcm_disable_pd 1: VCM is not disabled in standby state	N	N
	2:0	0x0000	vcm_slew Programmable counter to define the mode and the step transition time to refresh the target code to VCM DAC. vcm_slew=0: mode 0, refresh the code directly to target code vcm_slew>0: mode 1, increment/decrement 1 code every step transition time to target code step transition time = Tsysclk * 16 * Legal values: [0, 7].	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12530 R0x30F2	15:0	0x0000	vcm_new_code (R/W)	N	N
	New target code to VCM DAC. Legal values: [0, 255].				
12532 R0x30F4	15:0	0x0000	vcm_step_time (R/W)	N	N
	Programmable counter to define how many system clocks for each step time. vcm step time = Tsysclk * 16 * (vcm_step_time[15:0] + 1) Legal values: [0, 65535].				
12536 R0x30F8	15:0	0x0003	gpio_ctrl (R/W)		
	15:2	X	Reserved		
	1	0x0001	gpio1_oe GPIO1 output enable	N	N
	0	0x0001	gpio0_oe GPIO0 output enable	N	N
12592 R0x3130	15:0	0x7801	otpm_tcfg_write_01 (R/W)		
	15:8	0x0078	otpm_tcfg_write_01_write_1 Duration of TMG_WR_PROGRAM state in the RTL module otpm_core_tmg_40is This value multiplied by 256 equals the duration hvstate equals 3'b110. Legal values: [0, 255].	N	N
	7:4	0x0000	otpm_tcfg_write_pre2 Duration of TMG_WR_PRE2 state in the RTL module otpm_core_tmg_40is This equals the delay between vcmn_write going high and the address being assigned to the OTPM addr port. Legal values: [0, 15].	N	N
	3:0	0x0001	otpm_tcfg_write_pre1 Duration of TMG_WR_PRE1 state in the RTL module otpm_core_tmg_40is This equals the delay between hvstate=3'b010 and vcmn_write going high. Legal values: [0, 15].	N	N
12594 R0x3132	15:0	0x0021	otpm_tcfg_write_23 (R/W)		
	15:8	0x0000	Reserved		
	7:4	0x0002	otpm_tcfg_write_post2 Duration of TMG_WR_POST3 state in the RTL module otpm_core_tmg_40is. This value multiplied by 4 equals the delay between vcmn_standby going high and hvstate being set to 3'b000. Legal values: [0, 15].	N	N
	3:0	0x0001	otpm_tcfg_write_post1 Duration of TMG_WR_POST2 state in the RTL module otpm_core_tmg_40is. This equals the delay between vcmn_write going low and vcmn_standby going high. Legal values: [0, 15].	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12596 R0x3134	15:0	0x0D95	otpm_tcfg_read_01 (R/W)	N	N
	15	0x0000	otpm_tcfg_read_grab This bit determines when to grab the data from the OTPM: 0 = data is sampled when the OTPM IP pin goes high. 1 = data is sampled after a time determined by bits 14:12.	N	N
	14:12	0x0000	otpm_tcfg_read_read When bit 15 is set these bits multiplied by 8 determines the duration of TMG_RD_READ state in the RTL module otpm_core_tmg_40is. This equals the delay between hvstate=3'b101 and the dout data from the OTPM is grabbed. Legal values: [0, 7].	N	N
	11:8	0x000D	otpm_tcfg_read_post3 Duration of TMG_WR_POST3 state in the RTL module otpm_core_tmg_40is. This equals the delay between vcmn_standby going high and hvstate=3'b000. Legal values: [0, 15].	N	N
	7:4	0x0009	otpm_tcfg_read_post2 Duration of TMG_RD_POST2 state in the RTL module otpm_core_tmg_40is. This equals the delay between vcmn_read going low and vcmn_standby going high. Legal values: [0, 15].	N	N
	3:0	0x0005	otpm_tcfg_start2 Duration of TMG_RD_START2 state in the RTL module otpm_core_tmg_40is. This equals the delay between vcmn_read going high and hvstate=3'b001. Legal values: [0, 15].	N	N
12598 R0x3136	15:0	0x0000	otpm_tcfg_read_23 (R/W)	N	N
	15:12	0x0000	Reserved		
	11:8	0x0000	otpm_tcfg_state_cnt Scaling value for the OTPM timing. Add one and multiply that value by two master clock cycles to get the OTPM timing step size. All other programmable timing values must be multiplied by this OTPM step size to get the real value. Legal values: [0, 15].	N	N
	7:0	0x0000	Reserved		
12602 R0x313A	15:0	0x0000	otpm_manual_l (R/W)		
	Data to be written to/read back from OTPM in single write/read mode When ECC bypass = 0, this register corresponds to [15:0] of the 32-bit data of the OTPM address. When ECC bypass = 1, this register corresponds to [15:0] of the 40-bit data of the OTPM address. Legal values: [0, 65535].				
12604 R0x313C	15:0	0x0000	otpm_manual_h (R/W)		
	Data to be written to/read back from OTPM in single write/read mode When ECC bypass = 0, this register corresponds to [31:16] of the 32-bit data of the OTPM address. When ECC bypass = 1, this register corresponds to [31:16] of the 40-bit data of the OTPM address. Legal values: [0, 65535].				
12606 R0x313E	15:0	0x0000	otpm_manual_extra (R/W)		
	Data to be written to/read back from OTPM in single write/read mode. When ECC bypass = 0, this register is not used. When ECC bypass = 1, this register corresponds to [39:32] of the 40-bit data of the OTPM address. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12632 R0x3158	15:0	0x0000	slave_mode_control (R/W)		
	15	0x0000	vd_trig_new_frame vd trigger new frame 1: Enables slave mode	N	N
	14	0x0000	vd_timer vd timer 1: Limits the detection of slave mode trigger pulse around internal start of frame	N	N
	13	0x0000	vd_trig_grst vd triggered grst 1: Enables slave mode in global reset mode	N	N
	12:0	X	Reserved		
12634 R0x315A	15:0	0x0000	global_flash_start (R/W)	N	Y
	Global Flash Start If global_seq_trigger[2]=1 (Global Flash enabled) and global_seq_trigger[6]=1 (Use Flash Start), when a Global Reset sequence is triggered, the FLASH output signal will be pulsed during the integration phase of the Global Reset sequence. The start of the FLASH pulse is determined by global_flash_start. If global_flash_start<global_rst_end, the FLASH pulse will only be asserted at a fixed delay after global_rst_end. The FLASH output will not be asserted if global_flash_start>global_read_start. Legal values: [0, 65535].				
12636 R0x315C	15:0	0x0000	global_bulb_trigger_count (R/W)		
	Bulb Trigger Count If global_seq_trigger[1]=1 (Global Bulb enabled) when a Global Reset sequence is triggered and global_seq_trigger[10]=1 (Bulb Trigger Timer), the end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale). Legal values: [0, 65535].				
12638 R0x315E	15:0	0x0000	global_seq_trigger (R/W)	N	Y
	15:12	0x0000	global_seq_trigger_bulb_trig_scale Bulb Trigger Scale If global_seq_trigger[1]=1 (Global Bulb enabled) when a Global Reset sequence is triggered and global_seq_trigger[10]=1 (Bulb Trigger Timer), the end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale). Bulb Trigger Scale determines the number of cycles per count: 00 = 256 cycles per count 01 = 1024 cycles per count 10 = 64 cycles per count 11 = 1 cycle per count Legal values: [0, 15].	N	N
	11	X	Reserved		
	10	0x0000	global_seq_trigger_bulb_trig_tmr Bulb Trigger If global_seq_trigger[1]=1 (Global Bulb enabled) when a Global Reset sequence is triggered this bits determines how the integration time is controlled: 0 = The end of the integration phase is controlled by the level of trigger (global_seq_trigger[0], or the associated GPI input). 1 = The end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale).	N	Y
	9:8	X	Reserved		
	7	0x0000	global_seq_trigger_flash_sync When set, the flash output in global reset bulb mode will start after the falling edge of the global reset trigger signal.	N	Y

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	6	0x0000	global_seq_trigger_use_flash_start When set, the start of the FLASH pulse is determined by global_flash_start.	N	Y
	5:4	0x0000	global_seq_trigger_global_scale Global Scale Decoded value (called GlobalScaleFactor) of this field is used as the step size for duration of integration time/shutter starting from end of row reset phase of Global reset. The field is decoded as 0 = 512 1 = 2048 2 = 128 3 = 32 I.E. for integration time, of a value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N - global_reset_end[15:0])* GlobalScaleFactor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 3].	N	N
	3	X	Reserved		
	2	0x0000	global_seq_trigger_global_flash Global Flash 0 = When a Global Reset sequence is triggered, the FLASH output will remain negated. 1 = When a Global Reset sequence is triggered, the FLASH output will pulse during the integration phase.	N	Y
	1	0x0000	global_bulb Global Bulb 0 = Shutter open is triggered from bit[0] and shutter close is timed from the trigger point. 1 = Shutter open and close are triggered from bit[0]. This corresponds to the shutter "B" setting on a traditional camera, where "B" originally stood for "Bulb" (the shutter setting used for synchronization with a magnesium foil flash bulb) and was later considered to stand for "Brief" (an exposure that was longer than the shutter could automatically accommodate).	N	N
	0	0x0000	global_trigger Global Trigger When bit[1]=0, a 0-to-1 transition of this bit initiates (triggers) a global reset sequence. When bit[1]=1,a 0-to-1 transition of this bit initiates a global reset sequence, and leaves the shutter open; a 1-to-0 transition of this bit closes the shutter. These operations can also be controlled from the signal interface by enabling one of the GPI[3:0] signals as a trigger input.	N	N
12640 R0x3160	15:0	0x00EC	global_rst_end (R/W)	N	N
	Controls the duration of the global reset row reset phase. A value of N gives a duration of N * 512 / vt_pix_clk_freq_mhz. Legal values: [0, 65535].				
12642 R0x3162	15:0	0x0317	global_shutter_start (R/W)	N	N
	Global Shutter Start Bits 15-0 of a 24-bit value which controls the delay before the assertion of the SHUTTER output during a global reset sequence. A value of N of the 24 bit field {global_stutter_start2[7:0], global_shutter_start} gives an assertion time of (N - global_reset_end[15:0])* GlobalScaleFactor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12644 R0x3164	15:0	0x0000	global_shutter_start2 (R/W)		
	Global Shutter Start 2 Bits 23-16 of a 24-bit value which controls the delay before the assertion of the SHUTTER output during a global reset sequence. A value of N of the 24 bit field {global_stutter_start2[7:0], global_shutter_start} gives an assertion time of (N - global_reset_end[15:0])* GlobalScaleFactor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 255].				
12646 R0x3166	15:0	0x0327	global_read_start (R/W)		
	Global Read Start Bits 15-0 of a 24-bit value which controls the delay before the start of the global reset readout phase (equivalent to the end of global reset integration phase). A value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N - global_reset_end[15:0])* GlobalScaleFactor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 65535].				
12648 R0x3168	15:0	0x0000	global_read_start2 (R/W)	N	N
	Global Read Start2 Bits 23-16 of a 24-bit value which controls the delay before the start of the global reset readout phase (equivalent to the end of global reset integration phase). A value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N - global_reset_end[15:0])* GlobalScaleFactor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 255].				
12658 R0x3172	15:0	0x0286	analog_control2 (R/W)		
	15:14	X	Reserved		
	13	0x0000	Reserved		
	12	0x0000	Reserved		
	11:10	X	Reserved		
	9:8	0x0002	Reserved		
	7	0x0001	Reserved		
	6:5	0x0000	Reserved		
	4	0x0000	pix_internal_reset Enable pixel internal reset timing. This sensor has pixel internal reset timing as default, so this register is not intended to be used.	N	N
	3	0x0000	Reserved		
	2	0x0001	Reserved		
	1:0	0x0002	Reserved		
12704 R0x31A0	15:0	0x0201	serial_format_descriptor_0 (RO)	N	N
	serial_format_descriptor_0 Read-only. Legal values: [0, 65535].				
12706 R0x31A2	15:0	0x0202	serial_format_descriptor_1 (RO)	N	N
	serial_format_descriptor_1 Read-only. Legal values: [0, 65535].				
12708 R0x31A4	15:0	0x0204	serial_format_descriptor_2 (RO)	N	N
	serial_format_descriptor_2 Read-only. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12710 R0x31A6	15:0	0x0301	serial_format_descriptor_3 (RO)	N	N
	serial_format_descriptor_3 Read-only. Legal values: [0, 65535].				
12712 R0x31A8	15:0	0x0302	serial_format_descriptor_4 (RO)	N	N
	serial_format_descriptor_4 Read-only. Legal values: [0, 65535].				
12714 R0x31AA	15:0	0x0304	serial_format_descriptor_5 (RO)	N	N
	serial_format_descriptor_5 Read-only. Legal values: [0, 65535].				
12716 R0x31AC	15:0	0x0000	serial_format_descriptor_6 (RO)		
	serial_format_descriptor_6 Read-only. Legal values: [0, 65535].				
12718 R0x31AE	15:0	0x0204	serial_format (R/W)	N	N
	15:10	X	Reserved		
	9:8	0x0002	serial__format_type serial interface type 2: MIPI 3:HiSPi 0 and 1 reserved.	N	N
	7:3	X	Reserved		
	2:0	0x0004	serial__format_lanes Serial data lanes Legal values: [0, 7].	N	N
12720 R0x31B0	15:0	0x0071	frame_preamble (R/W)	N	N
	frame preamble This timing value, expressed in op_pix_clk periods, must be large enough to allow the MIPI wake-up and start-of-frame short packet to be transmitted prior to the start of a frame of pixel data. The default value should be correct for most applications. Too small a value will result in an INSUFFICIENT_FRAME_PREAMBLE error being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].				
12722 R0x31B2	15:0	0x0042	line_preamble (R/W)		
	line preamble This timing value, expressed in op_pix_clk periods, must be large enough to allow the MIPI long packet header to be transmitted prior to the start of a line of pixel data. The default value should be correct for most applications. Too small a value will result in an INSUFFICIENT_LINE_PREAMBLE error being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12724 R0x31B4	15:0	0x2E78	mipi_timing_0 (R/W)		
	15:12	0x0002	t_hs_prepare Time (in clk cycles) to drive LP-00 prior to entering HS data transmission mode Legal values: [0, 15].	N	N
	11:8	0x000E	t_hs_zero Time, in op_pix_clk periods, to drive HS-0 before the sync sequence Legal values: [0, 15].	N	N
	7:4	0x0007	t_hs_trail Time, in op_pix_clk periods, to drive flipped differential state after last payload data bit of an HS transmission burst Legal values: [0, 15].	N	N
	3:0	0x0008	t_clk_trail Time, in op_pix_clk periods, to drive HS differential state after last payload clock bit of an HS transmission burst Legal values: [0, 15].	N	N
12726 R0x31B6	15:0	0x129D	mipi_timing_1 (R/W)		
	15:12	0x0001	t_clk_prepare Time, in op_pix_clk periods, to drive LP-00 prior to entering HS data transmission mode Legal values: [0, 15].	N	N
	11:6	0x000A	t_hs_exit Time, in op_pix_clk periods, to drive LP-11 after HS burst Legal values: [0, 63].	N	N
	5:0	0x001D	t_clk_zero Minimum time, in op_pix_clk periods, to drive HS-0 on clock lane prior to starting clock Legal values: [0, 63].	N	N
12728 R0x31B8	15:0	0x404C	mipi_timing_2 (R/W)		
	15:12	0x0004	t_bgap bandgap settling time Legal values: [0, 15].	N	N
	11:6	0x0001	t_clk_pre Time, in op_pix_clk periods, to drive the HS clock before any data lane might start up Legal values: [0, 63].	N	N
	5:0	0x000C	t_clk_post Time, in op_pix_clk periods, to drive the HS clock after the data lane has gone into low-power mode Legal values: [0, 63].	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12730 R0x31BA	15:0	0x028D	mipi_timing_3 (R/W)		
	15:13	0x0000	reg_vset reg_vset Legal values: [0, 7].	N	N
	12:7	0x0005	t_lpx Time, in op_pix_clk periods, of any low-power state period Legal values: [0, 63].	N	N
	6:0	0x000D	t_wake_up Time to recover from ultra low-power mode (ULPM). ULPM is exited by applying a mark state for (8192) * T_WAKE_UP * op_pix_clk Legal values: [0, 127].	N	N
12732 R0x31BC	15:0	0x000A	mipi_timing_4 (R/W)		
	15	0x0000	cont_tx_clk Continuous clock mode for MIPI 0: Disable 1: Enable	N	N
	14	0x0000	heavy_lp_load_in control of phy heavy_lp_load pin	N	N
	13:7	X	Reserved		
	6:0	0x000A	t_init Initialization time when first entering stop state (LP-11) after power up or reset. LP-11 is transmitted for a minimum of (1024) * T_INIT * op_pix_clk. Legal values: [0, 127].	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12734 R0x31BE	15:0	0xC003	mipi_config (R/W)		
	15	RO	reg_frame_sync Safe to update the frame synced registers 1: Safe to update the frame synced registers Read-only.	N	N
	14	RO	mipi_standby MIPI standby 1: MIPI standby Read-only.	N	N
	13	RO	mipi_rdy_for_data MIPI ready for data 1: MIPI ready for data Read-only.	N	N
	12:11	X	Reserved		
	10	0x0000	mipi_mirror_2lanes Mirror mipi lanes 0,1 to lanes 2,3	N	N
	9	0x0000	test_mipi_start_checksum Starts MIPI checksum 1: Starts MIPI checksum	N	N
	8:4	X	Reserved		
	3:2	0x0000	hispi_phy_mode HISPI PHY Mode 00: select SLVS phy signalling internal regulator 01: select SLVS phy signalling external regulator 10: select sub-LVDS phy signalling 11: select HiVcm phy signalling Legal values: [0, 3].	N	N
	1	0x0001	frame_cnt_reset Reset MIPI frame count 1: Reset MIPI frame count	N	N
	0	0x0001	frame_cnt_en Enables MIPI frame count 1: Enables MIPI frame count	N	N

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12736 R0x31C0	15:0	0x8000	hispi_timing (R/W)		
	15	0x0001	hispi_reva_comp should always be tied to "1"	N	N
	14:12	0x0000	hispi_timing_clock_del Delay applied to the clock lane in 1/8 unit interval (UI) steps. Legal values: [0, 7].	N	N
	11:9	0x0000	hispi_timing_data3_del Delay applied to Data Lane 3 in 1/8 unit interval (UI) steps. Legal values: [0, 7].	N	N
	8:6	0x0000	hispi_timing_data2_del Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps. Legal values: [0, 7].	N	N
	5:3	0x0000	hispi_timing_data1_del Delay applied to Data Lane 1 in 1/8 unit interval (UI) steps. Legal values: [0, 7].	N	N
	2:0	0x0000	hispi_timing_data0_del Delay applied to Data Lane 0 in 1/8 unit interval (UI) steps. Legal values: [0, 7].	N	N
12738 R0x31C2	15:0	0xFFFF	hispi_blanking (R/W)		
	HiSpi Blanking Data Legal values: [0, 65535].				
12740 R0x31C4	15:0	0xF555	hispi_sync_patt (R/W)		
	HiSpi Sync Pattern Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)	N	N
	15	RO	mipi_hispi_idle 1: MIPI/HiSPi idle Read-only.	N	N
	14	RO	checksum_valid 1: Checksum valid Read-only.	N	N
	13	0x0000	mask_framer_standby 1: Mask framer standby	N	N
	12	0x0000	transmit_checksum 1: Transmits checksum	N	N
	11:10	0x0000	hispi_mode_select Selects HiSPi mode 00: HiSPiS protocol 01: HiSPiSP protocol 10: HiSPi Actistart- SP8 protocol Legal values: [0, 3].	N	N
	9	0x0000	test_hispi_start_checksum 1: Start HiSPi checksum	N	N
	8	0x0000	io_tri_state_test 1: Initiates IO tri_state test	N	N
	7	0x0000	framer_test_mode_enable 1: Enables framer test mode.	N	N
	6:4	0x0000	framer_test_mode framer test modes Legal values: [0, 7].	N	N
	3	0x0000	blanking_data_enable 1: Enables blanking data	N	N
	2	0x0000	hispi_sp_protocol Selects HiSPi sp protocol 0: Packetized 1: Streaming	N	N
	1	0x0000	output_msb_first 1: Outputs MSB first	N	N
	0	0x0000	vert_left_bar_en 1: Vertical left bar enabled	N	N
12744 R0x31C8	15:0	0x0000	hispi_ckecksum0 (RO)	N	N
	hispi_ckecksum0 Read-only. Legal values: [0, 65535].				
12746 R0x31CA	15:0	0x0000	hispi_ckecksum1 (RO)	N	N
	hispi_ckecksum1 Read-only. Legal values: [0, 65535].				
12748 R0x31CC	15:0	0x0000	hispi_ckecksum2 (RO)		
	hispi_ckecksum2 Read-only. Legal values: [0, 65535].				
12750 R0x31CE	15:0	0x0000	hispi_ckecksum3 (RO)		
	hispi_ckecksum3 Read-only. Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12752 R0x31D0	15:0	0x3231	mipi_compress_8_data_type (R/W)		
	15:14	X	Reserved		
	13:8	0x0032	data_type_10_8_10 data type for 10_8_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0031	data_type_12_8_12 data type for 12_8_12 Legal values: [0, 63].	N	N
12754 R0x31D2	15:0	0x3534	mipi_compress_7_data_type (R/W)		
	15:14	X	Reserved		
	13:8	0x0035	data_type_10_7_10 data type for 10_7_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0034	data_type_12_7_12 data type for 12_7_12 Legal values: [0, 63].	N	N
12756 R0x31D4	15:0	0x3736	mipi_compress_6_data_type (R/W)	N	N
	15:14	X	Reserved		
	13:8	0x0037	data_type_10_6_10 data type for 10_6_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0036	data_type_12_6_12 data type for 12_6_12 Legal values: [0, 63].	N	N
12758 R0x31D6	15:0	0x3330	mipi_jpeg_pn9_data_type (R/W)	N	N
	15:14	X	Reserved		
	13:8	0x0033	data_type_pn9 data type for pn9 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0030	data_type_jpeg data type for jpeg Legal values: [0, 63].	N	N
12788 R0x31F4	15:0	0x0000	fuse_id1 (R/W)		
	Bits 15:0 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12790 R0x31F6	15:0	0x0000	fuse_id2 (R/W)	N	N
	Bits 31:16 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) Legal values: [0, 65535].				
12792 R0x31F8	15:0	0x0000	fuse_id3 (R/W)	N	N
	Bits 47:32 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) Legal values: [0, 65535].				
12794 R0x31FA	15:0	0x0000	fuse_id4 (R/W)	N	N
	Bits 63:48 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset) Legal values: [0, 65535].				
12796 R0x31FC	15:0	0x6E6C	i2c_ids (R/W)	N	N
	Two-wire serial interface (I2C) addresses. Legal values: [0, 65535].				
12798 R0x31FE	15:0	0x0000	customer_rev (RO)	N	N
	Customer revision Read-only. Legal values: [0, 127].				
14336 R0x3800	15:0	0x0000	otpm_data_000 (R/W)		
	OTPM_DATA_000 Legal values: [0, 65535].				
14338 R0x3802	15:0	0x0000	otpm_data_001 (R/W)		
	OTPM_DATA_001 Legal values: [0, 65535].				
14340 R0x3804	15:0	0x0000	otpm_data_002 (R/W)		
	OTPM_DATA_002 Legal values: [0, 65535].				
14342 R0x3806	15:0	0x0000	otpm_data_003 (R/W)		
	OTPM_DATA_003 Legal values: [0, 65535].				
14344 R0x3808	15:0	0x0000	otpm_data_004 (R/W)		
	OTPM_DATA_004 Legal values: [0, 65535].				
14346 R0x380A	15:0	0x0000	otpm_data_005 (R/W)		
	OTPM_DATA_005 Legal values: [0, 65535].				
14348 R0x380C	15:0	0x0000	otpm_data_006 (R/W)		
	OTPM_DATA_006 Legal values: [0, 65535].				
14350 R0x380E	15:0	0x0000	otpm_data_007 (R/W)		
	OTPM_DATA_007 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14352 R0x3810	15:0	0x0000	otpm_data_008 (R/W)		
	OTPM_DATA_008 Legal values: [0, 65535].				
14354 R0x3812	15:0	0x0000	otpm_data_009 (R/W)		
	OTPM_DATA_009 Legal values: [0, 65535].				
14356 R0x3814	15:0	0x0000	otpm_data_010 (R/W)		
	OTPM_DATA_010 Legal values: [0, 65535].				
14358 R0x3816	15:0	0x0000	otpm_data_011 (R/W)	N	N
	OTPM_DATA_011 Legal values: [0, 65535].				
14360 R0x3818	15:0	0x0000	otpm_data_012 (R/W)	N	N
	OTPM_DATA_012 Legal values: [0, 65535].				
14362 R0x381A	15:0	0x0000	otpm_data_013 (R/W)	N	N
	OTPM_DATA_013 Legal values: [0, 65535].				
14364 R0x381C	15:0	0x0000	otpm_data_014 (R/W)	N	N
	OTPM_DATA_014 Legal values: [0, 65535].				
14366 R0x381E	15:0	0x0000	otpm_data_015 (R/W)	N	N
	OTPM_DATA_015 Legal values: [0, 65535].				
14368 R0x3820	15:0	0x0000	otpm_data_016 (R/W)	N	N
	OTPM_DATA_016 Legal values: [0, 65535].				
14370 R0x3822	15:0	0x0000	otpm_data_017 (R/W)	N	N
	OTPM_DATA_017 Legal values: [0, 65535].				
14372 R0x3824	15:0	0x0000	otpm_data_018 (R/W)	N	N
	OTPM_DATA_018 Legal values: [0, 65535].				
14374 R0x3826	15:0	0x0000	otpm_data_019 (R/W)	N	N
	OTPM_DATA_019 Legal values: [0, 65535].				
14376 R0x3828	15:0	0x0000	otpm_data_020 (R/W)	N	N
	OTPM_DATA_020 Legal values: [0, 65535].				
14378 R0x382A	15:0	0x0000	otpm_data_021 (R/W)	N	N
	OTPM_DATA_021 Legal values: [0, 65535].				
14380 R0x382C	15:0	0x0000	otpm_data_022 (R/W)	N	N
	OTPM_DATA_022 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14382 R0x382E	15:0	0x0000	otpm_data_023 (R/W)	N	N
	OTPM_DATA_023 Legal values: [0, 65535].				
14384 R0x3830	15:0	0x0000	otpm_data_024 (R/W)	N	N
	OTPM_DATA_024 Legal values: [0, 65535].				
14386 R0x3832	15:0	0x0000	otpm_data_025 (R/W)	N	N
	OTPM_DATA_025 Legal values: [0, 65535].				
14388 R0x3834	15:0	0x0000	otpm_data_026 (R/W)		
	OTPM_DATA_026 Legal values: [0, 65535].				
14390 R0x3836	15:0	0x0000	otpm_data_027 (R/W)	N	N
	OTPM_DATA_027 Legal values: [0, 65535].				
14392 R0x3838	15:0	0x0000	otpm_data_028 (R/W)	N	N
	OTPM_DATA_028 Legal values: [0, 65535].				
14394 R0x383A	15:0	0x0000	otpm_data_029 (R/W)		
	OTPM_DATA_029 Legal values: [0, 65535].				
14396 R0x383C	15:0	0x0000	otpm_data_030 (R/W)		
	OTPM_DATA_030 Legal values: [0, 65535].				
14398 R0x383E	15:0	0x0000	otpm_data_031 (R/W)		
	OTPM_DATA_031 Legal values: [0, 65535].				
14400 R0x3840	15:0	0x0000	otpm_data_032 (R/W)		
	OTPM_DATA_032 Legal values: [0, 65535].				
14402 R0x3842	15:0	0x0000	otpm_data_033 (R/W)		
	OTPM_DATA_033 Legal values: [0, 65535].				
14404 R0x3844	15:0	0x0000	otpm_data_034 (R/W)		
	OTPM_DATA_034 Legal values: [0, 65535].				
14406 R0x3846	15:0	0x0000	otpm_data_035 (R/W)		
	OTPM_DATA_035 Legal values: [0, 65535].				
14408 R0x3848	15:0	0x0000	otpm_data_036 (R/W)	N	N
	OTPM_DATA_036 Legal values: [0, 65535].				
14410 R0x384A	15:0	0x0000	otpm_data_037 (R/W)	N	N
	OTPM_DATA_037 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14412 R0x384C	15:0	0x0000	otpm_data_038 (R/W)		
	OTPM_DATA_038 Legal values: [0, 65535].				
14414 R0x384E	15:0	0x0000	otpm_data_039 (R/W)	N	N
	OTPM_DATA_039 Legal values: [0, 65535].				
14416 R0x3850	15:0	0x0000	otpm_data_040 (R/W)	N	N
	OTPM_DATA_040 Legal values: [0, 65535].				
14418 R0x3852	15:0	0x0000	otpm_data_041 (R/W)	N	N
	OTPM_DATA_041 Legal values: [0, 65535].				
14420 R0x3854	15:0	0x0000	otpm_data_042 (R/W)	N	N
	OTPM_DATA_042 Legal values: [0, 65535].				
14422 R0x3856	15:0	0x0000	otpm_data_043 (R/W)		
	OTPM_DATA_043 Legal values: [0, 65535].				
14424 R0x3858	15:0	0x0000	otpm_data_044 (R/W)		
	OTPM_DATA_044 Legal values: [0, 65535].				
14426 R0x385A	15:0	0x0000	otpm_data_045 (R/W)		
	OTPM_DATA_045 Legal values: [0, 65535].				
14428 R0x385C	15:0	0x0000	otpm_data_046 (R/W)		
	OTPM_DATA_046 Legal values: [0, 65535].				
14430 R0x385E	15:0	0x0000	otpm_data_047 (R/W)	N	N
	OTPM_DATA_047 Legal values: [0, 65535].				
14432 R0x3860	15:0	0x0000	otpm_data_048 (R/W)	N	N
	OTPM_DATA_048 Legal values: [0, 65535].				
14434 R0x3862	15:0	0x0000	otpm_data_049 (R/W)	N	N
	OTPM_DATA_049 Legal values: [0, 65535].				
14436 R0x3864	15:0	0x0000	otpm_data_050 (R/W)		
	OTPM_DATA_050 Legal values: [0, 65535].				
14438 R0x3866	15:0	0x0000	otpm_data_051 (R/W)	N	N
	OTPM_DATA_051 Legal values: [0, 65535].				
14440 R0x3868	15:0	0x0000	otpm_data_052 (R/W)	N	N
	OTPM_DATA_052 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14442 R0x386A	15:0	0x0000	otpm_data_053 (R/W)		
	OTPM_DATA_053 Legal values: [0, 65535].				
14444 R0x386C	15:0	0x0000	otpm_data_054 (R/W)		
	OTPM_DATA_054 Legal values: [0, 65535].				
14446 R0x386E	15:0	0x0000	otpm_data_055 (R/W)	N	N
	OTPM_DATA_055 Legal values: [0, 65535].				
14448 R0x3870	15:0	0x0000	otpm_data_056 (R/W)	N	N
	OTPM_DATA_056 Legal values: [0, 65535].				
14450 R0x3872	15:0	0x0000	otpm_data_057 (R/W)	N	N
	OTPM_DATA_057 Legal values: [0, 65535].				
14452 R0x3874	15:0	0x0000	otpm_data_058 (R/W)	N	N
	OTPM_DATA_058 Legal values: [0, 65535].				
14454 R0x3876	15:0	0x0000	otpm_data_059 (R/W)	N	N
	OTPM_DATA_059 Legal values: [0, 65535].				
14456 R0x3878	15:0	0x0000	otpm_data_060 (R/W)	N	N
	OTPM_DATA_060 Legal values: [0, 65535].				
14458 R0x387A	15:0	0x0000	otpm_data_061 (R/W)	N	N
	OTPM_DATA_061 Legal values: [0, 65535].				
14460 R0x387C	15:0	0x0000	otpm_data_062 (R/W)	N	N
	OTPM_DATA_062 Legal values: [0, 65535].				
14462 R0x387E	15:0	0x0000	otpm_data_063 (R/W)	N	N
	OTPM_DATA_063 Legal values: [0, 65535].				
14464 R0x3880	15:0	0x0000	otpm_data_064 (R/W)	N	N
	OTPM_DATA_064 Legal values: [0, 65535].				
14466 R0x3882	15:0	0x0000	otpm_data_065 (R/W)	N	N
	OTPM_DATA_065 Legal values: [0, 65535].				
14468 R0x3884	15:0	0x0000	otpm_data_066 (R/W)	N	N
	OTPM_DATA_066 Legal values: [0, 65535].				
14470 R0x3886	15:0	0x0000	otpm_data_067 (R/W)	N	N
	OTPM_DATA_067 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14472 R0x3888	15:0	0x0000	otpm_data_068 (R/W)	N	N
	OTPM_DATA_068 Legal values: [0, 65535].				
14474 R0x388A	15:0	0x0000	otpm_data_069 (R/W)	N	N
	OTPM_DATA_069 Legal values: [0, 65535].				
14476 R0x388C	15:0	0x0000	otpm_data_070 (R/W)	N	N
	OTPM_DATA_070 Legal values: [0, 65535].				
14478 R0x388E	15:0	0x0000	otpm_data_071 (R/W)	N	N
	OTPM_DATA_071 Legal values: [0, 65535].				
14480 R0x3890	15:0	0x0000	otpm_data_072 (R/W)	N	N
	OTPM_DATA_072 Legal values: [0, 65535].				
14482 R0x3892	15:0	0x0000	otpm_data_073 (R/W)	N	N
	OTPM_DATA_073 Legal values: [0, 65535].				
14484 R0x3894	15:0	0x0000	otpm_data_074 (R/W)	N	N
	OTPM_DATA_074 Legal values: [0, 65535].				
14486 R0x3896	15:0	0x0000	otpm_data_075 (R/W)	N	N
	OTPM_DATA_075 Legal values: [0, 65535].				
14488 R0x3898	15:0	0x0000	otpm_data_076 (R/W)	N	N
	OTPM_DATA_076 Legal values: [0, 65535].				
14490 R0x389A	15:0	0x0000	otpm_data_077 (R/W)	N	N
	OTPM_DATA_077 Legal values: [0, 65535].				
14492 R0x389C	15:0	0x0000	otpm_data_078 (R/W)	N	N
	OTPM_DATA_078 Legal values: [0, 65535].				
14494 R0x389E	15:0	0x0000	otpm_data_079 (R/W)	N	N
	OTPM_DATA_079 Legal values: [0, 65535].				
14496 R0x38A0	15:0	0x0000	otpm_data_080 (R/W)	N	N
	OTPM_DATA_080 Legal values: [0, 65535].				
14498 R0x38A2	15:0	0x0000	otpm_data_081 (R/W)	N	N
	OTPM_DATA_081 Legal values: [0, 65535].				
14500 R0x38A4	15:0	0x0000	otpm_data_082 (R/W)	N	N
	OTPM_DATA_082 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14502 R0x38A6	15:0	0x0000	otpm_data_083 (R/W)	N	N
	OTPM_DATA_083 Legal values: [0, 65535].				
14504 R0x38A8	15:0	0x0000	otpm_data_084 (R/W)	N	N
	OTPM_DATA_084 Legal values: [0, 65535].				
14506 R0x38AA	15:0	0x0000	otpm_data_085 (R/W)	N	N
	OTPM_DATA_085 Legal values: [0, 65535].				
14508 R0x38AC	15:0	0x0000	otpm_data_086 (R/W)	N	N
	OTPM_DATA_086 Legal values: [0, 65535].				
14510 R0x38AE	15:0	0x0000	otpm_data_087 (R/W)	N	N
	OTPM_DATA_087 Legal values: [0, 65535].				
14512 R0x38B0	15:0	0x0000	otpm_data_088 (R/W)	N	N
	OTPM_DATA_088 Legal values: [0, 65535].				
14514 R0x38B2	15:0	0x0000	otpm_data_089 (R/W)	N	N
	OTPM_DATA_089 Legal values: [0, 65535].				
14516 R0x38B4	15:0	0x0000	otpm_data_090 (R/W)	N	N
	OTPM_DATA_090 Legal values: [0, 65535].				
14518 R0x38B6	15:0	0x0000	otpm_data_091 (R/W)	N	N
	OTPM_DATA_091 Legal values: [0, 65535].				
14520 R0x38B8	15:0	0x0000	otpm_data_092 (R/W)	N	N
	OTPM_DATA_092 Legal values: [0, 65535].				
14522 R0x38BA	15:0	0x0000	otpm_data_093 (R/W)	N	N
	OTPM_DATA_093 Legal values: [0, 65535].				
14524 R0x38BC	15:0	0x0000	otpm_data_094 (R/W)	N	N
	OTPM_DATA_094 Legal values: [0, 65535].				
14526 R0x38BE	15:0	0x0000	otpm_data_095 (R/W)	N	N
	OTPM_DATA_095 Legal values: [0, 65535].				
14528 R0x38C0	15:0	0x0000	otpm_data_096 (R/W)	N	N
	OTPM_DATA_096 Legal values: [0, 65535].				
14530 R0x38C2	15:0	0x0000	otpm_data_097 (R/W)	N	N
	OTPM_DATA_097 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14532 R0x38C4	15:0	0x0000	otpm_data_098 (R/W)	N	N
	OTPM_DATA_098 Legal values: [0, 65535].				
14534 R0x38C6	15:0	0x0000	otpm_data_099 (R/W)	N	N
	OTPM_DATA_099 Legal values: [0, 65535].				
14536 R0x38C8	15:0	0x0000	otpm_data_100 (R/W)	N	N
	OTPM_DATA_100 Legal values: [0, 65535].				
14538 R0x38CA	15:0	0x0000	otpm_data_101 (R/W)	N	N
	OTPM_DATA_101 Legal values: [0, 65535].				
14540 R0x38CC	15:0	0x0000	otpm_data_102 (R/W)	N	N
	OTPM_DATA_102 Legal values: [0, 65535].				
14542 R0x38CE	15:0	0x0000	otpm_data_103 (R/W)	N	N
	OTPM_DATA_103 Legal values: [0, 65535].				
14544 R0x38D0	15:0	0x0000	otpm_data_104 (R/W)	N	N
	OTPM_DATA_104 Legal values: [0, 65535].				
14546 R0x38D2	15:0	0x0000	otpm_data_105 (R/W)	N	N
	OTPM_DATA_105 Legal values: [0, 65535].				
14548 R0x38D4	15:0	0x0000	otpm_data_106 (R/W)	N	N
	OTPM_DATA_106 Legal values: [0, 65535].				
14550 R0x38D6	15:0	0x0000	otpm_data_107 (R/W)	N	N
	OTPM_DATA_107 Legal values: [0, 65535].				
14552 R0x38D8	15:0	0x0000	otpm_data_108 (R/W)	N	N
	OTPM_DATA_108 Legal values: [0, 65535].				
14554 R0x38DA	15:0	0x0000	otpm_data_109 (R/W)	N	N
	OTPM_DATA_109 Legal values: [0, 65535].				
14556 R0x38DC	15:0	0x0000	otpm_data_110 (R/W)	N	N
	OTPM_DATA_110 Legal values: [0, 65535].				
14558 R0x38DE	15:0	0x0000	otpm_data_111 (R/W)	N	N
	OTPM_DATA_111 Legal values: [0, 65535].				
14560 R0x38E0	15:0	0x0000	otpm_data_112 (R/W)	N	N
	OTPM_DATA_112 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14562 R0x38E2	15:0	0x0000	otpm_data_113 (R/W)	N	N
	OTPM_DATA_113 Legal values: [0, 65535].				
14564 R0x38E4	15:0	0x0000	otpm_data_114 (R/W)	N	N
	OTPM_DATA_114 Legal values: [0, 65535].				
14566 R0x38E6	15:0	0x0000	otpm_data_115 (R/W)	N	N
	OTPM_DATA_115 Legal values: [0, 65535].				
14568 R0x38E8	15:0	0x0000	otpm_data_116 (R/W)	N	N
	OTPM_DATA_116 Legal values: [0, 65535].				
14570 R0x38EA	15:0	0x0000	otpm_data_117 (R/W)	N	N
	OTPM_DATA_117 Legal values: [0, 65535].				
14572 R0x38EC	15:0	0x0000	otpm_data_118 (R/W)	N	N
	OTPM_DATA_118 Legal values: [0, 65535].				
14574 R0x38EE	15:0	0x0000	otpm_data_119 (R/W)	N	N
	OTPM_DATA_119 Legal values: [0, 65535].				
14576 R0x38F0	15:0	0x0000	otpm_data_120 (R/W)	N	N
	OTPM_DATA_120 Legal values: [0, 65535].				
14578 R0x38F2	15:0	0x0000	otpm_data_121 (R/W)	N	N
	OTPM_DATA_121 Legal values: [0, 65535].				
14580 R0x38F4	15:0	0x0000	otpm_data_122 (R/W)	N	N
	OTPM_DATA_122 Legal values: [0, 65535].				
14582 R0x38F6	15:0	0x0000	otpm_data_123 (R/W)	N	N
	OTPM_DATA_123 Legal values: [0, 65535].				
14584 R0x38F8	15:0	0x0000	otpm_data_124 (R/W)	N	N
	OTPM_DATA_124 Legal values: [0, 65535].				
14586 R0x38FA	15:0	0x0000	otpm_data_125 (R/W)	N	N
	OTPM_DATA_125 Legal values: [0, 65535].				
14588 R0x38FC	15:0	0x0000	otpm_data_126 (R/W)	N	N
	OTPM_DATA_126 Legal values: [0, 65535].				
14590 R0x38FE	15:0	0x0000	otpm_data_127 (R/W)	N	N
	OTPM_DATA_127 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14592 R0x3900	15:0	0x0000	otpm_data_128 (R/W)	N	N
	OTPM_DATA_128 Legal values: [0, 65535].				
14594 R0x3902	15:0	0x0000	otpm_data_129 (R/W)	N	N
	OTPM_DATA_129 Legal values: [0, 65535].				
14596 R0x3904	15:0	0x0000	otpm_data_130 (R/W)	N	N
	OTPM_DATA_130 Legal values: [0, 65535].				
14598 R0x3906	15:0	0x0000	otpm_data_131 (R/W)	N	N
	OTPM_DATA_131 Legal values: [0, 65535].				
14600 R0x3908	15:0	0x0000	otpm_data_132 (R/W)	N	N
	OTPM_DATA_132 Legal values: [0, 65535].				
14602 R0x390A	15:0	0x0000	otpm_data_133 (R/W)	N	N
	OTPM_DATA_133 Legal values: [0, 65535].				
14604 R0x390C	15:0	0x0000	otpm_data_134 (R/W)	N	N
	OTPM_DATA_134 Legal values: [0, 65535].				
14606 R0x390E	15:0	0x0000	otpm_data_135 (R/W)	N	N
	OTPM_DATA_135 Legal values: [0, 65535].				
14608 R0x3910	15:0	0x0000	otpm_data_136 (R/W)	N	N
	OTPM_DATA_136 Legal values: [0, 65535].				
14610 R0x3912	15:0	0x0000	otpm_data_137 (R/W)	N	N
	OTPM_DATA_137 Legal values: [0, 65535].				
14612 R0x3914	15:0	0x0000	otpm_data_138 (R/W)	N	N
	OTPM_DATA_138 Legal values: [0, 65535].				
14614 R0x3916	15:0	0x0000	otpm_data_139 (R/W)	N	N
	OTPM_DATA_139 Legal values: [0, 65535].				
14616 R0x3918	15:0	0x0000	otpm_data_140 (R/W)	N	N
	OTPM_DATA_140 Legal values: [0, 65535].				
14618 R0x391A	15:0	0x0000	otpm_data_141 (R/W)	N	N
	OTPM_DATA_141 Legal values: [0, 65535].				
14620 R0x391C	15:0	0x0000	otpm_data_142 (R/W)	N	N
	OTPM_DATA_142 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14622 R0x391E	15:0	0x0000	otpm_data_143 (R/W)	N	N
	OTPM_DATA_143 Legal values: [0, 65535].				
14624 R0x3920	15:0	0x0000	otpm_data_144 (R/W)	N	N
	OTPM_DATA_144 Legal values: [0, 65535].				
14626 R0x3922	15:0	0x0000	otpm_data_145 (R/W)	N	N
	OTPM_DATA_145 Legal values: [0, 65535].				
14628 R0x3924	15:0	0x0000	otpm_data_146 (R/W)	N	N
	OTPM_DATA_146 Legal values: [0, 65535].				
14630 R0x3926	15:0	0x0000	otpm_data_147 (R/W)	N	N
	OTPM_DATA_147 Legal values: [0, 65535].				
14632 R0x3928	15:0	0x0000	otpm_data_148 (R/W)	N	N
	OTPM_DATA_148 Legal values: [0, 65535].				
14634 R0x392A	15:0	0x0000	otpm_data_149 (R/W)	N	N
	OTPM_DATA_149 Legal values: [0, 65535].				
14636 R0x392C	15:0	0x0000	otpm_data_150 (R/W)	N	N
	OTPM_DATA_150 Legal values: [0, 65535].				
14638 R0x392E	15:0	0x0000	otpm_data_151 (R/W)	N	N
	OTPM_DATA_151 Legal values: [0, 65535].				
14640 R0x3930	15:0	0x0000	otpm_data_152 (R/W)	N	N
	OTPM_DATA_152 Legal values: [0, 65535].				
14642 R0x3932	15:0	0x0000	otpm_data_153 (R/W)	N	N
	OTPM_DATA_153 Legal values: [0, 65535].				
14644 R0x3934	15:0	0x0000	otpm_data_154 (R/W)	N	N
	OTPM_DATA_154 Legal values: [0, 65535].				
14646 R0x3936	15:0	0x0000	otpm_data_155 (R/W)	N	N
	OTPM_DATA_155 Legal values: [0, 65535].				
14648 R0x3938	15:0	0x0000	otpm_data_156 (R/W)	N	N
	OTPM_DATA_156 Legal values: [0, 65535].				
14650 R0x393A	15:0	0x0000	otpm_data_157 (R/W)	N	N
	OTPM_DATA_157 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14652 R0x393C	15:0	0x0000	otpm_data_158 (R/W)	N	N
	OTPM_DATA_158 Legal values: [0, 65535].				
14654 R0x393E	15:0	0x0000	otpm_data_159 (R/W)	N	N
	OTPM_DATA_159 Legal values: [0, 65535].				
14656 R0x3940	15:0	0x0000	otpm_data_160 (R/W)	N	N
	OTPM_DATA_160 Legal values: [0, 65535].				
14658 R0x3942	15:0	0x0000	otpm_data_161 (R/W)	N	N
	OTPM_DATA_161 Legal values: [0, 65535].				
14660 R0x3944	15:0	0x0000	otpm_data_162 (R/W)	N	N
	OTPM_DATA_162 Legal values: [0, 65535].				
14662 R0x3946	15:0	0x0000	otpm_data_163 (R/W)	N	N
	OTPM_DATA_163 Legal values: [0, 65535].				
14664 R0x3948	15:0	0x0000	otpm_data_164 (R/W)	N	N
	OTPM_DATA_164 Legal values: [0, 65535].				
14666 R0x394A	15:0	0x0000	otpm_data_165 (R/W)	N	N
	OTPM_DATA_165 Legal values: [0, 65535].				
14668 R0x394C	15:0	0x0000	otpm_data_166 (R/W)	N	N
	OTPM_DATA_166 Legal values: [0, 65535].				
14670 R0x394E	15:0	0x0000	otpm_data_167 (R/W)	N	N
	OTPM_DATA_167 Legal values: [0, 65535].				
14672 R0x3950	15:0	0x0000	otpm_data_168 (R/W)	N	N
	OTPM_DATA_168 Legal values: [0, 65535].				
14674 R0x3952	15:0	0x0000	otpm_data_169 (R/W)	N	N
	OTPM_DATA_169 Legal values: [0, 65535].				
14676 R0x3954	15:0	0x0000	otpm_data_170 (R/W)	N	N
	OTPM_DATA_170 Legal values: [0, 65535].				
14678 R0x3956	15:0	0x0000	otpm_data_171 (R/W)	N	N
	OTPM_DATA_171 Legal values: [0, 65535].				
14680 R0x3958	15:0	0x0000	otpm_data_172 (R/W)	N	N
	OTPM_DATA_172 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14682 R0x395A	15:0	0x0000	otpm_data_173 (R/W)	N	N
	OTPM_DATA_173 Legal values: [0, 65535].				
14684 R0x395C	15:0	0x0000	otpm_data_174 (R/W)	N	N
	OTPM_DATA_174 Legal values: [0, 65535].				
14686 R0x395E	15:0	0x0000	otpm_data_175 (R/W)	N	N
	OTPM_DATA_175 Legal values: [0, 65535].				
14688 R0x3960	15:0	0x0000	otpm_data_176 (R/W)	N	N
	OTPM_DATA_176 Legal values: [0, 65535].				
14690 R0x3962	15:0	0x0000	otpm_data_177 (R/W)	N	N
	OTPM_DATA_177 Legal values: [0, 65535].				
14692 R0x3964	15:0	0x0000	otpm_data_178 (R/W)	N	N
	OTPM_DATA_178 Legal values: [0, 65535].				
14694 R0x3966	15:0	0x0000	otpm_data_179 (R/W)	N	N
	OTPM_DATA_179 Legal values: [0, 65535].				
14696 R0x3968	15:0	0x0000	otpm_data_180 (R/W)	N	N
	OTPM_DATA_180 Legal values: [0, 65535].				
14698 R0x396A	15:0	0x0000	otpm_data_181 (R/W)	N	N
	OTPM_DATA_181 Legal values: [0, 65535].				
14700 R0x396C	15:0	0x0000	otpm_data_182 (R/W)	N	N
	OTPM_DATA_182 Legal values: [0, 65535].				
14702 R0x396E	15:0	0x0000	otpm_data_183 (R/W)	N	N
	OTPM_DATA_183 Legal values: [0, 65535].				
14704 R0x3970	15:0	0x0000	otpm_data_184 (R/W)	N	N
	OTPM_DATA_184 Legal values: [0, 65535].				
14706 R0x3972	15:0	0x0000	otpm_data_185 (R/W)	N	N
	OTPM_DATA_185 Legal values: [0, 65535].				
14708 R0x3974	15:0	0x0000	otpm_data_186 (R/W)	N	N
	OTPM_DATA_186 Legal values: [0, 65535].				
14710 R0x3976	15:0	0x0000	otpm_data_187 (R/W)	N	N
	OTPM_DATA_187 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14712 R0x3978	15:0	0x0000	otpm_data_188 (R/W)	N	N
	OTPM_DATA_188 Legal values: [0, 65535].				
14714 R0x397A	15:0	0x0000	otpm_data_189 (R/W)	N	N
	OTPM_DATA_189 Legal values: [0, 65535].				
14716 R0x397C	15:0	0x0000	otpm_data_190 (R/W)	N	N
	OTPM_DATA_190 Legal values: [0, 65535].				
14718 R0x397E	15:0	0x0000	otpm_data_191 (R/W)	N	N
	OTPM_DATA_191 Legal values: [0, 65535].				
14720 R0x3980	15:0	0x0000	otpm_data_192 (R/W)	N	N
	OTPM_DATA_192 Legal values: [0, 65535].				
14722 R0x3982	15:0	0x0000	otpm_data_193 (R/W)	N	N
	OTPM_DATA_193 Legal values: [0, 65535].				
14724 R0x3984	15:0	0x0000	otpm_data_194 (R/W)	N	N
	OTPM_DATA_194 Legal values: [0, 65535].				
14726 R0x3986	15:0	0x0000	otpm_data_195 (R/W)	N	N
	OTPM_DATA_195 Legal values: [0, 65535].				
14728 R0x3988	15:0	0x0000	otpm_data_196 (R/W)	N	N
	OTPM_DATA_196 Legal values: [0, 65535].				
14730 R0x398A	15:0	0x0000	otpm_data_197 (R/W)	N	N
	OTPM_DATA_197 Legal values: [0, 65535].				
14732 R0x398C	15:0	0x0000	otpm_data_198 (R/W)	N	N
	OTPM_DATA_198 Legal values: [0, 65535].				
14734 R0x398E	15:0	0x0000	otpm_data_199 (R/W)	N	N
	OTPM_DATA_199 Legal values: [0, 65535].				
14736 R0x3990	15:0	0x0000	otpm_data_200 (R/W)	N	N
	OTPM_DATA_200 Legal values: [0, 65535].				
14738 R0x3992	15:0	0x0000	otpm_data_201 (R/W)	N	N
	OTPM_DATA_201 Legal values: [0, 65535].				
14740 R0x3994	15:0	0x0000	otpm_data_202 (R/W)	N	N
	OTPM_DATA_202 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14742 R0x3996	15:0	0x0000	otpm_data_203 (R/W)	N	N
	OTPM_DATA_203 Legal values: [0, 65535].				
14744 R0x3998	15:0	0x0000	otpm_data_204 (R/W)	N	N
	OTPM_DATA_204 Legal values: [0, 65535].				
14746 R0x399A	15:0	0x0000	otpm_data_205 (R/W)	N	N
	OTPM_DATA_205 Legal values: [0, 65535].				
14748 R0x399C	15:0	0x0000	otpm_data_206 (R/W)	N	N
	OTPM_DATA_206 Legal values: [0, 65535].				
14750 R0x399E	15:0	0x0000	otpm_data_207 (R/W)	N	N
	OTPM_DATA_207 Legal values: [0, 65535].				
14752 R0x39A0	15:0	0x0000	otpm_data_208 (R/W)	N	N
	OTPM_DATA_208 Legal values: [0, 65535].				
14754 R0x39A2	15:0	0x0000	otpm_data_209 (R/W)	N	N
	OTPM_DATA_209 Legal values: [0, 65535].				
14756 R0x39A4	15:0	0x0000	otpm_data_210 (R/W)	N	N
	OTPM_DATA_210 Legal values: [0, 65535].				
14758 R0x39A6	15:0	0x0000	otpm_data_211 (R/W)	N	N
	OTPM_DATA_211 Legal values: [0, 65535].				
14760 R0x39A8	15:0	0x0000	otpm_data_212 (R/W)	N	N
	OTPM_DATA_212 Legal values: [0, 65535].				
14762 R0x39AA	15:0	0x0000	otpm_data_213 (R/W)	N	N
	OTPM_DATA_213 Legal values: [0, 65535].				
14764 R0x39AC	15:0	0x0000	otpm_data_214 (R/W)	N	N
	OTPM_DATA_214 Legal values: [0, 65535].				
14766 R0x39AE	15:0	0x0000	otpm_data_215 (R/W)	N	N
	OTPM_DATA_215 Legal values: [0, 65535].				
14768 R0x39B0	15:0	0x0000	otpm_data_216 (R/W)	N	N
	OTPM_DATA_216 Legal values: [0, 65535].				
14770 R0x39B2	15:0	0x0000	otpm_data_217 (R/W)	N	N
	OTPM_DATA_217 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14772 R0x39B4	15:0	0x0000	otpm_data_218 (R/W)	N	N
	OTPM_DATA_218 Legal values: [0, 65535].				
14774 R0x39B6	15:0	0x0000	otpm_data_219 (R/W)	N	N
	OTPM_DATA_219 Legal values: [0, 65535].				
14776 R0x39B8	15:0	0x0000	otpm_data_220 (R/W)	N	N
	OTPM_DATA_220 Legal values: [0, 65535].				
14778 R0x39BA	15:0	0x0000	otpm_data_221 (R/W)	N	N
	OTPM_DATA_221 Legal values: [0, 65535].				
14780 R0x39BC	15:0	0x0000	otpm_data_222 (R/W)	N	N
	OTPM_DATA_222 Legal values: [0, 65535].				
14782 R0x39BE	15:0	0x0000	otpm_data_223 (R/W)	N	N
	OTPM_DATA_223 Legal values: [0, 65535].				
14784 R0x39C0	15:0	0x0000	otpm_data_224 (R/W)	N	N
	OTPM_DATA_224 Legal values: [0, 65535].				
14786 R0x39C2	15:0	0x0000	otpm_data_225 (R/W)	N	N
	OTPM_DATA_225 Legal values: [0, 65535].				
14788 R0x39C4	15:0	0x0000	otpm_data_226 (R/W)	N	N
	OTPM_DATA_226 Legal values: [0, 65535].				
14790 R0x39C6	15:0	0x0000	otpm_data_227 (R/W)	N	N
	OTPM_DATA_227 Legal values: [0, 65535].				
14792 R0x39C8	15:0	0x0000	otpm_data_228 (R/W)	N	N
	OTPM_DATA_228 Legal values: [0, 65535].				
14794 R0x39CA	15:0	0x0000	otpm_data_229 (R/W)	N	N
	OTPM_DATA_229 Legal values: [0, 65535].				
14796 R0x39CC	15:0	0x0000	otpm_data_230 (R/W)	N	N
	OTPM_DATA_230 Legal values: [0, 65535].				
14798 R0x39CE	15:0	0x0000	otpm_data_231 (R/W)	N	N
	OTPM_DATA_231 Legal values: [0, 65535].				
14800 R0x39D0	15:0	0x0000	otpm_data_232 (R/W)	N	N
	OTPM_DATA_232 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14802 R0x39D2	15:0	0x0000	otpm_data_233 (R/W)	N	N
	OTPM_DATA_233 Legal values: [0, 65535].				
14804 R0x39D4	15:0	0x0000	otpm_data_234 (R/W)	N	N
	OTPM_DATA_234 Legal values: [0, 65535].				
14806 R0x39D6	15:0	0x0000	otpm_data_235 (R/W)	N	N
	OTPM_DATA_235 Legal values: [0, 65535].				
14808 R0x39D8	15:0	0x0000	otpm_data_236 (R/W)	N	N
	OTPM_DATA_236 Legal values: [0, 65535].				
14810 R0x39DA	15:0	0x0000	otpm_data_237 (R/W)	N	N
	OTPM_DATA_237 Legal values: [0, 65535].				
14812 R0x39DC	15:0	0x0000	otpm_data_238 (R/W)	N	N
	OTPM_DATA_238 Legal values: [0, 65535].				
14814 R0x39DE	15:0	0x0000	otpm_data_239 (R/W)	N	N
	OTPM_DATA_239 Legal values: [0, 65535].				
14816 R0x39E0	15:0	0x0000	otpm_data_240 (R/W)	N	N
	OTPM_DATA_240 Legal values: [0, 65535].				
14818 R0x39E2	15:0	0x0000	otpm_data_241 (R/W)	N	N
	OTPM_DATA_241 Legal values: [0, 65535].				
14820 R0x39E4	15:0	0x0000	otpm_data_242 (R/W)	N	N
	OTPM_DATA_242 Legal values: [0, 65535].				
14822 R0x39E6	15:0	0x0000	otpm_data_243 (R/W)	N	N
	OTPM_DATA_243 Legal values: [0, 65535].				
14824 R0x39E8	15:0	0x0000	otpm_data_244 (R/W)	N	N
	OTPM_DATA_244 Legal values: [0, 65535].				
14826 R0x39EA	15:0	0x0000	otpm_data_245 (R/W)	N	N
	OTPM_DATA_245 Legal values: [0, 65535].				
14828 R0x39EC	15:0	0x0000	otpm_data_246 (R/W)	N	N
	OTPM_DATA_246 Legal values: [0, 65535].				
14830 R0x39EE	15:0	0x0000	otpm_data_247 (R/W)	N	N
	OTPM_DATA_247 Legal values: [0, 65535].				

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Table 6: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14832 R0x39F0	15:0	0x0000	otpm_data_248 (R/W)	N	N
	OTPM_DATA_248 Legal values: [0, 65535].				
14834 R0x39F2	15:0	0x0000	otpm_data_249 (R/W)	N	N
	OTPM_DATA_249 Legal values: [0, 65535].				
14836 R0x39F4	15:0	0x0000	otpm_data_250 (R/W)	N	N
	OTPM_DATA_250 Legal values: [0, 65535].				
14838 R0x39F6	15:0	0x0000	otpm_data_251 (R/W)	N	N
	OTPM_DATA_251 Legal values: [0, 65535].				
14840 R0x39F8	15:0	0x0000	otpm_data_252 (R/W)	N	N
	OTPM_DATA_252 Legal values: [0, 65535].				
14842 R0x39FA	15:0	0x0000	otpm_data_253 (R/W)	N	N
	OTPM_DATA_253 Legal values: [0, 65535].				
14844 R0x39FC	15:0	0x0000	otpm_data_254 (R/W)	N	N
	OTPM_DATA_254 Legal values: [0, 65535].				
14846 R0x39FE	15:0	0x0000	otpm_data_255 (R/W)	N	N
	OTPM_DATA_255 Legal values: [0, 65535].				
16326 R0x3FC6	15:0	0x0123	tempsens_calib1 (R/W)	N	N
	user calibration register 1 Legal values: [0,65535].				
16328 R0x3FC8	15:0	0x4567	tempsens_calib2 (R/W)	N	N
	user calibration register 2 Legal values: [0,65535].				
16330 R0x3FCA	15:0	0x89AB	tempsens_calib3 (R/W)	N	N
	user calibration register 3 Legal values: [0,65535].				
16332 R0x3FCC	15:0	0xCDEF	tempsens_calib4 (R/W)	N	N
	user calibration register 4 Legal values: [0,65535].				

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Revision History

Rev. C 3/26/13

- Updated Frame Sync'd and Bad Frame columns in Table 4, “SMIA Configuration Register Descriptions,” on page 27, Table 5, “SMIA Parameter Limits Register Descriptions,” on page 34, and Table 6, “Manufacturer-Specific Register Descriptions,” on page 37

Rev. B 9/7/12

- Updated to preliminary
- Updated to Rev. 3 database

Rev. A 1/20/12

- Initial release

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Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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