Summary of Changes

Dear Associate Editor,

Below is an item-by-item response to the comments provided by the reviewers. As per the suggestion raised by the second reviewer, the title of the paper has been changed to “Radiation Hardened Latch Designs for Double and Triple Node Upsets”.

Reviewer 1:

- *In the simulation, only weak particle of 5 fC were used Strong as well as weak particle should be used;*
    - For the latches tested, the magnitude of the pulse (and by default the injected charge) does not have a direct correlation on the latch’s ability to tolerate an error. For all latches tested, a pulse will not be stored in the storage loop no matter the pulse size. Specifically, the presented latches that are SEU tolerant will not upset unless two nodes have simultaneous pulses. DNU tolerant latches will not upset unless three nodes have simultaneous pulses and TNU tolerant latches will not upset unless four nodes have simultaneous pulses. This is clarified in the last paragraph of the Section 3. A simulation for the larger pulses is described in Section 5 with a waveform for a category in each proposed design showing the response for large charge DNU and TNU injections of 1 pC. This confirms that the approaches tolerate the error.
- *Critical charge (i.e. maximal charge which the existing and proposed latch can tolerate) need to be shown.*
    - Similar to the above concern, the latches do not have a critical charge in the conventional sense as the number of pulses, not the magnitude, contribute to the ability of the latch to tolerate a pulse. Investigation into existing literature for latch designs using a similar design principle show that the critical charge is not a commonly used metric.
- *Table 1 showed delay time; but it is not shown that it is D-Q or CLK-Q delay time.*
    - Table 1 has been amended such that the “Delay” entry is the D->Q delay
- *Some classes of soft error tolerant scheme incurs bad setup-hold time. Those for conventional and proposed latches should be shown in the evaluation section.*
    - Setup and hold times are typically characterized for flip-flops and existing literature seems to only consider the propagation (D->Q) delay for latch designs. Thus, the authors believe that the D->Q delay is sufficient to judge the performance and suitability of both conventional and proposed latch designs. This is justified because the latches are set when the CLK is set to high which puts the latch in transparent mode. The value stored in the latch is that which is on the input when the CLK (or commonly referred to as the Enable) moves to a low value. In this case, the only timing constraint is that the overlap between the input data (D) and the CLK is equal to or greater than the D->Q delay of the latch. The second paragraph of the introduction has been updated to state that one of the reasons for focusing on the latch was that they do not have setup and hold time issues and that they can form the basis for flip-flop designs.
- *The wires in Fig. 19 are very thin.*
    - I have made the lines thicker for Fig. 21 (previously Fig. 19) so they should be more visible.

Reviewer 2:

- *The title is too general and could be used for other papers in this area. It would be good to choose a title that is specific to the unique aspects of your paper.*
    - The title was changed to: Radiation Hardened Latch Designs for Double and Triple Node Upsets

Reviewer 3:

- *In section 2, I think a latch is introduced as "DNUCS" but then is refered as "DNCS".*
    - Section 2 Paragraph 1: DNUCS is changed to DNCS and the acronym is defined.
- *I think a figure for the DNCS and the HSMUF will increase the readability of the paper.*
    - Section 2 Paragraph 3: HSMUF acronym was not defined because its definition was not given in the reference. The figure for this latch was already in the paper but a reference to the figure was placed in the first sentence. A figure for the DNCS. Fig. 2 and Fig. 3 give the schematic of the DNCS latch. In section 2 paragraph 1, the figure is referenced.
- *In particular, many proposed latches are named just with the acronyms, the full name of these gate should be added.*
    - Section 2 Paragraph 4: The DONUT latch acronym was defined
- *In section 3, it is not specified the purpose of signal "INP" in figure 5 and this compromises the clearness of the text.*
    - Fig 5: INP changed to INPUT to clarify that the pin is an input
- *The detailed explanation of the HRDNUT begin at page 4, col.1, line 49, but the figure, which can help to read the description is not quoted at all.*
    - Section 3 Paragraph 5: The last sentence of the paragraph quotes the schematic.
- *In section 4, the authors honestly admit that a complete verification of the TNU robustness is "tedious", I would suggest to define this task in a more formal way.*
    - Section 4 Paragraph 1: The word tedious was changed to difficult. The sentence as a whole had awkward wording which was addressed.
- *In addition, the previous paper is not correctly quoted. The reference to the previous article is put in the middle of section 3. The "HRDNUT" is presented in section 1 and its description is at the beginning of section 3 but there is no reference to the previous work.*
    - Section 1 Paragraph 7: A citation to the previous paper is added in the first sentence.

The paper has been proofread and any remaining typos that were found were fixed.