A Methodology to Evaluate the Aging Impact on Flip-Flops Performance

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***Abstract* — The impact of aging effects, in terms of circuit performance and reliability, is one of the new recent challenges in VLSI design targeting the most advanced CMOS technologies. This work proposes an effective methodology to aging analysis in flip-flops. The estimation method proposed previously for combinational logic gates is exploited and improved herein to address such sequential gates. Three different conventional static flip-flops have been used as case studies to demonstrate and validate the proposed methodology.**

Keywords — Digital circuit, CMOS, flip-flop, aging, performance, reliability, BTI, TDDB, HCI.

I. INTRODUCTION

The constant reduction of MOS device dimensions has created new challenges in integrated circuit (IC) design. Physical effects, such as leakage currents, process variability, and radiation have to be overcome to ensure high performance, low power and reliability of digital circuits in the most advanced CMOS technologies. In this sense, the three main effects associated to the circuit aging are the bias temperature instability (BTI) [1], the time dependent dielectric breakdown (TDDB) [2] and the hot carrier injection (HCI) [3]. According to the particular aging effect, one can observe the degradation of transistor threshold voltage, the creation of electrical current conduction path through the transistor gate, or the modification of the saturation current in the transistor channel, so resulting in significant impact in circuit speed and power consumption.

In terms of CMOS gates, latches and flip-flops (FF) are crucial elements in modern VLSI systems, being the main responsible for the data flow and data storage. Moreover, in comparison to combinational circuit parts, such sequential gates are the most instantiated gates in ICs, representing circa 30%-50% of the entire circuit area and energy budget [4-6]. Several different FF topologies are known, and the election of the most suitable one for a specific application is not always a straightforward task. It depends on their performance, power consumption, reliability and, most currently, their aging characteristics.

This work presents a novel methodology to evaluate the aging impact in FFs. The influence of BTI, HCI and TDDB in FF performance is taken into account on the proposed evaluation procedure. It can be easily applied to different FFs topologies. This work explores the estimation method proposed for combinational circuits by Butzen *et al.* in [7]. However, sequential gates present particularities when compared to combinational circuits that must be accounted for. It comprises the internal nodes in high-impedance state and the logic loops for data memorization. As a result, the method proposed in [7] has been adapted and improved for FF analysis. The methodology proposed herein for aging analysis of FFs is demonstrated taking into account three conventional topologies as case studies, although it can be easily extended to different clocked storage elements.

This rest of this paper is organized as follows. Related work is discussed in Section II. In Section III, it is presented a brief background on flip-flop timing characteristics and aging effects, with special attention on how to identify the stress condition in transistor arrangements. In Section IV, the proposed methodology is described. Section V presents the aging evaluation procedure in three case studies. Finally, in Section VI, the conclusions are outlined.

II. RELATED WORK

Several works have evaluated different FF topologies, in terms of performance and power consumption analysis, as well as through the comparison of them [8-10]. In [8], it is analyzed a group of clock storage elements in the context of a practical application. The most efficient storage element is identified in a pipeline stage. In [9], a general design flow is proposed to optimize FFs under constraints within energy-delay space. The logical effort method is applied, and the impact of local interconnections is taken into account in the design. A comparison with a wider range of FFs classes and topologies is performed in [10]. Such analysis involves some effects arising in nanometer technologies and that affect the energy-delay-area tradeoff. The related works mentioned above present comprehensive analysis of different FF topologies. However, none of them targets the aging effects.

Regarding combinational circuits, in [11], a method to predict the degradation of circuit speed over a long period of time under NBTI effect is presented. Whereas, in [12], a gate delay model considering BTI and HCI is proposed. Both methods have been demonstrated and validated through ISCAS benchmark circuits.

978-1-4799-1132-5/13/$31.00 ©2013 IEEE

In terms of wearout FF analysis, the main effort has been focused on BTI effect [13-16]. In [13], an analysis of FF under NBTI effects is carried out. Different FF topologies have their timing characteristics compared. Particular FF design for runtime failure prediction is proposed in [14]. Design techniques aiming to reduce the impact of BTI effects are proposed in [15]. Dual threshold assignment is applied in several FF topologies, whereas transistor sizing strategy is discussed in [16], in order to attain a NBTI-aware flip-flop. In those works, the aging effect impact is restricted to BTI, and a more general methodology of aging analysis in sequential gates (latches and flip-flops) cannot be derived from them.

III. BACKGROUND

A. Flip-Flop Timing Characteristics

Differently from combinational circuits, where the timing constraints are related exclusively to signal propagation delay from input to output nodes, in FFs the setup time and the hold time characteristics are of particular interest to use appropriately such sequential gates.

In terms of signal propagation delay or 'delay arcs' in FFs, the clock-to-Q (T_{CQ}) delay is the time period between clock (C) activate edge and the changing of the logic value on the output node (Q). In order to evaluate the performance, FFs can be characterized considering T_{CQ} and setup skew. Setup skew corresponds to the time interval between the arrival of input data (D) and the clock edge.

On the other hand, FF delay has been defined as the interval between the arrival of the input signal D and the output Q transition, called T_{DQ} [17]. It is not an intuitive delay arc since the input D alone is not able to provoke a signal transition at the output node Q. For large values of setup skew, the propagation delay clock-to-Q is constant and minimum (T_{CQmin}). However, for small values of setup skew, the flip-flop operates in metastability, which increases T_{CQ} [18]. As a consequence, initially T_{DQ} decreases when decreasing setup skew, but tends to increase again when the decreasing too much the setup skew. This results in a minimum value of T_{DQ} delay (T_{DQmin}) achieved by selecting an 'optimum' setup skew, so corresponding to the figure-of-merit of FF performance.

The optimum setup skew which leads minimum data-to-Q is defined as 'setup time', which is a time constraint that refers to the setup skew necessary for the clock to reliably capture the input data. The hold skew, in turn, defined as the amount of time the input data is stable after the clock edge, presents similar behavior to the setup skew. Hence, hold time refers to the hold skew necessary for the clock to reliably store the data.

B. MOS Aging Effects

The aging effects in MOS devices are resulted from the superposition of many individual complex physical phenomena, such as BTI, TDDB and HCI [1]-[3]. Although there is no single physical modeling known to represent aging degradation in MOS transistor, its electrical characteristics affected by each effect is well established [19]. The severe degradation conditions in transistor operation are also known [20]. In terms of design, these two factors are quite relevant to find the most appropriate circuit implementation in terms of wearout characteristics.

BTI and TDDB mechanisms degrade the transistor during the steady state. BTI increases the transistor threshold voltage, impacting on the circuit speed, whereas TDDB degrades the isolation properties of gate dielectric, increasing the tunneling current across the transistor gate terminal. The stress condition associated to those effects is similar, and occurs when the gate voltage of PMOS and NMOS transistors are, respectively, Vg='0' and Vg='1', and gate-to-source voltages (Vgs) corresponds to negative and positive power supply voltage (Vdd), respectively, as illustrated in Fig. 1(a) and Fig. 1(b).

In terms of circuit analysis, such stress condition is directly related to the CMOS gate signal probability. Moreover, the transistor arrangements in both pull-up and pull-down logic planes in the gate have to be also considered due to Vgs dependence. Several works compute the degradation using only the gate signal probability [1][21]. In order to achieve more accurate results, this work a novel methodology for flip-flop aging analysis based on the estimation method proposed in [7] for combinational circuits. The principle of transistor stress probability (TSP) is introduced in [7]. Basically, it is computed by a procedure that identifies the transistor stress conditions, as illustrated in Fig. 1(a) and in Fig. 1(b), in any transistor arrangement according to the signal probability.

On the other hand, HCI degrades the transistor when it is transitioning. It also increases the transistor threshold voltage [3]. Since this phenomenon is associated to carriers flowing through the transistor channel, the higher mobility of electrons, when compared to holes, becomes the NMOS devices more susceptible to HCI effect than the PMOS ones. The degradation in NMOS transistor occurs when a rise transition on the gate causes a fall transition into the drain region, as illustrated in Fig. 1(c). The severity of HCI degradation is exponentially related to the transistor drain-to-source voltage (Vds) [7]. Since the transistors connected to the output node are the ones that experience maximum Vds, the gate signal switching information is not enough to compute properly the degradation. The transistor arrangement has to be included in the analysis. Following the methodology proposed in [7], the transistor switching stress probability (TSwP) is considered in this work. TSwP is computed by a procedure that identifies as degraded devices only the switching transistors that experience maximum Vds, as seen in Fig. 1(c).

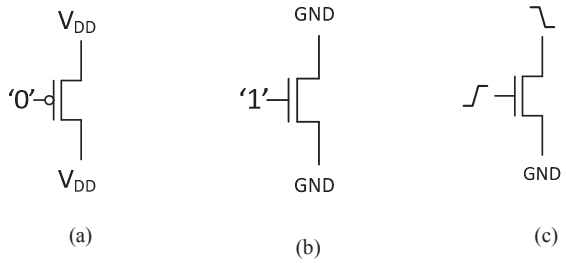

Fig. 1. Transistor under BTI stress in PMOS (a) and NMOS (b), and under HCI stress (c).

IV. Flip-Flop Aging Analysis Methodology

The aging analysis in FFs may receive special attention due to the existence of the memorization capacity at internal nodes of the topology. Such nodes are not always controlled directly by the primary inputs of the circuit. The voltage value of such 'unreachable' nodes is usually defined by previous state values, so increasing the complexity of the estimation procedure. The identification of the memorization nodes and the computation of all possible combinations are the key factors to provide an accurate analysis of FF aging behavior.

The first step of the proposed methodology is to calculate TSP and TSwP values of each transistor in the circuit, according to the procedure defined in [7]. It is evaluated considering all D and CK input signal combinations, as well as the logic values of internal memory nodes.

In the second step, the threshold voltage degradation (ΔV_{th}) of each transistor is computed according to the stress probabilities, i.e., the TSP and TSwP parameters. ΔV_{th} is resulted from the BTI and HCI aging effects. The BTI impact on transistor threshold voltage (ΔV_{th_BTI}) can be expressed as follows:

$$\Delta V_{th\ BTI} = a\ .\ (TSP\ .\ t)^n \quad (1)$$

where 'a' is a technology dependent constants, 't' is time, and 'n' is the BTI time exponential constant that incorporates the temperature dependency. Moreover, the time exponential constant 'n' is different for each type of transistor, so being different for NBTI and PBTI effects.

The HCI impact on NMOS transistor threshold voltage (ΔV_{th_HCI}), on the other hand, is calculated as follows:

$$\Delta V_{th\ HCI} = b\ .\ (TSwP\ .\ t)^m \quad (2)$$

where 'b' is a technology dependent constants, 't' is time, and 'm' is the HCI time exponential constant. In the scope of this work, it is applied only to NMOS transistors.

The threshold voltage degradation of each PMOS transistor is ΔV_{th_BTI}, and in the NMOS devices is obtained by adding ΔV_{th_BTI} and ΔV_{th_HCI}. The maximum degradation of 50 mV is taken into account, and reflects five years degradation in nanometer technologies [21].

In the third step of the methodology, a resistor between gate and drain (R_{GD}) can emulate the gate tunneling current increment caused by the TDDB progressive effect, before the gate oxide breakdown [2]. Such resistors can be estimated as follows:

$$R_{GD} = K\ .\ (TSP\ .\ t)^p \quad (3)$$

where 't' is time, whereas 'K' and 'p' are technology dependent constants.

In the final step, the aged FF is characterized through electrical simulations, considering ΔV_{th} and R_{GD} estimated for each device present in the FF topology, and then compared to the not aged (fresh) FF version.

V. Case Studies

To demonstrate the proposed methodology for FF aging evaluation, three cases of study are discussed in detail in the following.

Consider the conventional static transmission gate flip-flop (TGFF), depicted in Fig. 2 [22]. First of all, TSP and TSwP of each one of the 22 transistors in the circuit is calculated. TSP is evaluated considering all D and CK input signal probabilities, and the logic values of M1 and M2 memory nodes. Although there are four variables, it corresponds to eight combinations for static analysis, because only one of memory nodes (M1 or M2) is actually unknown at time, being the other one determined by the CK input signal value. TSwP, in turn, is computed to sixteen possibilities for switching conditions. It corresponds to all the possible combinations between data and clock transitions (high-to-low and low-to-high) and the memory nodes states (0 and 1). The values obtained for each device seen in Fig. 2 are shown in Table I.

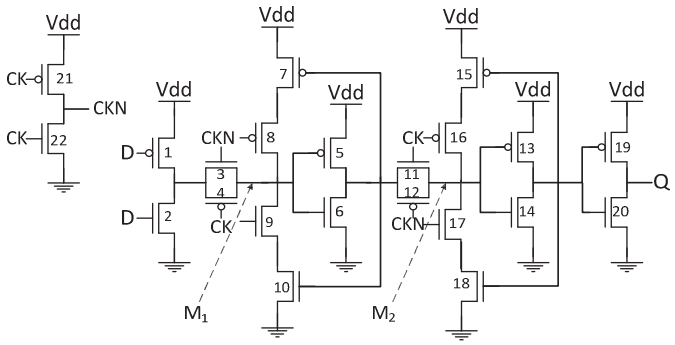

Fig. 2. Transmission gate flip-flop (TGFF) [22].

TABLE I. Stress Probability Values on Devices in Fig. 2.

Transistor	TSP	TSwP	Transistor	TSP	TSwP
1	0.5	0	12	0.25	0
2	0.5	0.25	13	0.5	0
3	0.25	0.125	14	0.5	0.0625
4	0.25	0	15	0.5	0
5	0.5	0	16	0.25	0
6	0.5	0.1875	17	0.25	0
7	0.5	0	18	0.5	0
8	0.25	0	19	0.5	0
9	0.25	0	20	0.5	0.0625
10	0.5	0	21	0.5	0
11	0.25	0.125	22	0.5	0.25

Based on the transistors stress probabilities, now it is possible to calculate the threshold voltage degradation of each device. For instance, consider the transistor number 2 indicated in Fig. 2, which is a NMOS transistor, and then can present threshold degradation by BTI and HCI effects. According to the TSP and TSwP values, and equations (1) and (2), the following degradations calculated are ΔV_{th_BTI} = 15.27 mV and ΔV_{th_HCI} = 25.22 mV, which results in a total threshold voltage increasing equal to 40.49 mV. Extending this reasoning to all other transistors, the computed ΔV_{th} for TGFF are obtained, as shown in Table II.

TABLE II. THRESHOLD VOLTAGE DEGRADATION ON DEVICES IN FIG. 2.

Transistor	ΔV_{th} (mV)	Transistor	ΔV_{th} (mV)
1	45.81	12	40.81
2	40.49	13	45.81
3	31.43	14	27.88
4	40.81	15	45.81
5	45.81	16	40.81
6	37.11	17	13.60
7	45.81	18	15.27
8	40.81	19	45.81
9	13.60	20	27.88
10	15.27	21	45.81
11	31.43	22	40.49

As explained before, the resistors (R_{GD}) values can be obtained using the pre-calculated TSP values and the equation (3), and are shown in Table III.

TABLE III. GATE-TO-DRAIN RESISTANCE ON DEVICES IN FIG. 2.

Transistor	R_{GD} (kΩ)	Transistor	R_{GD} (kΩ)
1	1595.5	12	51056.7
2	1595.5	13	1595.5
3	51056.7	14	1595.5
4	51056.7	15	1595.5
5	1595.5	16	51056.7
6	1595.5	17	51056.7
7	1595.5	18	1595.5
8	51056.7	19	1595.5
9	51056.7	20	1595.5
10	1595.5	21	1595.5
11	51056.7	22	1595.5

In the final step of the proposed methodology, the aged TGFF is characterized in order to compare the not aged TGFF version to new one with the updated threshold voltage values and including the resistors R_{GD} in the circuit. In Table IV is provided $T_{CQ,min}$, $T_{DQ,min}$, setup time and hold time for high-to-low and low-to-high output transitions. The results show that the FF delay $T_{DQ,min}$ increases 19% on average.

TABLE IV. AGING IMPACT IN TRANSMISSION GATE FLIP-FLOP (TGFF).

	$T_{CQ,min}$	$T_{DQ,min}$	Setup	Hold
high-to-low				
Fresh circuit (ps)	19.60	51.23	28.46	-7.34
Aged circuit (ps)	22.80	62.99	34.69	-4.19
Increment (ps)	3.20	11.76	6.23	3.15
low-to-high				
Fresh circuit (ps)	25.94	47.05	16.51	-7.11
Aged circuit (ps)	30.22	56.25	21.51	-5.56
Increment (ps)	4.28	9.20	5.00	1.55

All results presented in this paper were obtained through HSPICE simulations using 32nm PTM parameters [23].

In the second case of study, a modified TGFF (TGFFv2) has been created by swapping the transistor positions of the tri-state inverters present in the original TGFF structure, as depicted in Fig. 3. For instance, the transistors number 7 and 8 were swapped in comparison to the circuit shown in Fig. 2.

According to stress probability estimation, only the transistors number 8, 9, 16 and 17 present different TSP or TSwP values different from the ones calculated for the original TGFF, given in Table I. Consequently, only in such transistors, the threshold voltage degraded due aging present different values from the ones given in Table II, and different gate-to-drain resistances from the values shown in Table III. The new values of TSP and TSwP, ΔV_{th} and R_{GD} for such specific transistors are given in Table V, in Table VI and in Table VII, respectively.

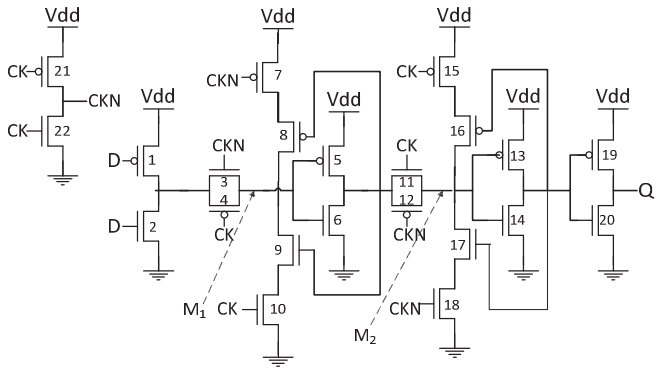

Fig. 3. Modified transmission gate flip-flop (TGFFv2).

TABLE V. STRESS PROBABILITY VALUES ON DEVICES IN FIG. 3.

Transistor	TSP	TSwP	Transistor	TSP	TSwP
8	0.5	0	16	0.5	0
9	0.5	0	17	0.5	0

TABLE VI. THRESHOLD VOLTAGE DEGRADATION ON DEVICES IN FIG. 3.

Transistor	ΔV_{th} (mV)	Transistor	ΔV_{th} (mV)
8	40.81	16	40.81
9	13.60	17	13.60

TABLE VII. GATE-TO-DRAIN RESISTANCE ON DEVICES IN FIG. 3.

Transistor	R_{GD} (kΩ)	Transistor	R_{GD} (kΩ)
8	51056.7	16	51056.7
9	51056.7	17	51056.7

The third topology considered to demonstrate the proposed methodology was the transmission gate master-slave flip-flop (TGMSFF) [13], illustrated in Fig. 4. The values of TSP and TSwP, ΔV_{th} and R_{GD} for all transistors in the TGMSFF are given in Table VI, in Table IX and in Table X, respectively.

The results provided by the proposed analysis allow also compare the aging impact on different FF topologies. The $T_{DQ,min}$ delay for a low-to-high output transition can be considered to illustrate it. Moreover, one can still exploit the procedure to evaluate the degradation due to individual influence of aging effects, as illustrated in Table XI. The

results in Table XI are normalized in respect to the performance of the 'fresh' circuit, i.e., without aging influence.

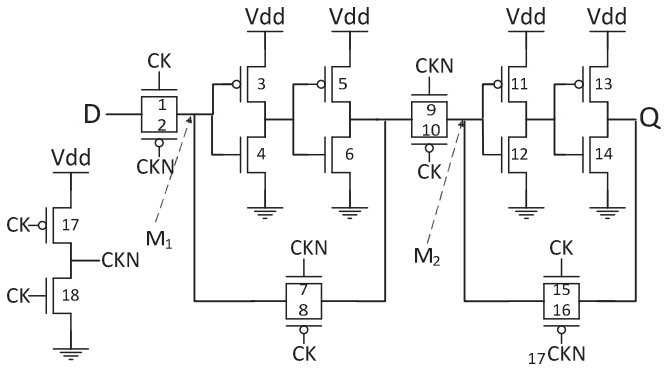

Fig. 4. Transmission gate master-slave flip-flop (TGMSFF) [13].

TABLE VIII. STRESS PROBABILITY VALUES ON DEVICES IN FIG. 4.

Transistor	TSP	TSwP	Transistor	TSP	TSwP
1	0.25	0.125	10	0	0
2	0.25	0	11	0	0
3	0.5	0	12	0.0625	0.0625
4	0.5	0.1875	13	0	0
5	0.5	0	14	0.0625	0.0625
6	0.5	0.1875	15	0	0
7	0.25	0	16	0	0
8	0.25	0	17	0	0
9	0.25	0.125	18	0.25	0.25

TABLE IX. THRESHOLD VOLTAGE DEGRADATION ON DEVICES IN FIG. 4.

Transistor	ΔV_{th} (mV)	Transistor	ΔV_{th} (mV)
1	31.44	10	40.82
2	40.82	11	45.81
3	45.81	12	27.88
4	37.11	13	45.81
5	45.81	14	27.88
6	37.11	15	13.61
7	13.61	16	40.82
8	40.82	17	45.81
9	31.44	18	40.49

TABLE X. GATE-TO-DRAIN RESISTANCE ON DEVICES IN FIG. 4.

Transistor	R_{GD} (kΩ)	Transistor	R_{GD} (kΩ)
1	51056.7	10	51056.7
2	51056.7	11	1595.5
3	1595.5	12	1595.5
4	1595.5	13	1595.5
5	1595.5	14	1595.5
6	1595.5	15	51056.7
7	51056.7	16	51056.7
8	51056.7	17	1595.5
9	51056.7	18	1595.5

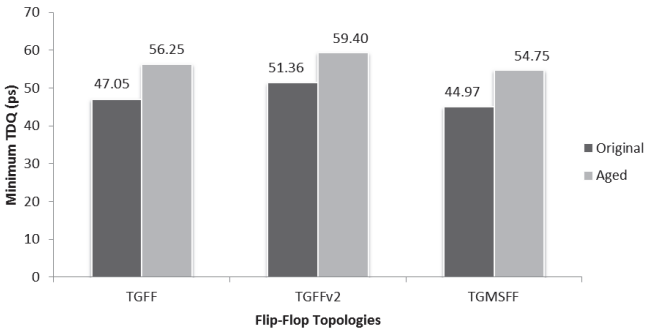

Fig. 5. Aging impact on the performance of different flip-flop topologies.

TABLE XI. MINIMUM D-TO-Q DELAY UNDER BTI, HCI, TTDB AND ALL COMBINED AGING EFFECTS IMPACT (AGED).

	BTI	HCI	TDDB	Aged
TGFF	1.16	1.05	1.01	1.21
TGFFv2	1.10	1.06	0.97	1.16
TGMSFF	1.15	1.03	1.01	1.19

VI. CONCLUSIONS

In this paper, a novel methodology to evaluate the aging impact on flip-flops is proposed, based on the estimation method presented in [7] for combinational circuit. It provides a detailed analysis of each transistor degradation in the circuit, as well as allows compare different topologies, in terms of individual influence of each aging mechanism and all them combined, so representing a useful procedure for supporting most advanced flip-flop design.

ACKNOWLEDGEMENTS

Research partially supported by Brazilian funding agencies CAPES, CNPq and FAPERGS, under grant 11/2053-9 (Pronem).

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