Hardened by Design Techniques for Implementing Multiple-Bit Upset Tolerant Static Memories

Daniel R. Blum and José G. Delgado-Frias
Department of Electrical Engineering and Computer Science
Washington State University
Pullman, WA 99164-2752
{dblum, jdelgado}@eecs.wsu.edu

Abstract— **We present a novel MBU-tolerant design, which utilizes layout-based interleaving and multiple-node disruption tolerant memory latches. This approach protects against grazing incidence particle strikes, which produce disruptions with the widest possible spatial separation. Advantages with respect to size, complexity, and MBU tolerance are realized when this approach is compared to existing solutions.**

I. Introduction

Transient errors may occur in ICs when radioactive particles impact them. Individual upsets that directly affect memory are known as Single Event Upsets (SEUs), while upsets that originate in logic are known as Single Event Transients (SETs). Many approaches have been designed to deal with SEUs and SETs [1]. However, most of these schemes cannot withstand multiple-node and Multiple-Bit Upsets (MBUs). MBUs are a growing concern in environments that possess substantial high-energy ion activity (e.g. in space) [2]. Because of this, additional techniques must be devised to protect against multiple disruptions.

Error Correcting Codes (ECCs), chip-level interleaving, and temporal redundancy are existing schemes that provide MBU tolerance. Multiple-bit correcting ECCs require significant overhead, and they may fail when faced with a large number of upsets. Chip-level interleaving is effective, although the requirement of multiple chips per circuit is expensive. Finally, temporal redundancy does not possess robust MBU tolerance unless full system-level redundancy is implemented. This paper addresses this issue through the presentation of a layout interleaving scheme and multiple-node disruption tolerant (MNDT) memory latches. By combining these two techniques, protection from grazing and non-grazing MBU-inducing particle strikes can be achieved.

MBU probability is strongly dependent on node spacing, feature size, and supply voltage. As feature sizes shrink, MBUs are becoming more of an issue. The linear Energy Transfer (LET), range, track radius, and angle of incidence of the particle inducing upset are also important. In general, particles that deposit more energy, have a longer range, and have a larger radius are more likely to induce MBU. Additionally, grazing strikes have the capability to cause much greater problems than normal incidence strikes [2-3].

II. Ion Trajectories and Layout Interleaving

Particle strikes that produce MBU fall in two general categories: Strikes virtually parallel to the IC surface that pass through sensitive regions of multiple nodes, and strikes that travel at an appreciable angle to the surface. Parallel strikes leave behind a linear trail of charge, and disrupt nodes along a line tracing the ion path. In general, these grazing strikes can affect the most nodes and nodes separated by the greatest distances. On the other hand, non-grazing particles may disrupt multiple nodes within a certain radius via diffusion, charge sharing or secondary particle scattering. If multiple nodes are disrupted by such a particle strike, the disruption pattern tends to form a cluster stretched along the angle of incidence [3-5]. Fig. 1 depicts some typical upset patterns of grazing and non-grazing strikes [6-9].

It is possible to improve the MBU resistance of SEU/SET-tolerant latches, such as the DICE design in [10], by increasing the layout spacing between nodes in every cell. While it is impractical to use this strategy alone to prevent upset from grazing strikes, other strikes can be reasonably mitigated in this fashion. Grazing strikes have been shown to affect nodes separated by 300μm in [11], while non-grazing strikes typically affect a radius on the order of 10μm or less [2]. The layout of multiple cells could be interleaved in such a way as to increase the spacing between nodes in the same cell without substantially increasing the overall layout area. For example, consider interleaving the layouts of four-node DICE latches. If four such latches are interleaved, each pair of nodes within the same latch can be separated by one node from a different latch. Spacing between nodes in the same latch is increased by a factor of n if n^2 memory latches are interleaved. Note that this specific example is vulnerable to grazing strikes. The following sections address this issue.

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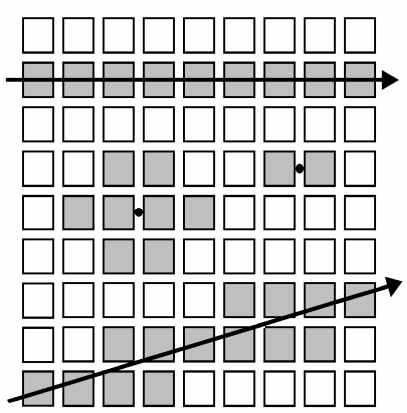

Fig. 1. MBU upset patterns resulting from grazing incidence and non-grazing incidence particle strikes. The arrows represent grazing strikes, while the dots depict non-grazing strikes. The gray boxes symbolize typical disruption patterns initiated by these particle strikes.

III. Multiple-Node Disruption Tolerant Latches

Most current SEU and SET-hardened memory structures can recover from only one disruption at a time. These hardened cells may fail in environments where MBUs occur. It is possible to decrease this probability of failure by adopting cells that tolerate multiple-node disruptions. Additionally, cells that can tolerate multiple disruptions have the potential to avoid upset due to grazing particle strikes that deposit a line of charge. If three or more nodes must be disrupted to flip a cell, it is possible to arrange the layout so that no line passes through a set of mutually vulnerable nodes.

At a minimum, five nodes are required to preserve sufficient information to tolerate dual faults in a latch. Six nodes (three true and three complement) are required to achieve this goal with balanced feedback. Unfortuntately, the complexity required of such six node latches is very high. For example, one six node approach (not illustrated here) requires 84 transistors. Fortunately, this complexity can be significantly reduced by adopting structures with eight nodes. Adding additional nodes increases the amount of information stored by the cell, reducing the relative impact of a multiple-node disrupion. This allows fewer transistors to be used to control the nodes in the latch.

Fig. 2 illustrates an eight node MNDT latch. The architecture is similar to that of a pair of connected Barry/Dooley cells [12-13]. The interconnections are arranged in such a manner as to preserve sufficient information when faced with dual-node disruptions and allow for recovery after disruptions dissipate. Let sets V = {Va, Vb, Vc, Vd} and /V = {/Va, /Vb, /Vc, /Vd}. If the two disrupted nodes are in different sets, then none of the other six nodes will be affected. During recovery, at least one of the upset nodes will be immediately pulled to the proper state, followed by the second node. Alternatively, if the two affected nodes are in the same set, then they could possibly flip the state of a node in the complement set. Fortunately, this does not prevent at least one of the disrupted nodes from recovering immediately after the effects of the particle strike dissipate. After this, the other nodes quickly follow suit.

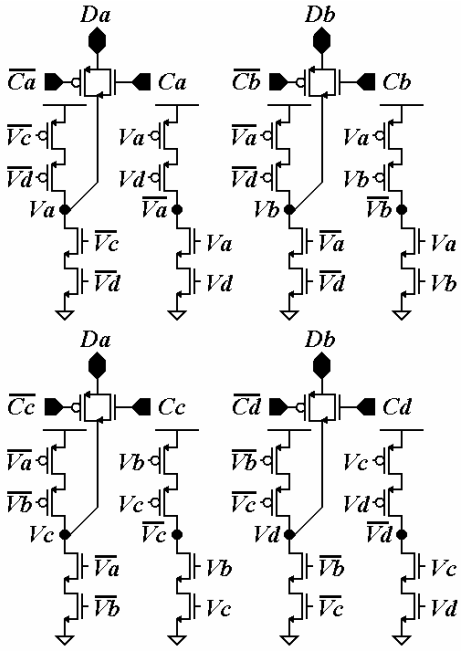

Fig. 2. Eight node latch with dual-node and limited triple-node disruption tolerance.

One additional advantage of this circuit is a limited ability to tolerate three-node disruptions. A number of the possible disruptions affecting two nodes from one set and one node from the complement set can be withstood. This occurs when the two disrupted nodes from the same set do not control a node in the complement set that is distinct from the third disrupted node. This characteristic simplifies the task of creating an MBU-tolerant layout for this circuit.

As an example of this limited ability to tolerate three-node disruptions, assume the initial latch state is 01010101. Nodes Va and Vb are flipped from 0 to 1, and node /Vb is flipped from 1 to 0. The resulting latch state is 11100101. None of the other five nodes are affected, as they are not controlled by some combination of Va, Vb, and /Vb. After the transient disruption dissipates, Va and Vb are pulled back down to 0 by their controlling nodes (/Vc, /Vd and /Va, /Vd). Finally, /Vb is pulled back up to 1 by Va, which restores the proper state of the latch.

IV. Layout Interleaving of MNDT Latches

In isolation, the usefulness of the multiple-node disruption tolerant latches described in the previous section is limited. The ability to tolerate multiple disruptions is mostly offset by the increase in area. However, if these latches are implemented with the layout interleaving technique described in Section II, a desirable characteristic can achieved. The most hazardous MBU mechanism can be avoided by arranging the layout so no line passes through a set of nodes that, if disrupted, would cause a latch to flip state. Grazing particle strikes deposit charge along a linear path, and they can upset nodes spaced by large distances. Bits spaced by 300μm were shown to have an appreciable probability of mutual upset in [11]. However, if no line contains a set of

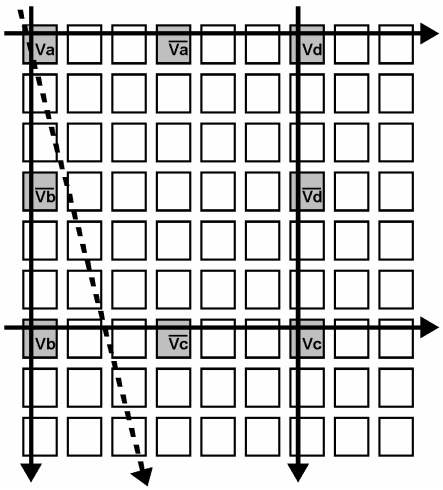

Fig. 3. Diagram of interleaved layout with selected grazing particle strikes. The solid lines represent strikes that pass through three nodes, while the dotted line represents a worst-case strike. All strikes can be tolerated with an appropriate level of interleaving.

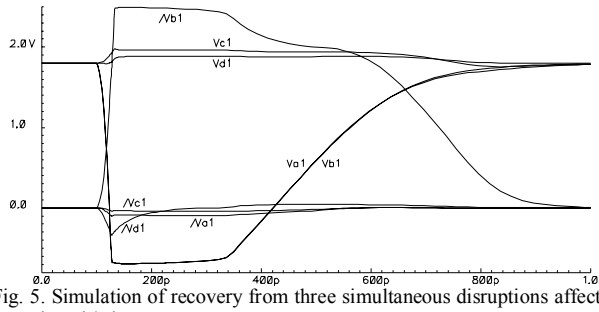

Fig. 5. Simulation of recovery from three simultaneous disruptions affecting Va, Vb and /Vb.

mutually vulnerable nodes, then the probability of upset resulting from this mechanism can be mitigated.

The eight node circuit presented in the previous section can tolerate a number of three-node disruptions, including the following sets: {*Va, /Va, Vd*}, {*Va, /Vb, Vb*}, {*Vb, /Vc, Vc*}, {*Vc, /Vd, Vd*}. Using this information, the layout depicted in Fig. 3 can be constructed with the purpose of avoiding upset due to multiple-node disruptions. Nine cells are interleaved, and so the spacing between nodes is increased by a factor of three. No line intersects a set of nodes that would, if disrupted, flip the state of the latch. This characteristic provides protection against grazing particle strikes, and it is illustrated in this figure. Additionally, since the spacing between each node is increased, tolerance to non-grazing particle strikes is provided. The level of interleaving can be adjusted to meet the demands of a particular situation. In particular, a worst-case grazing strike is represented by the dotted line in Fig. 3. This strike has the potential to disrupt four nodes via charge sharing [11]. The level of interleaving must be sufficient to avoid this possibility.

An implementation of the interleaved layout is shown in Fig. 4. This design was performed in 0.18µm CMOS, and it utilizes four metal layers for interconnections. The layout requires an area of is 36.4µm x 49.2µm. Fewer metal layers could be used at the cost of additional area. The minimum

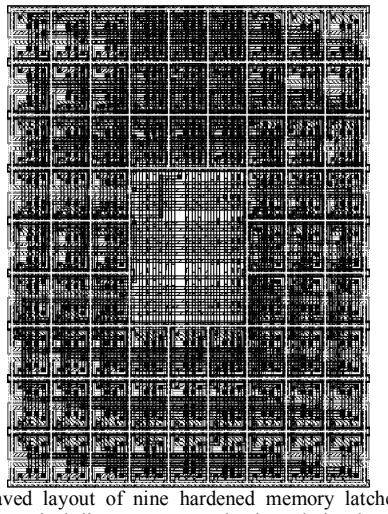

Fig. 4. Interleaved layout of nine hardened memory latches. The white horizontal and vertical lines represent the boundaries between memory nodes.

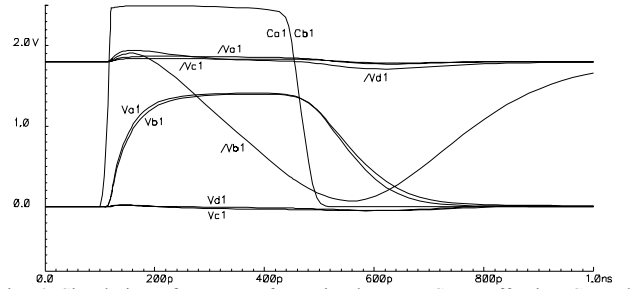

Fig. 6. Simulation of recovery from simultaneous SETs affecting Ca and Cb.

spacing between nodes in the same latch is 9.2 µm. Therefore, a worst-case particle strike must have an ion track radius of at least 4.6 µm to upset four nodes in the same cell along the dotted trajectory shown in Fig. 3. The vast majority of high-energy cosmic rays found in space have radii that are significantly less than this critical value [14].

Fig. 5 is a layout simulation illustrating recovery from three simultaneous disruptions affecting nodes *Va*, *Vb* and */Vb* in the same memory cell. Fig. 6 depicts the recovery from simultaneous SETs affecting enable lines *Ca* and *Cb*.

V. Comparison to Other Strategies

Existing MBU-tolerant schemes include ECCs, chip-level interleaving, and temporal redundancy. The ECCs can be broken down into schemes that operate on single data words and schemes that operate on blocks of data words. Hamming code is a single bit correcting code that functions by appending $\log_2(n+1)$ parity bits to each data word, where n is the total number of bits in the word. It can be extended to correct multiple upsets by utilizing more parity bits. Block level ECCs, such as Reed-Solomon code, perform calculations on groups of data words to achieve greater efficiency. Chip-level interleaving is implemented by distributing a single circuit across multiple chips. Finally, temporally redundant designs sample data at multiple instances in an attempt to detect and bypass faults.

TABLE I. COMPARISON OF MBU-TOLERANT APPROACHES

	Upset Correction	Redundancy (Cycle Time or Layout Area)	Grazing Protection	Multiple Chips	Latency
Proposed	3 per cell	4x (Area)	Yes	No	None
Two-Bit ECC	2 per word	log((n^2+n+2)/2) (Area)	No	No	Enc/Dec
Reed-Solomon	(n-k) / 2 symbols	(n-k) symbols (Area)	No	No	Enc/Dec
Chip Interleaving	Any	log(n+1) (Area)	Yes	Yes	Enc/Dec
Temporal Redundancy	Any	3x (Time)	Yes	No	3x + Voting

Table I presents a comparison between various MBU-tolerant approaches. These include the MNDT latches with interleaving, a two-bit correcting ECC, Reed-Solomon block code, chip level interleaving, and temporal redundancy. The table columns compare the upset correction capabilities, redundancy, grazing strike protection, requirement of multiple chips, and latency. An analysis of this data follows:

- The proposed approach is well balanced, as it protects against both grazing and non-grazing strikes, requires moderate redundancy, fits on one chip, and does not need latency inducing encoder, decoder, or voting circuitry.
- Multiple-bit correcting ECCs that operate on single words offer no protection against grazing strikes, require significant redundancy for moderate sized data words, and require encoding and decoding circuitry.
- Block level codes such as the Reed-Solomon approach are powerful, as they have correcting power equal to half the number of redundant symbols. However, they are only useful in large memories (such as those with 255 byte blocks), and they require encoders and decoders.
- Chip-level interleaving (placing each bit on a different chip) also provides robust MBU tolerance, although the use of multiple chips is not practical in many cases.
- Temporal redundancy is fully MBU-tolerant only when entire calculations are performed redundantly. In hybrid temporal-spatial redundant schemes, the spatially redundant circuitry is vulnerable to multiple upsets. With full temporal redundancy, performance is cut to one third of the original value, and is reduced further by voting.

VI. CONCLUSION

Design-hardened techniques have been developed and presented in this paper with the purpose of tolerating Multiple-Bit Upsets (MBUs) and multiple-node upsets. Specifically, layout interleaving was combined with MNDT memory latches. The increased spacing between nodes in a single latch and tolerance to multi-node disruptions provides substantial protection against non-grazing particle strikes that produce MBUs. More importantly, this scheme assures that grazing particles, which may disrupt distant nodes along their linear paths, cannot disrupt a set of nodes that would cause a latch to flip state. Few MBU-resistant schemes produced to date offer sufficient protection against grazing particle strikes. Those that do require substantial spacing between adjacent bits (even placing bits on separate chips), temporal redundancy, and/or the use of ECCs (expensive multiple-bit correcting codes are required in some schemes) [2, 4, 6, 8]. Due to this overhead, these schemes do not provide the high performance and balanced secondary characteristics of the proposed approach.

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