Radiation Hardened Latch Designs for Multi-Node Upsets

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Abstract—Due to technology scaling, radiation induced errors have become more common in data storage elements. This trend has led to the development of latches that are capable of tolerating the double node upset (DNU). Future scaling may also lead to the possibility of a triple node upset (TNU). While there is no existing work on TNU designs, current work on DNU tolerant designs either suffer from high area and performance overhead or are vulnerable to an error after a DNU thus making them unsuitable for clock gating. A novel latch design is proposed in which all internal and external nodes are capable of recovering the previous value after a single or double node upset. The proposed latch offers higher speed, lower power consumption and lower area requirements compared to all existing DNU tolerant latches capable of recovering all nodes. Additionally, a TNU tolerant latch and a pulse filtering circuit are proposed.

Index Terms—Soft Errors, Radiation Hardened Latch, Transient Pulses, Single Event Upset, Double Node Upset.

1 Introduction

As the transistor feature side continuously scales down to improve performance, modern circuitry continues to become more susceptible to radiation induced errors commonly referred to as a soft error. Soft errors can manifest from either neutron particles originating from space or alpha particles from packaging. A soft error occurs when an energetic particle hits the diffusion region of a reverse bias transistor. This, in turn, allows an ”off” transistor to temporarily conduct current which can cause a voltage change in a node connected to the affected transistor. If the error occurs in combinational logic, the resulting voltage pulse may be stored in a connected flip flop thus causing an error. On the other hand, if the error occurs in memory or a latch during the hold phase, the stored data may change. To mitigate this effect, there is a need for design methodologies that reduce the vulnerability of circuitry to radiation effects.

In this paper, we focus on the reliability of latches. There has been extensive research in the field of hardening latches against single even upsets (SEU). The simplest and most common design in safety critical applications is the triple modular redundancy (TMR) latch. This design consists of 3 standard latches connected to a 3-input majority voting circuit. While this design is robust against errors, it has the drawback of high area, delay and power consumption. For this reason there have been many other designs proposed that offer high SEU reliability with lower area, delay and power consumption. The first and most common cell is the DICE cell proposed in [1]. The design in [1] consists of eight cross-coupled PMOS and NMOS transistors connected in series which forms four nodes. Due to the relatively high delay and power consumption of the DICE latch, there have been many other SEU tolerant latch designs proposed that provide reliability using blocking Muller C-elements, redundancy or delay in the feedback path [2], [3], [4], [5], [6], [7], [8].

In more recent times, the further reduction of the transistor feature size has increase the likelihood of a single event causing a transient on multiple nodes simultaneously, commonly referred to as a single event multiple upset (SEMU). This trend necessitates the development of new latch designs that are tolerant to multiple node strikes to guarantee reliability in current and future technologies. As in the SEU case, the goal of these designs are to minimize the power, delay and area overheads. However, contrary to the SEU case, the latches are designed to tolerate two simultaneous errors, commonly referred to as a double node upset (DNU). Currently there are many existing latch designs that are tolerant to DNUs which are discussed in Section **??**.

Many modern circuit designs employ a technique commonly referred to as clock gating to further reduce the power consumption. Clock gating consists of setting the clock to a stable value or ”gating” the clock. If clock gating is used with a latch, it may need to hold the current state for many clock cycles. In the presence of DNUs, this increases the likelihood of multiple errors occurring during the hold phase. In many existing DNU tolerant designs, a DNU puts the latch to a vulnerable state in which the correct state could be lost if the latch experiences a further SEU or DNU before the transparent mode. Additionally, in many of these designs, a DNU moves the output to a high impedance state which implies that the data could discharge if the latch is gated for a sufficient number of cycles. For this reason, there is a need for new designs that are capable of holding the correct output value after a DNU for any number of clock cycles. In the paper, we classify all DNU tolerant designs as either DNU robust or DNU non-robust. A DNU robust design is defined as being capable of resisting further errors and by not allowing any high impedance states after a DNU

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occurs. A DNU non-robust design is a latch that does not meet the all of stated criteria.

In this work, we propose the HRDNUT (Highly Robust Double Node Upset Tolerant) latch which is a robust latch design that recovers all nodes to the previous state after a DNU occurs while maintaining lower power and area overheads compared to existing DNU robust designs. The paper is organized as follows: Section **??** consists of a discussion on existing DNU tolerant designs. Section **??** provides the design of the HRDNUT. Section **??** consists of a comparison of the HRDNUT to existing error tolerant latch designs. In Section **??** we conclude the paper.

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