Analysis and Mitigation of Multiple Radiation Induced Errors in Modern Circuits

by

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M.Sc., Electrical & Computer Engineering, Southern Illinois University, 2012

A Dissertation
Submitted in Partial Fulfillment of the Requirements for the
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Department of Electrical and Computer Engineering
in the Graduate School
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DISSERTATION APPROVAL

TITLE (ANALYSIS AND MITIGATION OF MULTIPLE RADIATION INDUCED ERRORS IN MODERN CIRCUITS)

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A Dissertation Submitted in Partial

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for the Degree of

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in the field of Electrical and Computer Engineering

Approved by:

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(Date of Approval)

AN ABSTRACT OF THE DISSERTATION OF

Adam Watkins, for the Doctor of Philosophy degree in Electrical and Computer Engineering, presented on November 2nd, at Southern Illinois University Carbondale. (Do not use abbreviations.)

TITLE: ANALYSIS AND MITIGATION OF MULTIPLE RADIATION INDUCED ERRORS IN MODERN CIRCUITS

MAJOR PROFESSOR: Dr. S. Tragoudas

Due to technology scaling, the probability of a high energy radiation particle striking multiple transistors has continued to increase. This, in turn has created a need for new circuit designs that are can tolerate multiple simultaneous errors. A common type of error in memory elements is the double node upset (DNU) which has continued to become more common. All existing DNU tolerant designs either suffer from high area and performance overhead, may lose the data stored in the element or are vulnerable to an error after a DNU occurs which makes the devices unsuitable for clock gating. In this dissertation, a novel latch design is proposed in which all nodes are capable for fully recovering their correct value after a single or double node upset which is referred to as DNU robust. The proposed latch offers lower delay, power consumption and area requirements compared to existing DNU robust designs.

Multiple simultaneous radiation induced errors are a current problem that must be studied in combinational logic. Typically, simulators are used early in the design phase which use a netlist and rudimentary information of the process parameters to determine the error rate of a circuit. Existing simulators are able to accurately determine the effects when the problem space is limited to one simultaneous error. However, existing methods do not provide accurate information when multiple concurrent errors occur due to inaccurate

approximation of the glitch shape when multiple errors meet at a gate. To improve existing error simulation, a novel analytical methodology to accurate determine the pulse shape when two simultaneous errors occur is proposed. Through extensive simulations, it was shown that the proposed methodology matches closely with HSPICE while providing a speedup of 15X.

The analysis of the soft error rate of a circuit has continued to be a difficult problem due to the calculation of the logical effect on a pulse generated by a radiation particle. The most common existing methods to determine logical effects use either exhaustive input pattern simulation or binary decision diagrams. The problem with both approaches is that simulation of the circuit can intractably time consuming. To solve this issue, a simulation tool is proposed which employs an adaptive partitioning algorithm to reduce the simulation time and space overheads of binary decision diagram based simulation. Compared to existing simulation tools, the proposed tool can simulate larger circuits faster.

DEDICATION

(NO REQUIRED FOR RESEARCH PAPER)

(The dedication, as the name suggests is a personal dedication of one's work. The section is OPTIONAL and should be double-spaced if included in the thesis/dissertation.)

ACKNOWLEDGMENTS

(NOT REQUIRED IN RESEARCH PAPER)

I would like to thank Dr. Jones for his invaluable assistance and insights leading to the writing of this paper. My sincere thanks also goes to the seventeen members of my graduate committee for their patience and understanding during the nine years of effort that went into the production of this paper.

A special thanks also to Howard Anton [**?**], from whose book many of the examples used in this sample research paper have been quoted. Another special thanks to Prof. Ronald Grimmer who provided the previous thesis template upon which much of this is based and for help with graphics packages.

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INTRODUCTION

The continued reduction of the transistor feature size has led to the increase in the vulnerability of modern circuits to error. This effect, in turn, has made modern circuits more susceptible to radiation induced errors in space and terrestrial environments. A radiation induced error, commonly referred to as a soft error, occurs when a high energy particle from space or packaging strikes a transistor. Shown in Fig. 1, the particle deposits energy in the active volume generating electron-hole pairs. This creates a new diffusion region that could allow a non-conducting device to temporarily conduct current. The mechanism causes a temporary voltage pulse, referred to as a single event transient (SET) to occur at the device.

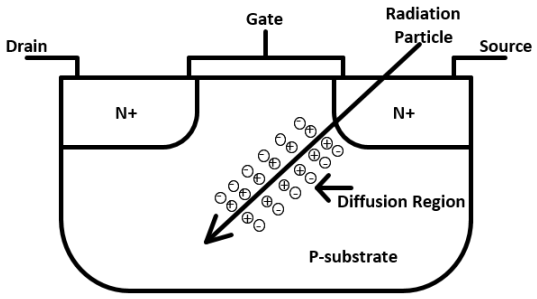

Figure 1. A energetic particle creating electron-hole pairs in a transistor.

In the case of a radiation particle striking a memory storage element, the data stored in the device can be changed. If the device loses its value due to a strike by a single particle, this is referred to as a single event upset (SEU). Additionally, due to the constant scaling down of the feature size, a single particle can also strike two transistors simultaneously which is referred to as a double node upset (DNU). Fig. 2 gives a diagram of a SEU tolerant latch to demonstrate the DNU phenomenon. In the diagram, radiation is denoted as a high energy particle which passes through two transistors on a DICE latch [1]. In the case of a SEU, the DICE latch would normally be able to tolerate the error. As can be observed, the particle passes through two transistors causing the respective node to switch

from "1" on the first node to "0" and from "0" to "1" on the second node. The upset of both nodes drives the remaining two nodes to an erroneous value. This observance is alarming since it signals that current designs are not sufficient for future processes. In turn, this provides a need for new memory element designs that can tolerate DNUs.

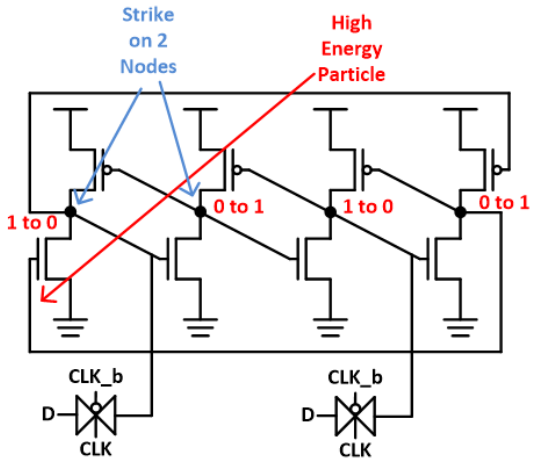

Figure 2. A particle striking two node concurrently causing a double node upset.

Additionally, modern circuit designs employ a technique referred to as clock gating. Clock gating is defined as setting the clock to constant value thus reducing the power consumed. Use of clock gating may lead to cases where the current state held by the memory element must be held for many clock cycles. This need leads to a much longer than normal vulnerable window in which an improperly hardened device may lose the stored value. While there are existing DNU tolerant designs [2, 3, 11], these designs move to a high impedance state after a DNU. If a DNU occurs while the latch is gated, the voltages within the latch may degrade. In Chapter 1, we aim to alleviate this problem by providing an efficient design that is capable of recovering all nodes after a DNU occurs. This, in effect, guarantees that the data will be held even if the latch is struck by a DNU while gated.

In addition to the effects on memory elements, accurate approximation of the error rate of a circuit is also important. The goal of circuit simulation is the accurate estimation

of the soft error rate (SER). In this work, the focus is on the evaluation of combinational circuits. Typically, this type of simulation entails the estimation of the resulting pulse shape when a particle strike a transistor, the determination of the boolean functions that allow the pulse to propagate and the estimation of the latching characteristics at an output flip-flop. Using these parameters, the probability of the pulse reaching an output flip-flop is determined. Assume that the probability of an error reaching and being latched in a flip-flop at output i of the circuit is represented as $P(O_i)$, the particle hit rate in a particular area is given as R_{PH}, the fraction of particle hits resulting in charge generation as R_{eff} and A_{cir} gives the area of the circuit. The equation for the SER at output O_i is given below [5].

$$SER_{O_i} = P(O_i) * R_{eff} * R_{PH} * A_{cir} \tag{1}$$

The focus of all SER estimation simulators is the calculation of the term $P(O_i)$. This is a difficult problem in combination circuits due to the presence of the following three masking factors: electrical masking, logical masking and temporal masking. Electrical masking deals with the calculation of the pulse shape as it propagates through the circuit. Logical masking is the estimation of the logical 1's and 0's and how they may mask the pulse. For example, if a NAND gate has a value of "0" on an input, the pulse will not propagate since the output will be held to a "1". Lastly, temporal masking involves the latching characteristics, specifically the set-up and hold times, of the output flip flop. Accurate consideration of all three masking effects is crucial to accurate SER estimation.

Accurate consideration of the electrical masking effect is an important but often simplified component of SER estimation. The most common method to calculate the pulse shape, proposed in [7] uses a linear line to approximate the rising and falling transitions giving a trapezoidal shape. While this method executes quickly and is easy to implement, it does not provide an accurate estimation of the pulse shape. As can be observed in Fig. [ref], a transient pulse does not take a trapezoidal shape in a real case. For this reason, accurate consideration of the pulse shape must consider the non-linear aspects of the pulse.

In [10], the authors proposed an enhanced pulse approximation method which is accurate within 5% of HSPICE. However, their method has the drawback that it can only consider a single pulse arriving at a gate. In the case of multiple transient pulses injected into a circuit, referred to as a multiple event transient (MET), the likelihood of two or more pulses arriving at a gate simultaneously as shown in Fig. 4 is substantially increased. To accommodate this trend, future soft error simulators must accurately consider this effect.

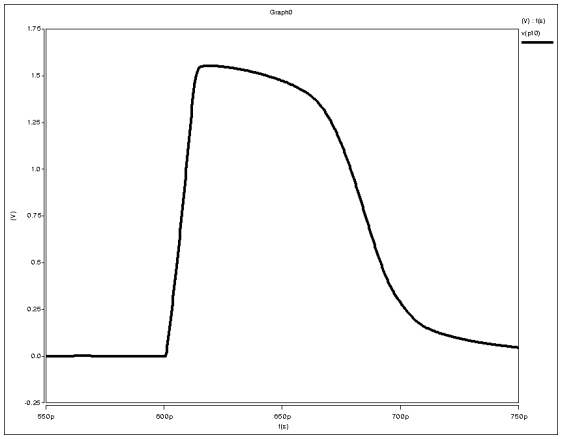

Figure 3. An example of a radiation induced transient pulse.

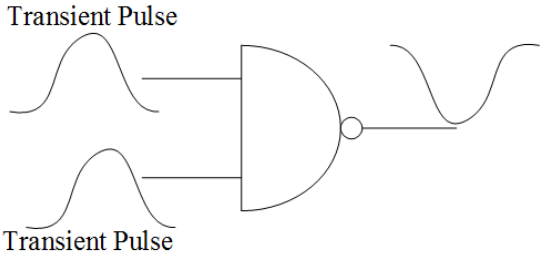

Figure 4. Two pulses arriving at a gate input.

In addition to the electrical masking effect, the logical masking effect must also be accurately considered. Many existing methods use Monte Carlo based simulation which consists of either exhaustively apply all patterns or randomly applying a subset of patterns. [10, 9, 6, 13, 8] While these methods are able to simulate with a very low memory overhead, they have an intractable execution time for circuits with more than 30 inputs. This problem

is further compounded by the fact that due to the nearly infinite number of possible pulse durations and strike locations. To alleviate this issue, the authors in [14] propose the use of probabilistic transfer matricies [PTM]. While the matricies do provide exact calculation of the logical masking effect, their memory usage blows up even for relatively small circuits. As an improvement to the use of PTMs, the use of decision diagrams have become more common. [12, 4] Decision diagrams offer an improved approach since they balance the cost of execution time and memory consumption. However, decision diagrams are not a perfect solutions since, like PTMs, blow up if the circuit is sufficiently large. To solve this issue, the authors in [12] propose the use of partitioning to limit the size of the decision diagrams. The drawback with this approach is that each time the circuit is partitioned, additional error is added to the result. To ensure that the effect on the result is low, the number of partitions should be minimized based on the system used and amount of time allowed.

In this dissertation, novel approaches to the aforementioned problems are proposed. In Chapter 1, a latch design is proposed which is capable of recovering all nodes after a DNU. This design has specific applications in circuits that employ clock gating. Chapter 2 provides an enhanced analytical pulse approximation algorithm which can determine the output pulse shape when two pulses arrive at a gate input. The method is implemented and compared to existing algorithms and HSPICE. Chapter 3 discusses a soft error simulator which adaptively partitions the circuit based on the size of the BDD functions. Results are provided which compare the effect of the partitioning algorithm on the calculation of the SER. Lastly, Chapter 4 concludes the dissertation.

CHAPTER 1

SYSTEMS OF LINEAR EQUATIONS AND MATRICES

1.1 INTRODUCTIONS TO SYSTEMS OF LINEAR EQUATIONS

In this section we introduce base terminology and discuss a method for solving systems of linear equations.

A line in the xy-plain can be represented algebraically by an equation of the form

$$a_1x + a_2y = b$$

An equation of this kind is called a linear equation in the variables x and y. More generally, we define a linear equation in the n variables $x_1, \ldots, x_n$ to be one that can be expressed in the form

$$a_1x_1 + a_2x_2 + \cdots + a_nx_n = b \tag{1.1}$$

where $a_1, a_2, \ldots a_n$ and b are real constants.

Definition. A finite set of linear equations in the variables $x_1, x_2, \ldots, x_n$ is called a *system of linear equations*.

Not all systems of linear equations has solutions. A system of equations that has no solution is said to be *inconsistent*. If there is at least one solution, it is called *consistent*. To illustrate the possibilities that can occur in solving systems of linear equations, consider a general system of two linear equations in the unknowns x and y:

$$a_1x + b_1y = c_1$$

$$a_2x + b_2y = c_2$$

The graphs of these equations are lines; call them l_1 and l_2. Since a point (x, y) lies on a line if and only if the numbers x and y satisfy the equation of the line, the solutions of the

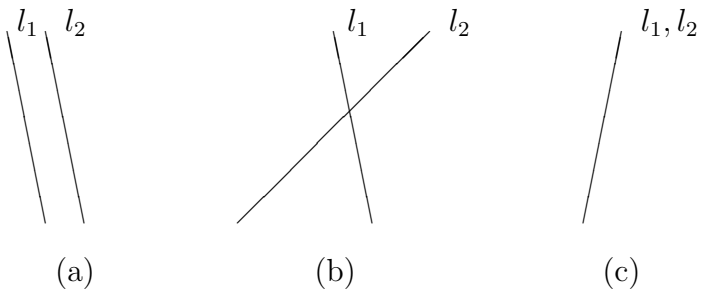

Figure 1.1. (a) no solution, (b) one solution, (c) infinitely many solutions

system of equations will correspond to points of intersection of l_1 and l_2. There are three possibilities:

The three possiblities illustrated in Figure 2.1 are as follows:

(a) l_1 and l_2 are parallel, in which case there is no intersection, and consequently no solution to the system.

(b) l_1 and l_2 intersect at only one point, in which case the system has exactly one solution.

(c) l_1 and l_2 coincide, in which case there are infinitely many points of intersection, and consequently infinitely many solutions to the system.

Although we have considered only two equations with two unknowns here, we will show later that this same result holds for arbitrary systems; that is, every system of linear equations has either no solutions, exactly one solution, or infinitely many solutions.

1.2 GAUSSIAN ELIMINATION

In this section we give a systematic procedure for solving systems of linear equations; it is based on the idea of reducing the augmented matrix to a form that is simple enough so that the system of equations can be solved by inspection.

Remark. It is not difficult to see that a matrix in row-echelon form must have zeros below each leading 1. In contrast a matrix in reduced row-echelon form must have zeros above and below each leading 1.

As a direct result of Figure 2.1 on page 12 we have the following important theorem.

Theorem 1.2.1. *A homogenous system of linear equations with more unknowns than equations always has infinitely many solutions*

The definition of matrix multiplication requires that the number of columns of the first factor A be the same as the number of rows of the second factor B in order to form the product AB. If this condition is not satisfied, the product is undefined. A convenient way to determine whether a product of two matrices is defined is to write down the size of the first factor and, to the right of it, write down the size of the second factor. If, as in Figure 2.2, the inside numbers are the same, then the product is defined. The outside numbers then give the size of the product.

Although the commutative law for multiplication is not valid in matrix arithmetic, many familiar laws of arithmetic are valid for matrices. Some of the most important ones and their names are summarized in the following proposition.

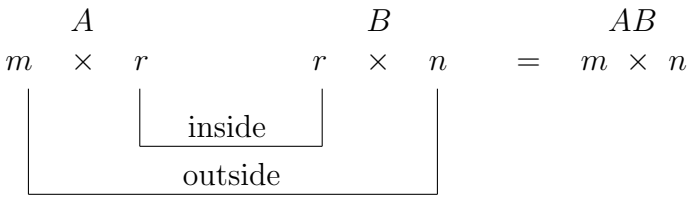

Figure 1.2. Inside and outside numbers of a matrix multiplication problem of $A \times B = AB$, showing how the inside dimensions are dropped and the dimensions of the product are the outside dimenions.

Proposition 1.2.2. *Assuming that the sizes of the matrices are such that the indicated operations can be performed, the following rules of matrix arithmetic are valid.*

(a) $A + B = B + A$ *(Commutative law for addition)*

(b) $A + (B + C) = (A + B) + C$ *(Associative law for addition)*

(c) $A(BC) = (AB)C$ *(Associative law for multiplication)*

1.3 FURTHER RESULTS ON SYSTEMS OF EQUATIONS

In this section we shall establish more results about systems of linear equations and invertibility of matrices. Our work will lead to a method for solving n equations in n unknowns that is more efficient than Gaussian elimination for certain kinds of problems.

1.3.1 Some Important Theorems

Theorem 1.3.1. *If A is an invertible $n \times n$ matrix, then for each $n \times 1$ matrix B, the system of equations $AX = B$ has exactly one solution, namely, $X = A^{-1}B$.*

Proof. Since $A(A^{-1}B) = B$, $X = A^{-1}B$ is a solution of $AX = B$. To show that this is the only solution, we will assume that X_0 is an arbitrary solution, and then show that X_0 must be the solution $A^{-1}B$.

If X_0 is any solution, then $AX_0 = B$. Multiplying both sides by A^{-1}, we obtain $X_0 = A^{-1}B$. □

Theorem 1.3.2. *Let A be a square matrix.*

(a) If B is a square matrix satisfying $BA = I$,then $B = A^{-1}$.

(b) If B is a square matrix satisfying $AB = I$, then $B = A^{-1}$.

In our later work the following fundamental problem will occur over and over again in various contexts.

Let A be fixed $m \times n$ matrix. Find all $m \times 1$ matrices B such that the system of equations $AX = B$ is consistent.

If A is an invertible matrix, Theorem 2.3.2 completely solves this problem by asserting that for every $m \times n$ matrix B, $AX = B$ has the unique solution $X = A^{-1}B$.

CHAPTER 2

SYSTEMS OF LINEAR EQUATIONS AND MATRICES

2.1 INTRODUCTIONS TO SYSTEMS OF LINEAR EQUATIONS

In this section we introduce base terminology and discuss a method for solving systems of linear equations.

A line in the xy-plain can be represented algebraically by an equation of the form

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$$a_1x_1 + a_2x_2 + \cdots + a_nx_n = b \tag{2.1}$$

where $a_1, a_2, \ldots a_n$ and b are real constants.

Definition. A finite set of linear equations in the variables $x_1, x_2, \ldots, x_n$ is called a *system of linear equations*.

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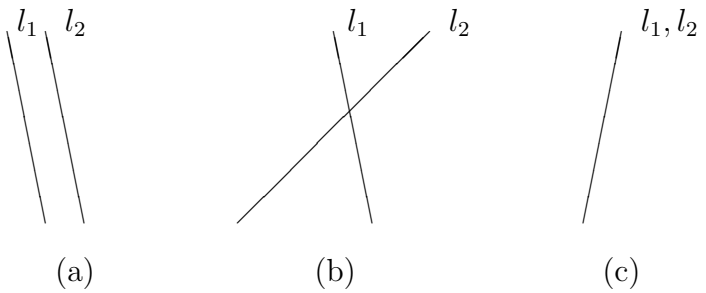

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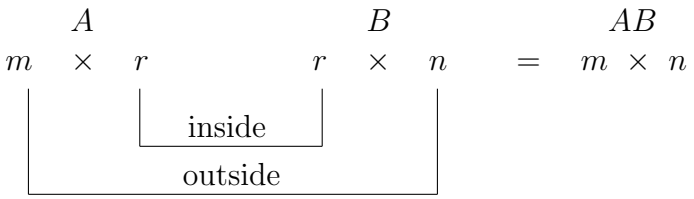

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CHAPTER 3

EXAMPLES

Some examples of the definitions found in the file ps-defs.tex follow below.

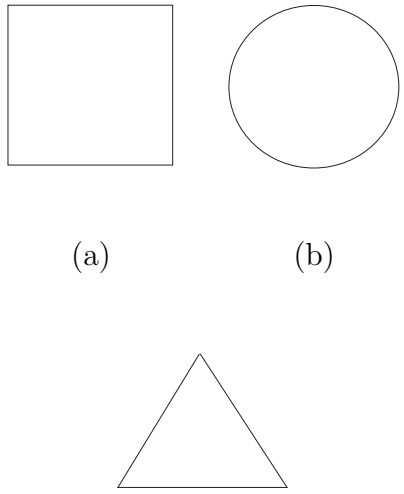
Here are examples of how you can use equation numbers with multiple line equations.

$$\begin{aligned}(f+(g+h))(a) &= f(a)+(g+h)(a)\\ &= f(a)+(g(a)+h(a))\\ &= (f(a)+g(a))+h(a)\\ &= (f+g)(a)+h(a)\\ &= ((f+g)+h)(a)\end{aligned} \tag{3.1}$$

$$\begin{aligned}(f+(g+h))(a) &= f(a)+(g+h)(a)\\ &= f(a)+(g(a)+h(a))\\ &= (f(a)+g(a))+h(a)\\ &= (f+g)(a)+h(a)\\ &= ((f+g)+h)(a)\end{aligned} \tag{3.2}$$

$$\begin{aligned}(f+(g+h))(a) &= f(a)+(g+h)(a)\\ &= f(a)+(g(a)+h(a))\\ &= (f(a)+g(a))+h(a)\\ &= (f+g)(a)+h(a)\\ &= ((f+g)+h)(a)\end{aligned} \tag{3.3}$$

Below is a figure which shows how to line up small figures on multiple lines. The .dvi version is immediately below. The .pdf version may be found underneath the complete figure and commented out. If you exchange the sections commented out, then you can compile a .pdf file.



(a) (b)

(c)

Figure 3.1. Two rows of graphics: (a) Square (b) Circle (c) Rectangle

Three figures across the page requires fairly small figures to fit within the Graduate School margins.

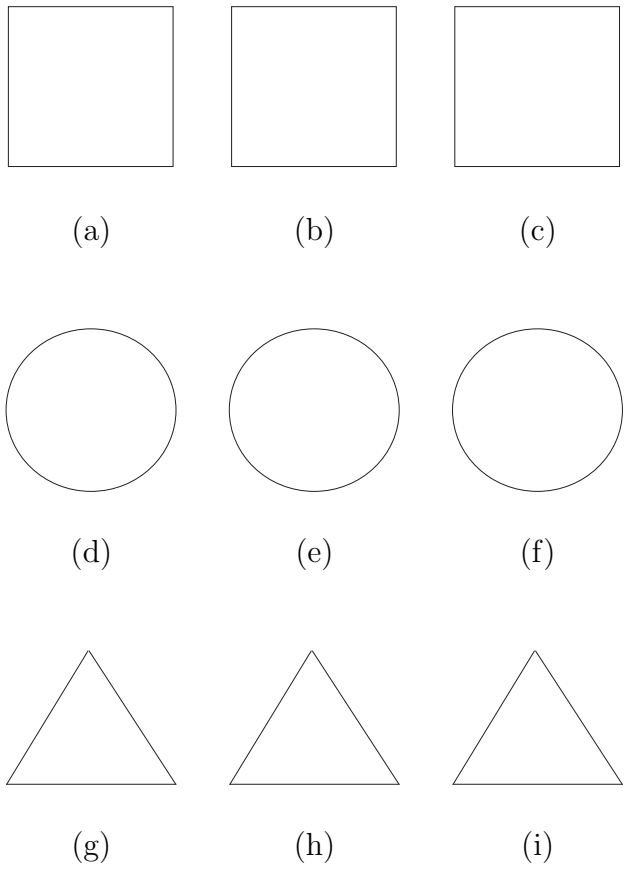


Figure 3.2. Three rows of graphics: (a)–(c) Squares. (d)–(f) Circles. (g)–(i) Ovals.

The verbatim environment can be useful when using data from a spreadsheet as is done below.

```
 X,TRUE_SUR,MSE SIM,MSE ZHAO,MSE JIAN,MSE PZHAO,MSE PJIAN
 0.0  0.7520  0.03864  0.01407  0.01407  0.01180  0.01223
 4.0  0.7273  0.04079  0.01675  0.01675  0.01479  0.01551
 8.0  0.7035  0.04203  0.01923  0.01923  0.01675  0.01817
12.0  0.6524  0.04581  0.02157  0.02135  0.01932  0.02043
16.0  0.6029  0.05146  0.02345  0.02266  0.02304  0.02320
20.0  0.5551  0.05343  0.02498  0.02393  0.02627  0.02509
24.0  0.5089  0.05449  0.02677  0.02453  0.02936  0.02641
28.0  0.4641  0.05706  0.02901  0.02442  0.03315  0.02722
32.0  0.4209  0.05719  0.02910  0.02341  0.03558  0.02776
36.0  0.3790  0.05656  0.02974  0.02229  0.03745  0.02667
40.0  0.3385  0.05518  0.02940  0.02119  0.03864  0.02618
44.0  0.2994  0.05344  0.02989  0.02054  0.03928  0.02531
48.0  0.2615  0.04950  0.02803  0.01906  0.03855  0.02414
52.0  0.2249  0.04582  0.02712  0.01812  0.03849  0.02229
56.0  0.1895  0.04101  0.02454  0.01578  0.03632  0.01918
60.0  0.1552  0.03564  0.02282  0.01315  0.03372  0.01629
64.0  0.1220  0.03216  0.02124  0.00997  0.03188  0.01391
68.0  0.0900  0.02420  0.01730  0.00688  0.02551  0.01070
72.0  0.0590  0.01592  0.01254  0.00363  0.01811  0.00622
76.0  0.0290  0.00865  0.00838  0.00110  0.00886  0.00368
```

Figure 3.3. Use of verbatim environment

On the following page is an example of how to rotate text that is too long to fit within the horizontal margins that are required.

$$
A = \begin{pmatrix}
-(\hat{\theta}_{D_1}(3;1) - \hat{\theta}_{D_1}(1;1)) & 0 & 0 & \cdots & 0 & 0 \\
(\hat{\theta}_{D_1}(3;1) - \hat{\theta}_{D_1}(1;1)) & -(\hat{\theta}_{D_2}(3;1) - \hat{\theta}_{D_2}(1;1)) & 0 & \cdots & \cdots & 0 \\
0 & (\hat{\theta}_{D_2}(3;1) - \hat{\theta}_{D_2}(1;1)) & -(\hat{\theta}_{D_3}(3;1) - \hat{\theta}_{D_3}(1;1)) & \ddots & \cdots & 0 \\
\vdots & \ddots & \ddots & \ddots & \ddots & 0 \\
0 & \cdots & 0 & 0 & (\hat{\theta}_{D_{n-1}}(3;1) - \hat{\theta}_{D_{n-1}}(1;1)) & -(\hat{\theta}_{D_n}(3;1) - \hat{\theta}_{D_n}(1;1)) \\
0 & 0 & 0 & 0 & 0 & (\hat{\theta}_{D_n}(3;1) - \hat{\theta}_{D_n}(1;1))
\end{pmatrix},
$$

$$
\begin{pmatrix} A_1 \\ A_2 \\ \vdots \\ A_n \end{pmatrix},
$$

Figure 3.4. Matrix Rotated 90 degrees.

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