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March 3, 2017

Dear TETC Editors,

Please find the enclosed manuscript "Radiation Hardened Latch Designs for Multi-Node Upsets" which we would like to submit as an original research article to the Reliability-aware Design and Analysis Methods for Digital Systems: from Gate to System Level special edition in the IEEE Transaction on Emerging Topics in Computing. In this manuscript, we focus on the development of radiation hardened latch designs that are hardened to radiation induced double and triple node upsets. In addition we created a new classification of latch designs based on their suitability for clock gating. An initial version of this work has been published in the 2016 IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2016) titled "A Highly Robust Double Node Upset Tolerant Latch". A document explaining the differences of the submitted manuscript and the published conference version are included with the submission of this paper.

Regards,

Adam Watkins, PhD