Radiation Hardened Latch Designs for Multi-Node Upsets

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Abstract—As the process feature size continues to scale down, the susceptiblity of logic circuits to radiation induced error has increased. This trend has led to the increase in sensitivity of circuits to multi-node upsets. In these circuits, the memory elements are the most vulnerable to error since data is held within the element. Previously, work has been done to harden latches against single event upsets (SEU). Currently, there has been a concerted effort to design latches that are tolerant to double node upsets (DNU). Future process technologies may lead to the likelihood of the a triple node upset (TNU). Base on this trend, a novel DNU tolerant design and TNU tolerant design are proposed. In addition to this, the DNU is designed to be robust for use in clock gating. This design is used as a basis for the TNU tolerant design. Through experimentation, it is shown that the DNU design is more efficient than all other DNU robust designs. The TNU tolerant latch is shown to have an overhead of (PUT NUMBERS HERE).

Index Terms—Soft Errors, Radiation Hardened Latch, Transient Pulses, Single Event Upset, Double Node Upset.

1 Introduction

As the transistor feature size continuously scales down to improve performance, modern circuitry continues to become more susceptible to radiation induced errors commonly referred to as a soft error. Terrestrial soft errors can manifest from either neutron particles originating from cosmic rays or alpha particles from packaging. In space, a soft error can come from gamma rays, protons, neutrons, electrons and heavy ions [1]. A soft error of any source occurs when a particle hits the diffusion region of a reverse bias transistor. This, in turn, allows an ”off” transistor to temporarily conduct current which can cause a voltage change in a node connected to the affected transistor. If the error occurs in combinational logic, the resulting voltage pulse may be propagated to a circuit output and capture by a flip-flop thus causing an error. Additionally, the error my occur directly on an internal latch of a flip-flop causing immediate data corruption. Due to this possibility, there is a need for new latch designs that can tolerate errors.

There has been extensive research in the field of hardening latches against single even upsets (SEU). The most straight forward hardening design is the use of triple modular redundancy (TMR). This design consists of 3 standard latches connected to a 3-input majority voting circuit. While this design is robust against errors, it has the drawback of high area, delay and power consumption. For this reason there have been many other designs proposed that offer high SEU reliability with lower area, delay and power consumption. The first and most common design is the DICE cell proposed in [2]. The design in [2] consists of 4 one-input c-elements connected in series. Two of the nodes are connected to a pass-gate which allows data to be loaded. When an error occurs in the DICE latch, the struck node is flipped. The two nodes connected to the struck node are set to a high impedance state and one node remains error-free. Since the error-free node is strongly driven to the correct value, it drives the remaining nodes back to the correct value. While this design work well for a single node, it is not capable of handling multi-node errors.

While the DICE latch is efficient in area, it suffers from high delay. For this reason there has been multitude of SEU tolerant devices that have been proposed. The SEU tolerant designs follow one of two approaches to hardening: sizing transistors such that the critical charge exceeds the maximum injected charge for the intended environment and by designing circuits that functionally tolerate the error. For the former designs, such as [9], they are typically performance and area efficient. The drawback with these types of designs is that they require accurate estimates for the maximum injected charge. If the maximum charge is found to be too high, a designer using this type of latch would have to choose between performance and reliability.

The latter type of latch, such as [3], [4], [5], [6], [7], [8], have the advantage of recovering from a SEU regardless of the injected charge due to the logical functions of the latch forcing recovery of affected node. In cases where the maximum injected charge is not excessively high, the latches have higher performance and area overheads. However, these type of latches are preferable in many cases since the maximum charge may be unknown or very high.

In modern processes, the transistor size is small enough that a radiation particle may strike multiple simultaneous transistors. Cases where this type of strike may occur are commonly referred to as a single event multiple upset (SEMU). In addition to the SEMU case, high radiation environments may allow for the manifestation of a multiple event multiple upset (MEMU). In this case, multiple radiation particles strike internal transistors simultaneously. When either a SEMU or MEMU strike a latch, they may upset multiple nodes. If two nodes are upset in the latch, this

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is referred to as a double node upset (DNU). If three nodes are upset, this is called a triple node upset (TNU). The DNU is currently of great concern as the feature size has allowed for a sharp increase in the occurrence of DNUs. Section (REFERENCE SECTION HERE) provides an overview of all existing DNU latches. To the author's knowledge, there has been no research done on the occurrence of the TNU. It can be inferred however, that future processes or high radiation environments, such as a mission to Mars or Europa, will allow for the TNU to be of large concern.

To save power, many modern circuit designs employ a technique commonly referred to as clock gating to further reduce the power consumption. Clock gating consists of shutting off the clock to a stable value or "gating" the clock. If clock gating is used in a latch, it may need to hold the stored value for many clock cycles. If the latch is struck by a radiation error while gated, it could lead to a loss of data. This may occur if the latch has high-impedance states after an error. If an error occurs, the high-impedance nodes may slowly discharge causing a loss in data. To remedy this issue, researchers have proposed the addition of output circuitry to hold the data. However, as shown in Section (REFERENCE SECTION HERE), the additional circuitry adds a large overhead to the delay and power consumption.

To solve this problem, we propose the HRDNUT (Highly Robust Double Node Upset Tolerant) latch which is an efficient DNU tolerant design that is capable of recovering all nodes after an error occurs. The recovery feature provides a distinct advantage over previous designs in cases where clock gating is used since it removes the need for the additional circuit since no nodes are held to a high-impedance state after an error. Designs that are DNU tolerant and exhibit this behavior are referred to as DNU-robust. Any design that is DNU tolerant and does has high-impedance states is referred to a DNU-non-robust. The proposed design is throughly compared to existing designs and is more efficient than the existing DNU-robust design in [14] in power, delay and area. The design is also compared to all existing DNU tolerant latches and the most common SEU tolerant latches.

In addition to the DNU latch, we also propose the TNU-latch which is a TNU tolerant latch that is based on the HRDNUT. While this latch is non-robust, it provides a simple and efficient solution suitable for high reliability applications. To the author's knowledge, the TNU latch is the first of its kind.

Lastly, even though there are masking factors in combination logic, depending on the design, the error-rate in combinational logic is not insignificant. In cases where an error occurs, the resulting voltage pulse may propagate to the circuit output. As proposed in [4], one approach to remove this type of error is to apply a filtering circuit on the combinational logic output. In the case of mult-node upsets, the design in [4] is vulnerable to error. An improved design is also proposed.

The paper is organized as follows: Section [REFERENCE] provides a discussion on existing DNU tolerant latches, Section [REFERENCE] discusses the HRDNUT, Section [REFERENCE] gives the TNU-latch, Section [REFERENCE] consists of the explanation for the pulse filtering circuit, Section [REFERENCE] contains a comparison of the proposed latches to many existing designs and Section [REFERENCE] concludes the paper.

2 Existing DNU Tolerant Designs

Currently, there are a few existing DNU tolerant designs. The first proposed design found in [10], referred to as the DNCS latch, consists of two DICE cells connected to an output Muller C-element. This design tolerates DNU's since each DICE element requires a DNU to flip its state. Since the assumption is that only two errors can occur at once, in the worst case only one DICE element flips its state. Due to the C-element, the latch output does not change value. This design has been shown to be very resilient to DNUs at a very high cost of area, delay and power. The authors in [11] propose an enhanced design compared to [10]. Their latch design consists of six 2 input C-elements connected in series which are then fed into a 3 input C-element. Like the DNCS latch, this design offers high resiliency to DNUs, however the power consumption and area overheads are still very high.

More recently, a highly area and power efficient design has been proposed in [12] and is referred to as the HSMUF latch. Fig. 1 provides the design. The HSMUF uses the TP-DICE [13] structure which consists of 6 cross-coupled elements. In the case of a DNU, if the error is on an adjacent node (such as a strike on n1 and n2), the TP-DICE element will fully recover the previous state. However, if the strike occurs on two non-adjacent nodes, the TP-DICE will not fully recover leaving one output node with an erroneous value, one node at high impedance and the remaining output node held at the error-free value. To provide reliability, the three nodes are connected to a C-element, as in Fig. 1, which allows the correct value to be held at the latch output.

While all of the previously discussed designs do provide high DNU reliability, none of them are classified as DNU robust since a DNU will result in high impedance states on the internal and output nodes. If an error occurs after a DNU, these latch designs will flip their held value. A popular remedy to this issue is to place a weak keeper on the latch output as in Fig. 1. However, adding a weak keeper greatly increases the power, area and delay overheads since the output C-element must be re-sized so that the C-element's driving strength exceeds that of the keeper. According to our simulations in Section 4, the addition of the keeper to the HSMUF latch nearly triples the power consumption and delay. Additionally, the latch is still vulnerable to error after a DNU since the TP-DICE is in a high impedance state.

To the author's knowledge, the existing most efficient DNU robust design capable of recovering all nodes after a DNU is the DONUT latch [14] in Fig 2. The design, as proposed in their paper, uses only 36 transistors but has a much higher power consumption compared to the HSMUF (See Section 4). The reason for the high power consumption is due to contention on the input lines during the transparent mode. For example, if we observe node *n2* in Fig. 2 during the transparent mode, the node is driven by three cross-coupled elements. This contention will increase the amount of time required to change the node thus drastically increasing the dynamic power consumption. To optimize

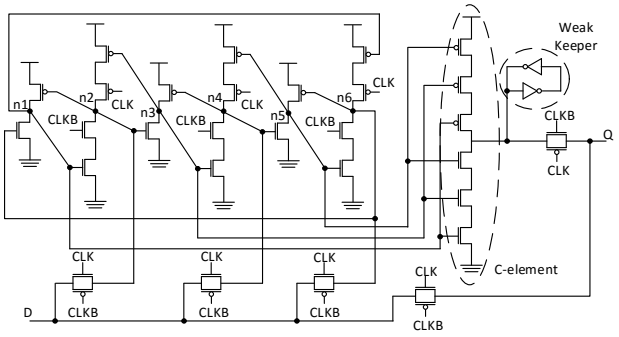

Fig. 1: HSMUF latch [12] with a weak keeper on the output.

their design, we create the 48 transistor DONUT-M latch in which each component connected to an input node is modified, as shown in Fig. 3 so that the line is at high impedance for the whole duration of the transparent mode. This, in effect, removes the data contention problem thus reducing the overall dynamic power and delay.

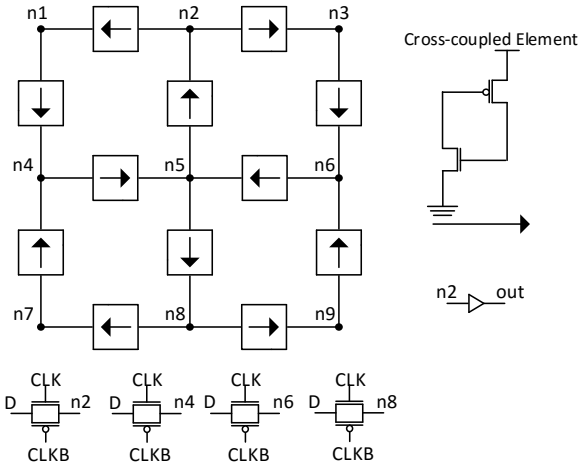

Fig. 2: DONUT latch as proposed in [14].

3 Proposed HRDNUT Latch Design

In this section we discuss the proposed DNU robust latch. The latch implementation is based on three cross connected storage loops connected to three C-elements. The basic design of the storage loop is given in Fig. 4. The data loop is based on the standard latch design with a 3-input C-element inserted to replace one of the inverters. The purpose of the C-element is to separate the feedback loop so that an error will not be held. Additionally, a PMOS is connected to the positive clock signal (CLK) and a NMOS is connected to the negative clock signal (CLKB) to remove contention when data is loaded to the latch. As in the modified DONUT latch, the addition of these transistors drastically reduces the delay and power consumption.

Using the basic storage block we construct the block based latch as in Fig. 5. The latch was designed with the goal

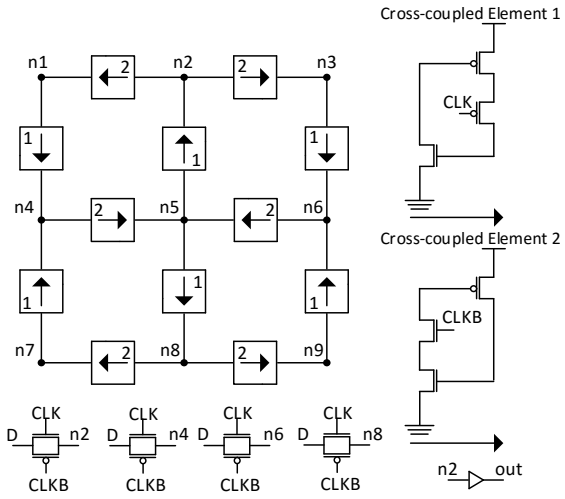

Fig. 3: Modified low-power DONUT latch.

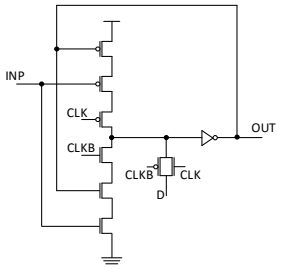

Fig. 4: Basic data storage loop block.

of ensuring that none of the nodes directly drove itself. For example, it can see that in Fig. 4 the node *out* is fed into the input of the 3-input C-element. If an error strikes node *out*, the cell will never be able to recover its previous state since one of the C-element inputs will be held to an erroneous value by its output. To prevent this issue, our design is based on cross-connecting three of the storage loop blocks so that the C-element is driven by three separate block outputs. In Fig. 5 we provide a basic latch design using this idea. If a single error occurs on any node in this design, the circuit is capable fully recovering the previous data.

To demonstrate this, consider a strike on node *n2*. When the strike occurs, the erroneous value will be propagated to the C-elements driving nodes *n1* and *n3*. However, since there is no change on *n1* or *n3*, the C-elements *C1* and *C3* will hold their previous value thus preventing the error from propagating to the output. Additionally, since node *n2* is driven by nodes *n1* and *n3*, *n2* will completely recover the correct state.

A problem, however, with the latch in Fig. 5 is that it is not capable of tolerating DNUs. For example, if an error occurs on nodes *n1* and *n2* the erroneous values will propagate to the inputs of C-element *C3* and flip the value of *n3* thus changing the output value. However, since the latch has recovery capability for SEUs, we modify it so it can tolerate DNUs and recover all nodes to the previous

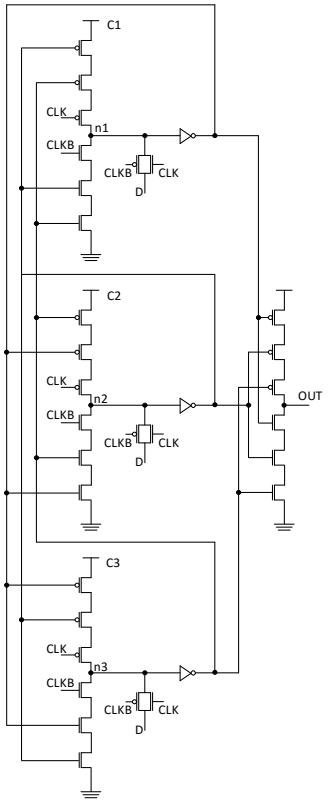

Fig. 5: Schematic of the block-based latch.

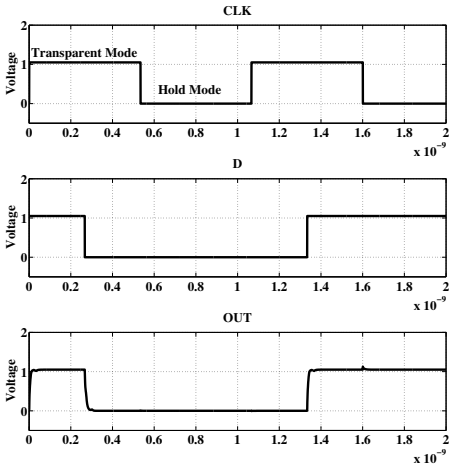

Fig. 6: Waveforms of the HRDNUT latch during normal operation.

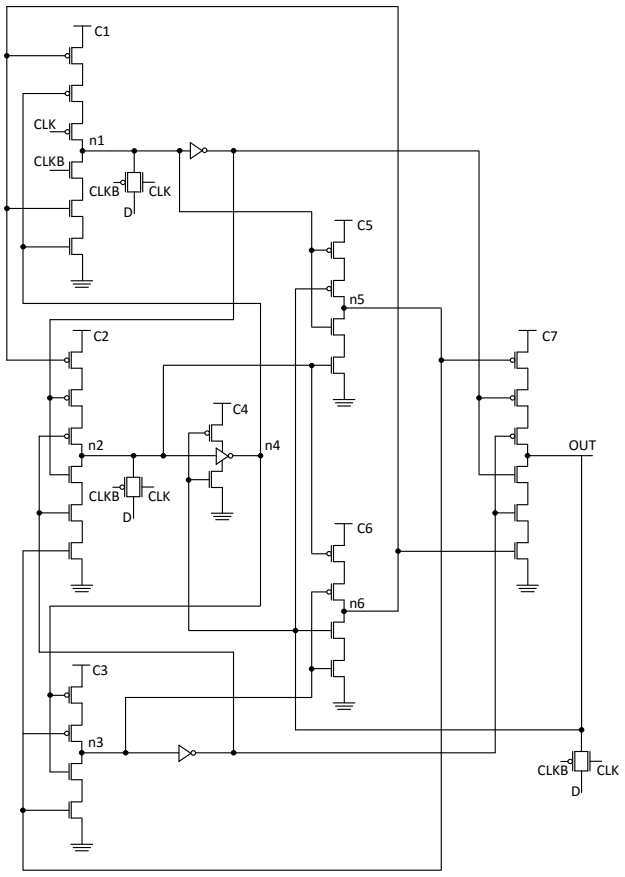

Fig. 7: Schematic of the HRDNUT latch.

state. In Fig. 7 we provide the schematic of the proposed HRDNUT latch. The design uses the block-based latch in Fig. 5 as a base and adds additional C-elements to prevent errors from being held by the data loop.

Initially, we will evaluate the HRDNUT latch during normal operation. When the positive clock signal (CLK) has a high value and the negative clock signal (CLKB) has a low value, the latch is in transparent mode. At this stage, the transistors connected to the clock signal in C-element *C1* deactivates the PMOS and NMOS stacks thus causing the node *n1* to be in a high impedance state. This, in effect, reduces data contention thus reducing delay and dynamic power consumption. Next, the data is loaded through the pass gates connected to nodes *n1*, *n22* and *out*. Since the output node *out* is loaded directly, the data to out delay is minimized and all nodes are set to their respective error free values. When CLK changes to a low value and CLKB to a high value, the latch moves into the hold mode. In this stage, the pass gates are deactivated and the state of the latch is held since each node is driven to the correct value using a C-element. Fig. 6 provides the waveforms of the CLK, D and OUT nodes for both the transparent and hold modes of operation.

In the case of an SEU, the HRDNUT retains the excellent resiliency of the block based latch and the ability to recover every node after an error. In the case of any internal node being struck by an error, the latch will not change value due to all internal C-elements requiring at least 2 identical input values to change values. In the case of an error hitting the output node *out*, the latch fully recovers since *out* does not directly drive C-element *C7*.

Lastly, we will evaluate the latch in the case of a DNU. Note that unless otherwise stated, it is assumed that the analysis applies to both when D=0 and D=1. For our analysis, we categorize the possible DNU strike combinations into 9 distinct cases based on their effect in the HRDNUT latch. The categories are discussed in detail below:

1) Consider strikes at nodes *n1* and *n2*. In this case, the error at *n1* will propagate to C-elements *C5* and *C7* but will not cause a flip since the error at *n2* will be blocked by C-element *C4*. Additionally, since the inputs of C-elements *C1* and *C2* are unchanged, the nodes will recover their initial values. This analysis can be applied to node combinations containing node *n2* except for the combination with node *out* since the error will be blocked by C-element *C4*.
2) In the case of a DNU upsetting nodes *n2* and *out*, the error at *n2* will propagate through C-element *C4*. However, C-elements *C1* and *C3* will block the error and nodes *n1*, *n3*, *n5* and *n6* will hold their values thus driving node *out* to the correct state.
3) Consider when a DNU strikes nodes *n1* and *n5*. In this case, the error at *n1* hits the output of C-element *C1* which is propagated to *C7*. The error on *n5* is also propagated to C-element *C7*. Since node *n3* and the inputs of C-elements *C1* and *C5* are unaffected by an error, the output retains the error-free value and the latch fully recovers the previous state. The above analysis also applies to the node combination (*n3*, *n6*).
4) In the case of a DNU hitting nodes *n3* and *n4*, the error at *n4* is propagated to C-element *C3* and the error at *n3* is propagated to *C7* and *C6*. After the error on *n3* subsides, *C4* will drive node *n4* and, due to the connection at *C3*, node *n3* back to the error-free value. The node combination (*n1*, *n1*) can be analyzed similarly. For the node combinations of (*n4*, *n5*) and (*n4*, *n6*), the latch will also recover the previous result since the inputs to *C4* are unchanged. This implies that after the error occurs at *n4*, the node will be driven back to the correct value thus also driving the nodes *n5* or *n6* back to the correct value.
5) When a DNU upsets the combination of *n4* and *out*, the error at *out* is propagated to *C4*, *C5* and *C6* and the error at *n4* to *C1* and *C3*. Since none of the inputs to *C7* are changed by the error, *out* is flipped back to its error-free value which drives *n4* through *C4* back to its previous state.
6) Consider when a DNU strikes nodes *n1* and *n3* being struck. In this case, the errors are propagated to C-elements *C2*, *C5*, *C6* and *C7*. However, since the errors do not manifest into an error on any other node, the latch fully recovers from the error.
7) When a DNU strikes the nodes *n1* and *n6*. The error at node *n6* propagates to *C1* and *C7* while the error at *n1* also propagates to *C7*. Due to the error-free node *n3* driving *C7*, the previous value is held at the output by *C7*. Additionally, *n3* will drive *C6* back to its previous value thus driving *C1* back to the error free state. This analysis can be applied similarly to the node combination of (*n3*, *n5*).
8) In the case where a DNU strikes nodes *n5* and *out* the error at *n5* propagates to *C7*, *C2* and *C3* and the error at *out* goes to *C4*, a PMOS in *C5* and a NMOS in *C6*. When the error-free value at *out* is 1, the value at *n5* is 0. The error at the nodes change the values to 0 and 1 respectively and the erroneous value at *out* is propagated to the PMOS at *C5* and the NMOS at *C6*. This, in effect, causes the PMOS at *C5* to be activated and the NMOS at *C6* to be deactivated. However, since nodes *n1* and *n2* remain error-free, the NMOS stack of *C5* will drive *n5* back to the correct value. This, in turn, forces *C7* to also drive *out* back to the error-free value. In the case where *out* has an ideal value of 0, the error will be fully recovered since the NMOS stack will be entirely driven by fault-free nodes. The above analysis can be applied to the node combination of (*n6*, *out*).
9) Lastly, we analyze the node combinations (*n1*, *out*), (*n3*, *out*) and (*n5*, *n6*). In these cases the errors do not cause a change on the inputs of any C-elements driving the node thus the previous value will always be recovered.

4 Simulation Results

The proposed HRDNUT latch has been implement using the 1.05V 32nm PTM library [15] and simulated in HSPICE. All transistors were set to the minimum size with the PMOS widths set to W=80nm and the NMOS widths set to W=40nm. To evaluate the DNU reliability of the design, current pulses were injected for every possible error combination. The injection current was calculated using the equation found in [16]. The equation is given below with τ as the technology dependent constant, Q_o as the injection current value and t as the variable for time.

$$I(t) = \frac{2Q_o}{\tau\sqrt{\pi}}\sqrt{\frac{t}{\tau}}e^{\frac{-t}{\tau}} \quad (1)$$

Using equation (1) τ was set to 32×10^{-12} and Q_o was set to $5fC$. In all simulations, the latch was operated at a frequency of 1Ghz. In Figs. 8-17, we present the waveforms for each case discussed in Section 3 and show that the HRDNUT is fully capable of recovering all nodes in the presence of a DNU.

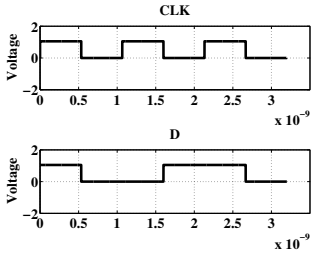

Fig. 8: Waveforms for CLK and D.

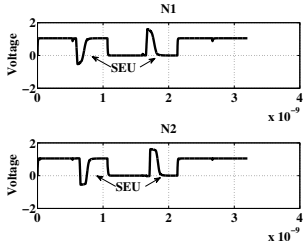

Fig. 9: Node pair n1 and n2 upset and recovery.

Next, we compare the HRDNUT to existing SEU and DNU tolerant methods. As in the HRDNUT latch, all latches were designed using the 32nm PTM library and operated at 1Ghz. For the analysis, we compare to the following SEU tolerant latches: DICE [2], FERST [4] and HIPER [3]. Additionally, we also compare to the following DNU tolerant designs: DNCS [10], Interception [11], HSMUF [12] and DONUT [14]. All transistors for the implemented latches were set to minimum width and length except for the

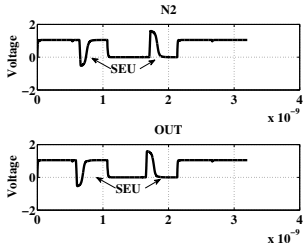

Fig. 10: Node pair n2 and out upset and recovery.

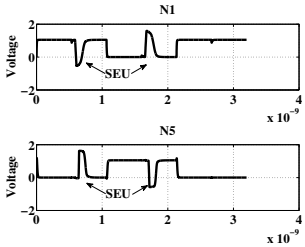

Fig. 11: Node pair n1 and n5 upset and recovery.

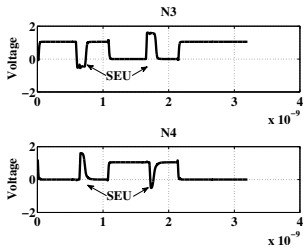

Fig. 12: Node pair n3 and n4 upset and recovery.

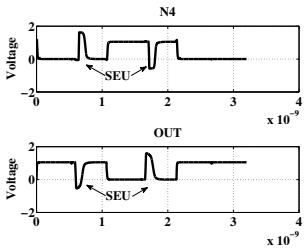

Fig. 13: Node pair n4 and out upset and recovery.

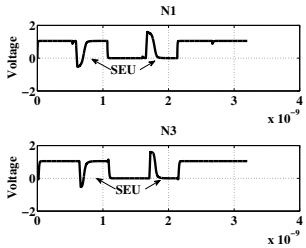

Fig. 14: Node pair n1 and n3 upset and recovery.

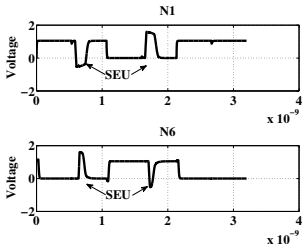

Fig. 15: Node pair n1 and n6 upset and recovery.

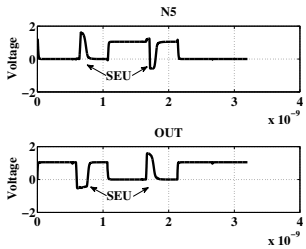

Fig. 16: Node pair n5 and out upset and recovery.

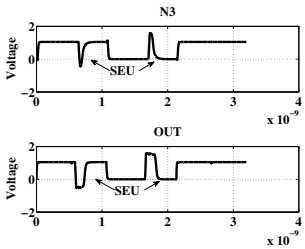

Fig. 17: Node pair n3 and out upset and recovery.

designs that use a C-element with a weak keeper. In these designs the C-element's PMOS width was set to W=320nm and the NMOS width was set to W=160nm and the weak keeper was sized to be at minimum width. The C-element was sized so that the output driving strength did not allow the keeper to drive an erroneous value in the event of an error.

To provide a fair comparison, we measure the propagation delay, average power consumption and area of all designs and categorize them base on whether they can tolerate a DNU and if they are robust from error after a DNU occurs. The delay was measured as the time between when a transition occurs on input D to when a transition was observed on the output. The average power was computed using the error-free operation for each latch for a duration of 200ns. To compare the area overhead, we adopt the unit size transistor (UST) metric as in [10] which represents the number of unit sized (minimum width is W=40nm in this case) transistors required for the design. Table 1 provides the results of these simulations.

TABLE 1: SPICE Simulations of Existing Latches using the 1.05V 32nm PTM library

Latch	DNU Immune	DNU Robust	Power (μW)	Delay (
DICE	No	No	1.332	8.145
FERST	No	No	3.178	31.64
HIPER	No	No	1.292	2.221
DNCS	Yes	No	4.948	22.48
[11]	Yes	No	5.606	79.16
HSMUF	Yes	No	1.871	1.062
HSMUF (Keeper)	Yes	No	3.787	3.945
DONUT [14]	Yes	Yes	4.021	14.72
DONUT-M (Section 2)	Yes	Yes	2.760	8.421
HRDNUT (Proposed)	Yes	Yes	2.450	2.310

According to Table 1 the only DNU robust designs are the two DONUT latch implementations and the HRDNUT. Compared to the modified DONUT latch, the HRDNUT provides DNU robustness while reducing the power consumption and number of transistors by 11.3% and 8.33% respectively while also reducing the delay by 72.5%. For the above reasons, the HRDNUT is the best design for clock gating applications due to its high robustness, even after a DNU occurs, and lower power, delay and area overheads.

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