ADITYA WAGH

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EDUCATION

Birla Institute of Technology and Science (BITS) Pilani

Pilani, India

Bachelor of Engineering with Honors in Electronics and Instrumentation

Aug 2015 - Jul 2019

GPA: 5.55

Relevant courses: Computer Programming, Probability & Statistics, Neural Networks and Fuzzy Logic, Discrete Mathematics, Digital Signal Processing, Digital Design, Microprocessors and Interfacing, Computer Architecture

CERTIFICATIONS

Neural Networks and Deep Learning

Coursera

deeplearning.ai

August, 2018

WORK EXPERIENCE

Integrated Systems Lab

Central Electronics Engineering Research Institute, Pilani

Research Assistant

Jul 2018 - Dec 2018

Project: Detection of faulty power transmission lines using Region Proposal Convolutional Neural Networks(RCNNs)

- Project focused on decreasing costs and safety of inspecting power transmission lines using unmanned drones, instead of manual helicopter inspection.
- Part of a team responsible for annotating a dataset of 8000 RGB and Infrared images of power transmisison cables. Used
 VIA Image Annotator for annotation.
- Responsible for modelling, training and optimising a Convolutional Neural Network to detect healthy power lines in those images.
- o Trained a masked region proposal convolutional neural network having a ResNet-101 and FPN Backbone.

PROJECTS

• Variable Computation in Recurrent Neural Networks (2017):

- o Modified a RNN model to make it learn to vary the amount of computation according to the sequence that they process.
- o Implemented a scheduler for the RNN unit which decides the computation required at the current timestep.
- o Reduced the number of operations for bit-level language modelling to around 50% compared to normal RNN unit.

Microphone Signal Conditioning System (2017):

- o Designed a signal conditioning circuit for a microphone using OPAMPS.
- Utilised the condenser microphone as a capacitance in the RC Filter Circuit.
- Interfaced the circuit with the computer using NI-DAQmx data acquisition card and created a UI in LabVIEW to interpret the noisy and filtered signals.

• Finite Impulse Response filter design using an adjustable window filter (2017):

- o Implemented an adjustable window function based on the combination of Blackman and Lanczos window.
- o Achieved a 75% better better side-lobe roll off ratio than Lanczos window.
- o Denoised an ECG Signal using this filter.

Positions of Responsibility

Vice-Chairperson

Jul 2017 - May 2018

IEEE Student Branch, BITS Pilani

Appointed as the Vice Chairperson of the IEEE Student Branch at BITS Pilani

- o Organised IEEE affiliated events like conclaves, workshops and various technical events throughout the year.
- Worked on promoting IEEE Student memberships in the campus by organising membership drives explaining it's benefits.
- o Responsible for setting up the IEEE hosted website for the chapter.
- o Conceived the organisational hierarchy of the chapter, introducing various managerial and technical posts.
- o Authored and published the first issue of IEEE Insight, the monthly newsletter of the chapter.

• Member, Governing Council(GC)

Aug 2018 - July 2019

Society for Students Mess Services, BITS Pilani

Elected as the Mess Representative of the Ranapratap-Ashok Mess which served more than 400 students. Part of the Quality, Health & Safety Environment(QHSE) committee and the Human Resource committee of the GC.

- o Mess Representative: Responsible for sanctioning leaves of the workers, collecting feedback and taking necessary actions.
- o QHSE: Drafted a QHSE framework for SSMS activities and conducted regular audits every semester.
- HR: Responsible for performance appraisals, providing education/medical loans and managing internal worker conflicts.

TECHNICAL PROFICIENCY

- **Development Languages**: Python, C, , C++, MATLAB, Verilog, bash, markdown, LATEX
- Frameworks and Libraries: Keras, Tensorflow, OpenCV, Linux, Git
- Application Softwares: MATLAB, Simulink, LabVIEW