ADITYA WAGH

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Education

- **Birla Institute of Technology and Science (BITS) Pilani** — **Pilani, India**
  Bachelor of Engineering with Honors in Electronics and Instrumentation, GPA*: 5.55* — *Aug 2015 – Jul 2019*
  Relevant courses: Computer Programming, Probability & Statistics, Neural Networks and Fuzzy Logic, Discrete Mathematics, Digital Signal Processing, Digital Design, Microprocessors and Interfacing, Computer Architecture
- **LVH Arts, Science & Commerce College** — **Nashik, India**
  Higher Secondary Ceritificate, MSBSHSE, Marks*: 85.69%* — *Aug 2013 – June 2015*
- **Symbiosis School** — **Nashik, India**
  All India Secondary School Examination, CBSE, GPA*: 10* — *Jun 2009 – May 2013*

Technical Proficiency

- **Development Languages**: Python, C, C++, MATLAB, Verilog, bash, markdown, LaTeX, HTML, CSS
- **Frameworks, Libraries and Operating Systems**: Keras, Tensorflow, OpenCV, Linux, Git
- **Application Softwares**: MATLAB, Simulink, LabVIEW

Certifications

- **Neural Networks and Deep Learning** — **Coursera**
  deeplearning.ai — *August, 2018*

Work Experience

- **Integrated Systems Lab** — **Central Electronics Engineering Research Institute, Pilani**
  Research Assistant — *Jul 2018 – Dec 2018*
  Project: Detection of faulty power transmission lines using Region Proposal Convolutional Neural Networks(RCNNs)
  - Project focused on decreasing costs and increasing safety of inspecting power lines by replacing helicopter inspection with drones.
  - Part of a team responsible for annotating a dataset of 8000 RGB and Infrared images of power transmisison cables.
  - Responsible for modelling, training and optimising a Convolutional Neural Network to detect healthy power lines.
  - Trained a masked region proposal convolutional neural network having a ResNet-101 and FPN Backbone.

Projects

- **Variable Computation in Recurrent Neural Networks (2017)**:
  - Modified a RNN model to make it learn to vary the amount of computation according to the sequence that they process.
  - Implemented a scheduler for the RNN unit which decides the computation required at the current timestep.
  - Reduced the number of operations for bit-level language modelling to around 50% compared to normal RNN unit.
- **Microphone Signal Conditioning System (2017)**:
  - Designed a signal conditioning circuit for a microphone using OPAMPS.
  - Utilised the condenser microphone as a capacitance in the RC Filter Circuit.
  - Interfaced the circuit with the computer using NI-DAQmx data acquisition card and interpreted noisy signals in LabVIEW.
- **Finite Impulse Response filter design using an adjustable window filter (2017)**:
  - Implemented an adjustable window function based on the combination of Blackman and Lanczos window.
  - Achieved a 75% better better side-lobe roll off ratio than Lanczos window.
  - Denoised an ECG Signal using this filter.

Positions of Responsibility

- **Vice-Chairperson** — *Jul 2017 - May 2018*
  IEEE Student Branch, BITS Pilani
  Organised IEEE affiliated events like conclaves, workshops and various technical events throughout the year.
  - Worked on promoting IEEE Student memberships in the campus by organising membership drives explaining it's benefits.
  - Responsible for setting up the IEEE hosted website for the chapter.
  - Conceived the organisational hierarchy of the chapter, introducing various managerial and technical posts.
  - Authored and published the first issue of IEEE Insight, the monthly newsletter of the chapter.
- **Member, Governing Council(GC)** — *Aug 2018 - July 2019*
  Society for Students Mess Services, BITS Pilani
  Part of the Quality, Health & Safety Environment(QHSE) and Human Resource(HR) committee
  - **Mess Representative:** Responsible for sanctioning leaves of the workers, collecting feedback and taking necessary actions.
  - **QHSE:** Drafted a QHSE framework for SSMS activities and conducted regular audits every semester.
  - **HR:** Responsible for performance appraisals, providing education/medical loans and managing internal worker conflicts.