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Sheet 2

(1) a) & b)

- Normal Pipelining = 200 ps
  - for single cycle processor, between two instructions
    = 200 + 100 + 200 + 200 + 100 = 800 ps
  - for pipelined processor = Max (time of stages)
    = 200 ps
  - Speedup = $\frac{\text{Single Cycle}}{\text{Pipeline}} = \frac{800}{200}$ ps

- After reducing ALU:
  - Single Processor = 200 + 100 + 150 + 200 + 100 = ~~750~~ ps
  - Pipelined processor = 200 ps
  - Speedup = $\frac{750}{200} = 3.75$

Speedup decreased by 0.9375

- After increasing ALU:
  - Single Processor = 850 ps
  - Pipeline Processor = 250 ps
  - Speedup = $\frac{850}{250} = 3.4$

Speedup decreased by 0.85

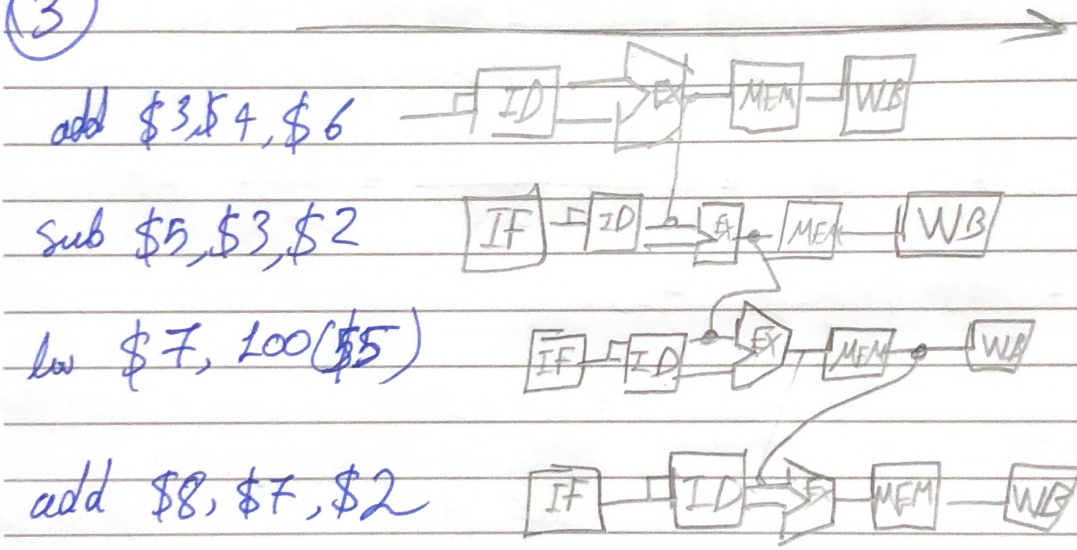
NOTES.

(2) a) it takes 100 ps * 10^6 instructions

$= 10^8$ ps to execute the program on a non-pipelined processor

b) A perfect 20-stage pipeline would speed up the execution by 20 times

(3)



(4)
- There is data dependancy through $3 between the first instruction and each subsequent instruction
- There is a data dependancy through $6 between the lw instruction and the last instruction
- For a five-stage pipeline, the data hazard between the 1st & 2nd & 3rd can be resolved by using forwarding

- The data dependancy between the load and the last add cannot be resolved by only using fowarding so it will cause a stall then $6 will be fowarded to the add instruction

(5) - At the end of 5th cycle:

- registers $6 & $1 are being read
- register $2 will be written