Abdelrahman Adel Sheet 1 17/12/2016

(1) a) All R-format instructions, in addition to lw will not work because will not be able to write the results to register file

b) All R-format except substract will work not correctly because ALU will perform substract instead of the requested operation

c) beq instruction will not work because ALU will do addition instead of substraction

d) beq will not execute correctly, the branch instruction will always be not taken even if it should

e) lw will not execute correctly because it will not be able to read from memory

f) Sw ill not work correctly because it will not be able to write to memory

(2) a) Jump and branch will write their target address to register file.

b)

c)

d) will always branch even if it shouldn't

e) All instructions will work correctly but IRWrite and IorD will safeguard

f) All instructions wont work correctly

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4) - modification required for data path to perform auto increment by one.

- The new write port will be controlled by a new "write2" signal

- a row bne should be added to truth table:

RegDst	0
ALUSrc	1
MemtoReg	1
RegWrite	1
MemRead	1
MemWrite	0
Branch	0
ALUOP	00
Write2	1

NOTES

⑥ a) The Control unit can begin generating Mem write after I-Mem is read. it must finish generating this signal before the clock cycle

The CU must generate after the instruction fetch and before end of cycle by a time large enough to write the data to data memory (D-mem access)

⑤ a) I-Mem, Regs, Mux, ALU, Mux

b) I-Mem, Regs, Mux, ALU, Mux

c) I-Mem, Regs, Mux, ALU, Mux, PC