

# Sustainability Benchmark of Subthreshold Level Shifters for IoT Applications

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**Abstract**—The advancement of semiconductor technology has intensified the demand for ultra-low-power ICs, especially in energy-constrained IoT applications. With continued scaling, the subthreshold operation has become a promising approach for minimizing power consumption. In advanced SoCs utilizing dynamic voltage and frequency scaling (DVFS), Level Shifters are essential for interfacing domains operating at different voltage levels. When one of the voltage islands functions at a subthreshold voltage, specialized Subthreshold Level Shifters (SLS) are employed to ensure reliable signal transition. Various SLS architectures are available in the industry, each evaluated based on conventional PPA (Power, Performance, and Area) metrics to determine their suitability for different applications. Beyond PPA, the integration of a sustainability evaluation paradigm broadens the analysis by assessing the fabrication and operational impact of a design, ensuring long-term efficiency and a reduced carbon footprint. In this work, a set of SLS architectures has been benchmarked using a novel sustainability-focused evaluation paradigm in 65nm Low Standby Power technology. This benchmark paradigm enables designers to choose the most efficient and sustainable SLS architecture among the available ones.

**Index Terms**—Level Shifter, Subthreshold, Sustainability metric, Low-power design, Embodied footprint, Operation footprint

## I. INTRODUCTION

In the VLSI industry, ICs are primarily evaluated on the basis of the power, performance, and area (PPA) trade-off, which determines design efficiency and reliability. Achieving an optimal balance is particularly challenging for low-power designs [1]. Beyond PPA, the growing emphasis on sustainability requires assessing the environmental impact of an IC from its fabrication to its operation [2].

The sustainability focus is particularly crucial in domains such as the Internet of Things (IoT) and wearable devices, where the subthreshold operation has emerged as an effective approach to achieve significant power reduction [3], [4]. However, circuits operating in this regime face challenges such as low drive strength, high propagation delays, and increased sensitivity to variations. These limitations become more critical when low-voltage domain circuits interface with nominal supply voltage blocks.

To bridge this multi-voltage domain communication, Level Shifters are employed, which ensure smooth signal transition between different voltage domains. Their effectiveness is determined by their ability to support large voltage shifts

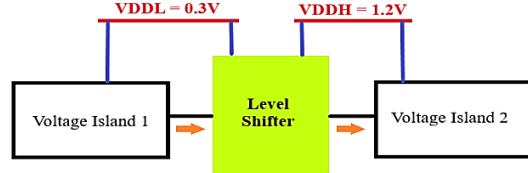


Fig. 1. Level Shifter reference block diagram

while minimizing power consumption, propagation delay, and area overhead. Subthreshold Level Shifters (SLS), designed for ultra-low-power applications, play a crucial role in such scenarios by bridging voltage transitions between the subthreshold and nominal voltage islands [5]. Fig. 1 illustrates an SLS block diagram that transitions signals from low voltage ( $VDDL = 0.3V$ ) to high voltage ( $VDDH = 1.2V$ ).

This work implements and benchmarks a curated set of conventional and advanced SLS architectures using a proposed sustainability-driven evaluation paradigm. This approach enables the evaluation of each design's efficiency by extending beyond conventional PPA metrics to include its environmental impact, accounting for both its fabrication and operational aspects. Thus, enabling designers to determine the most efficient and sustainable SLS architecture for specific applications by using the proposed Power, Performance, Area, and Sustainability (PPAS) evaluation paradigm.

A key advantage of this approach is that it facilitates the consideration of sustainability-aware decisions in the early phase of the chip design flow. This may result in a reduced carbon footprint for the SoC that incorporates sustainability-assessed Level Shifter cells. Furthermore, the SLS layout implementations designed in this work adopt a unique double-row standard cell format rather than the common single-row format, thus optimizing area efficiency and reducing the manufacturing footprint. This work is conducted using 65nm Low Standby Power technology from STMicroelectronics and implemented in the Cadence Virtuoso design environment.

## II. LOW-POWER AND SUSTAINABILITY CONSIDERATIONS IN SUBTHRESHOLD LEVEL SHIFTER (SLS)

The following sections discuss low-power design strategies and the significance of subthreshold operation in reducing power consumption. Additionally, the sustainability aspects

of design choices are discussed, emphasizing how low-power techniques, including subthreshold operation, influence the environmental and operational footprint of SLS architectures.

### A. Low-Power Design

In today's advanced technology processes, efficient power management is a critical design aspect apart from achieving high performance. Reducing power dissipation without compromising functionality is essential for enhancing operational lifespan and reliability. Hence, designers often resort to low-power design techniques in IC development, such as multi-threshold devices, power gating, etc [6]. Level Shifter is one such technique, which is being deployed in most of the advanced IC designs, especially in domains like IoT.

Level Shifters facilitate the interface between multiple voltage domains, as some regions within an IC may operate at lower voltages to reduce power consumption, while others require higher voltages to support performance-intensive operations [7]. In particular, when a voltage island functions in the low-power Subthreshold region, specialized Subthreshold Level Shifters (SLS) play a crucial role in ensuring reliable signal transitions while optimizing energy efficiency.

### B. Subthreshold Operation for Power Efficiency

As discussed in the previous section, designers often implement low-power design techniques for advanced IC development. Hence, the subthreshold operation has become a potential technique for them to achieve low-power consumption in modern circuits while maintaining efficient performance. In the subthreshold region, devices operate at voltages lower than their threshold voltage (VT), allowing them to transition using leakage current without the requirement of a strong inversion channel. In this region, the drain current follows an exponential dependence on gate voltage, thus consuming low-power. [8].

### C. Sustainability Considerations in Low-Power VLSI Design

Understanding the sustainability aspect is essential for choosing an efficient and reliable circuit architecture in the current ecological era. Sustainability emphasizes developing reliable products while minimizing their long-term environmental impact [9]. However, rather than developing a new sustainable architecture, this work proposes a sustainability evaluation paradigm to quantify and benchmark the environmental impact of various existing SLS architectures. This will allow designers to make sustainable design choices.

In VLSI industries, sustainability is generally assessed at the chip/product level by using standardized methods like Life Cycle Assessment (LCA) and the Greenhouse Gas (GHG) Emission Protocol. LCA evaluates the environmental impact of hardware components by quantifying their carbon emissions/footprint, while GHG classifies them into categories of Scope 1, Scope 2, and Scope 3. The carbon footprint (CFP) is generally divided into two key types: (a) Embodied footprint, which accounts for the emissions resulting from semiconductor fabrication & its infrastructure setup, and (b) Operational

footprint, which considers the energy usage and emissions produced throughout the functional life of the hardware [10].

Existing methods for sustainability evaluation generally work at a higher abstraction level, aiming to assess the carbon footprint of an IC/product after it has been manufactured. However, a method to help designers assess sustainability at the early stages of the chip design process, i.e., at individual computing logic cell selection (here, Level Shifter), is still not available. To tackle this challenge, this work presents a designer-centric paradigm for evaluating an individual SLS cell's carbon footprint arising from both its manufacturing and operational phases. Section IV provides insights into the proposed sustainability evaluation paradigm, validates it on the selected SLS architectures, and presents the corresponding results and analysis. However, before that, the following section introduces the set of selected SLS architectures.

## III. LEVEL SHIFTER

Prior to delving into the details of the proposed paradigm, a thorough understanding of Level Shifters is necessary, which forms its basis. So, this section gives a brief overview of Level Shifters and their importance in advanced IC. It further provides detailed post-layout observations of existing Figures of Merit for SLS architectures, serving as a basis for applying and evaluating the proposed PPAS paradigm in Section IV.

Level Shifters are a low-power design technique that enables signal transitions between lower and higher voltage domains or vice-versa, ensuring communication across different voltage islands in a multi-voltage SOC. This is essential to avoid data corruption in mixed-voltage environments and maintain signal integrity [7]. When a voltage island operates in the subthreshold region, dedicated SLS are utilized to maintain signal integrity and facilitate seamless voltage transitions.

### A. Subthreshold Level Shifter Architectures

This work implements and evaluates six different SLS architectures using the proposed sustainable benchmark paradigm. These architectures are designed to shift voltage from sub-threshold VDDL (0.3V) to nominal VDDH (1.2V) (as shown in Fig. 1) and are simulated at an operating frequency of 1 MHz with an external load of 100 fF in 65nm technology. Fig. 2 illustrates conventional SLS, while Fig. 3 depicts advanced SLS. The SLS architectures are detailed below.

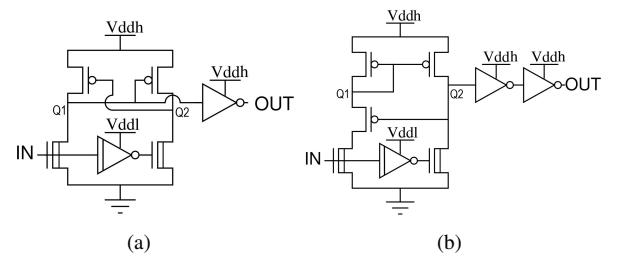


Fig. 2. (a) Cross-coupled Level Shifter (CCLS) [11] (b) Wilson Current Mirror Level Shifter (WCMLS) [11]. CCLS and WCMLS are conventional Level shifters that are implemented in this work.

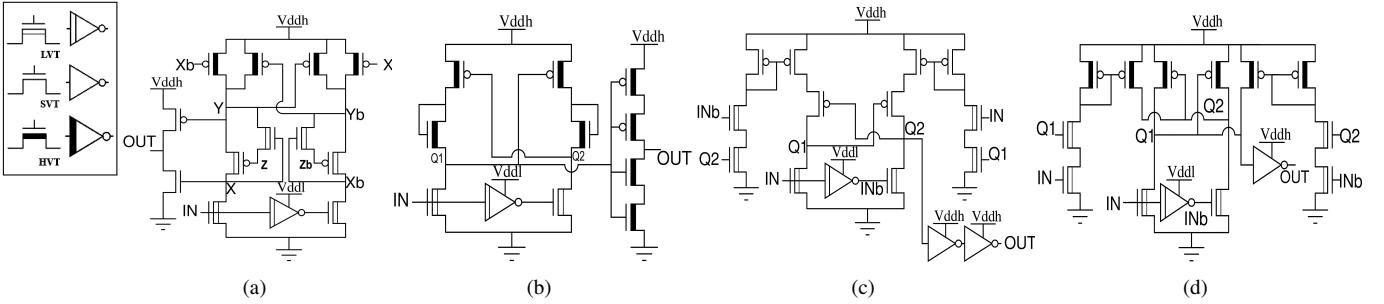


Fig. 3. (a) Deep Sub-threshold Energy Efficient Level Shifter (DSELS) [12] (b) Robust Subthreshold Level Shifter with Wide Conversion Range (RSWCRLS) [13] (c) Low-Power Subthreshold to Above-Threshold Voltage Level Shifter (LPSVTLS) [14] (d) Ultra-Wide-Range Energy-Efficient Level Shifter with CCLS/CMOS Hybrid Structure (C3MLS) [11]. DSELS, RSWCRLS, LPSVTLS, and C3MLS are advanced SLS that are implemented in this work.

**1) Cross-coupled Level Shifter (CCLS) [11]:** CCLS also known as Differential Cascode Voltage Switch, incorporates cross-coupled pull-up (PU) PMOS transistors pair to form a feedback mechanism for driving the output nodes to stable signal levels (as shown in Fig. 2(a)). To overcome the feedback effect for modifying the content on the output nodes, the pull-down (PD) NMOS needs to be sufficiently strong. Enhancing NMOS drive strength through larger device sizing or LVT variants increases area usage or requires additional fabrication steps, both contributing to a higher embodied footprint.

The feedback network minimizes leakage by stabilizing the output nodes at stable logic levels, ensuring low static power dissipation. However, it demands a high contention current, leading to increased dynamic power consumption.

**2) Wilson Current Mirror Level Shifter (WCMLS) [11]:** Current Mirror Level Shifter (CMLS) uses a current mirror mechanism to replicate a stable reference current across its branches, ensuring uniform current flow between varying voltage domains. This approach enables reliable voltage translation while preserving signal integrity across SLS transistors.

Unlike CCLS, CMLS does not have a cross-coupled feedback network, preventing transitional conflicts between PD and PU MOS. Thus, there is no need for an oversized NMOS here like in CCLS. This reduces contention, leading to lower power consumption. However, here, standby power remains high due to continuous static current flow through one of the circuit branches, determined by the input voltage level. A current-limiting MOS can be introduced in the reference branch at the Q1 node to improve current stability, thus forming Wilson Current Mirror Level Shifter (WCMLS), as shown in Fig. 2(b).

**3) Deep Sub-threshold Energy Efficient Level Shifter (DSELS) [12]:** This architecture builds on the CCLS feedback principle but incorporates a self-adaptive pull-up network to improve the speed of switching. It employs a multi-VT transistor strategy to enhance level-shifting efficiency while minimizing area, as illustrated in Fig. 3(a). A unique feature of this architecture is that it uses a PMOS-NMOS cross-coupled (PNCC) current limiter, which significantly limits the current contention and leakage by developing a feedback loop. For proper operation, the PNCC PMOS must operate in the subthreshold region ( $V_{GS_p} < V_{T_p}$ ) to regulate sufficient current flow, enabling the activation of the PNCC NMOS,

which subsequently transfers ' $VDDH - V_{T_n}$ ' to its source terminal i.e. at node Z or Zb.

In this architecture, precise transistor sizing is crucial as it directly impacts the threshold voltage (VT), which subsequently determines the input voltage of the PMCC PMOS gate, expressed as ' $VDDH - V_{T_n}$ ' supplied from the PNCC NMOS source i.e. at node Z or Zb. Furthermore, here, the output stage is designed with an inverter controlled by two separate inputs (split-input buffer), thus providing controlled leakage and energy efficiency. DSELS occupies less area and has very low dynamic and static power consumption. However, this design faces signal integrity issues due to floating nodes Z and Zb, which can affect circuit performance through intra-metal parasitic observed in post-layout extraction and fabrication.

**4) Robust Subthreshold Level Shifter With Wide Conversion Range (RSWCRLS) [13]:** In this design, the CCLS configuration has been modified to reduce current contention by using an NMOS-diode-based current limiter in the pull-up network on both branches, thus enhancing the level-shifting performance and increasing the robustness. Introducing a current limiter in the cross-coupled PU network weakens its pull-up strength by limiting and stabilizing the current.

However, the NMOS-diode-based current limiter introduces a voltage drop at the internal nodes Q1 and Q2, preventing them from achieving full-swing operation. Hence, the output inverter connected to those internal nodes might face a high short-circuit current. To overcome this issue, the internal nodes are connected to a stacked high-threshold voltage (HVT) inverter configuration, as shown in Fig. 3(b).

**5) Low-Power Subthreshold to Above-Threshold Voltage Level Shifter (LPSVTLS) [14]:** This architecture follows the CCLS principle while incorporating Dynamic Current Generators in the PU network to improve the output transition speed. It activates automatically during input voltage level transitions. Enhancing the transition speed reduces the propagation delay.

A key advantage of this architecture is that the dynamic current generators activate only during voltage transitions and remain inactive otherwise, thereby significantly reducing static power dissipation. Additionally, the current generator regulates the strength of the PU network by controlling the branch current, enabling the PD network to effectively modulate the output for reliable level shifting. For this design, maintaining

TABLE I  
POST LAYOUT SIMULATION OBSERVATIONS FOR KEY FIGURE OF MERITS (FOM) OF LEVEL SHIFTER

Design Version <sup>a</sup> [Only M1] - I [M1+M2 GND] - II		Level shifter configuration used <sup>b</sup> (CC/CM)	VT types used <sup>c</sup>		No. of extra masks used <sup>d</sup>	Dynamic Power (nW)	EPT (fJ)	Static Power (nW)	Total Power (nW)	Propagation Delay (ns)	Area ( $\mu\text{m}^2$ )	Cell width (no. of tracks)	% Variations for Delay ( $\sigma/\mu$ )
			NMOS	PMOS									
CCLS [11]	I	CC	LVT	LVT	2	105	210	63.7	169	10.5	19.76	19	11.0% (1.15/10.44)
	II		SVT	SVT		107	214	31.6	139	10.8	17.68	17	10.9% (1.18/10.82)
CMLS [11]	I	CM	LVT	LVT	2	109	218	506	615	15.1	9.36	9	34.7% (6.82/19.64)
	II		SVT	SVT		108	217	493	602	15.3	9.36	9	30.1% (5.42/18.02)
DSELS [12]	I	CC	LVT	LVT	3	8.54	17.1	4.13	12.7	33.7	12.48	12	32.2% (11.96/37.1)
	II		SVT	HVT		7.6	15.2	2.07	9.67	29.9	11.44	11	30.1% (9.83/32.69)
RSWCRLS [13]	I		LVT	LVT		5.16	10.3	11.1	16.3	13.4	10.4	10	16.8% (2.47/14.73)
	II		HVT	HVT		5	10	11.8	16.8	13.3	9.36	9	16.7% (2.42/14.53)
LPSVTLs [14]	I	CC + CM	LVT	LVT	2	26.7	53.4	3.75	30.5	14.7	17.68	17	202.9% (230.3/113.5)
	II		SVT	SVT		28.8	57.6	5.38	34.2	15.1	15.6	15	345.0% (896.4/259.8)
C3MLS [11]	I	CC + CM	LVT	LVT	3	15.1	30.3	10.6	25.7	15.9	13.52	13	28.0% (5.14/18.35)
	II		SVT	HVT		14.8	29.7	12.2	27	15.3	11.44	11	27.7% (4.9/17.66)

<sup>a</sup> “Design Version” represents the different versions of layout implementations for the particular SLS design architecture. More details about ‘Version I’ and ‘Version II’ are given in Fig. 4.

<sup>b</sup> “Level shifter configuration used” represents whether a Cross-coupled (CC) or Current mirror (CM) based configuration is used in the Level shifter architecture, as it affects the power consumption.

<sup>c</sup> STMicroelectronics 65nm technology provides the following VT device variants: High VT (HVT), Standard VT (SVT), and Low VT (LVT).

<sup>d</sup> “No. of extra masks” represents the extra number of optical masks required as compared to a basic design while fabricating the design on a silicon wafer. An extra VT usage requires an additional mask.

a symmetrical layout is critical for preserving signal integrity, although it results in greater area overhead. The schematic for this architecture is illustrated in Fig. 3(c).

6) *Ultra-Wide-Range Energy-Efficient Level Shifter With CCLS/CMLS Hybrid Structure (C3MLS) [11]:* This architecture enables ultra-wide voltage range level shifting by leveraging the strengths of both CCLS and CMLS topologies. It mitigates the limitations of one by incorporating the advantages of the other. While CCLS minimizes static power consumption but experiences high contention, CMLS reduces contention but exhibits higher static power consumption. By incorporating CMLS circuitry alongside CCLS in both branches (as shown in Fig. 3(d)), this design enhances performance while optimizing overall power dissipation.

Similarly to LPSVTLs, this design also incorporates dynamic current generators, thus effectively minimizing static power consumption. A key feature of this architecture is the use of high-threshold voltage (HVT) pull-up devices to limit the strength of the PU network, thus ensuring efficient transitions for updating nodes Q1 & Q2. This approach ensures reliable voltage shifting even with minimal transistor sizing.

### B. Post-Layout Analysis for key Figure of Merits

Section III-A provided an overview of the selected set of SLS. This section presents their simulation results, highlighting post-layout observations for each architecture’s key FOM as summarized in Table I. These observations were taken for level shifting from 0.3V (VDDL) to 1.2V (VDDH) at TT corner and 25 °C. The significance and methodologies for evaluating some of the key SLS FOMs are detailed as follows:

1) *Dynamic Power:* It is consumed during a circuit’s active operation and is influenced by factors such as switching factor ( $\alpha$ ), operating voltage, accumulated charge in switching current peak, and frequency of operation ( $f_{op}$ ). For analysis, a  $\alpha$  of 0.5 and  $f_{op}$  of 1 MHz were used. As level shifters operate

with dual supplies, VDDL and VDDH, power is computed separately for each and then aggregated.

2) *Static Power:* It arises primarily from leakage currents in devices, commonly called leakage power. Here, the average static power consumed by the SLS circuits is computed separately for VDDL & VDDH and then aggregated.

3) *No. of fabrication masks used:* Certain SLS leverage a multi-threshold device approach to enhance performance while maintaining area efficiency. Incorporating this strategy requires additional lithographic steps (masks) beyond the conventional process flow, contributing to a higher CFP.

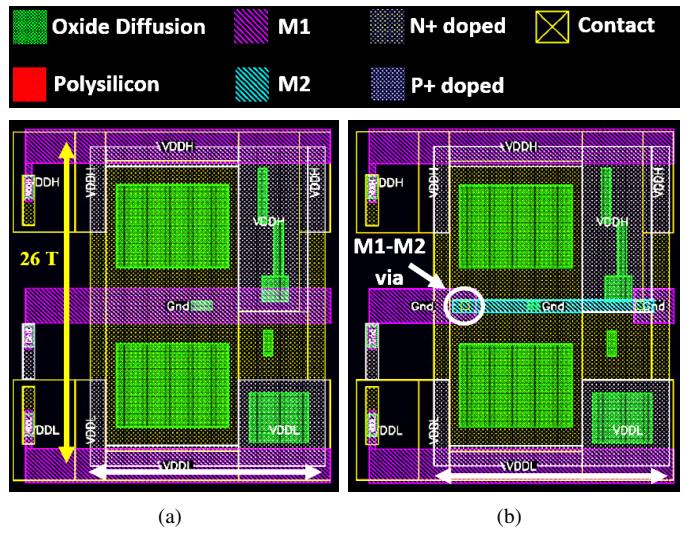


Fig. 4. (a) Version I layout (b) Version II layout. Conventions for SLS Layout implementation using a two-row format, equivalent to twice the height of standard 13-Track (13T) configuration (i.e., 26T). The design incorporates a shared ground (Gnd) supply rail positioned between two power supply rails — VDDH (1.2V) and VDDL (0.3V). Each SLS layout has been implemented in two variations: Version I, where the layout is designed exclusively using the Metal 1 (M1) layer, and Version II, in which the common Gnd supply rail is implemented using Metal 2 (M2), while the remaining interconnections are routed through M1

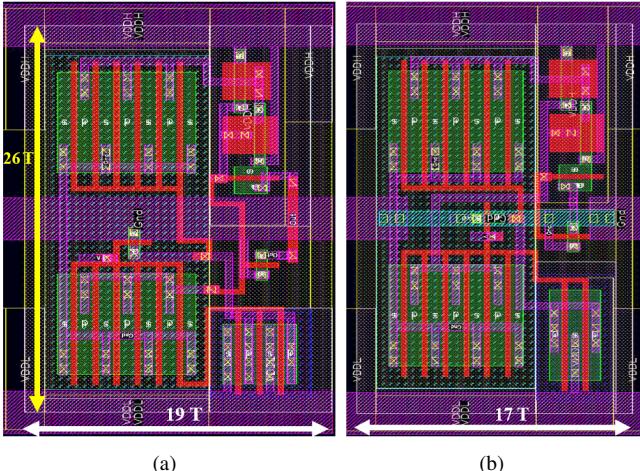


Fig. 5. (a) CCLS Version I (b) CCLS Version II. Layout variations of the CCLS architecture: Version I – Routing confined to M1, requiring 19 vertical tracks (19T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, reducing track usage to 17T.

4)  $\sigma/\mu$  variations for propagation delay: Monte Carlo analysis is essential for assessing fabrication-induced variability in post-layout designs.

5) Area: In this paper, the SLS layouts have been designed in a unique double-row format, equivalent to twice the height of the 13-Track (13T) standard cell configuration (in STM's 65nm library). This approach utilizes a shared ground (Gnd) supply rail between two power supply rails (VDDH and VDDL) that run across the '26T' perimeter boundary to enhance area efficiency. The technique has been implemented in two variations: (a) Version I, where the layout is designed exclusively using the Metal 1 (M1) layer as shown in Fig. 4(a), and (b) Version II, in which the common Gnd supply rail is implemented using Metal 2 (M2), while the

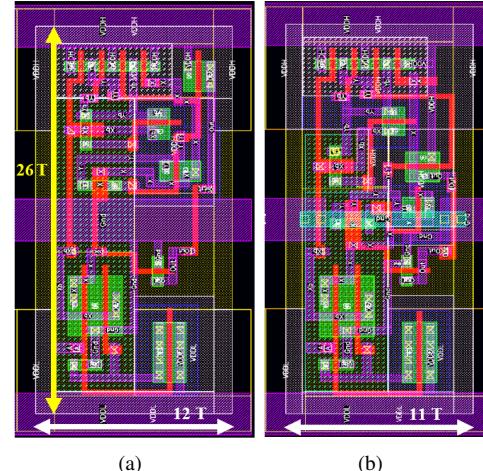


Fig. 7. (a) DSELS Version I (b) DSELS Version II. Layout variations of the DSELS architecture: Version I – Routing confined to M1, requiring 12 vertical tracks (12T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, reducing track usage to 11T.

remaining interconnections are routed through M1 as shown in Fig. 4(b). As illustrated in Fig. 4(b), the M2 Gnd rail is electrically connected to the M1 Gnd supply through M1-M2 vias, ensuring proper conductivity.

The SLS architecture layouts have been designed in different versions to analyze the effect of circuit performance, cell density, parasitics, and congestion on the sustainability evaluation. The designed SLS layouts are discussed below.

a) *CCLS*: CCLS architecture layout uses additional 'VTL\_N' and 'VTL\_P' CAD layers, i.e., two extra masks are required to manufacture it. Its Version I has a 19T cell width, whereas Version II reduces the width to 17T by utilizing an M2 track, as shown in Fig. 5.

b) *CMLS*: CMLS architecture layout uses additional 'VTL\_N' and 'VTL\_P' CAD layers, i.e., two extra masks are required to manufacture it. Its Version I has a 9T cell width, whereas Version II also has a width of 9T even after utilizing an M2 track, as shown in Fig. 6.

c) *DSELS*: DSELS architecture layout uses additional 'VTL\_N', 'VTL\_P', and 'VTH\_P' CAD layers, i.e., three extra masks are required to manufacture it. Its Version I has a 12T cell width, whereas Version II reduces the width to 11T by utilizing an M2 track, as shown in Fig. 7.

d) *RSWCRLS*: RSWCRLS architecture layout uses additional 'VTL\_N', 'VTL\_P', 'VTH\_N', and 'VTH\_P' CAD layers, i.e., four extra masks are required to manufacture it. Its Version I has a 10T cell width, whereas Version II reduces the width to 9T by utilizing an M2 track, as shown in Fig. 8.

e) *LPSVTLS*: LPSVTLS architecture layout uses additional 'VTL\_N' and 'VTL\_P' CAD layers, i.e., two extra masks are required to manufacture it. Its Version I has a 17T cell width, whereas Version II reduces the width to 15T by utilizing an M2 track, as shown in Fig. 9.

f) *C3MLS*: C3MLS architecture layout uses additional 'VTL\_N', 'VTL\_P', and 'VTH\_P' CAD layers, i.e., three

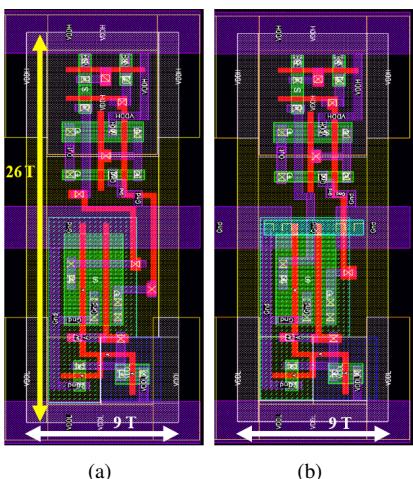


Fig. 6. (a) CMLS Version I (b) CMLS Version II. Layout variations of the CMLS architecture: Version I – Routing confined to M1, requiring 9 vertical tracks (9T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, didn't result in track reduction.

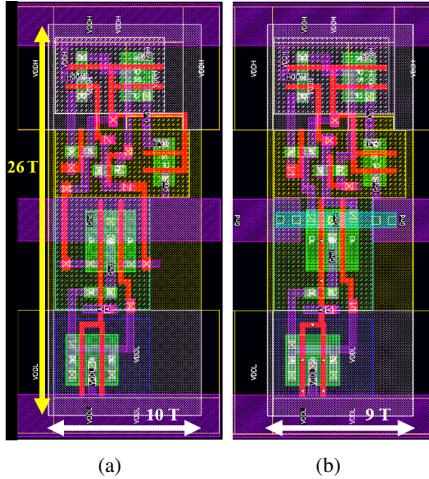


Fig. 8. (a) RSWCRLS Version I (b) RSWCRLS Version II. Layout variations of the RSWCRLS architecture; Version I – Routing confined to M1, requiring 10 vertical tracks (10T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, reducing track usage to 9T.

extra masks are required to manufacture it. Its Version I has a 13T cell width, whereas Version II reduces the width to 11T by utilizing an M2 track, as shown in Fig. 10.

#### IV. SUSTAINABILITY ASSESSMENT IN SLS DESIGNS

This section discusses the proposed approach to evaluate sustainability, enabling designers to assess the long-term efficiency of various SLS architectures early in the design flow. This allows for a well-informed selection of the most sustainable option available for seamless integration into SoC implementations for low-power IoT applications.

##### A. Proposed sustainability evaluation metrics

The proposed set of metrics can help to evaluate a Level shifter's architectural sustainability in terms of embodied and

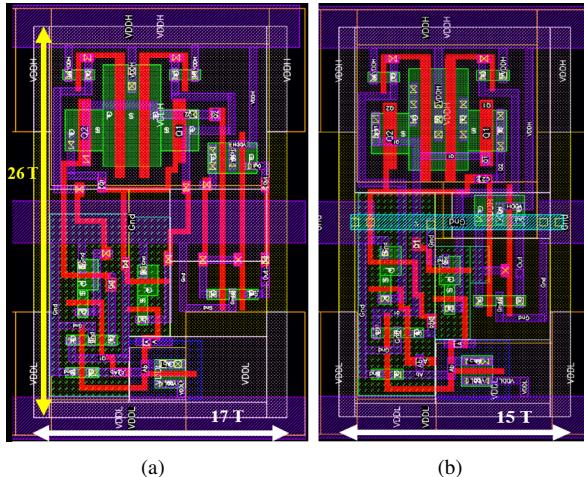


Fig. 9. (a) LPSVTLs Version I (b) LPSVTLs Version II. Layout variations of the LPSVTLs architecture; Version I – Routing confined to M1, requiring 17 vertical tracks (17T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, reducing track usage to 15T.

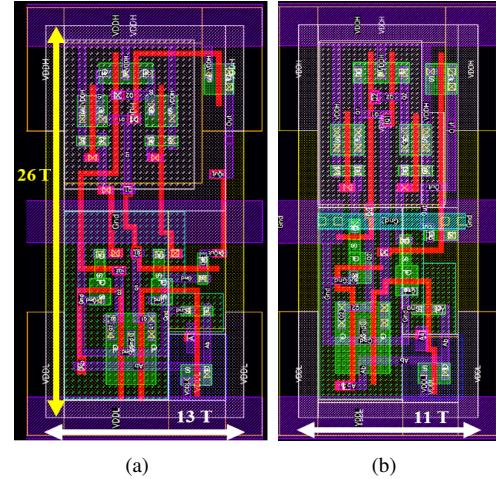


Fig. 10. (a) C3MLS Version I (b) C3MLS Version II. Layout variations of the C3MLS architecture; Version I – Routing confined to M1, requiring 13 vertical tracks (13T), and Version II – Incorporating GND rail in M2 while keeping rest of the routing in M1, reducing track usage to 11T.

operational CFP. The metrics estimate CFP in energy units (mWh), which can be further converted into equivalent CO<sub>2</sub> emissions. The defined metrics are as follows.

*1) Embodied footprint:* The embodied footprint of a VLSI design accounts for the energy consumption and emissions generated during semiconductor manufacturing, encompassing the raw material extraction, transportation, chip fabrication stages, etc. Eq. (1) assesses the environmental impact of SLS manufacturing by estimating the energy consumed during its fabrication, providing a basis for the evaluation.

$$\text{Embodied footprint} = k \times \text{Area} \times \text{Mask\_factor} \times \text{Congestion\_factor} \quad (1)$$

*a) k:* It is a constant that represents the average fabrication energy consumed per  $\mu\text{m}^2$  area in a given technology node. In this analysis, data corresponding to the 65nm technology node has been utilized [15].

*b) Area:* Represents the layout area of the SLS cell under sustainability analysis, measured in  $\mu\text{m}^2$  unit.

*c) Mask\_factor:* As discussed in Section III-B3, the use of additional masks increases energy consumption during the fabrication process and, therefore, impacts sustainability. ‘Mask\_factor’ signifies the percentage impact of an additional mask usage on fabrication energy consumption [15]. Table I outlines the additional mask details for the SLS designs.

*d) Congestion\_factor:* In Level Shifter standard cell layout design, utilizing tracks from upper metal layers (such as M2 in this work) contributes to increased congestion at the system level, hence affecting overall SoC routing efficiency. This added congestion introduces fabrication complexities, leading to higher energy consumption during manufacturing, which, in turn, affects sustainability. To account for this impact, the congestion factor is incorporated into Eq. (1).

2) *Operational footprint metric*: The operational footprint of a VLSI design reflects the total energy consumption and associated emissions throughout its functional life. Eq. (2) captures the operational impact of a SLS by evaluating the energy consumption of the dynamic and leakage components over the intended operating lifetime of an application ( $T_{\text{total}}$ ).

$$\begin{aligned} \text{Operational footprint} &= (\text{Dynamic power} + \text{Leakage power}) \\ &\times T_{\text{total}} \end{aligned} \quad (2)$$

Here, for operational footprint analysis, the operating life of a SLS design is classified into Active, Standby, and Switched-off zones, represented as ratios of the total operating duration ( $T_{\text{total}}$ ). These ratios are given by  $\frac{T_{\text{active}}}{T_{\text{total}}}$ ,  $\frac{T_{\text{standby}}}{T_{\text{total}}}$ , and  $\frac{T_{\text{switchedoff}}}{T_{\text{total}}}$ , respectively. Dynamic power is consumed only during active operation; thus, Eq. (3) accounts for the active ratio of the total operating time. In contrast, leakage power is drawn in both active and standby modes, so Eq. (4) considers the timing ratios for both modes.

$$\text{Dynamic power} = Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f_{\text{op}} \times \frac{T_{\text{active}}}{T_{\text{total}}} \quad (3)$$

$$\begin{aligned} \text{Leakage power} &= \left( I_{\text{active}} \times V_{\text{active}} \times \frac{T_{\text{active}}}{T_{\text{total}}} \right) \\ &+ \left( I_{\text{standby}} \times V_{\text{standby}} \times \frac{T_{\text{standby}}}{T_{\text{total}}} \right) \end{aligned} \quad (4)$$

In Eq. (3) and (4),

a)  $Q_{\text{dyn}}$ : Represents the dynamic charge consumed during the switching operation of the SLS.

b)  $\alpha$ : Represents switching factor based on application.

c)  $V_{\text{active}}$ : Represents active mode operation voltage.

d)  $V_{\text{standby}}$ : Represents standby mode operation voltage.

e)  $f_{\text{op}}$ : Represents frequency of operation.

f)  $I_{\text{active}}$ : Represents the current drawn from the voltage source in the active mode of operation ( $V_{\text{active}}$ ).

g)  $I_{\text{standby}}$ : Represents the current drawn from the voltage source in the standby mode of operation ( $V_{\text{standby}}$ ).

### B. Sustainability Benchmark: Trends and Observations

Section IV-A provided a detailed discussion of the proposed metrics and their significance. Here, these metrics are applied to benchmark the selected SLS designs, evaluating how different design choices impact sustainability. For SLS analysis in IoT applications, here  $\frac{T_{\text{active}}}{T_{\text{total}}}$ ,  $\frac{T_{\text{standby}}}{T_{\text{total}}}$ , and  $\frac{T_{\text{switchedoff}}}{T_{\text{total}}}$  are considered 5%, 25%, and 70% respectively.

1) *Embody footprint*: This section evaluates the framework's adaptability in analyzing the effects of layout area optimization and additional metal utilization on sustainability.

In Industry, Level Shifter standard cell layouts are usually designed using the lowest routing layer available in a technology (here, M1). This can result in increased area consumption. Therefore, utilizing upper routing layers may allow designers to achieve a denser layout. However, this approach can introduce challenges at the SoC level. Utilizing upper metal layers for designing a standard cell layout reduces the available routing resources for cell interconnects within

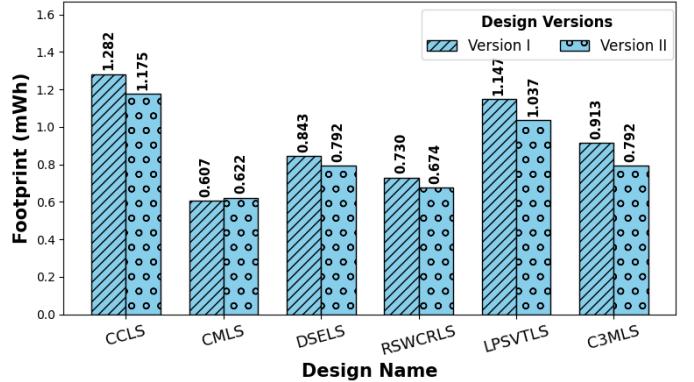


Fig. 11. Embodied footprint for Version I and II of CCLS, CMLS, DSELS, RSWCRLS, LPSVTLs, and C3MLS Subthreshold Level shifters

the SoC, thus leading to increased congestion and fabrication complexity. As a result, the Embodied footprint may increase.

These impacts are validated by analyzing the 'Embodied footprint' metric proposed in Eq. (1) on the selected set of SLS as shown in Fig. 11. The following observations can be derived from Table I and Fig. 11.

- Versions I and II of the conventional CCLS exhibit the highest Embodied footprint among all the SLS designs, as they occupy the largest layout area. Hence, CCLS is the least sustainable choice in terms of manufacturing.
- Versions I and II of the conventional CMLS exhibit the least Embodied footprint among all the SLS designs, as they have the densest layout. Hence, CMLS is the most sustainable choice in terms of manufacturing.
- Versions I and II of the conventional CMLS share the same area. However, due to additional M2 track usage in Version II, congestion increases, raising its Embodied footprint to 0.62 mWh, making it comparatively less sustainable. For all other designs, Version II has a lower Embodied footprint and greater sustainability than Version I, as its decreased area has a more significant impact on the embodied/manufacturing footprint, outweighing the minimal effect of increased congestion from the incorporation of an additional M2 track.
- Versions II of CMLS and RSWCRLS share the same area and congestion impact. However, additional VT mask usage in RSWCRLS results in a higher Embodied footprint compared to CMLS.

2) *Operational footprint*: This section evaluates the framework's adaptability in analyzing the impact of operating performance and lifetime reliability on sustainability. As discussed in Section IV-A2, the Operational footprint of an SLS design depends on its dynamic and leakage characteristics. The dynamic power consumption further depends on  $\alpha$  and  $f_{\text{op}}$  of the usage application, and hence depending upon the chosen application, the Operational footprint may vary.

In Fig. 12, the above impact is validated on the SLS architectures by evaluating their Operational footprint for an IOT application with  $\alpha = 0.3$  and  $f_{\text{op}} = 100$  MHz according

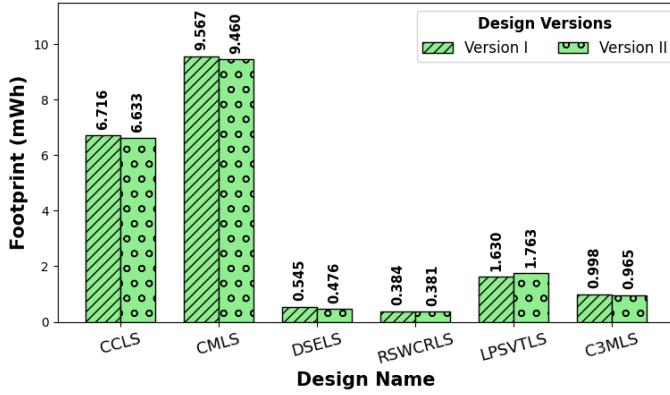


Fig. 12. Operational footprint for Version I and II of CCLS, CMLS, DSELS, RSWCRLS, LPSVTLS, and C3MLS Subthreshold Level shifters

to Eq. (2). Observations from Fig. 12 are as follows.

- Operational footprint of an SLS design can't be judged only on the basis of its layout efficiency, as it might depend upon several other performance parameters. However, it can be estimated using the proposed metric. Notably, Operational Footprint varies by application, meaning a different design may be the most sustainable option depending on specific usage conditions and requirements.
- Versions I and II of the conventional CMLS exhibit the highest Operational footprint among all the SLS designs. Hence, it is the least sustainable choice in this case.
- Versions I and II of RSWCRLS exhibit the least Operational footprint among all the SLS designs. Hence, it is the most sustainable choice in this case.

3) *Total footprint:* In Fig. 11 and Fig. 12, an individual assessment of manufacturing and operational impact was observed. However, this section evaluates the framework's adaptability in analyzing their combined effect on sustainability (as shown in Fig. 13). Following insights can be drawn from it.

- RSWCRLS has the least Total footprint among all SLS designs, making it the most sustainable option overall.

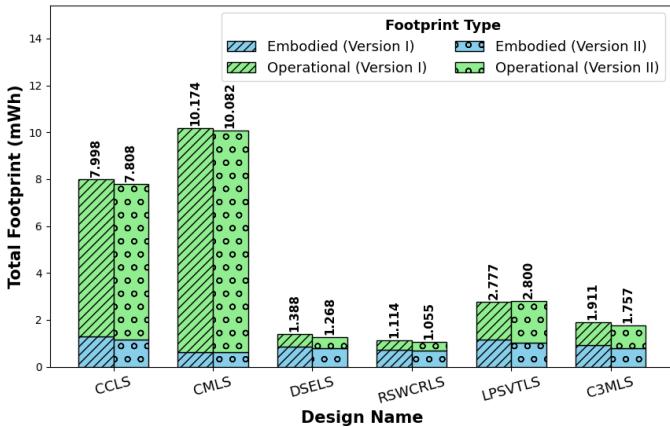


Fig. 13. Total footprint for Version I and II of CCLS, CMLS, DSELS, RSWCRLS, LPSVTLS, and C3MLS Subthreshold Level shifters

- CMLS, which had the least Embodied Footprint, now has the highest Total Footprint.

## CONCLUSION

In modern multi-voltage domain ICs, Level Shifters have become essential for enabling mixed-voltage communication, especially Subthreshold Level Shifters in ultra-low-power applications. While many advanced SLS designs are available, the conventional PPA metric is still used to determine efficiency, even in this ecological era. To address this, we proposed and validated a sustainability evaluation and benchmarking paradigm to identify the most efficient and environmentally friendly SLS architecture. Additionally, a unique double-row layout implementation was presented to examine SLS area efficiency and its impact on sustainability.

## REFERENCES

- [1] M. Yin et al., "Power, performance, and area evaluation across 180nm-28nm technology nodes based on benchmark circuits," IEICE Electronics Express, vol. 21, no. 9, pp. 20240194–20240194, Apr. 2024, doi: <https://doi.org/10.1587/elex.21.20240194>.
- [2] A. Hopf, A. Ismail, H. Ehm, D. Schneider and G. Reinhart, "Energy-Efficient Semiconductor Manufacturing: Establishing an Ecological Operating Curve," 2022 Winter Simulation Conference (WSC), Singapore, 2022, pp. 3453–3464, doi: [10.1109/WSC57314.2022.10015333](https://doi.org/10.1109/WSC57314.2022.10015333).
- [3] I. Lee, D. Sylvester and D. Blaauw, "A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1443–1449, May 2017, doi: [10.1109/JSSC.2017.2654326](https://doi.org/10.1109/JSSC.2017.2654326).
- [4] B. H. Calhoun, J. Bolus, S. Khanna, A. D. Jurik, A. C. Weaver and T. N. Blalock, "Sub-threshold operation and cross-hierarchy design for ultra low power wearable sensors," 2009 ISCAS, Taipei, Taiwan, 2009, pp. 1437–1440, doi: [10.1109/ISCAS.2009.5118036](https://doi.org/10.1109/ISCAS.2009.5118036).
- [5] T.-H. Chen, J. Chen, and L. T. Clark, "Subthreshold to Above Threshold Level Shifter Design," Journal of Low Power Electronics, vol. 2, no. 2, pp. 251–258, Aug. 2006, doi: <https://doi.org/10.1166/jolpe.2006.071>.
- [6] Abdellatif Bellouaour and M. Elmasy, Low-Power Digital VLSI Design. Springer Science & Business Media, 2012.
- [7] Sanjay Churiwala and S. Garg, Principles of VLSI RTL Design. Springer Nature, 2011. doi: <https://doi.org/10.1007/978-1-4419-9296-3>.
- [8] B. Razavi, Design of Analog CMOS : Integrated circuits, 2nd ed., 2017.
- [9] "Report of the world commission on environment and development: Our common future," 1987, <https://sustainabledevelopment.un.org/content/documents/5987our-common-future.pdf>, (accessed March 1, 2025).
- [10] U. Gupta et al., "Chasing Carbon: The Elusive Environmental Footprint of Computing," IEEE Micro, vol. 42, no. 4, pp. 1–1, 2022, doi: <https://doi.org/10.1109/MM.2022.3163226>.
- [11] C. Huang and H. Jiao, "C3MLS: An Ultra-Wide-Range Energy-Efficient Level Shifter With CCLS/CMLS Hybrid Structure," in IEEE Journal of Solid-State Circuits, vol. 58, no. 10, pp. 2685–2695, Oct. 2023, doi: [10.1109/JSSC.2023.3266221](https://doi.org/10.1109/JSSC.2023.3266221).
- [12] R. Balaji, R. K. Siddharth, S. Naik, Y. B. N. Kumar, M. H. Vasantha and E. Bonizzoni, "A 11-ns, 3.85-fJ, Deep Sub-threshold, Energy Efficient Level Shifter in 65-nm CMOS," 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1–5, doi: [10.1109/ISCAS46773.2023.10181677](https://doi.org/10.1109/ISCAS46773.2023.10181677).
- [13] W. Zhao, A. B. Alvarez and Y. Ha, "A 65-nm 25.1-ns 30.7-fJ Robust Subthreshold Level Shifter With Wide Conversion Range," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 7, pp. 671–675, July 2015, doi: [10.1109/TCSII.2015.2406354](https://doi.org/10.1109/TCSII.2015.2406354).
- [14] S. R. Hosseini, M. Saberi and R. Lotfi, "A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 10, pp. 753–757, Oct. 2014, doi: [10.1109/TCSII.2014.2345295](https://doi.org/10.1109/TCSII.2014.2345295).
- [15] D. Kline et al., "Sustainable IC design and fabrication," 2017 Eighth International Green and Sustainable Computing Conference (IGSC), Orlando, FL, USA, 2017, pp. 1–8, doi: [10.1109/IGCC.2017.8323572](https://doi.org/10.1109/IGCC.2017.8323572).