Advance Digital Droop Detector Circuit

Submitted by

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Certificate

This is to certify that the capstone titled “Advance Digital Droop Detector Circuit” submitted by Shivani Mishra and Debangshu Mahanayak for the partial fulfilment of the requirements for the degree of Master of Technology in VLSI & Embedded Systems is a record of the bonafide work carried out by them under my guidance and supervision in the VLSI Circuits & System Lab group at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree.

Dr. Anuj Grover

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Abstract

Voltage droop, a transient reduction in supply voltage, poses a significant challenge in high-speed digital circuits, potentially leading to performance degradation and timing violations. Detecting and profiling droops is critical for maintaining system reliability. While analog methods like SAR ADCs provide precision, they often suffer from higher complexity and slower response times. This project focuses on a digital approach using thermometer code generation, which is faster, scalable, and seamlessly integrates into digital workflows.

The system utilizes an inverter-based delay line to introduce controlled delays that vary with supply voltage droop. A series of transmission gate-based D flip-flops is placed at each delay stage, clocked by the system clock and its complement. As voltage droop increases, the propagation delay through the inverter chain grows, causing the flip-flops to sequentially latch either '1' or '0', thereby generating a thermometer code. This code transitions from (111…11) to (110…00), providing a direct digital representation of the droop magnitude. The digital methodology ensures fast and accurate droop detection with high resolution, leveraging the simplicity and speed of digital circuits while overcoming the latency and complexity of analog solutions.

CHAPTER-1

INTRODUCTION

1.1 Introduction

The supply voltage (Vdd) level in systems-on-a-chip (SoCs) is a critical determinant of power consumption and performance. Ensuring voltage stability is crucial as supply-voltage fluctuations, or voltage droop, can degrade performance and potentially lead to malfunctions. These fluctuations, caused by parasitic inductance and resistivity within the power delivery network (PDN), are exacerbated by rapid changes in current consumption due to dynamic processor activities, such as switching and architectural power-saving events. The phenomenon, commonly referred to as the voltage droop. Decoupling capacitors, placed across the PDN on the board, package, and die, aim to stabilize Vdd however, these capacitors may introduce resonant frequencies, leading to Vdd droops during current surges. Power-gated PDNs, which utilize switchable sleep transistors for localized power management, face unique challenges such as switching noise from logic cell activity and rush current noise during wake-up phases.

Designing efficient PDNs involves balancing power efficiency with power integrity. Traditional strategies focus on minimizing supply noise while maintaining performance, while modern approaches emphasize advanced PDN architectures tailored for multi-core chips and SoCs. These architectures integrate global and local grids with decoupling capacitors to address the dual objectives of voltage stability and leakage power reduction, stabilizing supply voltage in SoCs is an intricate challenge driven by dynamic resource utilization, scaling trends, and power gating designs. Addressing this issue is critical for enhancing the performance and energy efficiency of high-performance processors.

1.2 Power Delivery Network (PDN) and Voltage Droop

A Power Delivery Network (PDN) is essential in VLSI designs, responsible for distributing stable power supply and returning electrical current across all components in a system. It comprises on-chip power grids, off-chip packages, voltage regulator modules (VRMs), and decoupling capacitors. PDNs are often structured as pseudo-distributed RLC networks, where parasitic resistances, inductances, and capacitances significantly influence stability. High-frequency

switching activities and dynamic workloads introduce challenges such as voltage droops, impedance peaks, and jitter, which degrade signal integrity and can cause timing errors. Decoupling capacitors are hierarchically placed to stabilize voltage levels, reduce impedance, and mitigate transient spikes, ensuring stable power delivery. Advanced optimization techniques, including model order reduction (MOR) and simulated annealing, are employed to improve capacitor placement and minimize power supply noise. As transistor sizes shrink and clock frequencies rise, PDNs must balance robustness, efficiency, and cost to maintain power integrity and meet the demands of modern VLSI systems.

1.3 Droop Profiles and Mitigation

Voltage droop refers to a temporary reduction in supply voltage, often occurring due to sudden changes in current demand in high-performance digital circuits like processors. The behaviour of voltage droop can be classified into 1st-order, 2nd-order, and 3rd-order effects, each with unique characteristics and requiring specific mitigation strategies.

1st-order voltage droop represents the immediate voltage drop caused by IR losses in the power delivery network (PDN) due to rapid current increases. This droop occurs on a nanosecond timescale and is typically mitigated using decoupling capacitors (decaps), which provide local charge reservoirs to counter sudden demand. Additionally, on-chip voltage regulators can quickly respond to load variations to stabilize the supply. In contrast, 2nd-order droop arises from the LC resonance of the PDN, leading to a slower oscillatory response that occurs on the microsecond scale. This is often managed through active charge injection from switched capacitors or dynamic voltage scaling (DVS), which gradually adjusts the supply voltage based on workload demands.

3rd-order voltage droop occurs over longer timescales, typically in milliseconds, and is caused by sustained high current loads or thermal effects, which can strain the regulator or power grid. To address this, techniques like CPU throttling reduce power consumption by lowering clock frequency or disabling cores temporarily. Dual Mode Logic (DML) offers an alternative by dynamically switching between low-power and high-performance operating modes based on workload requirements.

Additional mitigation strategies include hierarchical decap placement to provide localized charge supply across the chip, adaptive clocking to synchronize with droop conditions, and resonance dampers to reduce LC oscillation effects. At the architectural level, asynchronous logic design can minimize timing violations caused by droop by reducing dependency on synchronous clocking. By understanding the nature and impact of different orders of voltage droop, targeted solutions can ensure reliable and efficient operation in power-intensive circuits.

1.4 Problem Statement

Voltage droop is a critical challenge in modern integrated circuits (ICs), arising from rapid changes in current demand during high-frequency switching or load variations in the power delivery network (PDN). These fluctuations cause transient voltage drops due to the parasitic inductance, resistance, and capacitance inherent in the PDN, which can lead to timing violations, degraded signal integrity, and even circuit malfunction. As transistor scaling continues and operating frequencies increase, the susceptibility to voltage droops becomes more pronounced, exacerbating the problem in advanced systems such as high-performance processors, GPUs, and SoCs. Additionally, power-saving techniques like dynamic clocking and power gating, while efficient, further contribute to abrupt current surges, intensifying droop-related issues. The need for robust droop detection and mitigation mechanisms is critical to ensure stable and reliable operation, particularly in systems with stringent performance and power efficiency requirements. Addressing this issue is essential to avoid performance degradation, maintain timing margins, and ensure the overall reliability of modern electronic systems.

CHAPTER-2

LITERATURE REVIEW

In the literature review section of our report, we will examine existing research and scholarly articles related to our topic. This involves reviewing a variety of sources, such as research papers and conference proceedings, to understand the current state of knowledge, identify gaps, and establish how our project contributes to the broader field. By analysing prior work, we aim to build on existing insights, highlight the significance of our study, and demonstrate its unique contribution. This process serves as a guide, helping us navigate the foundation laid by previous researchers before embarking on our own journey.

2.1 PDN and Its Design Challenges-

A Power Delivery Network (PDN) encompasses all the devices and interconnects that distribute power supply and return electrical current across an electronic system's board. The increasing clock frequencies and transistor scaling in integrated circuits (ICs) pose significant challenges for designing robust PDNs. The primary goal is to ensure stable power delivery while effectively managing power supply noise to keep it within acceptable thresholds. Rapid load changes, transient spikes, and high current demands can result in significant power supply noise, such as impedance peaks, voltage droops, and jitter—commonly measured as a timing uncertainty metric. These issues can ultimately lead to the malfunction of integrated circuits if not properly addressed.

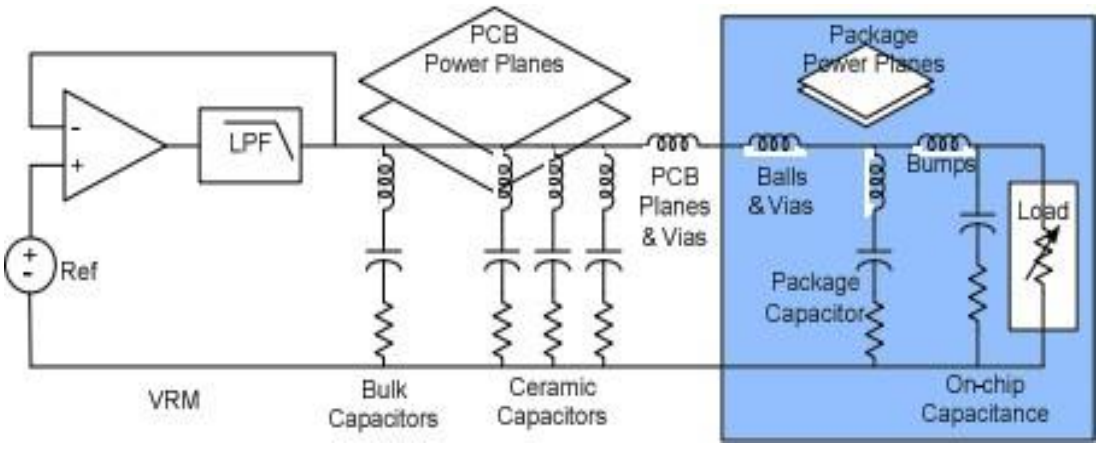

Fig 2.1.1: Proposed Voltage Biasing circuit for 3-stage Current Starved Ring Oscillator

2.2 PDN Impedance Profile (Frequency Response)-

The impedance profile serves as a critical system-level metric to evaluate the quality and performance of a Power Delivery Network (PDN). Ideally, the impedance profile should be as low and flat as possible across all operating frequencies to ensure minimal voltage noise and stable power delivery. However, parasitic elements inherent in the die and package often lead to significant resonances at high frequencies, causing peaks in the impedance profile. These peaks can exacerbate power supply noise and compromise signal integrity, particularly during high-frequency switching activities. By analyzing the impedance profile, engineers can identify potentially problematic frequency ranges and take proactive measures, such as optimizing decoupling capacitor placement or modifying PDN design, to mitigate noise and enhance overall system reliability and efficiency.

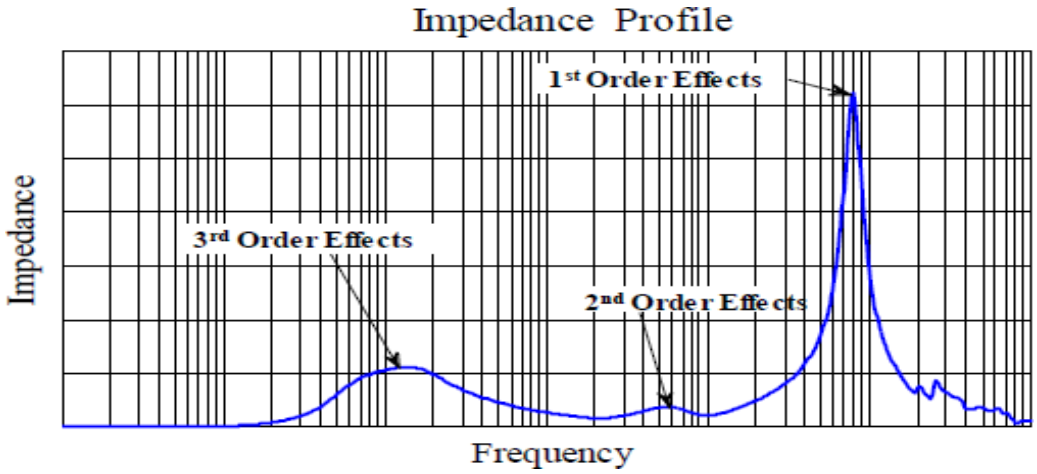

Fig 2.2: Impedance Profile

2.3 PDN Voltage Droops (Time Responses)

Voltage droop is a critical phenomenon in Power Delivery Networks (PDNs), driven by various factors at different stages. The first-order voltage droop is primarily influenced by on-die capacitance, resistive parasitic, and package connections, directly impacting the chip's performance. Frequency-domain effects appear as voltage droops in the time domain, which can lead to operational errors or system failures. The second-order droop is predominantly dictated by package capacitance and occasionally by connector pins, while the third-order droop arises from voltage regulator capacitance and nearby bulk capacitance. As the magnitude and duration of voltage droop events increase, the system's ability to tolerate them diminishes, jeopardizing signal integrity. This underscores the importance of implementing.

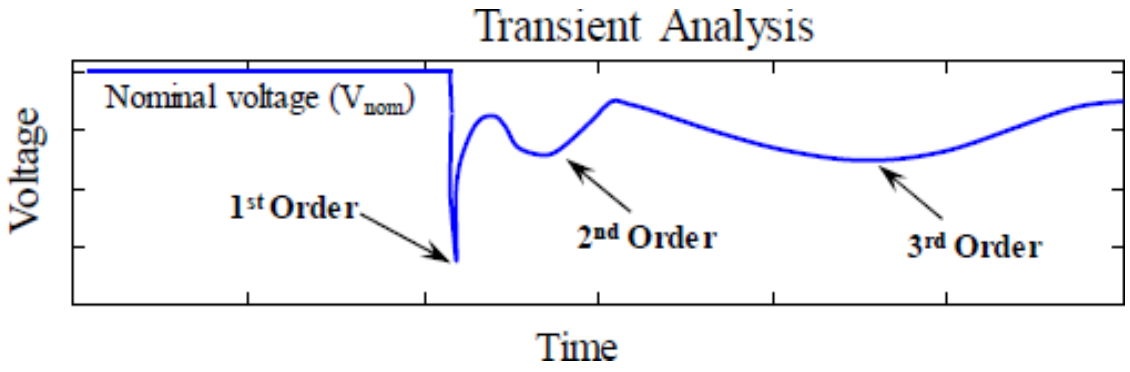

Fig 2.3: Result of the Voltage droop

2.4 Droop Effects and how often it happens in Advanced SoC Design

Advanced CPUs, GPUs, and other IPs in modern SoCs face growing complexity to deliver high single-thread performance while maintaining power efficiency, particularly in high-end mobile, infrastructure, and automotive computing systems. This increasing complexity results in higher maximum current draw, leading to significant transient current fluctuations. These fluctuations, often triggered by abrupt activity changes or load variations at the PDN impedance resonance frequency, cause voltage droops at transistor junctions. Addressing these droops during sign-off timing closure is critical to prevent brown-out events during transient operations. To analyze voltage droops, three fundamental current sources—impulse, step, and sinusoidal—are examined, with the maximum droop observed under sinusoidal current pulses. The frequency of these events depends on factors such as the specific device in use, its activity level, and the operating clock frequency, emphasizing the need for careful PDN design and analysis.

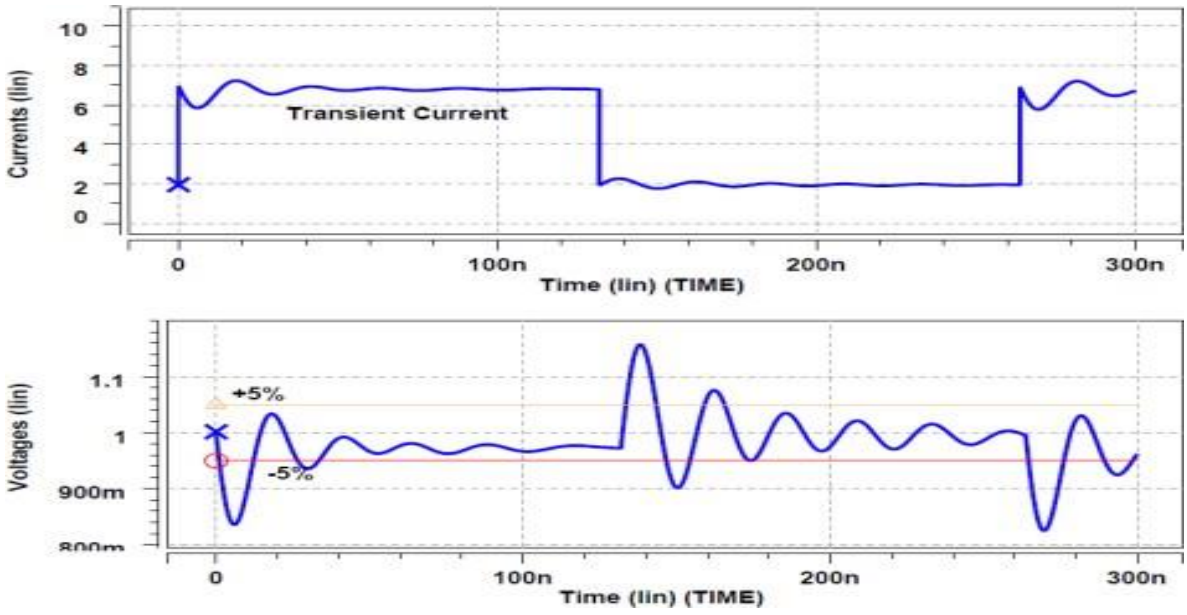

Fig 2.4: The on-chip voltage has dips and peaks associated with the current transients and rings out in a damped sinusoid at the PDN resonant frequency.

2.5 Voltage Droop Profiling

Voltage variation analysis in integrated circuits (ICs) or power distribution networks is essential to ensure reliable and efficient performance, particularly in high-performance computing applications. Current consumption in SPEC benchmarks, such as earthquake, apsi, bzip, and mcf, is classified into step, pulse, and resonating current profiles. Step and pulse currents are major contributors to voltage fluctuations and timing violations, with the worst-case scenarios occurring during simultaneous core power-on events. Implementing staggered core power-on intervals effectively mitigates these fluctuations, stabilizing voltage levels. However, resonating currents at the system's resonant frequencies can induce severe voltage swings, emphasizing the importance of comprehensive voltage analysis to optimize PDN design and maintain system integrity.

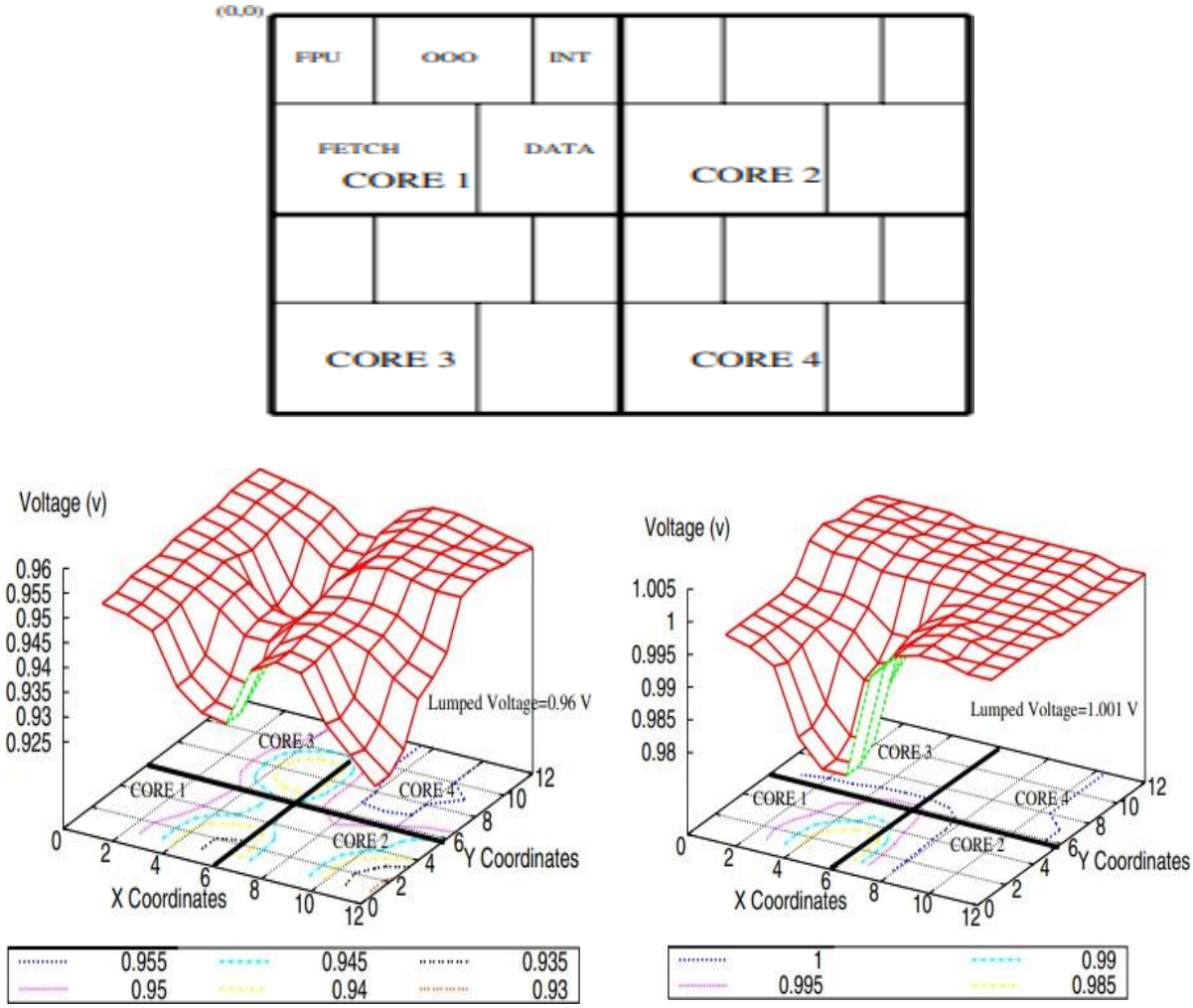

Fig 2.5.1 A four-core chip floorplan, Core 1 running bzip, Voltage variation across the chip for a snapshot of bzip

To analyze the use of a distributed power-delivery network in chip multiprocessor (CMP) architectures, we begin by examining the current consumption profiles of various workloads based on a set of SPEC benchmarks. Figure 5 illustrates the current profiles for four SPEC benchmarks—equake, apsi, bzip, and mcf—on a single core. From the observed characteristics, we classify current consumption profiles into three main categories.

The first category, Step Currents, occurs when a core suddenly changes its state, such as a sudden increase or decrease in activity after long periods of inactivity due to events like cache misses or branch mispredictions. Step currents can also arise when the firmware switches cores between sleep and active states. The second category, Pulse Currents, refers to brief and sudden changes in core activity, typically caused by short stalls or transient events. Figures 2.52(a) and 2.5.2(b) show examples of these short-duration pulses with varying widths. The third category, Resonating Currents, involves periodic current variations, often due to recurring loops in an application. These currents are particularly problematic when they occur near the resonant frequency of the power-delivery network, as seen in Figures 2.5.2(c) and 2.5.2(d) for the bzip and mcf benchmarks, respectively.

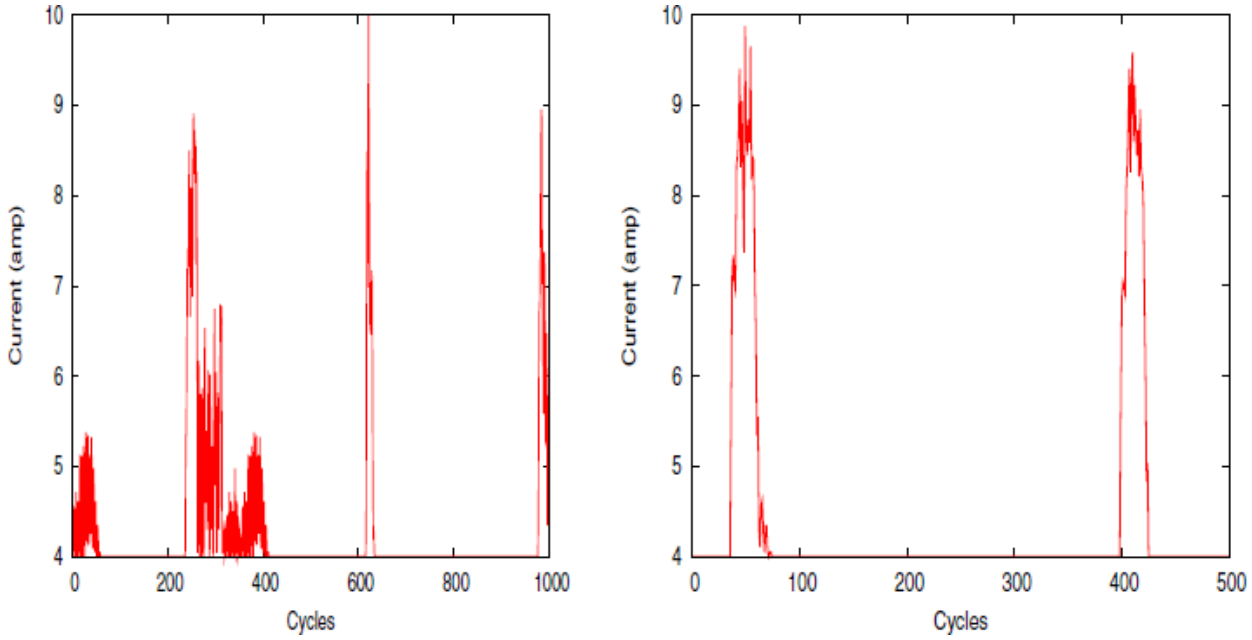

Fig: 2.5.2(a,b): Droop Nature for Pulse Input (equake, apsi)

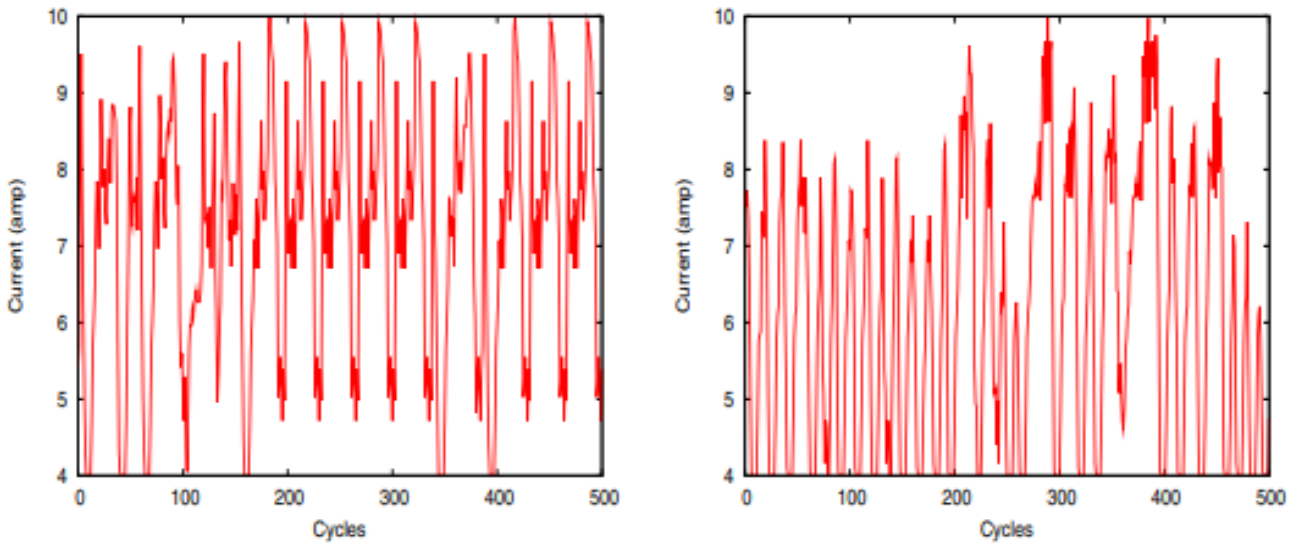

Fig 2.5.2(b,C): Snapshot of current consumption for equake, apsi, bzip and mcf for a single core

2.6 Voltage Droop Detector

The droop detector identifies voltage droops by monitoring propagation delay changes in the SDMDL (Synchronous Delay Monitor Delay Line) and asserts a FLAG signal when a droop is detected. Upon detection, the SDMDL reconfigures as a Digitally Controlled Oscillator (DCO) operating at a reduced frequency, temporarily serving as the system clock (CLKOUT) to prevent timing violations. The DCO frequency gradually increases to align with the input clock (CLKIN) frequency, avoiding abrupt current surges. Once aligned, the GFRC smoothly switches CLKOUT back to CLKIN without glitches or supply voltage overshoot.

Droop detection techniques fall into two categories: digital and analog. Digital detectors translate voltage droops into delay variations of logic gates, using methods like delay lines sensitive to AC Vdd levels or ring oscillators that modulate output frequency based on Vdd droops. These fully digital solutions are simpler and provide high-resolution supply level indications but require extensive calibration across DC Vdd levels, temperature, and aging due to sensitivity to these parameters, limiting their real-time accuracy. Analog detectors, in contrast, use comparators to identify droops by detecting Vdd crossing predefined thresholds. They require fewer calibration points but depend on precision reference voltages, offering robust detection under varying conditions. Both approaches highlight the importance of accurate droop detection to ensure reliable system operation.

2.6.1 Digital Droop Detector-

Digital droop detectors are designed to translate voltage droops into delay variations in logic gates, offering a fully digital and high-resolution approach to supply level monitoring. These detectors often utilize delay lines, where delays depend on the AC Vdd level, or ring oscillators, which modulate Vdd droops into output frequency changes. While simpler to design and implement, these systems are highly sensitive to DC Vdd levels, temperature, and aging, requiring extensive 3-D calibration and backend characterization. The proposed design addresses these challenges with a shared dual-mode delay line (SDMDL) consisting of 100 delay cells. The SDMDL functions as both a TDC-based droop detector and a DCO-based droop mitigator. It detects droops by observing propagation delays and asserting a FLAG signal when thresholds are breached. Upon detection, the SDMDL reconfigures as a DCO operating at a slower frequency, temporarily serving as the system clock (CLKOUT) to prevent timing violations. The DCO frequency is gradually increased to match the input clock (CLKIN), avoiding abrupt current surges, and the source of CLKOUT is seamlessly switched back to CLKIN via GFRC without glitches or overshoot. The detector supports external tuning of the droop detection threshold (DRth) to compensate for process variations, ensuring robust droop detection and mitigation in digital systems.

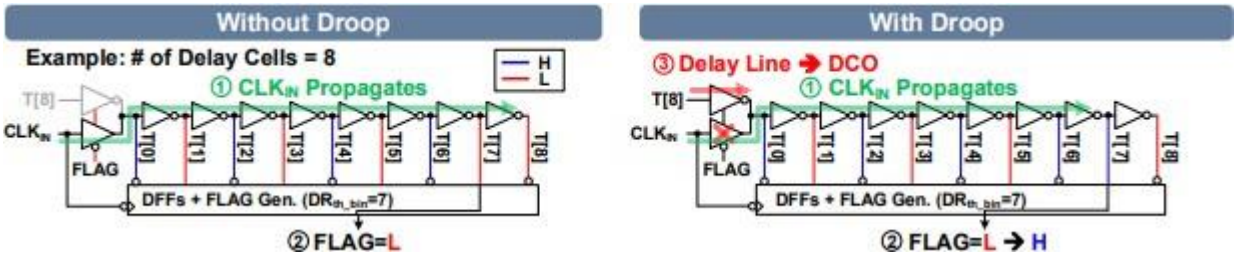

Fig- 2.6 Digital droop detection scheme.

2.6.2 Analog Droop Detector-

The proposed droop detector features a supply filter, offset comparators, and a clock phase generator to monitor voltage droops effectively. The supply filter generates a stable reference voltage (QDVdd) using a low-pass RC filter and a unity-gain buffer to suppress noise and drive the offset comparators. The offset comparators employ a novel inverter-based architecture with auto-zeroing for high accuracy and minimal dependency on process, voltage, and temperature (PVT) variations. They measure droop size by comparing the noisy voltage (NDVdd) with QDVdd and output a 3-bit thermometer code to indicate droop severity. The clock phase generator creates overlapping clock phases for seamless integration and evaluation transitions, preventing dead zones or capacitor discharge. The detector operates on a quiet analog Vdd and supports configurable thresholds for system-specific requirements, making it efficient and robust for voltage

droop detection and mitigation

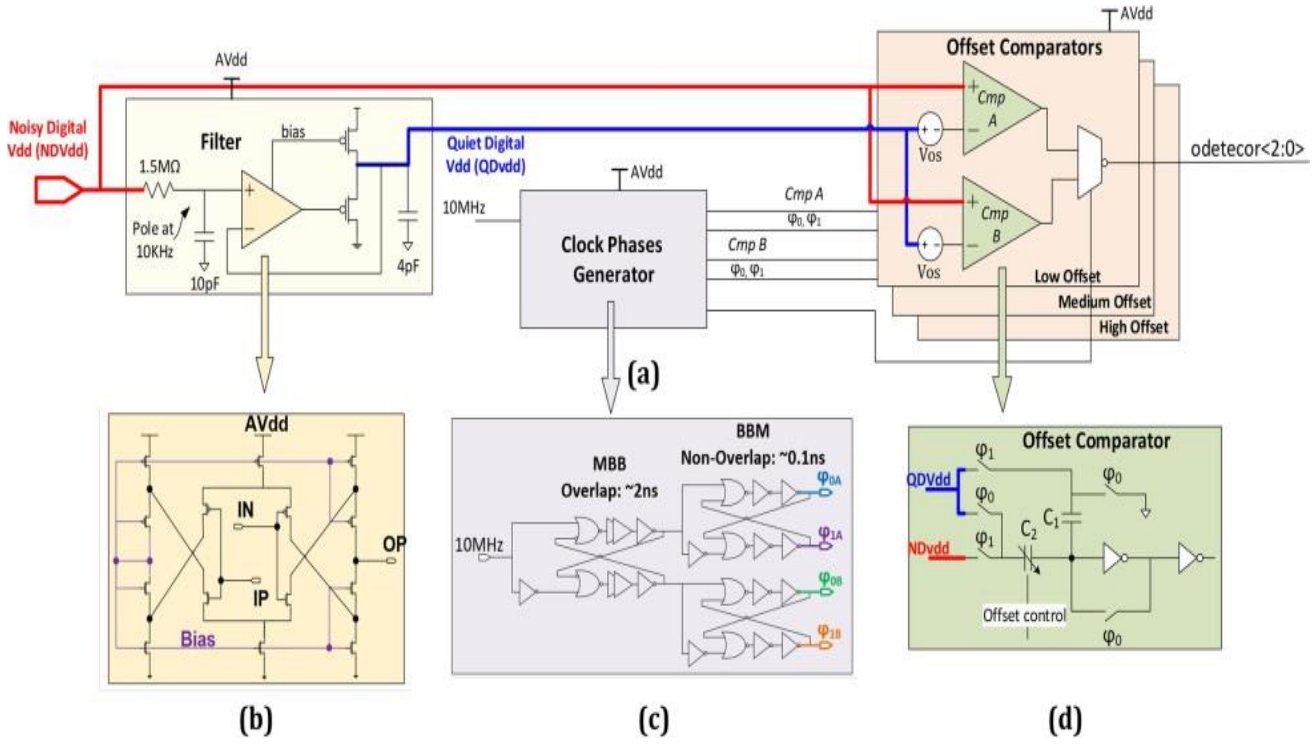

Fig 2.6.1 (a) Block diagram of the droop detector top-level, comprising a parallel three droop levels detector, a filter, and a phase generator. (b) Transistor-level diagram of the VCDA instantiated in the filter. (c) Diagram of the clock phase generator, consisting of one MBB circuit and two BBM circuits. (d) Schematic of the detector's offset comparator.

2.7 Voltage Droop Mitigation Techniques-

Droop mitigation techniques encompass a wide range of methods aimed at stabilizing supply voltage and preventing performance degradation in electronic systems. Decoupling capacitors (decaps) are commonly used to locally supply charge during transient events, reducing voltage fluctuations. Low-Dropout Regulators (LDOs) provide stable power delivery with precise voltage control but may struggle with high-frequency noise. Guard bands involve over-provisioning voltage to ensure safe operation, though this reduces power efficiency. Dual-mode delay lines (DMDLs)**,** such as those in droop detectors, temporarily adjust clock frequencies to avoid timing violations during droop events. Charge injection methods rapidly supply current to the load, effectively countering transient voltage drops. Critical Path Monitors (CPMs) dynamically adjust performance to account for voltage changes, ensuring reliability. Other techniques, like adaptive voltage scaling and on-chip voltage regulators, complement these approaches, providing robust and efficient droop mitigation tailored to system requirements.

2.7.1 LDOs

Low-Dropout Regulators (LDOs) are widely used in integrated circuits (ICs) as efficient voltage regulation solutions to mitigate droops and maintain power stability. By providing a steady output voltage with minimal dropout from the input supply, LDOs ensure reliable operation even under fluctuating load conditions. They operate by adjusting a pass transistor based on feedback from the output voltage, dynamically compensating for variations caused by transient currents or noise in the power delivery network (PDN). Research highlights their effectiveness in applications requiring low noise and fast transient response, making them essential for sensitive analog and digital circuits. Advanced designs incorporate techniques such as adaptive biasing and feedforward ripple cancellation to enhance their droop mitigation capabilities, especially in high-frequency domains. LDOs are particularly advantageous in systems with tight power and noise constraints, such as mobile SoCs and high-performance processors, where they provide localized voltage regulation and complement other droop mitigation methods like decoupling capacitors and charge injection circuits. Their compact design, ease of integration, and ability to stabilize voltage at the point of load make LDOs a crucial component in modern ICs.

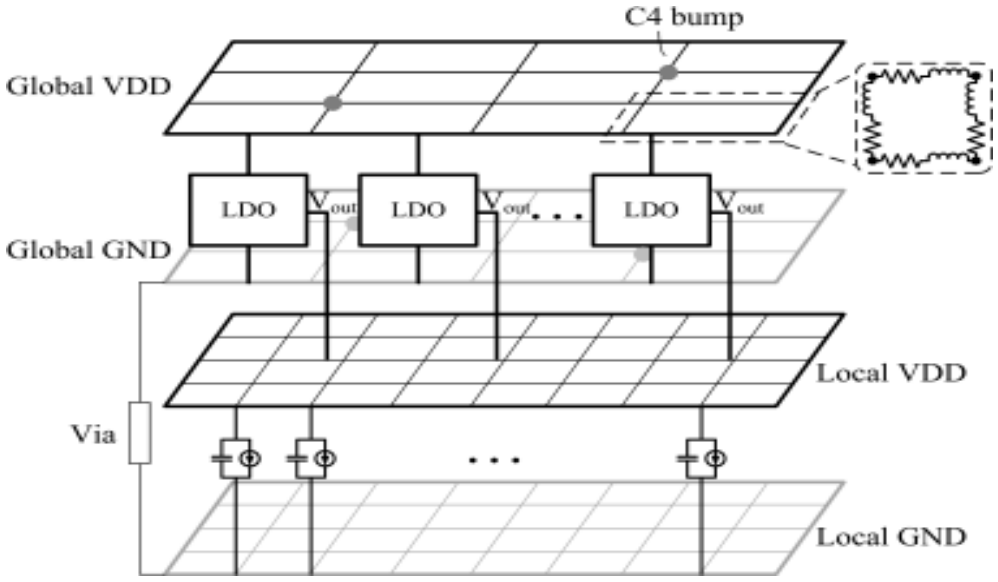

Fig 2.7.1- A detailed on-chip power grid model with LDOs

2.7.2 CPM with CPU Throttling

Critical Path Monitors (CPMs) are a dynamic approach to mitigating voltage droops and ensuring robust performance in integrated circuits (ICs) by continuously monitoring and managing timing margins in real-time. CPMs track delays along the critical paths of a circuit, identifying potential timing violations caused by supply voltage fluctuations, temperature variations, or aging effects. By integrating timing sensors along these paths, CPMs provide precise feedback to adjust operational parameters such as clock frequency, voltage, or gate states dynamically. Research indicates that CPMs can be coupled with adaptive voltage scaling (AVS) or clock gating techniques to optimize power efficiency while maintaining performance. These monitors are particularly effective in high-performance systems, where timing margins are narrow, and supply noise is a significant concern. CPMs not only enhance droop tolerance but also reduce the need for over-provisioning through guard bands, offering a more efficient and scalable solution for modern ICs. Their integration into power delivery networks (PDNs) underscores their importance in addressing real-time challenges in voltage stability and timing integrity.

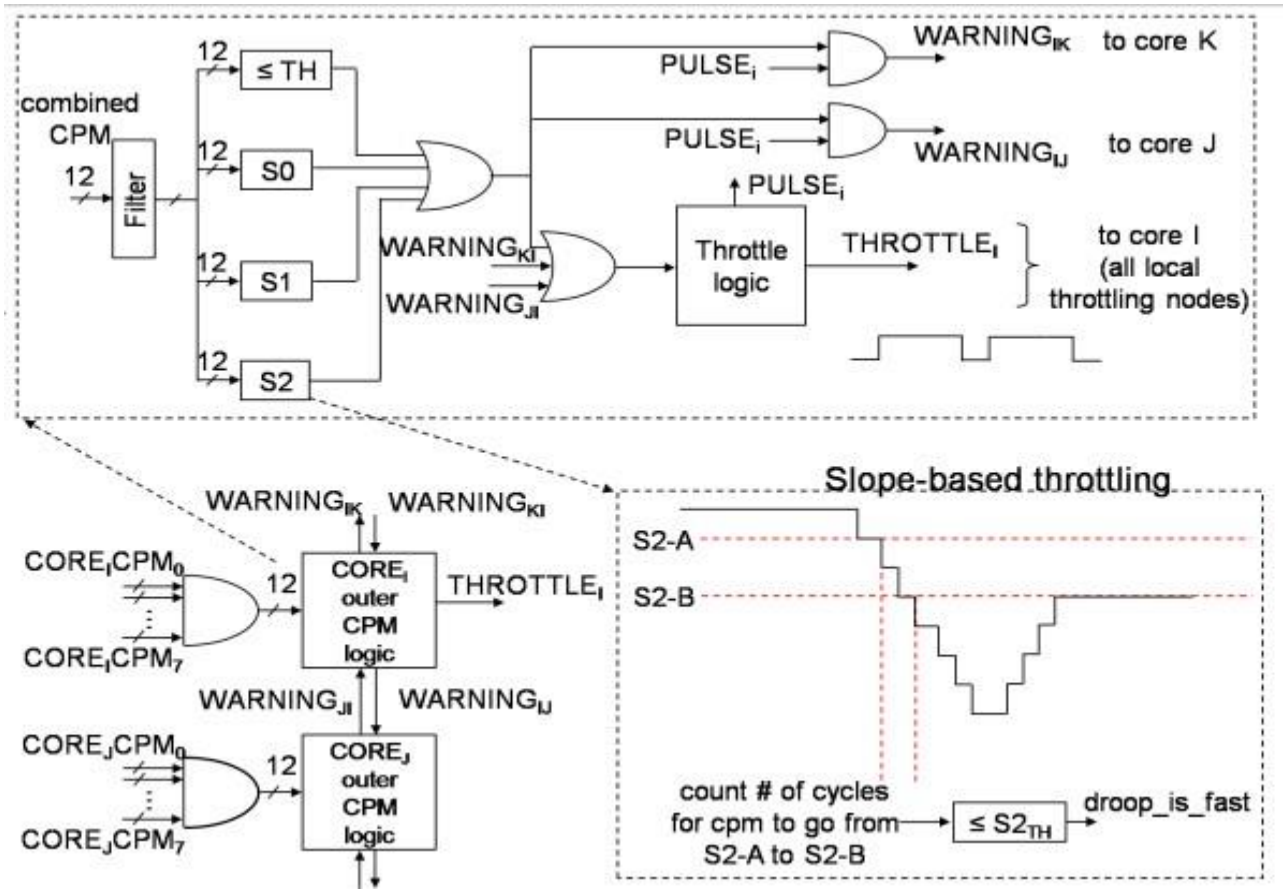

Fig-2.7.2 : Centralized CPM processing in each core based on local CPM value, slope, or nearest neighbour throttling.

2.7.3 CI Method

The charge injection (CI) method is an effective droop mitigation technique designed to stabilize supply voltage during transient events by rapidly injecting charge into the power delivery network (PDN). This approach relies on on-chip charge reservoirs, such as capacitors or specially designed circuits, that store energy and release it during supply voltage drops caused by high-frequency switching or load variations. When a droop is detected, the stored charge is discharged into the PDN, counteracting the voltage dip and maintaining operational stability. Research shows that charge injection methods are particularly beneficial in scenarios where traditional decoupling capacitors may be insufficient, such as in high-performance computing and advanced SoCs with tight timing constraints. The method's effectiveness depends on the precision and speed of droop detection mechanisms, as well as the design of the injection circuits to minimize overshoot and ensure consistent performance. Compared to other techniques, charge injection offers a low-latency solution to droop mitigation, making it an attractive option for applications requiring robust power integrity and high reliability.

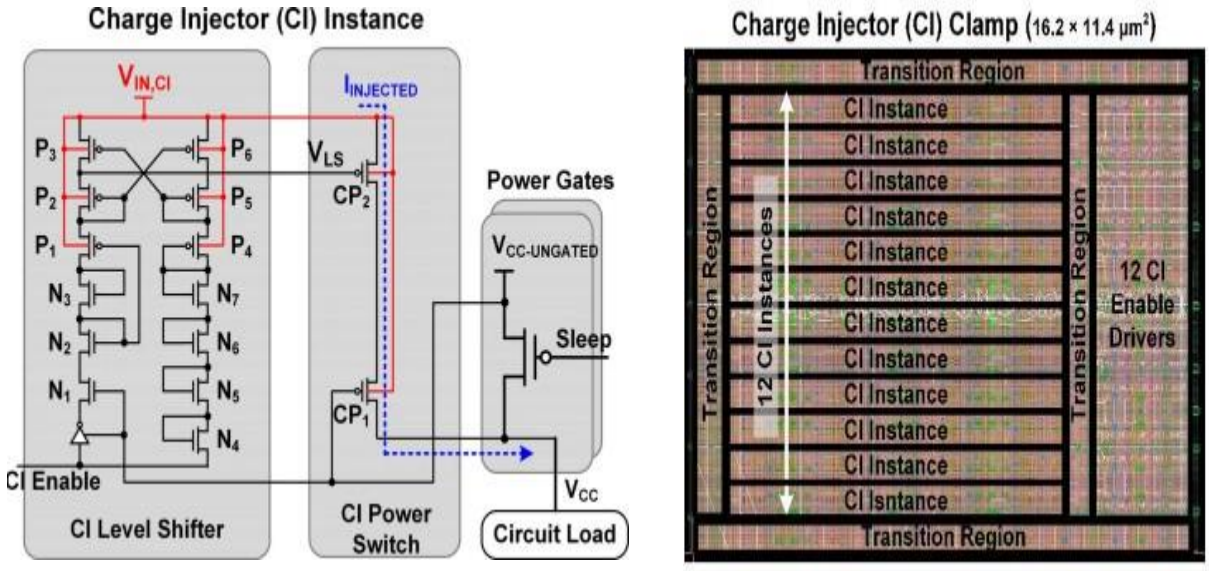

Fig- 2.7.3 Schematic of a CI instance (CI LS + CI power switch), CI clamp layout

2.7.4 DML

Dual-Mode Logic (DML) is a versatile logic family capable of switching between a low-power static mode and a high-performance dynamic mode, making it ideal for energy-efficient and high-speed applications. At the gate level, a DML gate integrates a static CMOS design with an additional clocked transistor to enable dynamic operation. In dynamic mode, the output is pre-charged or pre-discharged by the clocked transistor and then evaluated for speed optimization, while static mode conserves energy. This

flexibility allows for selective dynamic mode activation in critical timing paths, enabling higher performance where needed, while maintaining energy efficiency elsewhere. DML designs can be segmented, gradually accelerating specific paths during voltage droops by switching critical gates to dynamic mode, thereby preserving timing integrity and circuit functionality. A critical path replica is used to optimize pre-charge and evaluation phases. DML implementations, such as a 28 nm FD-SOI multiplier-accumulator (MAC), have demonstrated significant energy savings and performance gains over CMOS designs. By leveraging DML's dynamic capabilities, droop mitigation is achieved by selectively accelerating gates in critical paths, ensuring stable operation under varying supply voltages without corrupting circuit outputs. This approach, coupled with a lookup table for acceleration levels, allows cycle-specific adaptations to droop conditions, enhancing reliability and efficiency in modern systems.

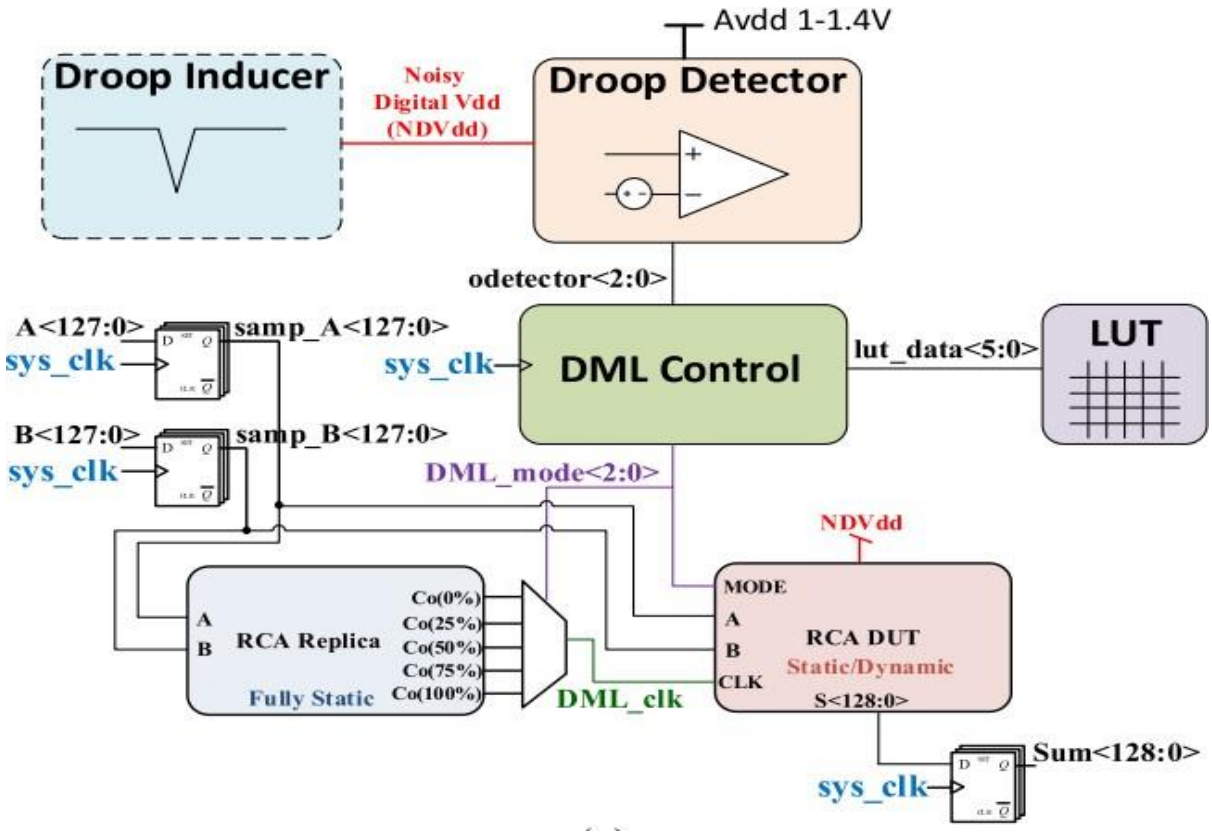

Fig-2.7.4: Block diagram of the droop mitigation scheme by using DML

CHAPTER-3

DESIGN ANALYSIS & PROPOSED WORK

3.1 Different Type of Droop Detector Circuit

As discussed in the literature parts, Voltage droop detectors ensure system reliability by identifying voltage fluctuations and preventing timing violations. The digital droop detector detects droops by monitoring delay variations in a shared dual-mode delay line. Upon detection, it reconfigures as a Digitally Controlled Oscillator (DCO) to temporarily serve as the system clock at a reduced frequency, gradually realigning with the input clock to prevent current surges. Analog droop detectors, using comparators and reference voltages, measure droops by comparing noisy and filtered voltage levels. While analog detectors are robust and require fewer calibration points, digital detectors, though more sensitive to environmental variations, offer high resolution, full digital integration, and external tunability for enhanced supply level monitoring.

3.1.1 Advantages of Digital Droop Detector Over Analog:

1. **High Resolution:** Digital detectors provide precise monitoring of voltage levels, translating droops into delay variations or frequency modulations.
2. **Simpler Design:** Fully digital implementation reduces the complexity of analog components like comparators and reference voltage generators.
3. **Integration Flexibility:** Digital designs are easily integrated into modern digital systems without requiring separate analog design expertise.
4. **External Tunability:** The droop detection threshold (DRth) can be dynamically adjusted to compensate for process variations, ensuring consistent performance across conditions.
5. **Scalability:** Digital detectors scale well with technology nodes, aligning with trends in advanced semiconductor processes.

3.1.2 Why Choose Digital Over Analog:

1. **Ease of Calibration:** Although digital detectors require initial 3D calibration, they offer flexibility in tuning thresholds post-deployment, unlike analog detectors dependent on precise reference voltages.
2. **System Integration:** Digital detectors seamlessly integrate with existing digital system components, reducing overhead in mixed-signal design.

3. **Adaptability:** Digital droop detectors can dynamically adjust thresholds and operation modes, providing adaptability in real-time scenarios.
4. **Compact Design:** Digital implementations typically require fewer specialized components, reducing overall area and power consumption.

For systems where high resolution and seamless digital integration are priorities, digital droop detectors are the preferred choice despite calibration challenges.

3.2 Design Analysis

The design of this digital droop detection system integrates advanced concepts in voltage monitoring, metastability handling, and digital circuit design to create an efficient solution for modern System-on-Chip (SoC) applications. Below is a detailed analysis of the key components and techniques used in this project:

3.2. Core Design Components

- **Delay Line**:
  The delay line is a crucial component that converts voltage droops into measurable delay variations. Propagation delays in the delay cells are directly influenced by supply voltage levels, providing a dynamic response to transient droops.
- **D Flip-Flop (DFF) Chain**:
  The chain of DFFs captures the delayed signals from the delay line, generating a thermometer code that indicates the severity of the droop. This approach ensures high-resolution monitoring with minimal complexity.
- **Thermometer Code Generation**:
  The thermometer code provides a visual representation of droop severity by marking the number of stages affected by delay variations. This coding mechanism allows for straightforward droop analysis.

3.2.2 Metastability Handling

- **Challenges Addressed**:
  Setup violations and metastability issues in the DFF chain, caused by delays near the clock edge, are a significant concern in high-frequency operations.
- **Techniques Used**:
  - **Adder-Based Correction**: Adds metastable bits to neighbouring stable bits, ensuring reliable outputs and maintaining the integrity of the thermometer code.

Bit Ignoring: Unpredictable bits resulting from metastability are strategically neglected, relying on redundancy in the thermometer code for error resilience.

3.3.3 Design Optimizations

- **Delay Line Calibration**:
  The delay line is optimized to balance sensitivity and response time, allowing precise detection of supply voltage variations.
- **Configurable Thresholds**:
  The system supports external tuning of droop detection thresholds, enabling customization for specific application requirements.
- **Buffer Sizing**:
  Buffer sizing is analysed to minimize delay variations while ensuring stable propagation of signals through the delay line. Larger buffers mitigate positive delays but increase power consumption, requiring careful trade-off analysis.

This analysis highlights the systematic approach taken in designing a robust and efficient droop detection system, addressing challenges like metastability, delay variability, and scalability while ensuring compatibility with future SoC architectures.

3.3 Proposed Work

3.3.1 Delay chain

In this specific design, a inverter based buffer stage is being designed. The inverter circuit, so as the buffer chain produces a delay when a lower supply voltage is applied. The lower the supply voltage higher the output delay of that inverter. The delay (td) through a single stage is inversely proportional to the supply voltage (Vdd) as per the equation:

$$td \propto \quad CL \cdot Vdd \,/\, Idrive$$

Here, CL is the load capacitance and $Idrive$ depends on Vdd. Lowering Vdd reduces power but significantly increases delay due to reduced $Idrive$

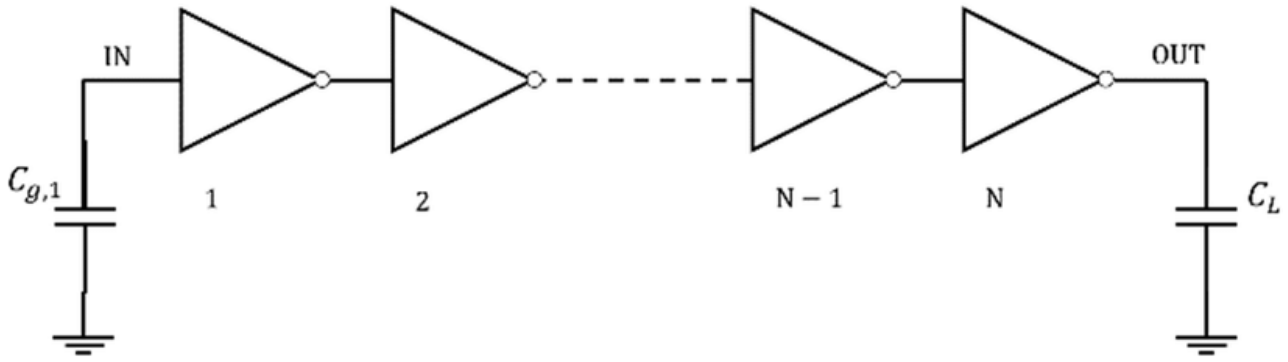

Fig 3.2.1: Inverter Based Buffer Chain

3.3.2 Transmission Gate Based D-FlipFlop Design

A transmission gate-based D flip-flop (TG-DFF) is often preferred in high-speed applications like a thermometer code generator due to its reduced propagation delay compared to static logic designs. The TG-DFF achieves faster transitions by minimizing the number of active stages in the signal path, leading to lower overall clock-to-output delay ($tclk \rightarrow Q$). Its reduced latency minimizes timing skew between stages, which is critical for maintaining the monotonicity of the thermometer code.

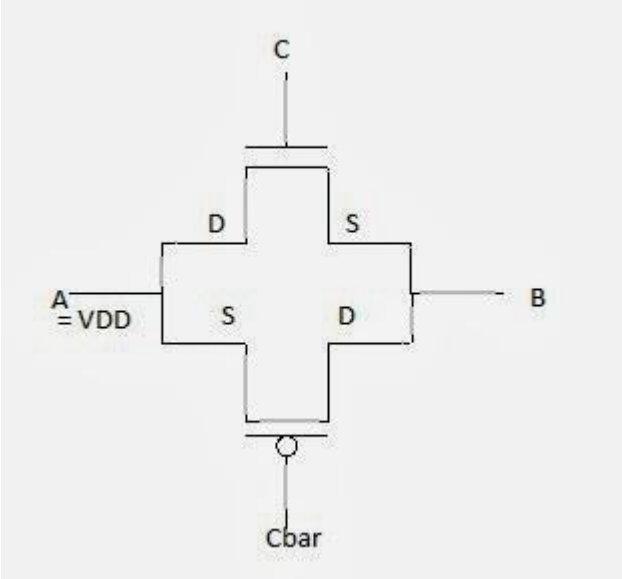

Fig: (3.2.2): CMOS Based Transmission Gate

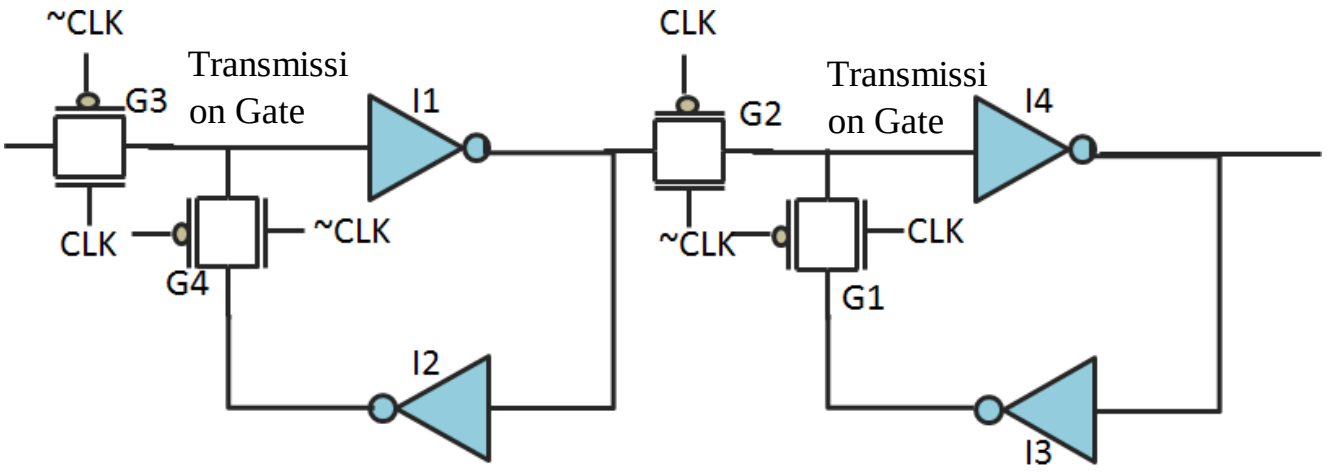

Fig: (3.2.3): Transmission Gate Based D FliFlop Design

3.2.3 Thermometer Code generate:

In the thermometer code generation system, the same clock signal propagates through a delay line and drives the clock inputs of the D flip-flops (DFFs) placed at each stage. The data pin of each DFF receives the delayed version of the clock signal. When a voltage droop occurs, the increased delay in the clock signal at the data pin results in a timing mismatch, causing the DFF to latch a '0'. Conversely, without a droop, the timing alignment ensures the DFF latches a '1'. This creates a clear binary transition from (111…11) to (110…00), accurately representing the delay-induced changes in the clock signal. The resolution of the delay stages and proper synchronization ensure precise detection and monotonicity of the thermometer code, crucial for droop detection.

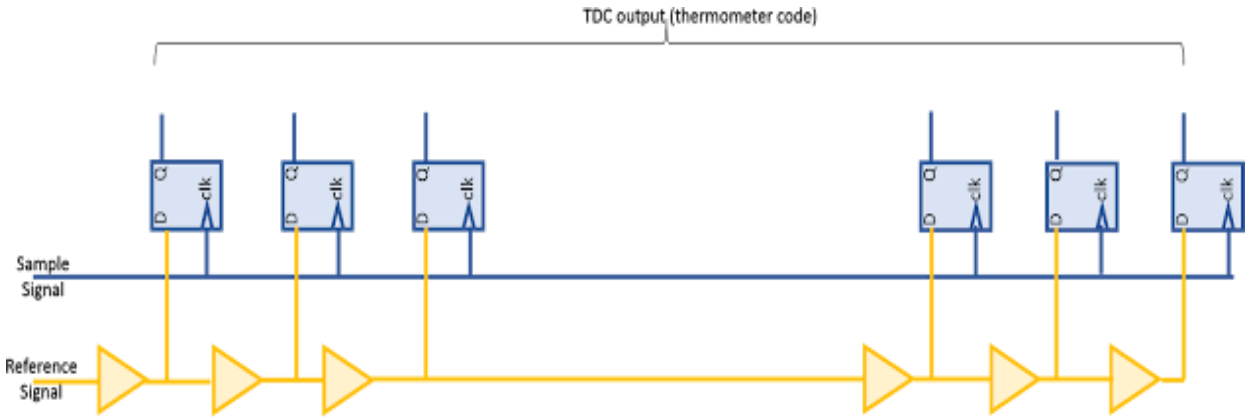

Fig: (3.2.4): A Thermometer Code Generator using DFF from a Delay Line

The resolution of the thermometer code is defined by the relationship between voltage droop and the delay introduced at each stage. For example, if a 10mV voltage drop (from 970 mV to 960 mV) causes sufficient delay at a specific stage for a D flip-flop to latch a '0' in consecutive bit position, then each subsequent 10 mV drop improves one additional bit from 1 to 0 in the thermometer code. This ensures that for a small step in voltage (e.g., 10 mV), the thermometer code decrements precisely by one bit, providing high resolution for detecting and profiling voltage droops across the delay line stages.

To calculate the number of bits planned for a voltage range from 1.06V to 960mV with a resolution of 10mV per stage:

1. Determine the total voltage range:

Voltage range=1.06 V−0.96 V=0.10 V=100 mV

2. Divide the range by the resolution per stage:

$$\text{Number of stages (bits)} = \frac{100\,\text{mV}}{10\,\text{mV/stage}} = 10\,\text{stages (bits)}$$

Thus, 10 bits are planned to represent the voltage range from 1.06V to 960mV, with each stage corresponding to a 10mV drop.

3.2.4 Reset of The Flops:

To minimize jitter and ensure reliable operation, the D flip-flops in the thermometer code generator are reset at the negative edge of the clock. This reset mechanism clears any residual state or metastability issues before the next sampling cycle, improving the

accuracy of the code transition. By aligning the reset with the clock's negative edge, the system ensures that all flip-flops are prepared to capture the delayed clock transitions cleanly, reducing the impact of noise and maintaining the integrity of the thermometer code under varying droop condition.

CHAPTER-4
RESULTS & ANALYSIS

At the starting of the Design, Inverter based Buffer Circuit is made and A buffer chain is being proposed of 10 stages for analyzing delay vs staging affect with a lower voltage supply.

The pMOS and the nMOS are taken for high Vt devices for better delay implementation on the delay line. Different ports are created for various Supply voltage application for a perfect droop measurement.

4.1 Circuit Schematic:

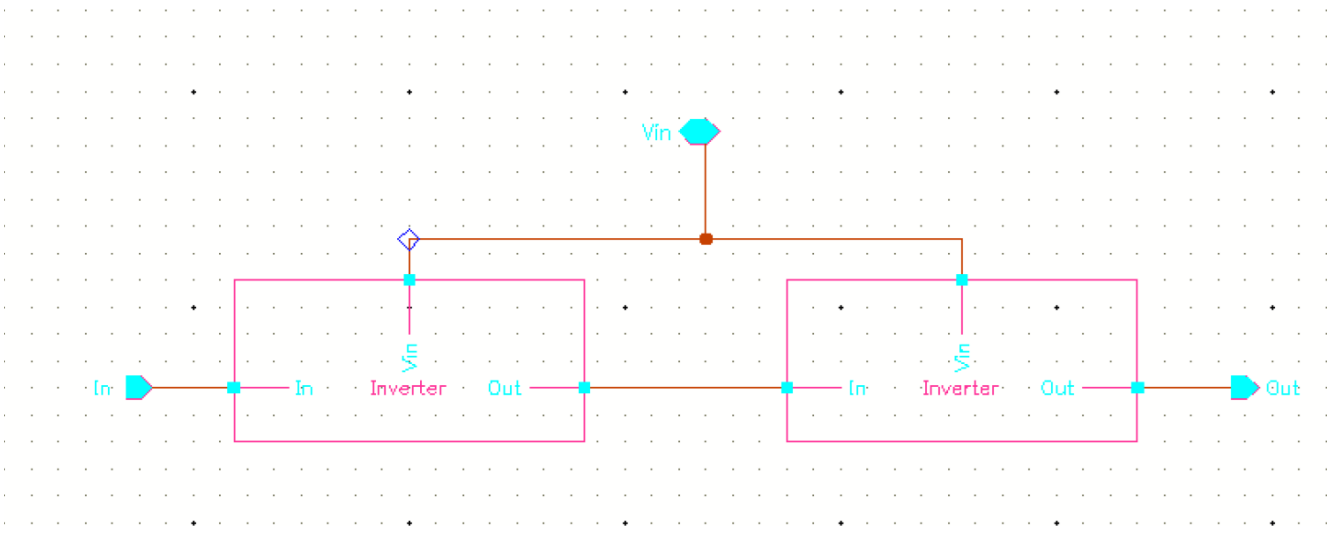

Fig 4.1.1: Schematic of an Inverter Based Buffer

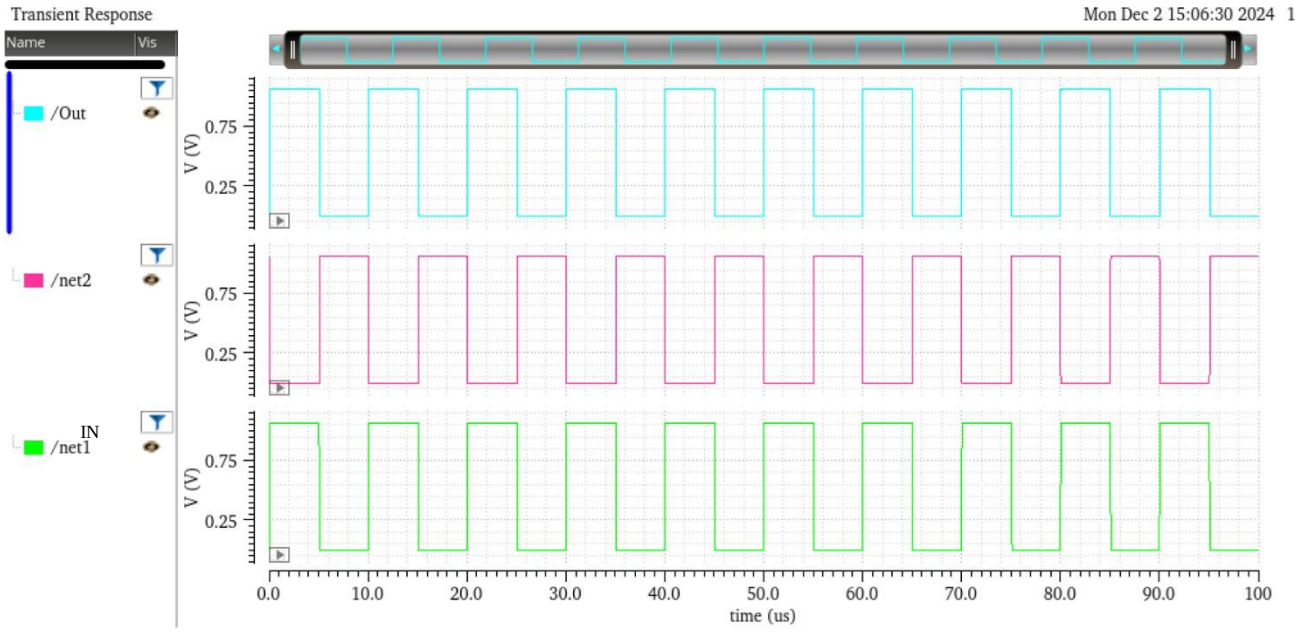

Fig: 4.1.2: Working Waveform of the Buffer

4.1.1 Staging effect of buffers:

Buffers are cascaded into stages and in/Out Delay observed. A linear type delay profile is being observed, where a single stage contributes around 0.1ns of Delay.

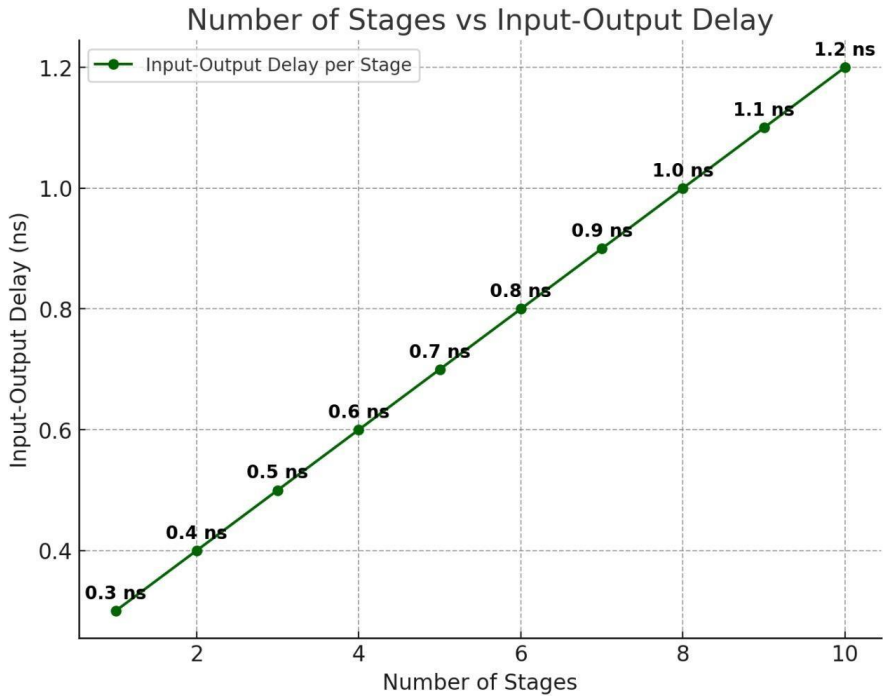

Fig: 4.1.3: Buffer Stages vs Delay Plot

4.1.2 Buffer Size vs Delay:

In counter of different staging of buffers, sizing effects in delays can also be implemented. So different (W/L) ratios are plotted against their corresponding delays. Here is the tabular represent of the points where W/L ratio changed of a single buffer and corresponding single stage delay counted. *The insight of -ve delay is discussed in later part.*

W, L (W/L) µm	DELAY (ns)
W=3, L=1, W/L= 3	9.6nS
W=1.6, L=0.8, W/L=2	8.3ns
W=1.2, L=0.6, W/L=2	6.2ns
W=0.4, L=0.2, W/L =2	(-ve) 1.2ns

4.2 Buffer Based Delay Line Design:

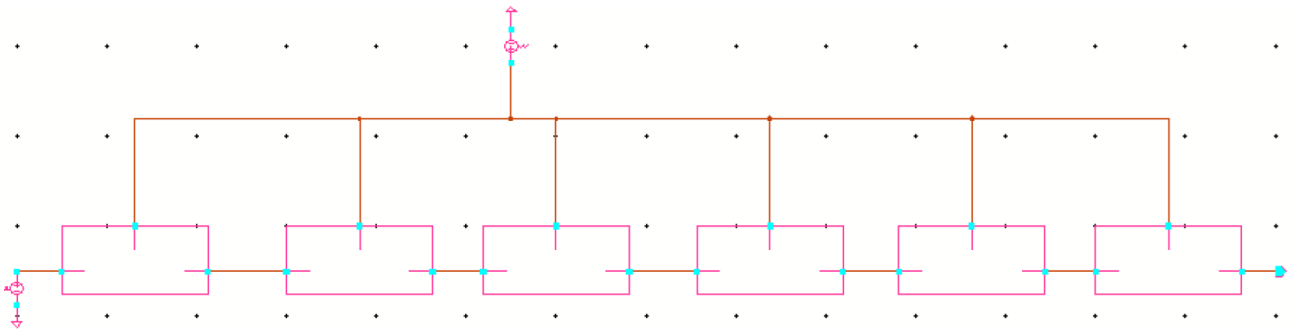

Fig: 4.2.1: Buffer Based Delay Line Design with variable Supply Voltage

Delay is observed when a drooped supply voltage applied to a delay chain. The delay keeps increasing with increased drop in supply voltage. After a particular drop when voltage again settled to 1.06V the delay of total stage becomes a constant (≈ 0.41ns) and a highest (≈ **0.**63ns) at highest voltage drop.

4.3 Voltage Droop vs Delay Observation:

Supply Voltage	In-Out Delay
1.01939V	0.45 nS
958.249mV	0.5 nS
909.6323mV	0.58 nS
883.8524mV	0.63 nS
896.147mV	0.6 nS
916.1487mV	0.568 nS
1.0336V	0.436 nS
1.06V	0.417 nS

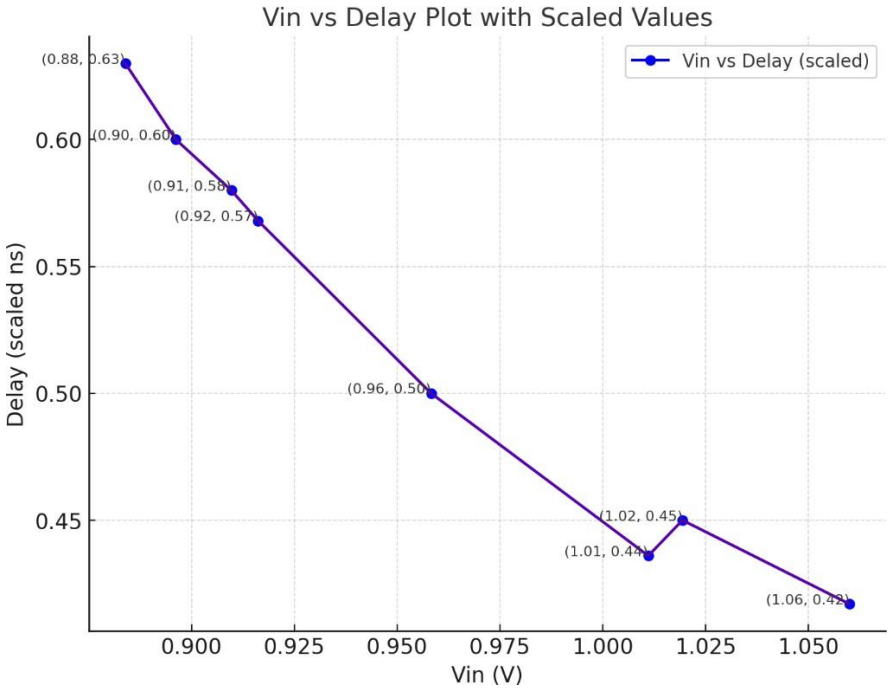

Fig: 4.3.1: Supply Voltage vs Delay Graph

4.3.1 Delay Observations:

In an inverter or buffer-based chain, when a pulse is applied, the source signal inherently exhibits some skew due to its rise and fall times. However, the standard-sized inverter or buffer has a high driving capability, which helps reduce this skew by quickly charging or discharging the load capacitance. As a result, the output signal, which lags slightly behind the input due to the inherent delays of the chain, may show a time advance at the 50% threshold of both the input and output waveforms. This phenomenon results in a negative delay, where the output transitions before the expected time, effectively reducing the overall propagation delay seen in the signal path.

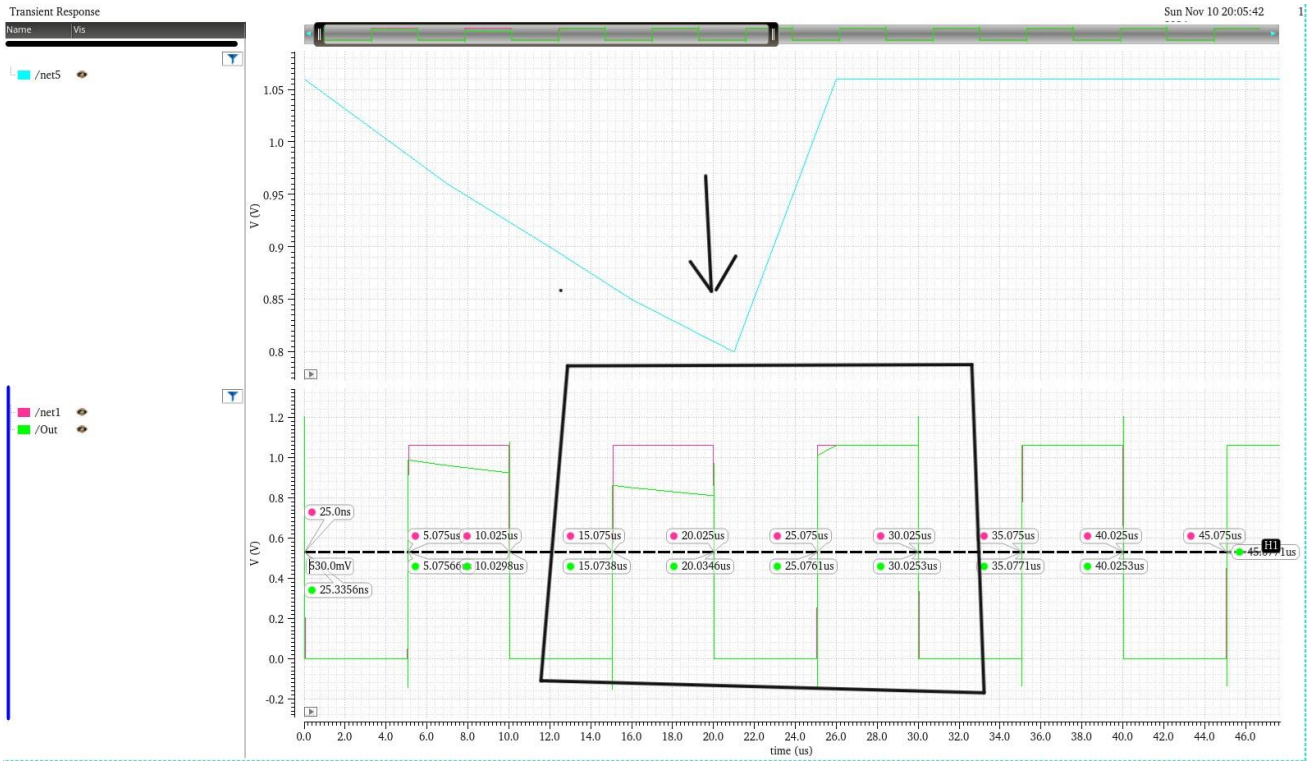

Fig: 4.3.2: Here in the second pulse in the positive edge a -1.2ns of delay and in the negative edge a -2.1ns of delay is being observed.

To calculate the perfect delay in a buffer or inverter chain, it is common to sample the output from the 2nd or 3rd stage of the buffer chain, as opposed to the immediate first output. This is because the first output may exhibit some skew or negative delay due to the fast switching of the first buffer, as discussed earlier. By taking the output from the second or third buffer, you allow the signal to settle and reach a more stable

transition, minimizing the impact of any initial distortions or timing mismatches introduced by the first stage.

The second or third output stage typically reflects the delayed signal more accurately, as it would have had time to propagate through a few stages, providing a more reliable measure of the overall delay. This approach helps in achieving a consistent delay profile by ensuring that the timing characteristics of the signal are more representative of the chain's overall behaviour, rather than any transient effects seen at the very first stage.

A negative delay also observed in a standard or lower sized single stage buffer, this concept of negative delay in smaller buffers versus positive delay in larger buffers arises from the electrical behaviour of logic gates and the parasitic associated with them.

1. **Small Buffer (Negative Delay)**:
    - When a small or standard-size buffer is used, the input capacitance is minimal, and the output load driven by the buffer is also small if they are staged together.
    - In some cases, the switching transition of the output appears faster than the input signal's full swing (due to fast initial charging of the gate capacitance at the input). This creates the "negative delay" because the output transition seems to lead the complete input signal transition.
    - The phenomenon is heavily dependent on signal rise/fall times and circuit parasitic.
2. **Large Buffer (Positive Delay)**:
    - A larger buffer has a higher input capacitance and is usually designed to drive heavier loads. The increased capacitance takes more time to charge/discharge, introducing a positive delay in signal propagation.
    - As the buffer size increases, the input gate capacitance and output parasitic grow proportionally, resulting in a cumulative delay that increases with the size of the buffer.
    - This is a direct result of the RC (resistance-capacitance) time constant, which dominates the delay characteristics in larger buffers.
3. **Transition from Negative to Positive Delay**:
    - For very small buffers, the input load is so light that the transition delay is negligible or appears negative under certain conditions.
    - As the buffer size increases, the delay gradually transitions to a positive value, and this delay grows linearly or quadratically with the size of the buffer due to the increased capacitance and resistance.

4.4 Transmission Gate Design:

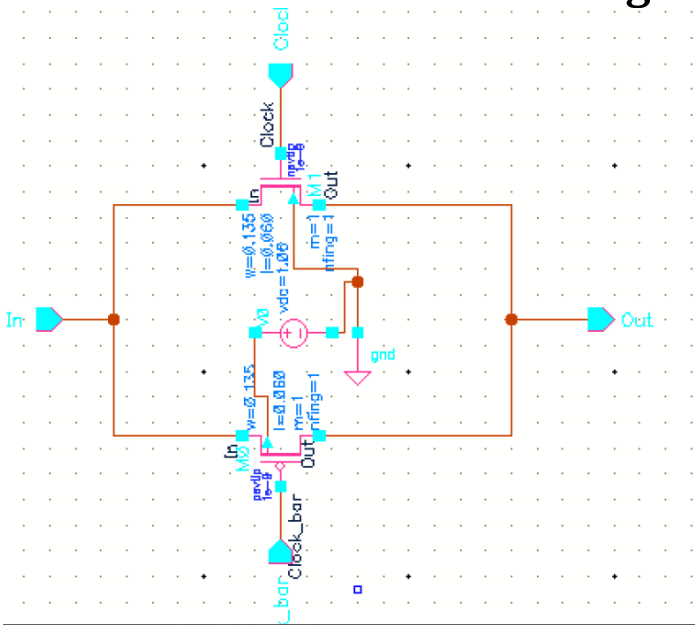

Fig: 4.4.1: A CMOS Transmission Gate is designed with 4 terminals

A low Vth nMOS, pMOS is being used for fatser performance and accurate code generation.

In a low-Vt transmission gate, where speed is the primary goal, the reduced threshold voltage allows for faster switching, but this comes at the cost of compromised stability. When a pulse and its complementary signal (clock and clock_bar) are applied to the transmission gate, the output is ideally perfect when both transistors are on, as the transmission gate conducts with minimal delay. However, when both transistors turn off, the output can become imperfect, exhibiting a sloppy output, typically floating close to 0V instead of a clean logic '0'. This issue arises due to charge sharing and threshold leakage in the off state, particularly with low-Vt devices. To overcome this, an inverter can be inserted at the output to ensure the lowered voltage is correctly interpreted as logic '0'. The inverter pulls the output to a clean low voltage, mitigating issues like charge leakage and metastability, and stabilizing the output for reliable operation. This approach leverages the high-speed benefits of the low-Vt gate while compensating for its inherent drawbacks.

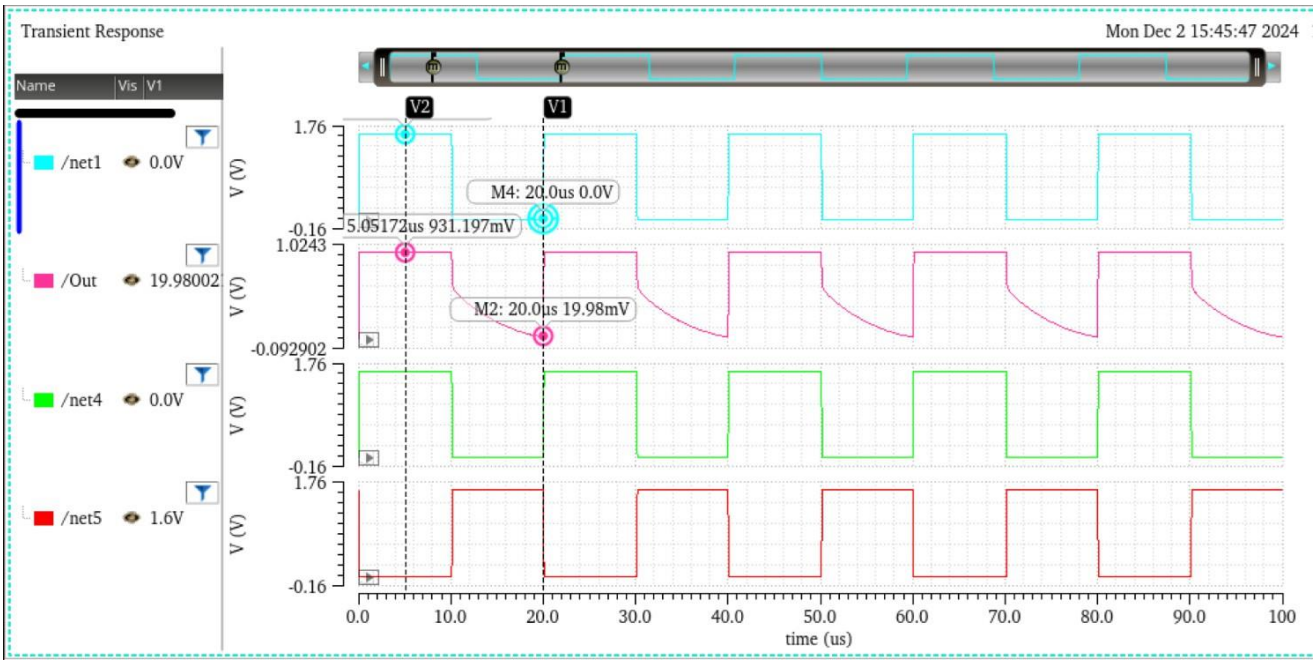

Fig: 4.4.2: Waveform of Transmission Gate output of a Pulsed Input

4.5 D Flip Flop Design:

A transmission gate-based D flip-flop offers faster operation due to its low-Vt devices, which enable rapid switching and reduced propagation delay. However, this speed comes at the cost of stability, as low-Vt transistors are more prone to charge sharing and threshold leakage when turned off.

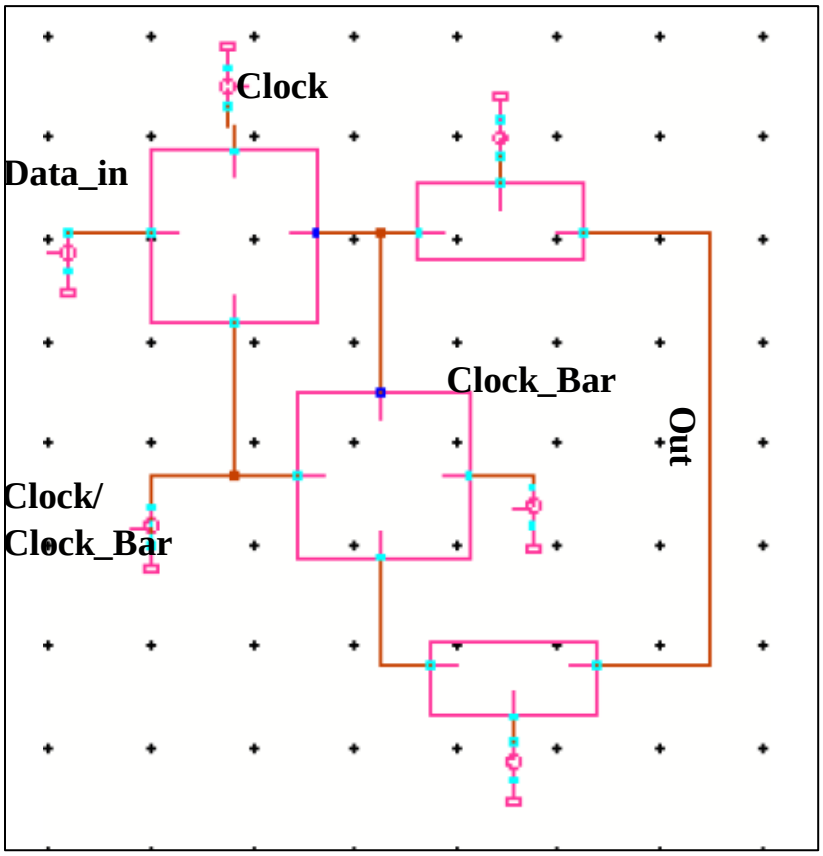

Fig: 4.4.1: Schematic View (-ve) Level Triggered Latch

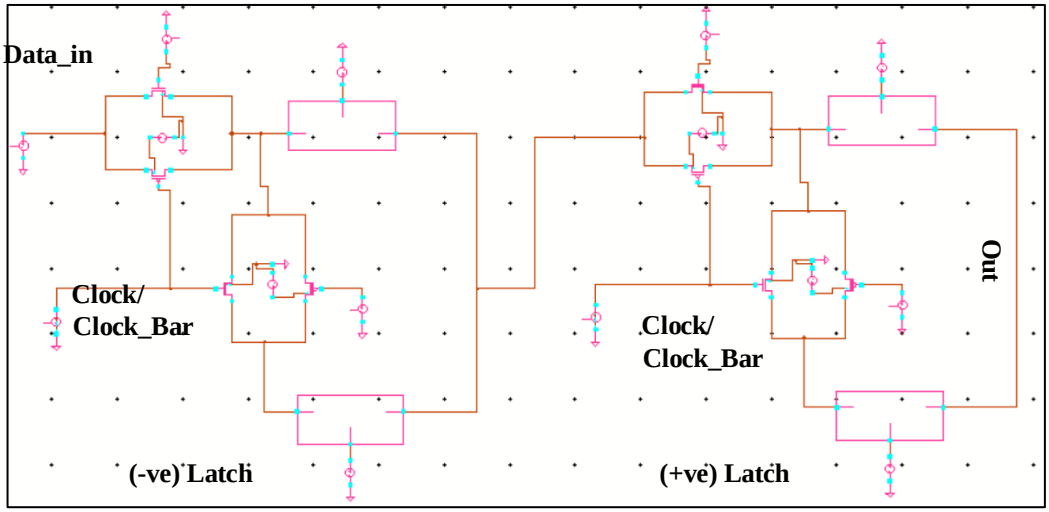

Fig:4.4.3: D FF design using 1 -ve latch 1 +ve latch

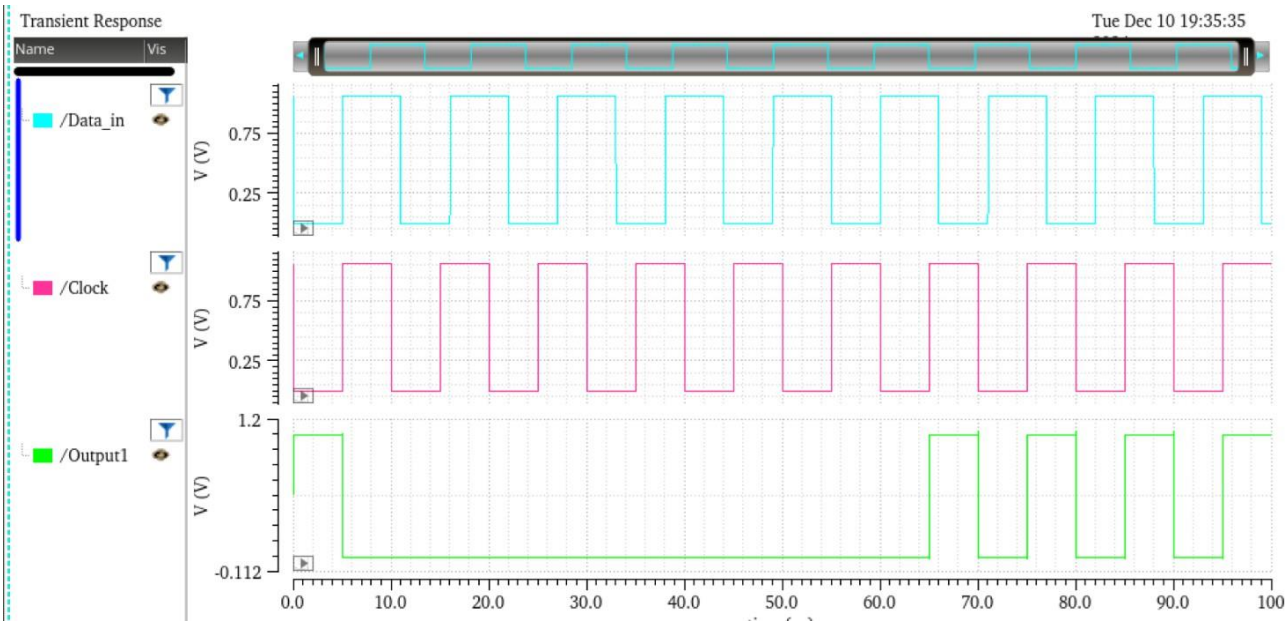

Fig: 4.4.3: Output Waveform of Positive Edge D Flip Flop

4.6 Metastability Encounter:

Metastability in a transmission gate-based D flip-flop occurs when the data input changes within the setup and hold window, causing the flip-flop to enter an undefined state. With low-Vt devices and minimal delay, the flip-flop becomes more susceptible to such conditions, as the timing margins are tighter. During metastability, the output remains in a transitional or unstable voltage level, failing to latch a definitive logic '0' or '1'. This instability results in imperfect latching of the signal, leading to unpredictable circuit behavior. Proper timing analysis, careful clock-data alignment, and introducing synchronization stages are crucial to mitigating metastability in high-speed designs like these.

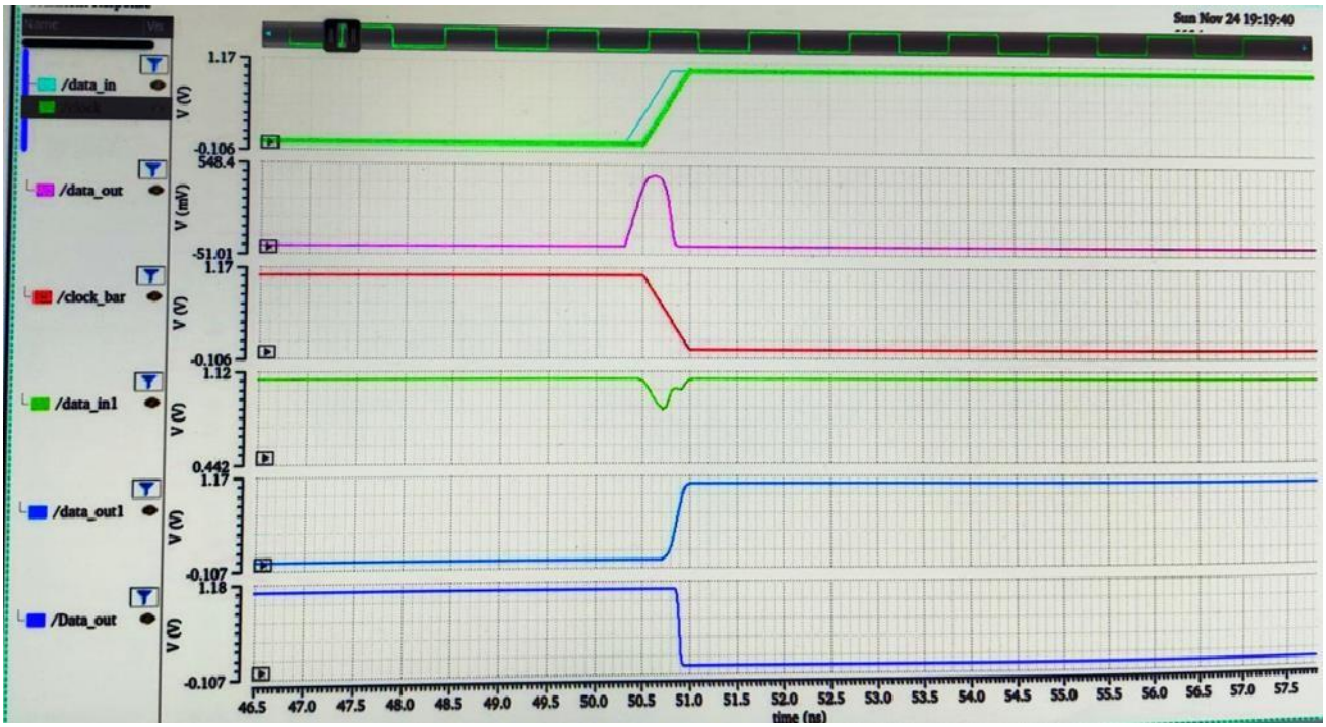

Fig: 4.5.1: Meta stable condition, Flop gets Wrong Output

- **Metastability in DFFs (Transmission Gate-Based):**
    - Metastability occurs when the data input (D) transitions too close to the clock edge, violating the setup or hold time requirements.
    - In this condition, the DFF may fail to resolve into a stable logic level and produce an intermediate voltage or "bump."
- **Setup Window Impact:**
    - The setup window is the time interval before the clock edge during which the input must remain stable for proper operation.
    - If the input violates the setup time (e.g., close to the clock edge), the DFF becomes more likely to enter a metastable state.
- **Voltage Bump Behaviour**:
    - A shorter violation of the setup window results in higher voltage bumps because the transmission gate inside the DFF struggles more to settle to a stable state.
    - With a longer violation of the setup window, the voltage bump is smaller because the metastability condition begins to resolve itself earlier.

- Transmission gates in metastable conditions partially conduct, creating an intermediate voltage at the output node.
- The closer the violation is to the clock edge, the less time the circuit has to suppress the voltage bump before the latch transitions, leading to higher bumps.

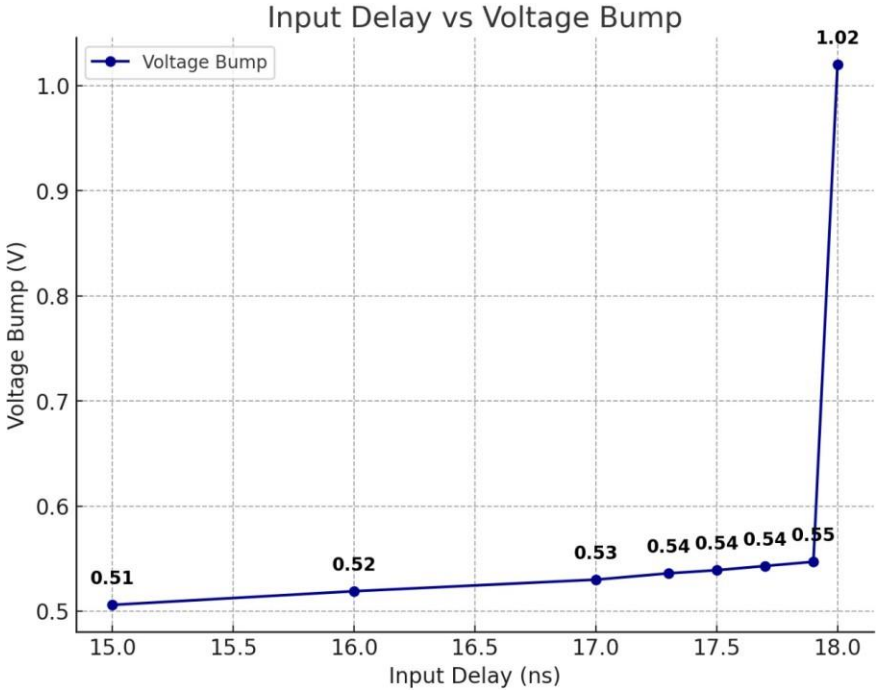

Fig:4.5.2: A D Flop (of setup time 18ns) counters its input signal delay vs metastable voltage bump plot.

For observation a DFF of 18ns set up time is encountered with a step input signal of approximately nearer setup values. Input signal is being applied remembering it set up time limit and starting from a lower delay to increasing straightly. The voltage in metastable bump is being observed and noted. And is being observed that more the delay input side more the chances of the metastable state to reach up to logic ‘1’. At nearest to the setup time the metastable state finally reaches to log’1’ and a voltage of 1.06V approximately.

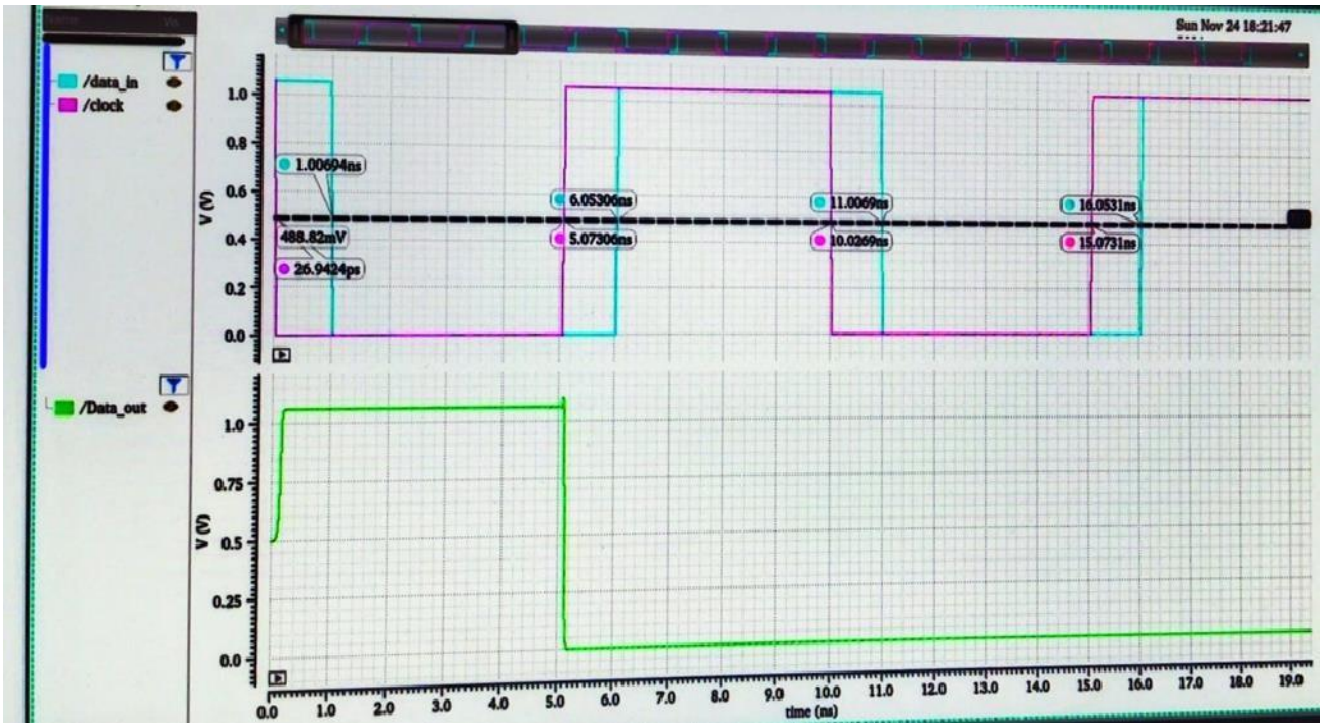

Fig: 4.5.3: Perfectly latched ass ‘0’ when the Delay is out of Setup and Hold Window

4.6.1 Metastability Encounter by Setup-Hold Window

To resolve metastability issues in a transmission gate-based D flip-flop, the setup and hold window must be minimized to reduce the likelihood of data transitions during critical timing intervals.

Using a small setup-hold window flip-flop design, which involves transistor-level optimizations like reducing parasitic capacitances and adjusting the aspect ratios (W/L) of the transmission gates for faster switching and tighter timing margins.

To encounter this, the basic block of DFF the Buffers so as the transistors of that size is being varied. The size is changed from its standard size to a W/L ratio of 2,3,4… so on and also later keeping W/L ratio same the W,L are changed and a clear variety of set up time of each case being observed. But the standard sized low Vt transistor only provides a lowest set up time as shown in the graph.

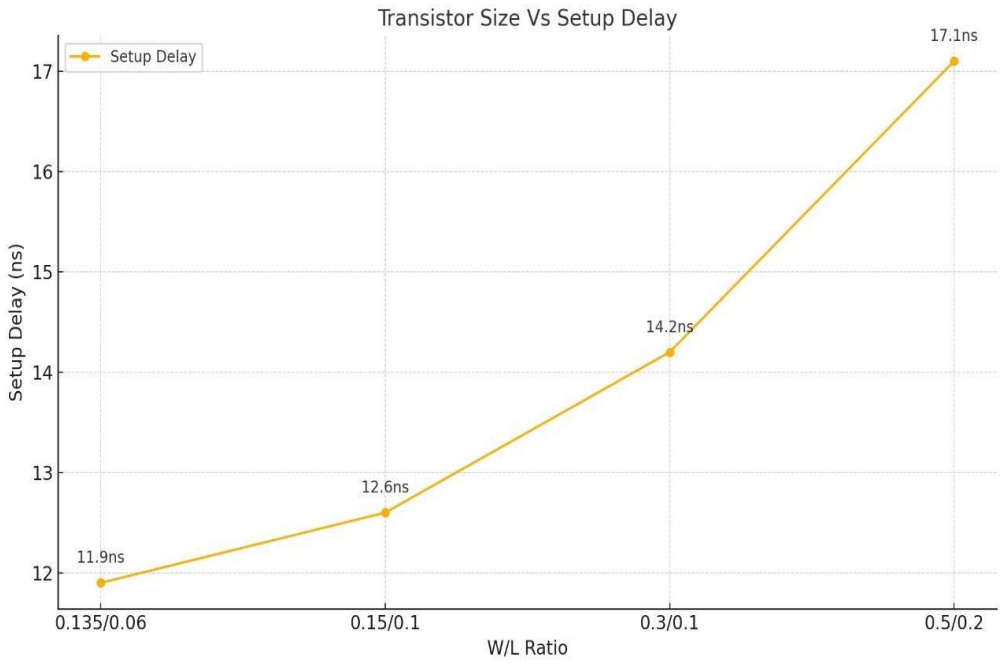

Fig:4.5.4: Transistor size of DFF vs Setup time Plot

4.6.2 Adder Based Metastability Encounter

When generating a thermometer code, encountering metastability in one of the bits can create an ambiguous logic state. Using an adder to handle this issue is a practical approach that resolves the metastable bit by combining it with a prominent, stable bit. This method effectively converts the uncertainty of the metastable bit into a valid binary result through arithmetic correction.

- **Metastable Bit Handling:** The metastable bit is added to a neighbouring stable bit to "absorb" the uncertainty and produce a reliable output.
- **Thermometer Code Recovery:** The adder ensures the generated thermometer code sequence remains intact despite metastability in one or more bits.
- **Simplified Resolution:** Instead of advanced synchronizers, this method uses straightforward arithmetic to address metastability.

To implement this concept an adder is being implemented where the metastable output of the flop is taken as bit A and strong logic ‘0’ or ‘1’ takes as bit B and Sum as A+B.

The results reflects that a better metastable bump input tries to catch up with the summation part more correctly.

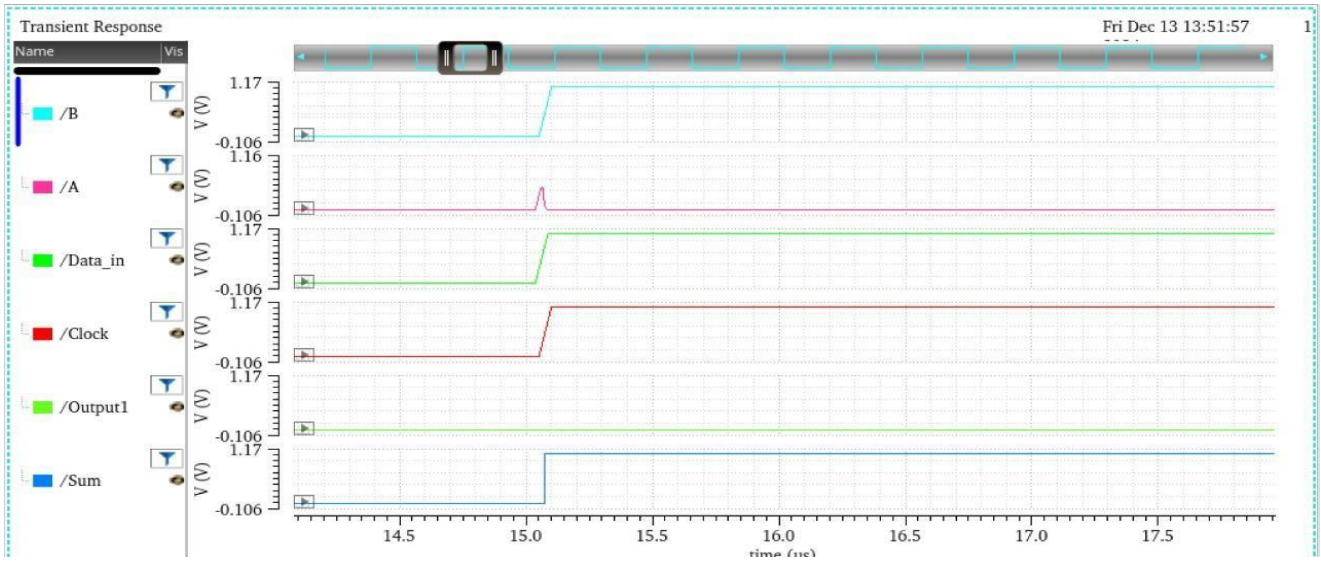

Fig: 4.5.5: Adder Output Shows ‘Sum’ where the inputs are ‘A’ ‘B’

4.6.3 Metastability Encounter using Bit Ignorance:

This method involves intentionally discarding one or more unreliable bits in situations where their inclusion could compromise the system's functionality

Instead of attempting to resolve or correct metastable bits, they are simply neglected or masked out from the final code generation process.

This ensures that the unreliable information does not propagate through the system.

1. Detecting Unreliable Bits:

- Use a metastability detector or monitor specific flip-flops for prolonged transition times (indicating metastability).

- Identify bits that fall outside the stable threshold.

2. Masking or Replacing Unstable Bits:

- Replace the metastable bit with a predefined value, such as `0`, to preserve the sequential integrity of the thermometer code.

- Alternatively, skip the bit entirely and continue processing the remaining bits.

3. Maintaining Code Sequence:

- If the metastable bit is ignored, ensure adjacent stable bits maintain the correct thermometer sequence.
- This can be done by enforcing logical continuity, such as filling skipped bits with the last stable value.

CHAPTER 5
CONCLUSION & FUTURE ENHANCEMENTS

5.1 Conclusion

Voltage droop, a transient reduction in supply voltage caused by sudden changes in current demand or power delivery network limitations, poses significant challenges to chip performance and reliability. Detecting and mitigating droops promptly is critical to ensuring stable operation in modern SoCs, where margins for error are minimal. This project focuses on the design and implementation of a digital droop detection system, which leverages delay variations in logic gates to effectively translate voltage droops into measurable parameters

- The system employs a delay line-based architecture integrated with a chain of D flip-flops (DFFs) to generate a thermometer code for precise droop detection. This method ensures high-resolution monitoring while maintaining a fully digital, scalable design suited for modern SoCs.

- The delay line plays a central role in this architecture, where propagation delays are directly influenced by supply voltage variations (Vdd droops). By cascading delay cells and synchronizing them with a clock signal, the delay line produces a dynamic response that the D flip-flop chain captures, enabling the generation of a reliable thermometer code. This code provides a real-time indication of droop severity, making it an efficient tool for supply level monitoring and mitigation.

- To address potential metastability issues, techniques such as bit ignoring and adder-based correction mechanisms are incorporated. These methods ensure that any unstable or ambiguous states caused by setup time violations do not compromise the integrity of the thermometer code. The design also supports configurable thresholds, allowing flexibility in adjusting droop detection sensitivity to suit system-specific requirements.

- The use of digital techniques overcomes challenges associated with process, voltage, and temperature (PVT) variations, offering greater reliability compared to analog counterparts. Furthermore, the project explores buffer sizing to manage

delay propagation, as well as methods to ensure stable transmission gate operation and efficient metastability handling in DFFs.

In summary, the project successfully combines advanced digital design concepts with practical engineering considerations to develop a robust, high-resolution droop detection and mitigation system. The use of delay lines, D flip-flops, and innovative metastability handling techniques ensures that the design is scalable, reliable, and adaptable for various SoC applications, addressing one of the most critical challenges in modern digital circuit design.

5.2 Future Enhancement:

- **Enhanced Droop Mitigation Strategies**: A case study where adaptive control mechanisms that dynamically adjust system performance (e.g., clock frequency) based on droop severity to further enhance reliability under extreme operating conditions may take part.

- **Higher Resolution and Faster Response**: Optimize the delay line and D flip-flop chain to achieve finer detection thresholds and faster response times, allowing for more precise and real-time voltage droop monitoring.

- **Error Correction Using Redundancy**: Develop advanced techniques for thermometer code error correction that leverage redundancy to mitigate the impact of metastable bits or unreliable outputs more efficiently.

- **Power Optimization**: Focus on reducing the power overhead of the delay line and DFF chain by exploring low-power design techniques, making the droop detection system suitable for ultra-low-power applications.

- **Hybrid Detection Mechanisms**: Combine digital and analog approaches within a single system to exploit the high resolution of digital techniques and the sensitivity of analog circuits for a more versatile detection framework.

- **Advanced Synchronizers for Metastability**: Incorporate advanced metastability-handling techniques, such as multi-stage synchronizers or metastability-resistant D flip-flops, to further enhance robustness in high-frequency operations.

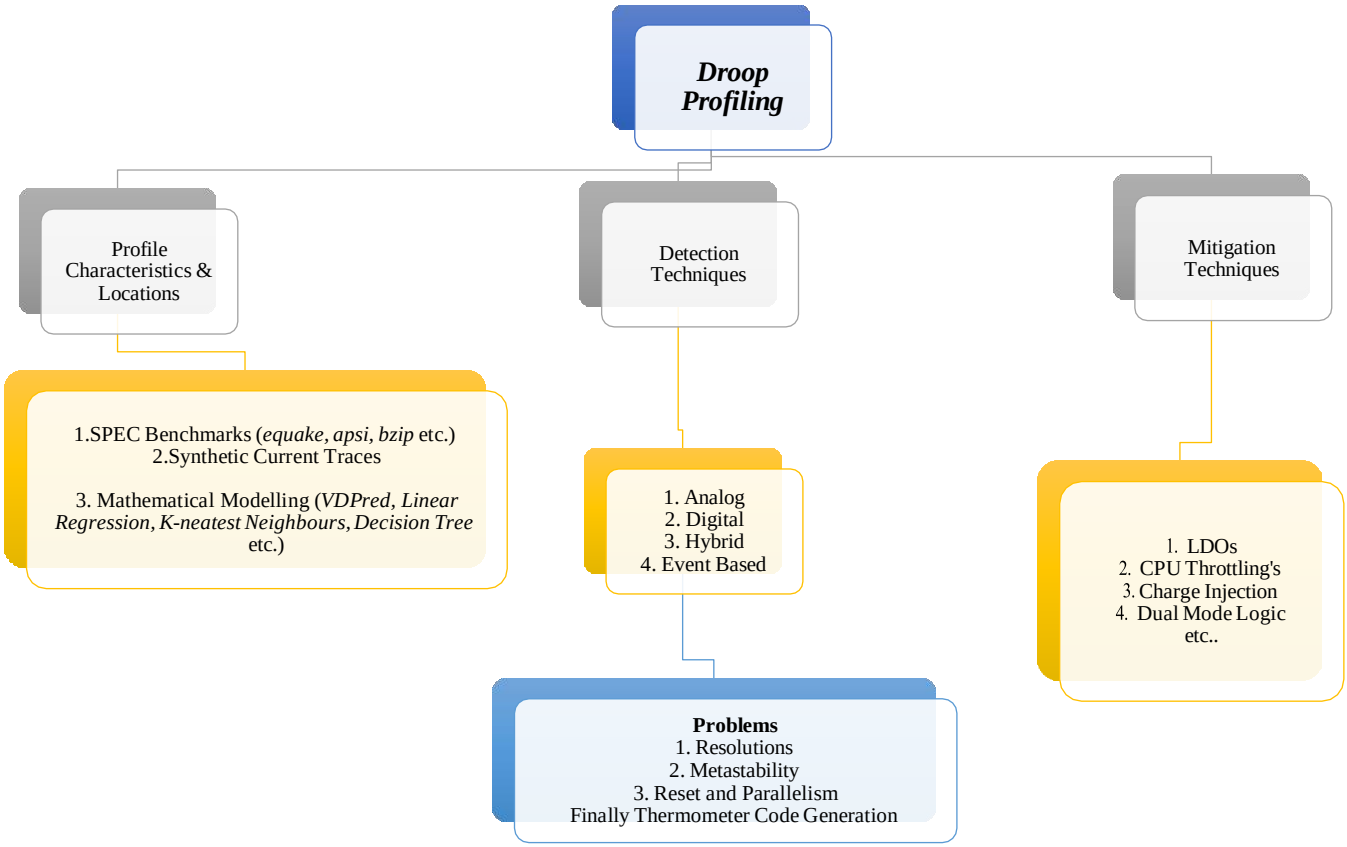

Fig: 5.1: Figure Depicts the whole 'Droop Profiling' topic where each branch represent an unique Problem Statement itself, Where Digital Detection part is just a subpart of Droop detection branch.

REFERENCE

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  Wing Oi Siu, Chak Sing Ng, Terrence Mak Department of Computer Science and Engineering, The Chinese University of Hong Kong, Hong Kong Email: fwosiu, csng, stmakg@cse.cuhk.edu.hk

- VDPred: Predicting Voltage Droop for Power-Efficient 3D Multi-core Processor Design *He Xiao*
  Cadence Design Systems, Inc. San Jose, CA, United States xiheasas@gmail.com Monodeep Kar, Georgia Institute of Technology Atlanta, GA, United States. Saibal Mukhopadhyay, Georgia Institute of Technology Atlanta, GA, United States, Sudhakar Yalamanchili, Georgia Institute of Technology Atlanta, GA, United States.

- Understanding Voltage Variations in Chip Multiprocessors using a Distributed Power-Delivery Network
  Meeta S. Gupta, Jarod L. Oatley, Russ Joseph, Gu-Yeon Wei and David M. Brooks Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA {meeta, jloatley, guyeon, dbrooks}@eecs.harvard.edu
  Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, IL
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- A Method for Mitigation of Droop Timing Errors Including a 500 MHz Droop Detector and Dual Mode Logic
  Yizhak Shifman, Graduate Student Member, IEEE, Inbal Stanger, Graduate Student Member, IEEE,
  Netanel Shavit, Graduate Student Member, IEEE, Ramiro Taco, Member, IEEE,
  Alexander Fish, Member, IEEE, and Joseph Shor, Senior Member, IEEE

- Power Supply Noise in a 22nm z13TM Microprocessor
  Pierce I-Jen Chuang1, Christos Vezyrtzis1, Divya Pathak2, Richard Rizzolo3, Tobias Webel4, Thomas Strach4, Otto Torreiter4, Preetham Lobo5, Alper Buyuktosunoglu1, Ramon Bertran1, Michael Floyd6, Malcolm Ware6, Gerard Salem7, Sean Carey8, Phillip Restle

- A Distributed Critical-Path Timing 65nm High-Performance Microprocessor
  Alan Drake, Robert Senger, Harmander Deogun, Gary Carpenter, latched in the edge detector on the rising edge of the system clock.
  Soraya Ghiasi Tuyet NguyeSn, or NaoyramaGn' N Jiaagmesus Ti, yuynlet,ichNaerlmFlaoyJd,a\miksas,PiokcahlaacloThcekCcPycMlesc

- A 28nm All-Digital Droop Detection and Mitigation Circuit Using A Shared Dual-Mode Delay Line with 14.8% Vmin Reduction and 42.9% Throughput Gain

Minyoung Kang, Sunghoon Kim, Youngmin Park, Sangsu Jeong, Dongsuk Jeon
Seoul National University, Seoul, Korea

- Droop Mitigation Using Critical-Path Sensors and an On-Chip Distributed Power Supply Estimation Engine in the z14TM Enterprise Processor
  Christos Vezyrtzis1, Thomas Strach2, Pierce I-Jen Chuang1, Preetham Lobo3, Richard Rizzolo4, Tobias Webel2, Pawel Owczarczyk4, Alper Buyuktosunoglu1, Ramon Bertran1, David Hui4, Susan M. Eickhoff4, Michael Floyd5, Gerard Salem6, Sean Carey4, Stelios G. Tsapepas4, Phillip J. Restle1

- On-Die Droop Detector for Analog Sensing of Power Supply Noise
  Ali Muhtaroglu, Member, IEEE, Greg Taylor, Senior Member, IEEE, and Tawfik Rahal-Arabi, Senior Member, IEEE.