

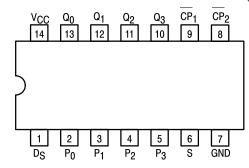
4-BIT SHIFT REGISTER

The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- · Synchronous, Expandable Shift Right
- · Synchronous Shift Left Capability
- Synchronous Parallel Load
- · Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

V_{CC} = PIN 14 GND = PIN 7

PIN NAMES

LOADING (Note a)

		пібп	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
<u>Po</u> -P3	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
<u>CP</u> 1	Serial Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
CP ₂	Parallel Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS95B

4-BIT SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX CERAMIC CASE 632-08



N SUFFIX PLASTIC CASE 646-06



D SUFFIX SOIC CASE 751A-02

ORDERING INFORMATION

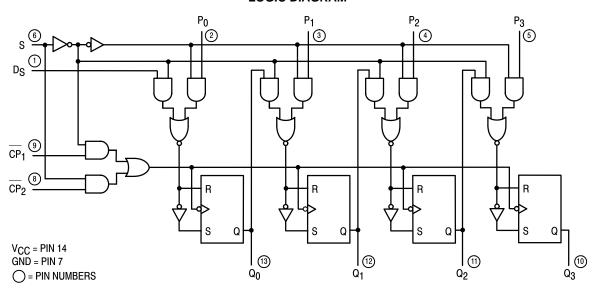
SN54LSXXJ Ceramic SN74LSXXN Plastic SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
loн	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS95B

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P₀–P₃) Data inputs and four Parallel Data outputs (Q₀–Q₃). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs (CP₁) and (CP₂). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, CP₂ is enabled. A HIGH to LOW transition on enabled CP₂ transfers parallel data from the P_0-P_3 inputs to the Q_0-Q_3 outputs.

When the Mode Control input (S) is LOW, CP1 is enabled. A

HIGH to LOW transition on enabled $\overline{CP_1}$ transfers the data from Serial input (DS) to Q₀ and shifts the data in Q₀ to Q₁, Q₁ to Q₂, and Q₂ to Q₃ respectively (right-shift). A left-shift is accomplished by externally connecting Q₃ to P₂, Q₂ to P₁, and Q₁ to P₀, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while CP2 is HIGH, or changing S from HIGH to LOW while CP1 is HIGH and CP2 is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

INPUTS					OUTPUTS			
S	CP ₁	CP ₂	DS	Pn	Q_0	Q ₁	Q_2	Q_3
L L	卢卢	X X	l h	X X	L H	q ₀ q ₀	91 91	92 92
Н	Х	۲	Х	Pn	P ₀	P ₁	P ₂	P ₃
7 7 7 7 7 7 7	L		× × × × × × × × × × × × × × × × × × ×	X X X X X	No Change No Change No Change Undetermined Undetermined No Change Undetermined			
	H 7 7 7 7	S CP1 L 7 H X 1 L 1 H 1 H 1 H 1 L 1 H 1 L 1 L	S CP ₁ CP ₂ L	S CP ₁ CP ₂ D _S L	S CP1 CP2 DS Pn L	S CP ₁ CP ₂ D _S P _n Q ₀ L	S CP1 CP2 DS Pn Q0 Q1 L L X I X L q0 L L X h X H q0 H X L X Pn P0 P1 L L L X X No Cr L H L X X No Cr L H L X X Undete L H X X No Cr L H X X Undete L H H X X Undete L H H X X Undete	S CP1 CP2 DS Pn Q0 Q1 Q2 L L X I X L q0 q1 L L X h X H q0 q1 H X L X X H Q0 q1 H X X H Q0 q1 Q1 Q1 H X X Pn P0 P1 P2 P2 L L X X X No Change No Change No Change No Change L H X X No Change No Change No Change L H X X X No Change No Ch

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

I = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

P_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS95B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Test Conditions	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V.,	Input I OW Voltage	54			0.7	V	Guaranteed Input	LOW Voltage for
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V	/ Outract III O I I V / I I I I I I		2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _I	
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
VOL	Outside I OMANd Its and			0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH}
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	per Truth Table
l	land HOLL Command				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V
ΊΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
IIL	Input HIGH Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
ICC	Power Supply Current				21	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$)

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
fMAX	Maximum Clock Frequency	25	36		MHz	
^t PLH	CP to Output		18	27	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L = 15 \text{ pF}}$
^t PHL	CF to Output		21	32	ns	2 - 10 pi

AC SETUP REQUIREMENTS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$)

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
tW	CP Pulse Width	20			ns	
t _S	Data Setup Time	20			ns	
t _h	Data Hold Time	20			ns	V _{CC} = 5.0 V
t _S	Mode Control Setup Time	20			ns	
t _h	Mode Control Hold Time	20			ns	

SN54/74LS95B

DESCRIPTION OF TERMS

SETUP TIME(ts) —is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (th) — is defined as the minimum time following

the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

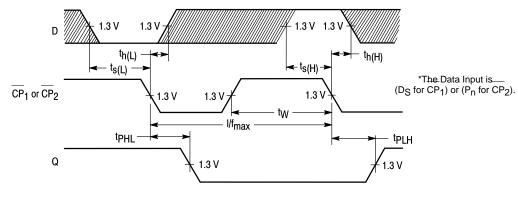


Figure 1

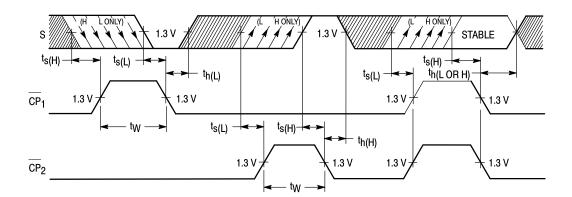
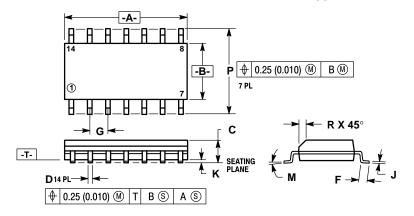
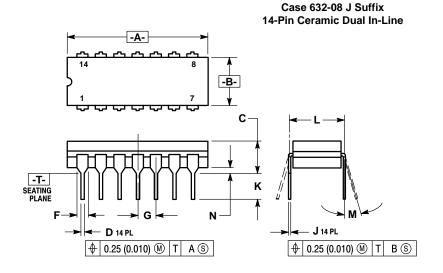


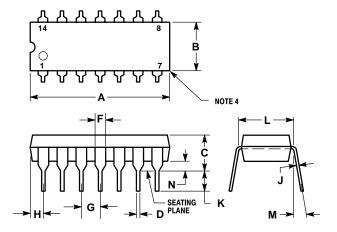
Figure 2

Case 751A-02 D Suffix 14-Pin Plastic **SO-14**





Case 646-06 N Suffix 14-Pin Plastic



NOTES:

- DIMENSIONS "A" AND "B" ARE DATUMS AND
 "T" IS A DATUM SURFACE.

 "T" IS A DATUM SURFACE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- IOLES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN
 FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE

- THE LEAD ENTERS THE CERAMIC BODY.
 5. 632-01 THRU -07 OBSOLETE, NEW STANDARD

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	19.05	19.94	0.750	0.785	
В	6.23	7.11	0.245	0.280	
С	3.94	5.08	0.155	0.200	
D	0.39	0.50	0.015	0.020	
F	1.40	1.65	0.055	0.065	
G	2.54	BSC	0.100 BSC		
J	0.21	0.38	0.008	0.015	
K	3.18	4.31	0.125	0.170	
L	7.62 BSC		0.300	BSC	
M	0°	15°	0°	15°	
N	0.51	1.01	0.020	0.040	

- NOTES:

 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

 3. DIMENSION "B" DOES NOT INCLUDE MOLD ELACH.
- FLASH
- ROUNDED CORNERS OPTIONAL. 646-05 OBSOLETE, NEW STANDARD 646-06.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	18.16	19.56	0.715	0.770	
В	6.10	6.60	0.240	0.260	
С	3.69	4.69	0.145	0.185	
D	0.38	0.53	0.015	0.021	
F	1.02	1.78	0.040	0.070	
G	2.54	BSC	0.100 BSC		
Н	1.32	2.41	0.052	0.095	
J	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	7.62	BSC	0.300	BSC	
M	0°	10°	0°	10°	
N	0.39	1.01	0.015	0.039	

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