MOTOROLA

# SN54/74LS95B

# 4-BIT SHIFT REGISTER

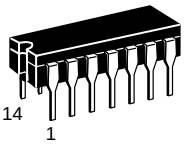
The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

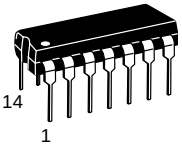
- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects

**4-BIT SHIFT REGISTER**

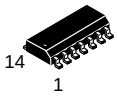
**LOW POWER SCHOTTKY**




**J SUFFIX**
CERAMIC
CASE 632-08




**N SUFFIX**
PLASTIC
CASE 646-06

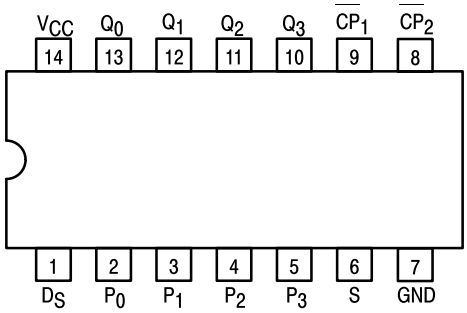



**D SUFFIX**
SOIC
CASE 751A-02

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXJ | Ceramic |
| SN74LSXXN | Plastic |
| SN74LSXXD | SOIC |

**CONNECTION DIAGRAM DIP** (TOP VIEW)




NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

$V_{CC}$ = PIN 14
GND = PIN 7

**PIN NAMES**

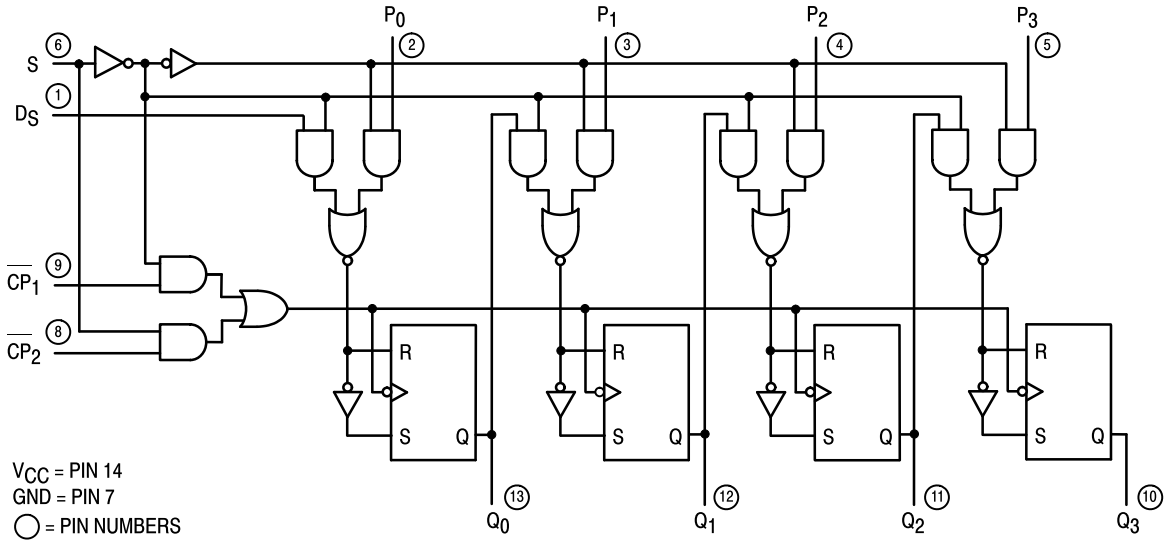
| | | **LOADING** (Note a) HIGH | LOW |
|---|---|---|---|
| S | Mode Control Input | 0.5 U.L. | 0.25 U.L. |
| $D_S$ | Serial Data Input | 0.5 U.L. | 0.25 U.L. |
| $\overline{P_0}-P_3$ | Parallel Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $\overline{CP_1}$ | Serial Clock (Active LOW Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| $CP_2$ | Parallel Clock (Active LOW Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0-Q_3$ | Parallel Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

**GUARANTEED OPERATING RANGES**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | –55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | –0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

**LOGIC DIAGRAM**




**FUNCTIONAL DESCRIPTION**

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial ($D_S$) and four Parallel ($P_0-P_3$) Data inputs and four Parallel Data outputs ($Q_0-Q_3$). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs ($CP_1$) and ($CP_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP_2}$ is enabled. A HIGH to LOW transition on enabled $\overline{CP_2}$ transfers parallel data from the $P_0-P_3$ inputs to the $Q_0-Q_3$ outputs.

When the Mode Control input (S) is LOW, $\overline{CP_1}$ is enabled. A HIGH to LOW transition on enabled $\overline{CP_1}$ transfers the data from Serial input ($D_S$) to $Q_0$ and shifts the data in $Q_0$ to $Q_1$, $Q_1$ to $Q_2$, and $Q_2$ to $Q_3$ respectively (right-shift). A left-shift is accomplished by externally connecting $Q_3$ to $P_2$, $Q_2$ to $P_1$, and $Q_1$ to $P_0$, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $CP_2$ is HIGH, or changing S from HIGH to LOW while $CP_1$ is HIGH and $CP_2$ is LOW will not cause any changes on the register outputs.

**MODE SELECT — TRUTH TABLE**

| OPERATING MODE | INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | S | $\overline{CP_1}$ | $\overline{CP_2}$ | $D_S$ | $P_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Shift | L | ↓ | X | l | X | L | $q_0$ | $q_1$ | $q_2$ |
| | L | ↓ | X | h | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | H | X | ↓ | X | $P_n$ | $P_0$ | $P_1$ | $P_2$ | $P_3$ |
| Mode Change | ↓ | L | L | X | X | No Change | | | |
| | ↑ | L | L | X | X | No Change | | | |
| | ↓ | H | L | X | X | No Change | | | |
| | ↑ | H | L | X | X | Undetermined | | | |
| | ↓ | L | H | X | X | Undetermined | | | |
| | ↑ | L | H | X | X | No Change | | | |
| | ↓ | H | H | X | X | Undetermined | | | |
| | ↑ | H | H | X | X | No Change | | | |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
$P_n$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| Symbol | Parameter | | Limits Min | Typ | Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | | | | 20 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input HIGH Current | | | | −0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 21 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | 25 | 36 | | MHz | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF |
| $t_{PLH}$<br>$t_{PHL}$ | CP to Output | | 18 | 27 | ns | |
| | | | 21 | 32 | ns | |

**AC SETUP REQUIREMENTS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_W$ | $\overline{CP}$ Pulse Width | 20 | | | ns | $V_{CC}$ = 5.0 V |
| $t_s$ | Data Setup Time | 20 | | | ns | |
| $t_h$ | Data Hold Time | 20 | | | ns | |
| $t_s$ | Mode Control Setup Time | 20 | | | ns | |
| $t_h$ | Mode Control Hold Time | 20 | | | ns | |

**DESCRIPTION OF TERMS**

SETUP TIME(ts) —is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (th) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

**AC WAVEFORMS**

The shaded areas indicate when the input is permitted to change for predictable output performance.

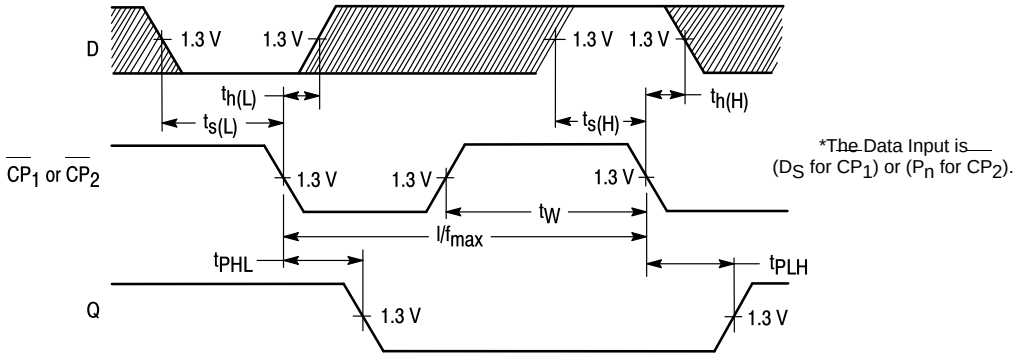



**Figure 1**

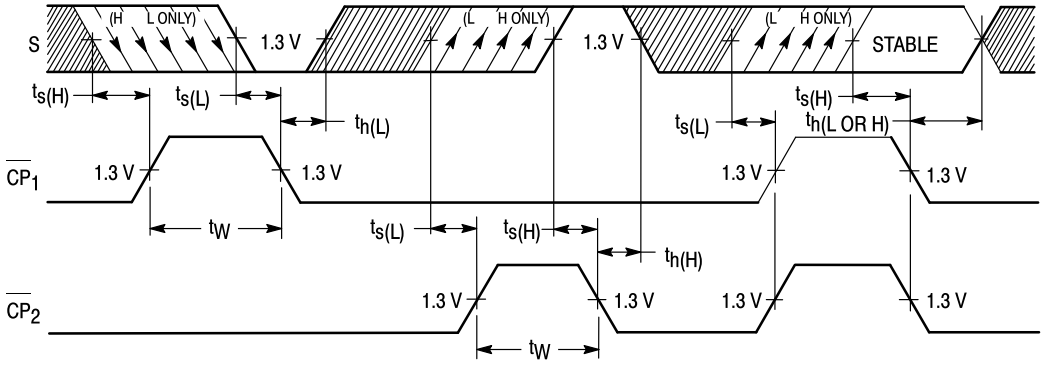
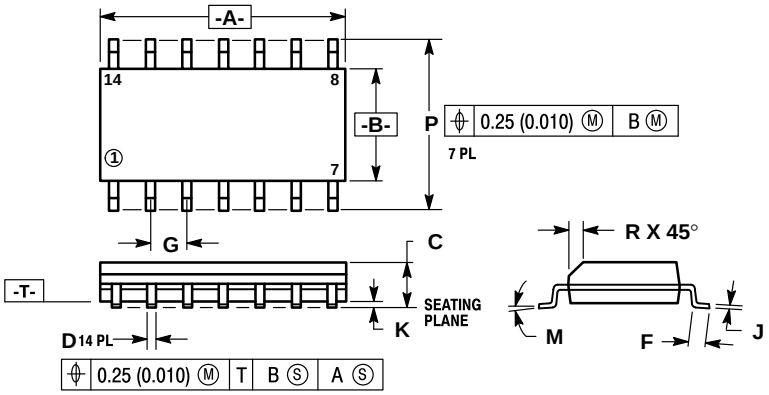



**Figure 2**

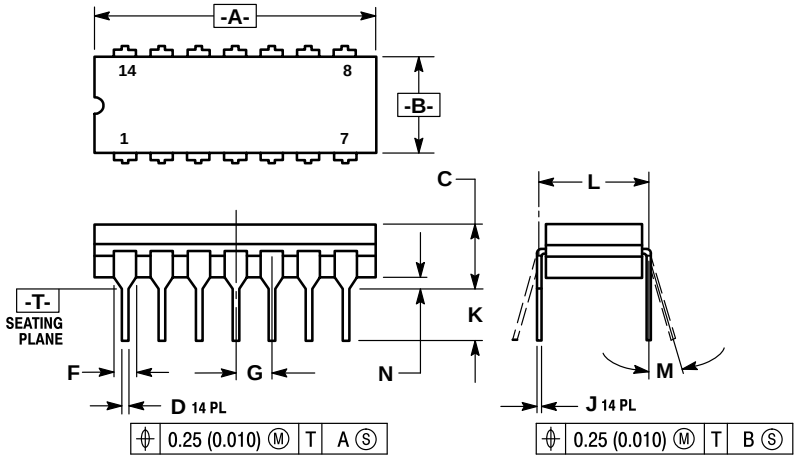
**Case 751A-02 D Suffix**
**14-Pin Plastic**
**SO-14**




NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

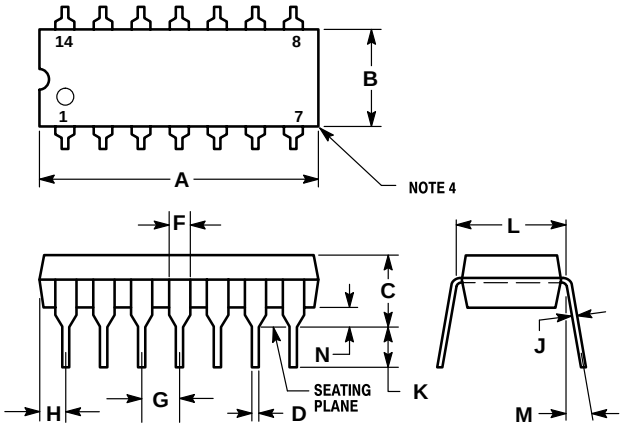
**Case 632-08 J Suffix**
**14-Pin Ceramic Dual In-Line**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.94 | 0.750 | 0.785 |
| B | 6.23 | 7.11 | 0.245 | 0.280 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.39 | 0.50 | 0.015 | 0.020 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 3.18 | 4.31 | 0.125 | 0.170 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.01 | 0.020 | 0.040 |

**Case 646-06 N Suffix**
**14-Pin Plastic**




NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. 646-05 OBSOLETE, NEW STANDARD 646-06.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 18.16 | 19.56 | 0.715 | 0.770 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.69 | 4.69 | 0.145 | 0.185 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.32 | 2.41 | 0.052 | 0.095 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.39 | 1.01 | 0.015 | 0.039 |

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