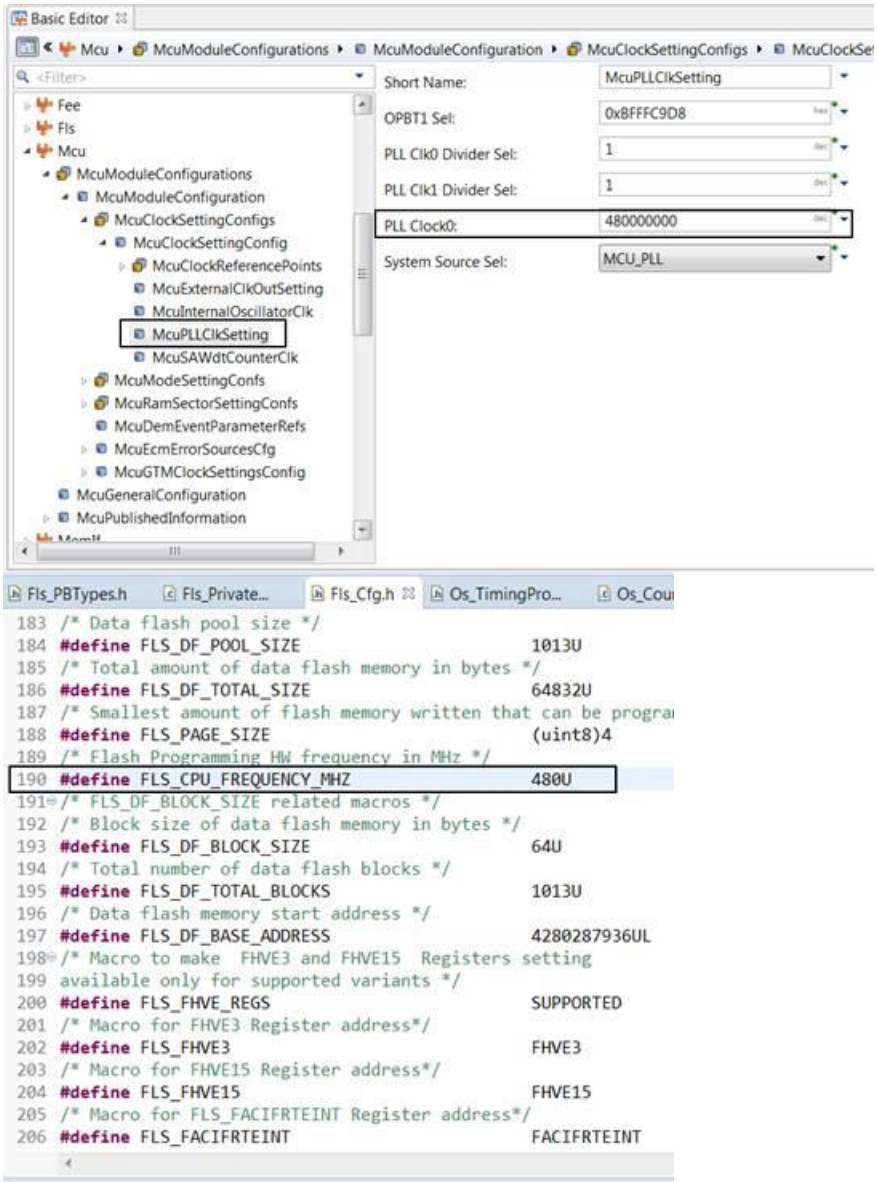
Readme CBD1601056

Note / Integration hints

Value of PLL_CLOCK0 is directly getting assigned to CPU frequency in code.



The value of “FLS_CPU_FREQUENCY_MHZ” in **Fls_Cfg.h** should be corrected manually by the correct value of CPU frequency.

Current SIP is tested with “FLS_CPU_FREQUENCY_MHZ” 240U. Every time you generate the project need to replace the value of “FLS_CPU_FREQUENCY_MHZ” in code ‘Fls_Cfg.h’. This is the known issue; developers are currently working on it.

Limitation / Restriction

1) This SIP currently supports only scalability class SC3 OS. In the next delivery we will provide scalability class SC4 OS. This limitation is because of the availability of system timer channels in OS for use. SC4 requires at least 2.

2) Following compiler options are not getting identified:

```
ccrh850: Warning: file '?shorten_loads' ignored with these options
ccrh850: Warning: file '?shorten_moves' ignored with these options
ccrh850: Warning: file '?delete' ignored with these options
ccrh850: Warning: file '?nofloatio' ignored with these options
ccrh850: Warning: file '?reserve_r2' ignored with these options
```