

November 1988 Revised November 1999

# 74AC04 • 74ACT04 Hex Inverter

#### **General Description**

The AC/ACT04 contains six inverters.

#### **Features**

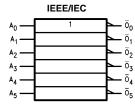
- I<sub>CC</sub> reduced by 50% on 74AC only
- Outputs source/sink 24 mA
- ACT04 has TTL-compatible inputs

# **Ordering Code:**

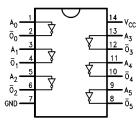
Order Number	Package Number	Package Description					
74AC04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body					
74AC04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74AC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74AC04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide					
74ACT04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body					
74ACT04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74ACT04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide					

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)

### **Logic Symbol**



### **Connection Diagram**



# **Pin Descriptions**

Pin Names	Description
A <sub>n</sub>	Inputs
$\overline{O}_n$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

#### **Absolute Maximum Ratings**(Note 1)

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>)

DC Input Diode Current (I<sub>IK</sub>)

 $V_I = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V<sub>I</sub>) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current (I<sub>OK</sub>)

 $V_{O} = -0.5V$ -20 mA  $V_O = V_{CC} + 0.5 V$ +20 mA

DC Output Voltage (V<sub>O</sub>) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source or Sink Current  $(I_O)$  $\pm 50 \text{ mA}$ 

DC V<sub>CC</sub> or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ ) ±50 mA Storage Temperature (T<sub>STG</sub>) -65°C to +150°C

Junction Temperature (T<sub>J</sub>)

PDIP 140°C

#### **Recommended Operating Conditions**

Supply Voltage (V<sub>CC</sub>)

AC 2.0V to 6.0V ACT 4.5V to 5.5V Input Voltage (V<sub>I</sub>) 0V to V<sub>CC</sub> Output Voltage (V<sub>O</sub>) 0V to  $V_{CC}$ Operating Temperature (T<sub>A</sub>) -40°C to +85°C

Minimum Input Edge Rate  $(\Delta V/\Delta t)$ 

**AC Devices** 

 $V_{\mbox{\footnotesize{IN}}}$  from 30% to 70% of  $V_{\mbox{\footnotesize{CC}}}$ 

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

**ACT Devices** 

V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

#### **DC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub>	$V_{CC}$ $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Syllibol		(V)	Тур	Gu	aranteed Limits	Uiilis	Conditions	
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$	
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		0.36	0.44		I <sub>OL</sub> = 12 mA	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)	
I <sub>IN</sub>	Maximum Input	5.5		±0.1	±1.0	μА	$V_{I} = V_{CC}$ , GND	
(Note 4)	Leakage Current	3.3		±0.1	±1.0	μΑ	VI = VCC, CIAD	
I <sub>OLD</sub>	Minimum Dynamic Output Current	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	(Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent	5.5		2.0	20.0	μА	$V_{IN} = V_{CC}$	
(Note 4)	Supply Current	0.0		2.0	23.0	μΛ	or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4:  $I_{\text{IN}}$  and  $I_{\text{CC}}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\text{CC}}$ .

Symbol	Parameter	$v_{cc}$	$T_A = -$	$+25^{\circ}$ C $T_{A} = -40^{\circ}$ C to $+85^{\circ}$ C		Units	Conditions
		(V)	Тур	Gı	aranteed Limits	Units	Conditions
V <sub>IH</sub>	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0	V	or V <sub>CC</sub> – 0.1V
V <sub>IL</sub>	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V
	Input Voltage	5.5	1.5	8.0	0.8	V	or V <sub>CC</sub> – 0.1V
V <sub>OH</sub>	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
	Output Voltage	5.5	5.49	5.4	5.4	V	1 <sub>OUT</sub> = -30 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 5)}$
V <sub>OL</sub>	Maximum LOW Level	4.5	0.001	0.1	0.1		
	Output Voltage	5.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5 5.5		0.36 0.36	0.44 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}0 = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 5)}$
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μА	$V_I = V_{CC}$ , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1V$
I <sub>OLD</sub>	Minimum Dynamic Output Current	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	(Note 6)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μА	V <sub>IN</sub> = V <sub>CC</sub> or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

# **AC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub> (V)	$T_A = +25^\circC$ $C_L = 50\;p$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$		Units
		(Note 7)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	4.5	9.0	1.0	10.0	20
		5.0	1.5	4.0	7.0	1.0	7.5	ns
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	4.5	8.5	1.0	9.5	20
		5.0	1.5	3.5	6.5	1.0	7.0	ns

Note 7: Voltage Range 3.3 is  $3.3V \pm 0.3V$ Voltage Range 5.0 is  $5.0V \pm 0.5V$ 

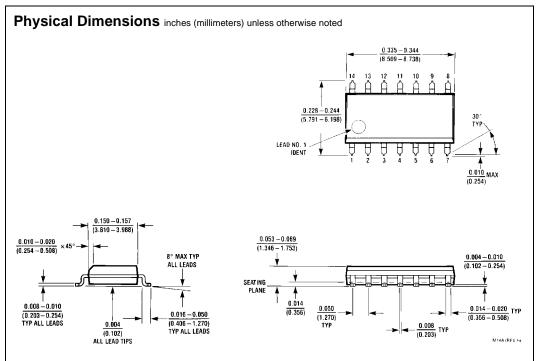
# **AC Electrical Characteristics for ACT**

		$V_{CC}$ $T_A = +25^{\circ}C$				T <sub>A</sub> = -40°C to +85°C		
Symbol	Parameter	(V)	C <sub>L</sub> = 50 pF			C <sub>L</sub> = 50 pF		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	1.0	6.0	8.5	1.0	9.0	ns
t <sub>PHL</sub>	Propagation Delay	5.0	1.0	5.5	8.0	1.0	8.5	ns

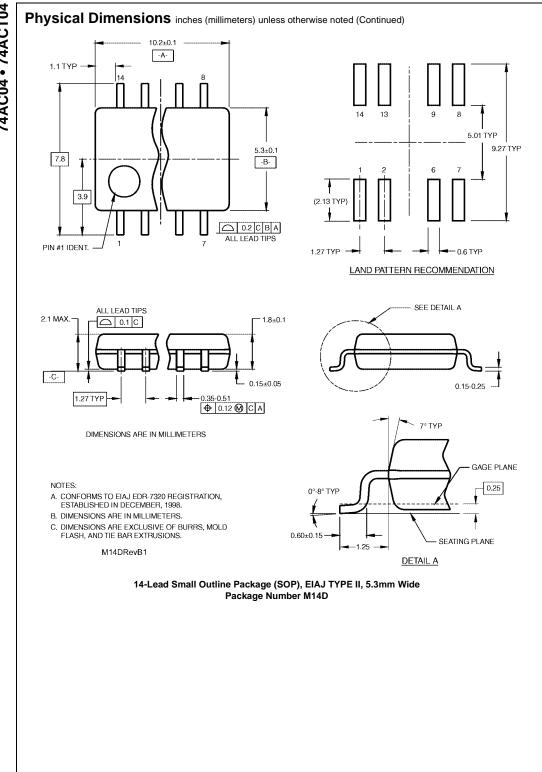
Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

# Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
V <sub>CC</sub>	Power Dissipation Capacitance	30.0	pF	V <sub>CC</sub> = 5.0V

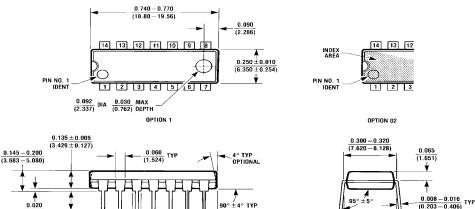


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body Package Number M14A



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 -A-7.72 4.16 6.4 4.4±0.1 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. SEE DETAIL A ALL LEAD TIPS 1.2 MAX - 0.90 +0.15 - 0.09-0.20 -C-- 0.10±0.05 0.19 - 0.30 **♦** 0.13 **№** A B**⑤** C**⑤** -12.00° TOP & BOTTOM R0.09 MIN-GAGE PLANE NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. 0.25 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. -1.00-R0.09 MIN MTC14RevC3 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

 $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 

 $0.100 \pm 0.010$ 

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0.280 (7.112)-MIN

 $0.325 + 0.040 \\
-0.015 \\
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 (8.255 + 1.016) \\
-0.381)$ 

N14A (REV.F)

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