[2] Application Notes and Technical Articles

1. The CCD Image Sensor

The CCD (charge-coupled device), a new functional semiconductor device, was developed in 1970 by Dr. Boyle at the Bell Research Laboratory, U.S.A.

As shown in Figure 1.1, it consists of a MOS capacitor with an electrode attached on top of the silicon dioxide on the semiconductor substrate surface. When voltage is applied between the electrode and the substrate, a depletion layer is formed in the region near the interface of the silicon dioxide and semiconductor interface, causing this region to become a low-energy-level potential well for the minority carrier. If a signal charge generated by light radiation is injected into this potential well, these signals are temporarily stored as analog quantities.

An explanation of the operating principle of the CCD analog shift register is as follows. The first case is an introductory explanation of three-phase driving. As shown in Figure 1.2, multiple MOS capacitor units are arranged in close proximity and signal charge is transferred from one MOS capacitor to the next. In other words, when the signal charge stored under Electrode $\phi 1$ at time t1 applies positive voltage to Electrode $\phi 2$, a portion of the signal charge shifts beneath Electrode $\phi 2$ (time: t2). Furthermore, decreasing the positive voltage of Electrode $\phi 1$ (time: t3) shifts the entire signal charge beneath Electrode $\phi 2$ (time: t4). When this operation is performed repeatedly, charge is transferred.

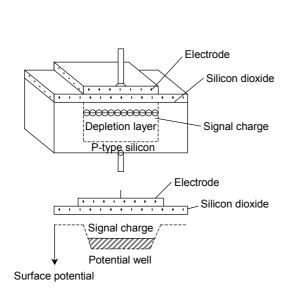


Figure 1.1 Basic Structural Diagram

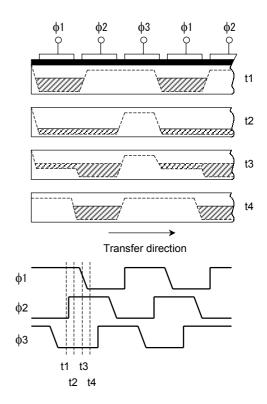


Figure 1.2 Operating Principle of CCD
Analog Shift Register

2. Principles of the CCD Linear Image Sensor

The CCD Image Sensor consists of three main regions: the Photosensitive Region, Transfer Region and Output Circuit Region. Figure 2.1 shows how a CCD image sensor is configured.

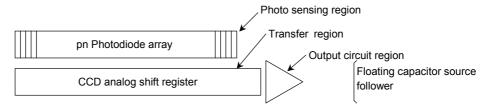


Figure 2.1 Configuration of a CCD Image Sensor

2.1 Photosensing Region

This region converts light energy into signal charge and temporarily stores the signal charge obtained.

Figure 2.2 shows an equivalent circuit which represents the theoretical configuration of the photosensing region. This region consists of photodiodes, MOS capacitors and shift gates. The light energy is photoelectrically converted by the photodiode to the signal charge, which is then stored in the MOS capacitor. This signal charge is transferred to the transfer region through the shift gate. Figure 2.3 shows a cross-section of the photosensing region and domonstrates its operation.

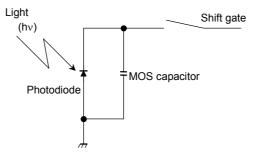


Figure 2.2 Theoretical Configuration of the Photosensing Region

2.2 Transfer Region

The tansfer region's scanning function transfers each signal charge generated in the photosensing region to the output circuit in turn. A simple two-phase drive is normally used with the clock pulses for charge transfer. In this case, as shown in Figure 2.4, one potential well stores charge and the neighboring one has isolates the charge for each pixel. In other words, since two wells operate as a unit, one pixel in the photosensing region corresponds to two potential wells. Therefore, a single pixel of the picture signal is output on each transfer clock pulse.

There are two configurations of CCD analog shift register: a single-channel type and a dual-channel type (TCD1208AP etc.). Figure 2.5 and Figure 2.6 show the two configurations. In the case of a dual channel, two registers alternately receive the signal charge transfer from successive pixels (odd-numbered pixels (1), (3), (5), (7) and even-numbered pixels (2), (4), (6), (8)).

A dual-channel CCD analog shift register is able to increase the pixel density and decrease the number of transfer steps to half, leading to reduction of charge loss during transfer. Moreover, a buried-channel CCD (buried CCD) structure is useful for reducing the transfer loss caused by such factors as charge traps in the vicinity of the semiconductor surface. Figure 2.7 shows a structural diagram of a cross-section of a buried-channel CCD.

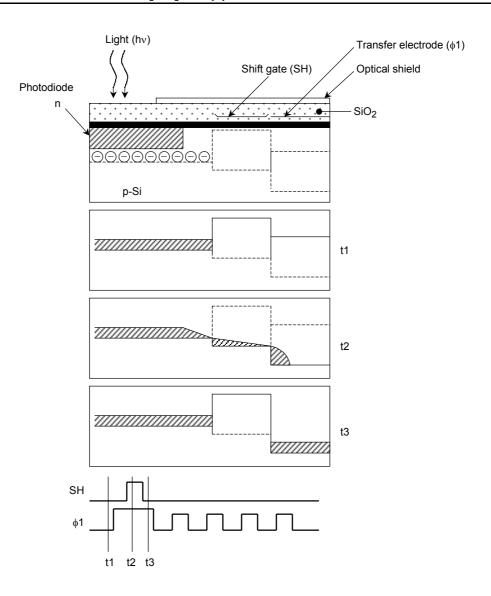


Figure 2.3 Structural Cross-Section and Operation of the Photosensing Region

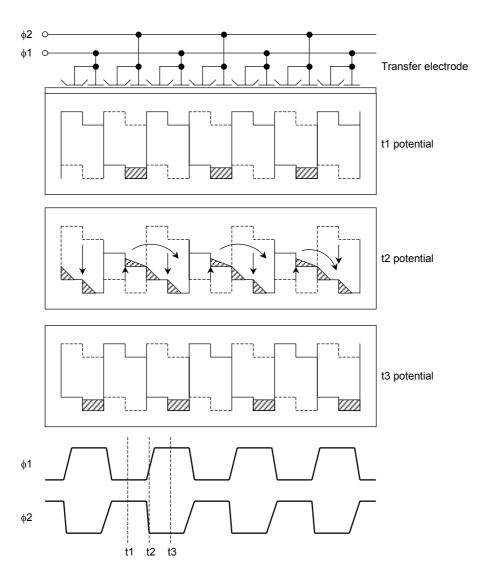


Figure 2.4 Operation of Two-Phase Drive

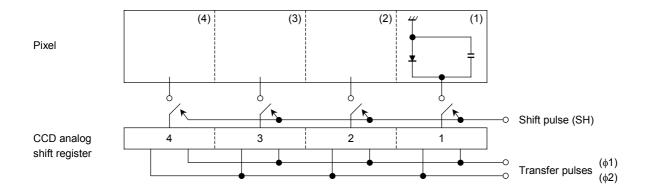


Figure 2.5 Configuration of a Single-Channel Register

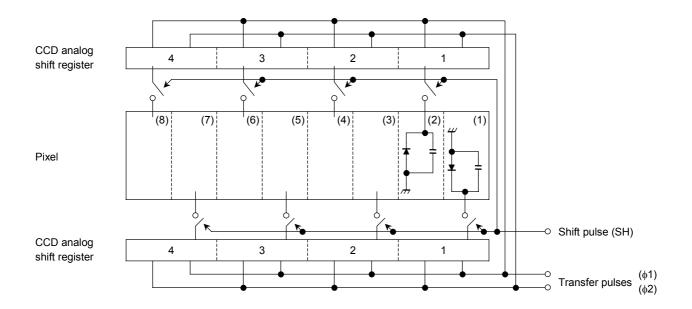


Figure 2.6 Configuration of a Dual-Channel Register

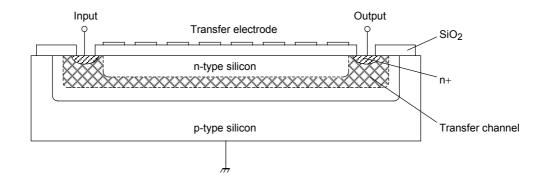


Figure 2.7 Structural Cross-Section of a Buried-Channel CCD

2.3 Output Circuit Region

The output region has a function to convert the signal charge which is transferred from the transfer region into voltage. The voltage of the floating capacitor is varied according to the signal charge.

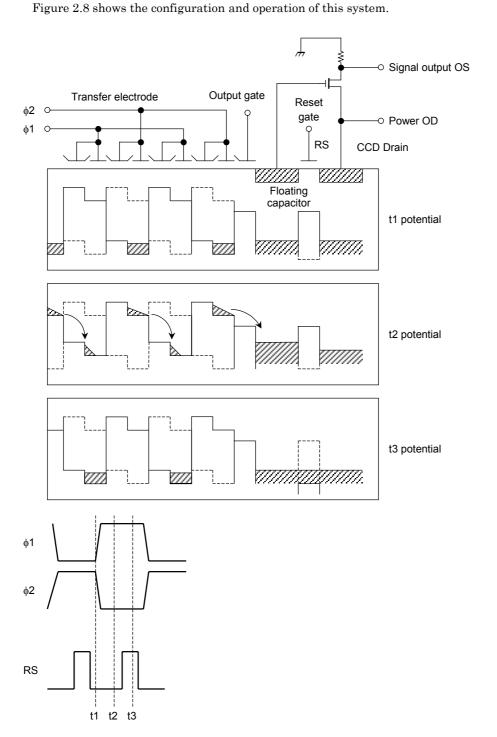


Figure 2.8 Configuration and Operation of the Output Circuit Region

2.4 Actual Operation

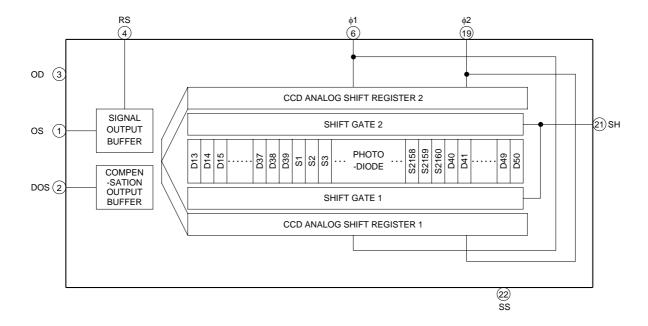
Following is an explanation on the actual operation using the TCD1208AP as an example.

Figure 2.9 shows a device configuration diagram of the 2160-pixel linear image sensor TCD1208AP.

The pn photodiode in the photosensing region contains 27 pixels (D13 to D39) on the front and 11 pixels (D40 to D50) on the rear, besides the 2160 pixels for the effective signal output.

Pixels D13 to D36 of the photodiode are covered with an optical shield, with the result that they are photosensitive.

Thus, this part can be used as the reference optical black level for use in detecting dark output. Though bits D0 to D12 contain no actual pixels, registers representing 13 pixels link the photo-sensing region and the output circuit region.



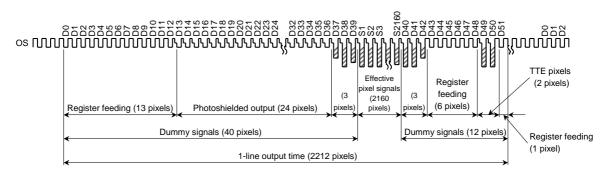


Figure 2.9 Device Configuration of the CCD Linear Sensor (TLD1208AP)

[2] Application Notes and Technical Articles

The DC power supply and pulse supply terminals required to operate the CCD image sensor are the power supply (OD terminal), ground (SS terminal), shift pulse (SH terminal), transfer pulses (ϕ 1, ϕ 2 terminals) and reset pulse (RS terminal).

The shift pulse SH switches the shift gate ON or OFF. Since the entire signal charge Q of the photo sensing region is transferred to the transfer region when the shift gate is switched ON, the integration time of the signals is the same as the cycle of the shift pulse SH. After the shift gate is switched OFF, the signal charge Q is sequentially transferred to the shift register by transfer pulses $\phi 1$ and $\phi 2$, and the signal charge Q flows into the floating capacitor through the output gate OG. This signal charge Q varies the voltage of the floating capacitor by $\Delta V = Q/C$. Variation in voltage is linked to the gate of the source follower as a preamplifier, changed to a current flowing to the load resistance, and output from the OS terminal as voltage signals.

To detect the signal for the next pixel, the voltage of the floating capacitor must be restored to its initial status. To do this, apply the reset pulse RS, switch the reset transistor to ON, and set the voltage of the floating capacitor to the voltage of the CCD drain.



3. Characteristics of the CCD Linear Image Sensor

3.1 Sensitivity

Sensitivity is the quantitative ratio of output voltage to exposure value and, from the standpoint of device configuration, is the product the photoelectric conversion gain and the output region gain. Although V/lx·s is widely used as the unit, the sensitivity varies widely according to the light source because the photoelectric conversion gain depends on the wavelength of the light source (i.e., it exhibits a spectral response). Illuminance is often converted to irradiance; see Figure 3.1 for reference.

Figure 3.2 shows the photoelectric conversion characteristic (i.e., input/output characteristic) of the CCD image sensor. Since the constant exposure value (illuminance \times integrationtime) yields a constant output, Figure 3.3 can be derived by putting the exposure value on the transverse axis. The linear line represents the expression $y = ax^{\gamma} + b$.

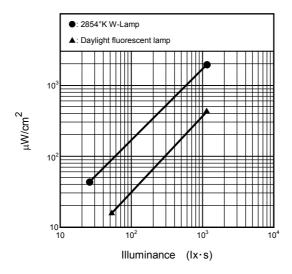


Figure 3.1 Conversion Table of Irradiance Illuminance (from measurements)

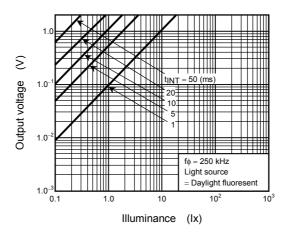


Figure 3.2 Photoelectric Conversion Characteristic (TCD1208AP)

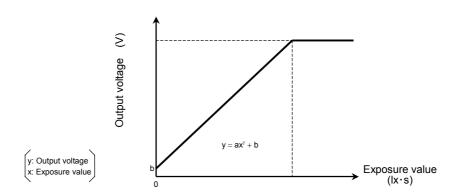


Figure 3.3 Photoelectric Conversion Characteristic

Slope parameter a represents the sensitivity. b is the output voltage when the exposure equals 0 (when dark) and is referred to as the dark output voltage. The value of γ is approximately 1. In addition, the exposure value at the knee point of this characteristic is referred to as the saturation exposure light quantity; the output signal is saturated even when the exposure value is increased above this level. The voltage at this time is called the saturation output voltage.

3.2 Spectral Response

Spectral response is the comparative response to exposure to light of different wavelengths. Because the structure of the photosensing region consists of a pn photodiode, its response to blue is much better than that of conventional MOS diode type sensors. Furthermore, the use of the MD (micro defect) wafer and p-Well structures suppresses sensitivity to long light wavelengths in order to better match the human visible range. Figure 3.4 shows the spectral response of a device that uses the MD wafer and p-Well.

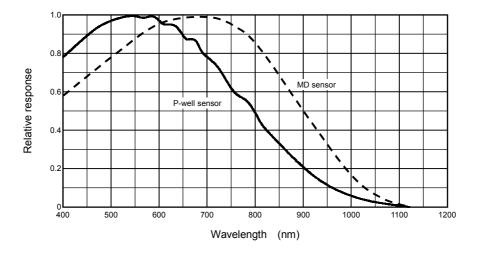


Figure 3.4 Spectral Response Characteristic

3.3 Saturation Output Voltage

When the output voltage reaches the saturation output voltage, it will not increase, even if further light is supplied, as shown in Figure 3.3. However, this does not mean that signal charge is no longer generated by the pn photodiode. The signal charge generated by the pn photodiode is stored in the potential well shown in Figure 1.2; if the quantity of signal charge is larger than the well's capacity, the signal charge overflows out of the well, diffusing to the neighboring well or to other parts. This causes not only loss of signal charge information but also spillover of charge into some areas where no

signal should exist, resulting in a false signal output. This situation is shown in Figure 3.5.

The charge diffused within the device is not eliminated even if the quantity of light injected into the image sensor is reduced. For example, when a document is scanned, black areas of the page may be falsely read as gray areas if the neighboring white areas cause saturation.

Thus, for proper operation of the image sensor, an operating condition must be stipulated to the effect that the output voltage shall never exceed the saturation output voltage.

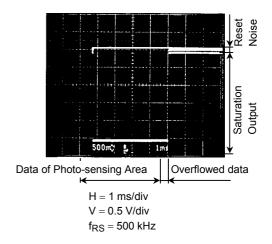


Figure 3.5 TCD1208AP Saturation
Output Waveform

3.4 Photoresponse Non-Uniformity (PRNU)

Photoresponse non-uniformity is the percentage of scattering in the response to each pixel. For many products, it is defined by the expression:

$$PRNU = \frac{\Delta x}{\overline{x}} \times 100(\%)$$

where \overline{x} is the average value for the output amplitude of all active pixels when a light with uniform luminosity is projected onto the photosensitive surface, and where Δx is the absolute value of the difference between the maximum (minimum) pixel output amplitude value and \overline{x} .

For some products, it is defined by the expression:

$$PRNU = \frac{x_{max} - x_{min}}{\overline{x}} \times 100(\%) \text{ (x}_{max} \cdot \text{ maximum output, x}_{min} \cdot \text{ minimum output)}$$

The PRNU value varies according to the light source used. For example, a daylight fluorescent lamp generally exhibits a lower PRNU value than a tungsten lamp. This is due to the fact that the tungsten lamp's infrared rays, which have a longer wavelength than visible light, penetrate the bottom of the pixel through which they enter the substrate. Each infrared ray generates an electron in the depths of the substrate. Sometimes this electron is absorbed by a neighboring pixel, not the one through which the ray originally

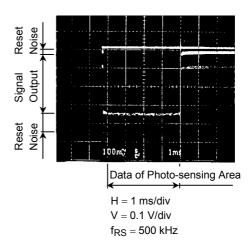


Figure 3.6 TCD1208AP Signal Output Waveform

entered the substrate. Figure 3.6 is an example output waveform showing the photosensitive non-uniformity of the TCD1208AP with respect to a daylight fluorescent lamp. Another factor in PRNU deterioration is the presence of scratches or stains on the image sensor's window glass. Even when scratches of the same size are present, the PRNU may indicate a different value from the optical system (the f-number of the lens).

3.5 Resolution (MTF)

Resolution is the ability to reproduce a detailed section of a photographed subject. Each photosensitive pixel of the CCD image sensor is clearly separated so that the sampling theorem is applied between these pixels and the input light images, allowing the resolution limit as determined by the Nyquist limit. Figure 3.7 shows the input light image projected on pixels through a lens, the pixels and their output level. The finer the input pattern, as shown in (a), (b) and (c), the smaller the level difference between white and black for the image signal becomes. The MTF (modulation transfer function) is the ratio of output signal contrast between black and white to input image contrast. This is a function of the spatial frequency, decreasing as the frequency rises.

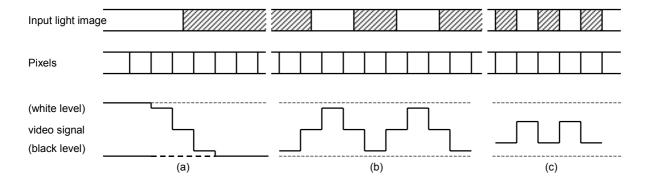


Figure 3.7 Difference in Output Level Due to Difference in the Spatial Frequency of the Input Light Image

The MTF is actually dependent on both the lens and the image sensor. If mirrors are used to reflect light onto the CCD, this affects the MTF too. Thus, the MTF of a reader using the CCD image sensor is the product of the lens MTF and the sensor MTF. In this case, the MTF is a response to the sine wave shown in Figure 3.9, not to the rectangular wave in Figure 3.8. The reason is as follows.

Firstly, if the original has a light distribution with a rectangular waveform, it is distorted through by the lens as shown in Figure 3.8 (b). Since the distorted image is projected onto the sensor, the picture data input to the sensor no longer has a rectangular waveform, removing the need to represent the sensor MTF lay a rectangular wave response. On the other hand, when the original has a light distribution with a sine waveform, as shown in Figure 3.9 (a), its shape does not change, even when passed through the lens; rather, it has a smaller amplitude due to the lens MTF. From this it follows that if this data is input into the sensor, output determined by the sensor MTF can be obtained.

Our CCD image sensor defines a sensor (a response to the sine wave) only, as shown in Figure 3.10. In this figure, the spatial frequency is defined for the sensor pixel, and the normalized spatial frequency is normalized by the spatial frequency at the Nyquist limit (corresponding to Figure 3.7 (c)).

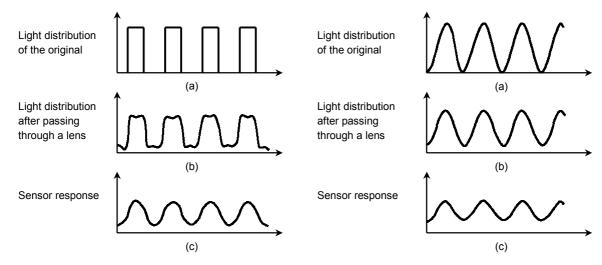


Figure 3.8 MTF of the Rectangular Wave Response

Figure 3.9 MTF of the Sine Wave Response

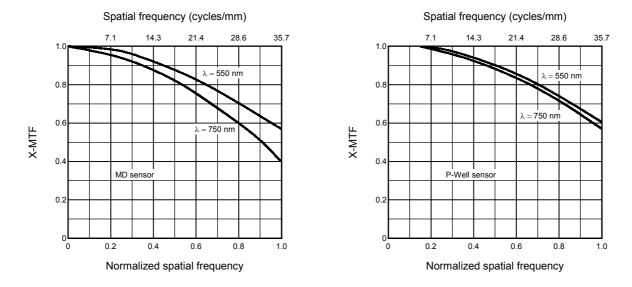


Figure 3.10 Modulation Transfer Function of X-Direction

The MTF of the CCD image sensor is dependent on the wavelength of the light source, deteriorating as the wavelength increases. The longer the wavelength, the deeper inside the silicon substrate the photoelectric conversion of the light takes place. Deterioration is caused by the diffusion effect of the carriers in the process of reaching the vicinity of the substrate surface from a deeper level (see Figure 3.11 (a)). The p-well structure is effective in preventing the deterioration of resolution due to the carrier diffusion effect. This structure is made by putting a thin p-type semiconductor layer on an n-type silicon substrate surface, then reverse-biasing this pn-junction; it acts as a drain for the carriers generated in the deep section of the substrate (see Figure 3.11) (b)).

Our measuring method for the MTF is based on the response obtained by shifting slit light onto the sensor pixel as shown in Figure 3.12. In this way the MTF for the main and sub-scanning directions can be obtained.

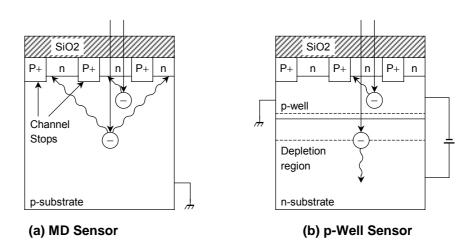


Figure 3.11 Sensor Cross Section

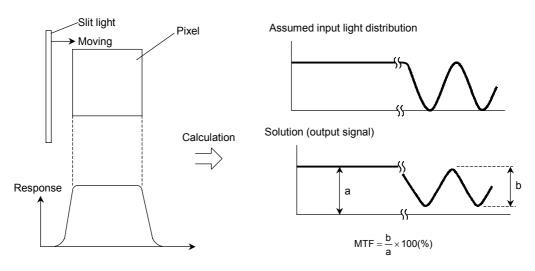


Figure 3.12 MTF Measuring Method

3.6 Dark Signal

A dark signal is the output voltage when the input light is 0.

There are two dark signals: one occurs in the photosensing region (the photodiode and storage electrode) and the other occurs in the transfer region (the CCD analog shift register). The electric charge is constant and the dark signal is proportional the to the operating time of each region. That is, in the photosensing region, a dark current occurs under the photodiode and storage electrode, and its magnitude is proportional to the integration time tINT (shift pulse cycle). In the transfer region, a dark current occurs under the transfer electrode, and its magnitude is proportional to the signal transit time of the CCD analog shift register area: i.e., it is proportional to the product of the clock pulse cycle and the number of shift register transfer steps. Therefore, the dark signal increases as the operating speed decreases. Furthermore, the dark signal output doubles with approximately each 8°C increase in ambient temperature. As previously described, as the operating speed decreases and the ambient temperature rises, the dark signal increases and the dynamic range of the video signals decreases. Figure 3.13 shows the dark signal temperature characteristic of the TCD1208AP. Figure 3.14 shows a dark signal waveform. The dark signals for the different effective pixels (pixels prefaced by an "s"-see Figure 2.9) are not identical. VDRK is defined as the average dark signal value of all the effective pixels; VMDK is defined as the maximum dark signal value out of all the effective pixels.

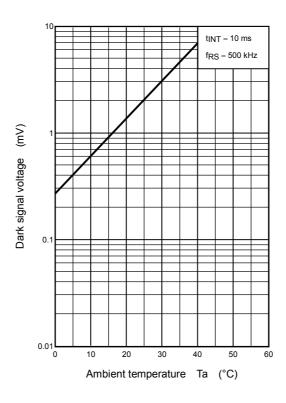


Figure 3.13 Temperature Characteristic of Dark Signal Output

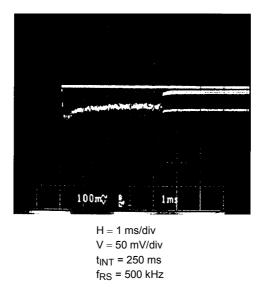


Figure 3.14 TCD1208AP Dark Signal Output Waveform

3.7 Transfer Efficiency

The CCD image sensor transfers the charge generated by a pn photodiode to the output circuit region by transferring potential wells step by step, as shown in Figure 2.4. When charge is transferred from one well to the next, the transfer is not 100% efficient; a fraction of the charge remains in the original well. The transfer efficiency is defined as the percentage of the charge transferred to the next well divided by the charge contained in the original well. The total transfer efficiency is defined as the percentage of the charge transferred to the final well.

Figure 3.15 shows a model where ε is the transfer efficiency for one step. If ε is constant for all steps, the charge Q in Figure 3.15 (a) will attain the state shown in Figure 3.15 (b) after n transfer steps. The charge distribution is given by the following.

expression:

$$Q0 = Q \times \varepsilon n$$

$$Qi = Q \times nCi \times \epsilon^{n-i} \times (1-\epsilon) i \text{ (here } i = 1, 2, 3, \dots n-1)$$

As shown above, this can be represented by a binominal distribution. Table 3.1 shows the relation between the transferred charge Q and the total transfer efficiency TTE, after 2048 transfer steps. TTE is defined using Q0 and Q1, and disregards Q2 and following Q values.



(a) State before Transfer

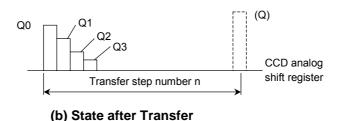


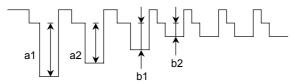
Figure 3.15 Explanatory Model of Total Transfer Efficiency

Table 3.1

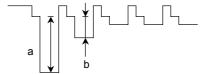
Transfer Efficiency ε	Q	Q0	Q1	Q2	TTE
99.999	100	98.0	2.0	0.0	98.0
99.997	100	94.0	5.8	0.2	94.2
99.996	100	92.1	7.5	0.3	92.5

TTE =
$$\frac{Q0}{Q0 + Q1} \times 100(\%)$$

Deterioration in transfer efficiency causes deterioration in the resolution of the video signals, due to the increase in crosstalk with neighboring pixels. Figure 3.16 shows the measurement from an actual CCD image sensor. Please note that a dual-channel CCD has two CCD analog shift registers and that the levels from each register are output alternately. Thus consecutive outputs are not from the same signal.



a1 is the last bit in register 1 and a2 the last bit in register 2 for photosensitive pixels



a is the last bit for photosensitive pixels

TEE1=
$$\frac{a1}{a1+b1} \times 100(\%)$$

TEE2 =
$$\frac{a2}{a2 + b2} \times 100(\%)$$

(a) Dual-Channel CCD

 $TTE = \frac{a1}{a+b} \times 100(\%)$

(b) Single-Channel CCD

Figure 3.16 Method for Measuring the Total Transfer Efficiency

3.8 Image Lag

In the photosensing region, the signal charge under the storage electrode or the photodiode is not completely shifted to the transfer region. Refer to Figure 2.3. For example, when the sensor reads a white area on the document in the first scanning cycle, and then this sensor reads a black area in the second scanning cycle, the sensor does not output a black level of 100% as the result of the second scan. Instead if outputs a gray level. The level of image lag depends on the opening time of the shift gate (= high level period of SH). The relation ship is shown in Figure 3.17.

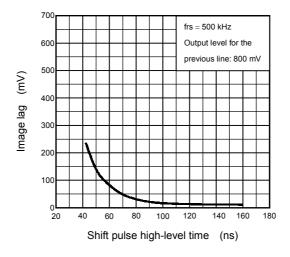


Figure 3.17 Relation Ship between Shift Pulse Time and Image Lag

4. Using a CCD Linear Image Sensor

This section describes how to use a typical CCD image sensor, the TCD1208AP.

4.1 Power Supply

The standard voltage mentioned in the technical data must be supplied. This voltage is supplied via the power terminal OD to each part of the chip.

The stability of the power supply voltage greatly affects the output signals. The varying gain of the output voltage VOS relative to the power supply voltage VOD is about 0.4; for example, when there is 1-V spike-type noise in the OD terminal, noise of approx. 0.4 V occurs in image signals. It is important to stabilize the DC voltage supplied to the OD terminal in order to generate image signals with a high signal-to-noise ratio.

If there are multiple power terminals or ground terminals, every terminal must be wired so as to provide the same electrical potential. Pins masked NC are unconnected; however, it is recommended that they be earthed.

4.2 Drive Pulse

a. Drive pulse

Also, for drive pulses, the amplitude values described in the technical data must be supplied. For the TCD1208AP, the transfer electrode capacity of the CCD analog shift register is up to 300 pF, requiring the selection of a clock driver capable of fully driving this capacity (see Figure 5.2). Moreover, because large currents momentarily flow in and out of the CCD from the clock driver, full attention must be paid to the wiring between the clock driver and the CCD, which should be of low impedance.

Look out for undershoot in the clock pulse waveform. Because the diodes that prevent destruction of the electrodes of the CCD image sensor are forward-biased by the undershoot, current flows in reverse and appears as noise on the clock pulse.

The timings of the shift pulse, transfer pulse and reset pulse are prescribed and should be set accordingly. Moreover, you must not stop the clock pulses except for the SH input period, or picture blemishes will occur. The recommended duty cycle for clock pulses is 50%, to prevent TTE deterioration.

Table 4.1 lists the electrical characteristics of the TCD1208AP, Table 4.1 is the timing diagram, and Table 4.2 describes the pulse waveforms.



Table 4.1 Electrical Characteristics of the TCD1208AP

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Unit	
Clock pulse voltage	V_{ϕ}			
Shift pulse voltage	V _{SH}	-0.3~8	V	
Reset pulse voltage	V _{RS}	-0.5~0	V	
Power supply voltage	V _{OD}			
Operating temperature	T _{opr}	-25~60	°C	
Storage temperature	T _{stg}	-40~100	°C	

Operating Conditions

Characteris	stic	Symbol	Min	Тур.	Max	Unit
Clock pulse voltage	H level	Vφ	4.5	5	5.5	V
	L level		0	0	0.3	
Shift pulse voltage	H level	V _{SH}	4.5	5	5.5	V
Shirt pulse voltage	L level		0	0	0.3	
Reset pulse voltage	H level	V _{RS}	4.7	5	5.5	V
	L level		0	0	0.3	
Power supply voltage		V _{OD}	4.7	5.0	5.3	V

Clock Characteristics

Characteristic	Symbol	Min	Тур.	Max	Unit
Clock pulse frequency	fφ	0.15	0.5	1.0	MHz
Reset pulse frequency	f _{RS}	0.3	1.0	2.0	MHz
Clock capacitance	C_{ϕ}	_	200	300	pF
Shift gate capacitance	C _{SH}	_	100	200	pF
Reset gate capacitance	C _{RS}	_	10	30	pF

b. Stopping the drive pulse

The drive pulses $(\phi 1, \phi 2)$ must not be stopped, except during the shift and line shift operations. In other words, when the storage time is set longer than the reading time for one line -effective pixels plus dummy pixels- (Figure 4.2), the drive pulse must be present for all operations other than the reading out of effective pixels and dummy pixels.

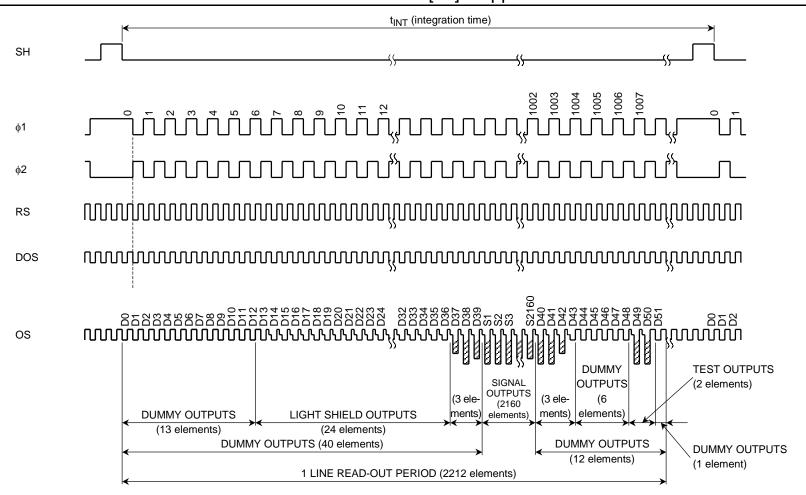


Figure 4.1 Timing Diagram for TCD1208AP

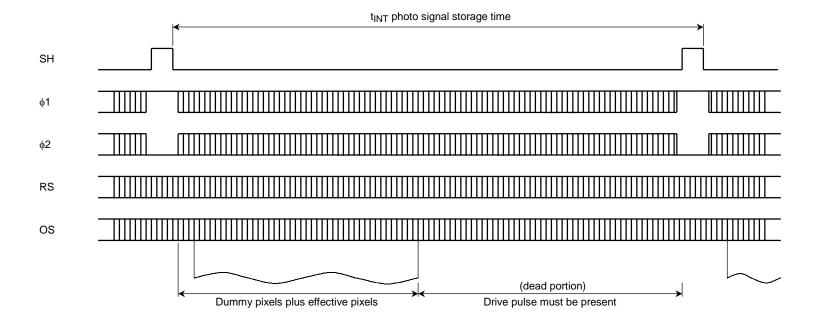


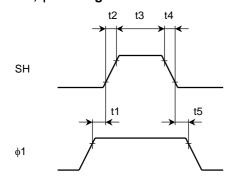
Figure 4.2 Drive Pulse

Table 4.2 Pulse Timing Requirements for the TCD1208AP

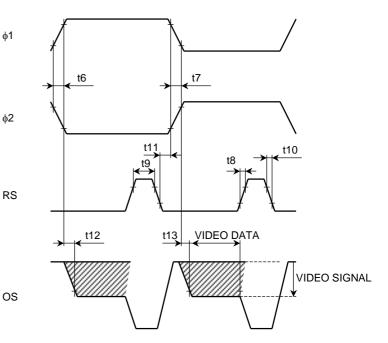
φ1

φ2

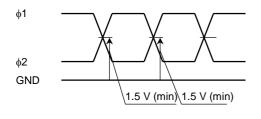
SH, $\phi 1$ Timing



φ1, φ2, RS, OS Timing



φ1, φ2 Cross point



Characteristic	Symbol	Min	Typ. (Note 1)	Max	Unit
Pulse timing of SH and φ1	t1, t5	0	100	I	ns
SH pulse rise time, fall time	t2, t4	0	50		ns
SH pulse width	t3	200	1000		ns
φ1 φ2 pulse rise time, fall time	t6, t7	0	100	ı	ns
RS pulse rise time, fall time	t8, t10	0	20	I	ns
RS pulse width	t9	40	250	-	ns
Pulse timing of φ1, φ2 and RS	t11	10	250		ns
Video data delay time (Note 2)	t12, t13	_	50	_	ns

Note 1: Typ. is when $f_{RS} = 1 \text{ MHz}$

Note 2: Load resistance is 100 $k\Omega$

4.3 Integration Time

The shift pulse cycle SH equals the integration time (tINT) for the video signals. Determining tINT establishes the following essential operating parameters for the CCD image sensor.

a. Exposure value:

The exposure value is the product of the luminosity of the photosensitive surface and tINT. It is best to set the exposure value to approximately 1/2 of the standard saturation exposure.

b. Pixel read-out speed:

The pixel read-out speed is determined by the clock frequency $f\phi$ of the CCD analog shift register; however, $f\phi$ and $t_{\rm INT}$ must satisfy the following condition:

$$\frac{(NS + ND)}{f\phi} \times \mu \leq t_{INT}$$

NS: Number of effective pixels

ND: Number of dummy pixels

μ: A coefficient for the transfer section configuration

Dual-channel = 1/2Single-channel = 1

c. Dark signal:

There are two dark signals: one occurs in the photosensing region and the other occurs in the transfer region. The dark signal in the photosensing region depends on the value of tINT and the dark signal in the transfer region depends on the value of $f\phi$ and the number of transfer steps.

d. Minimum integration time:

When you want to obtain 64-pixel data using the CCD image sensor, you cannot obtain the data by applying the SH pulse after read-out of the S64 signal. The reason is explained in Figure 4.3. Figure 4.3 (A) is a schematic drawing. Exposing the pn photodiode to light generates a video signal charge as shown in Figure 4.3 (B) (shaded area). Figure 4.3 (C) shows the transfer of the video signal charge to the CCD analog shift register on the SH pulse; Figure 4.3 (D) shows the completed read-out of S1 to S64. The next SH pulse input mixes the first signal charge with the second one, as shown in Figure 4.3 (E). The output waveform when the charge is read-out is as shown in Figure 4.3 (F); the area where the video signal charges mix generates the sum of the two the video signals.

The integration time must be set to be greater than the on-line read-out period listed in the individual technical data (see Figure 4.1).

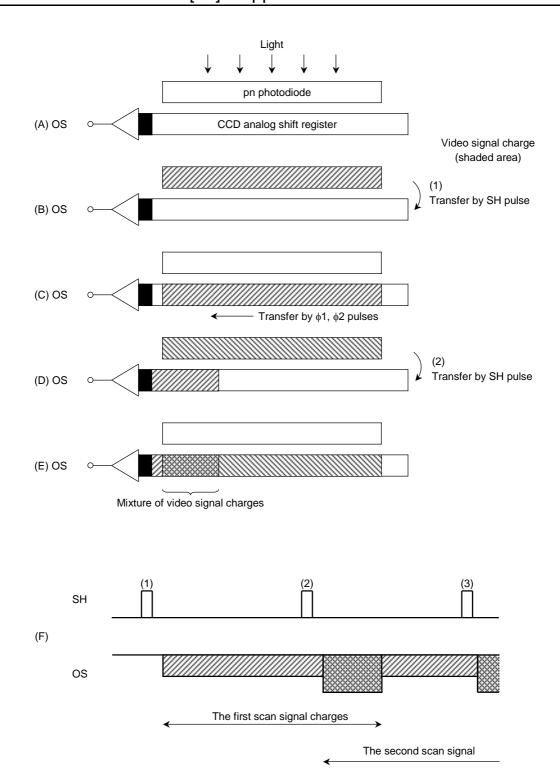


Figure 4.3 Problems with too Short an Integration Time

4.4 Signal Output

The output circuit for TCD1208AP consists of a source follower circuit as shown in Figure 2.8, and generates a constant offset voltage of about 3.5 V with a constant current.

The voltage is prescribed to be a DC output voltage; however, it varies from device to device. The dark signal and the video signal are output from the offset voltage as minus voltages (Figure 4.4).

The output signal contains noise caused by the reset pulse, RS. Since the compensation output (DOS) contains the same reset noise as the signal output (OS) the reset noise can be reduced by differential amplification.

Take note of the following guidelines for reducing the amount of noise mixed with the output signals:

- (1) Position the signal line and clock line as far apart as possible.
- (2) Use a thicker GND line.
- (3) Add an emitter-follower circuit, OC similar circuit when lengthening the sensor output (even though the output of the CCD sensor is designed to be output directly as low impedance output).

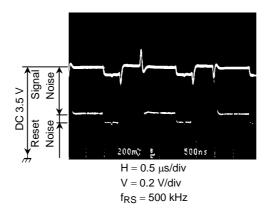


Figure 4.4 TCD1208AP Output Waveform

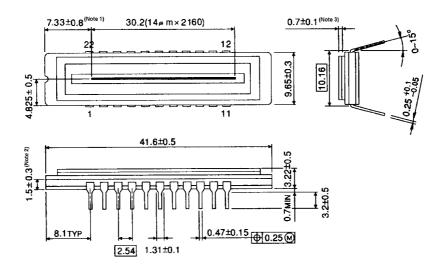
4.5 Packaging

(1) Precise positioning of photosensing region

As shown in Figure 4.5, the photosensing region of the CCD Sensor is positioned with a specified degree of precision with respect to a given reference point and reference surface on the T-CAPP (plastic) package. The tolerance of X, Y and Z are each specified at around 0.3 to 0.8 mm taking into consideration the precision of the dimensions of the plastic itself. A tolerance for the inclination to the reference surface is also specified. It may be better to think in terms of fine adjustments in the X, Y, Z and θ directions when mass-producing application products. (X, Y and Z indicate the directions shown in Figure 4.6; θ indicates the angle of displacement between the X-axis and the X, Y surface.)

As the stand-off heights of the leads are not uniform, insertion of a spacer between the printed circuit board and the CCD sensor keeps the sensor perpendicular to the Z-axis.

Unit: mm



Note 1: No.1 sensor element (S1) to edge of package

Note 2: Top of chip to bottom of package

Note 3: Glass thickness (n = 1.5)

Figure 4.5 Package Outline (TCD1208AP)

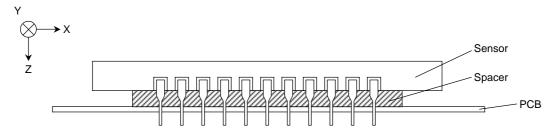


Figure 4.6 Using a Spacer

(2) Window glass

Dust or dirt adhering to the window glass on the photosensing region of the CCD sensor causes the PRNU value to deteriorate. Prior to use, be sure to clean the window glass surface with a soft cloth or gauze soaked in an organic cleaning solution, such as alcohol. A flaw in the glass will also affect the PRNU value, but there is no fixed relationship between the size, depth or shape of the flaw and the PRNU value. Also, the f-number of the lens used affects the PRNU value. Since the PRNU is measured by radiating light vertically onto the photosensing surface with the f-number set to about 10, an extremely oblique incidence may generate an erroneous measurement.

During the production process for application products, cleaning off dirt and applying tape to prevent glass flaws may generate high levels of static electricity (surface voltages of about 1200 V or more). This causes the PRNU value to deteriorate.

This phenomenon (known as the charge-up phenomenon) occurs when the charged static electricity on the glass surface discharges inside the sensor package and charges the surface of the photosensing picture element.

Figure 4.7 shows the process. Figure 4.8 is the output waveform for the CCD while the charge-up phenomenon is taking place.

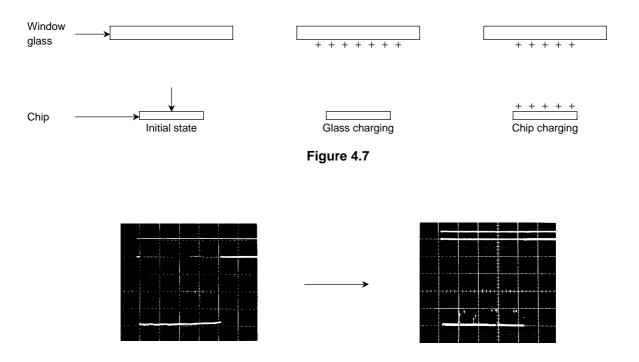


Figure 4.8

Method for preventing the charge-up phenomenon (example)

- Use alcohol to remove dust and dirt.
- If possible, do not use glass flaw prevention tape. If tape must be applied, use a non-adhesive and conductive brand of tape.

4.6 Light Source

The CCD image sensor responds to sideband light wavelengths. However, when inputting infrared rays, deterioration of the characteristics may occur, including uniformity deterioration, reduced resolution, etc. Therefore, the use of a light source with no infrared component, such as a daylight fluorescent lamp or green fluorescent light, is recommended. When the use of, for example, a tungsten lamp cannot be avoided, use it in conjunction with a filter that cuts out infrared radiation.

For AC lighting sources, including fluorescent lamps, a high frequency of several tens of kHz or more must be used because low frequencies such as 50 Hz or 60 Hz cause flickering. If the scanning time (integration time) is 10 ms and the power source of the light source is 30 kHz, the number of flickers during a scan is 600, and even shifting the scanning phase against the flickerings phase of the light source causes only a negligible change in the quantity of light for every scan.

LEDs can also be used as a light source in applications with an adequate integration time or for highly sensitive devices. Stable lighting can be achieved because LEDs permit DC lighting. In addition, since LEDs can be turned on and off at high speed, red/green data can be quickly written to a memory device for later processing by a microcontroller.

4.7 Static Electricity

The CCD image sensor has an electrostatic shield; however, this may be damaged by static electricity. In order to prevent an increased failure rate due to damage from static electricity during manufacturing, the following rules for handling devices must be enforced.

- (1) Prevent the generation of static electricity due to friction by operating the device with bare hands or while wearing cotton gloves, and by wearing non-static working clothes.
- (2) Discharge the floor, door, table, etc., of the working area using either an earth plate or earth wire, and by using an earth-return circuit as required.
- (3) Ground tools, such as soldering irons, pliers and tweezers.

5. Contact Image Sensor

5.1 Outline

The contact image sensor (contact sensor) is a sensor used to scan a document image onto sensor pixels at the same (1:1) size as the original (life-size). The special feature of this contact sensor is its ability to reduce the distance between document and sensor. Figure 5.1 shows a comparison with an optical reduction-type sensor. The contact sensor, in contrast, allows miniaturization of systems.

The lenses used with a contact sensor are special lenses known as rod lens arrays. These frequently use an LED array as the light source. Both rod lens arrays and LED arrays are vital components for system miniaturization.

To shiba has integrated both components in a contact sensor module. For further information, please see Chapter 6.

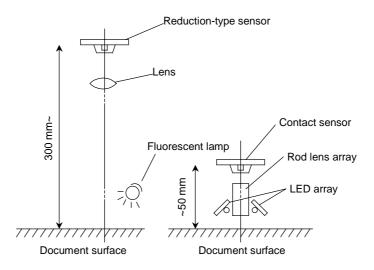


Figure 5.1 Optical System Structure

5.2 Classification

Contact sensors can be broadly divided into staggered-type sensors that use a staggered sequence of chips, and in-line-type sensors that use a linear sequence. Staggered-type sensors are further divided into monochrome and color sensors (shown in Figure 5.2).

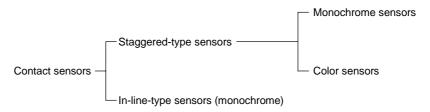


Figure 5.2 Contact Sensor Classification

(1) Staggered-Type Sensors

Because of limits to the size of the CCD image sensor semiconductor chips, where the reading length is long, several chips are arranged in one package to achieve the reading length. Figure 5.3 shows the layout of the TCD118AC chips where four chips are used in a staggered pattern. As these chips are not arranged in a line, they cannot read linear images at the same time. Internal line memory enables linear images to be obtained at one time when data are read from the chips.

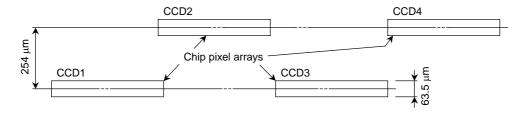


Figure 5.3 TCD118AC Chip Array

The following describes the color sensor. The color sensor consists of color filters placed over pixels. The filters are primary color filters (red, green, and blue). In the TCD126C, the filters and pixels are arranged as in Figure 5.4. The pixels are configured in a parallelogram to prevent moire. Moire is a spurious image produced when the pixel pitch and the pixel image pitch appear virtually simultaneously. This is the same kind of phenomenon as the hum caused by the combination of two closely spaced frequency sounds.

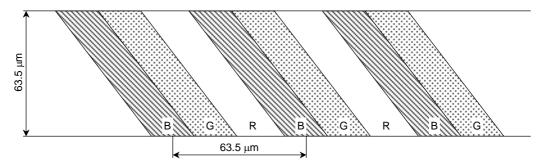


Figure 5.4 TCD126C Pixel Schematic

(2) In-Line-Type Sensors

Like staggered-type sensors, in-line-type sensors use several chips to obtain the reading length. The arrangement of those chips is linear, as shown in Figure 5.5. This layout allows linear image information to be read all at one time.

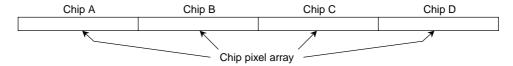


Figure 5.5 Layout of In-Line-Type Sensor Chip

5.3 Line Memory

As described in section 5.2.1, the line memory of staggered-type sensors has a function for compensating for the spatial slippage of the reading position caused by the chip arrangement.

The following explains how to use line memory.

Figure 5.6 is a circuit diagram of one of the chips used in the TCD118AC. Figure 5.7 shows the A-A' cross-section potential that appears in Figure 5.6 Line memory is actually composed of line shift gates. Inputting high-level voltage just to the $\phi V1$ pin sends the signal's charge to the line shift gate 1 ($\phi V1$) area. $\phi V1$ now returns to low-level voltage but even in this state, the signal charge does not shift from $\phi V1$. This state is known as memory operation. This state continues until the adjacent line shift gate ($\phi V2$) voltage goes high. When the $\phi V2$ voltage goes high, the signal charge is shifted from $\phi V1$ to $\phi V2$. After that, the charge is shifted in the same way until the $\phi V7$ and the $\phi V7$ memory operation are released by SH.

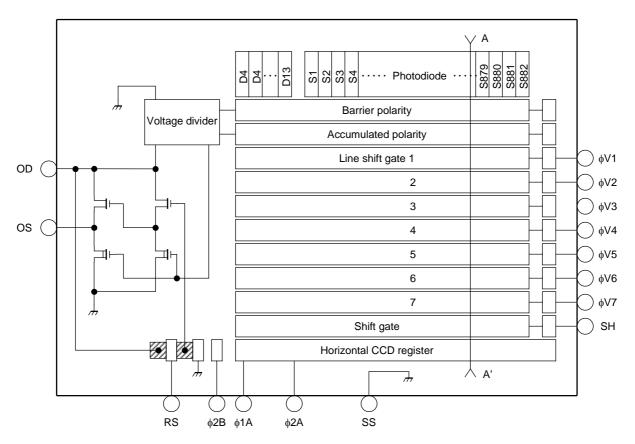


Figure 5.6 TCD118AC Chip Circuit Diagram

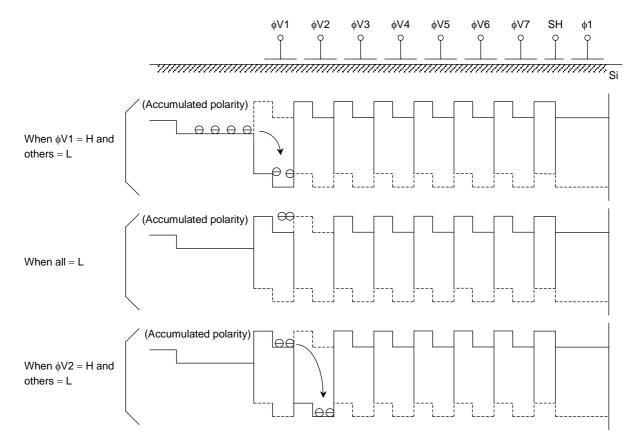


Figure 5.7 Potential of Line Memory Area

(1) How to Use Line Memory (1)

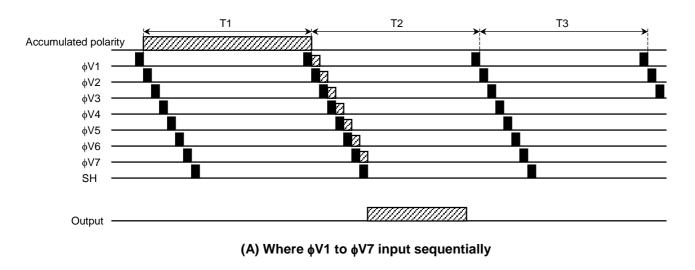
Figure 5.8 shows an example of line memory use. The (A) section of the diagram shows an example of sequentially inputting $\phi V1$ to $\phi V7$ and SH. The diagonal lines on the diagram indicate the location of the charge accumulated during interval T1. The charge is output during interval T2.

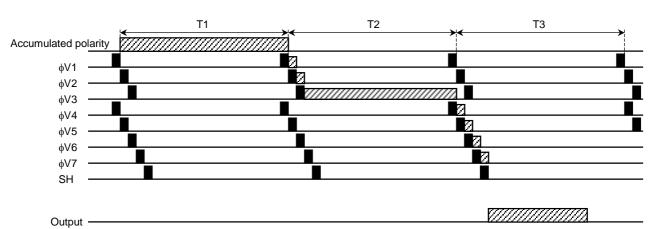
Figure 5.8 (B) shows the movement of the charge when the $\phi V3$ and $\phi V4$ pulse input sequence is reversed. In the reversal sequence, no $\phi V4$ pulse is input after the input of the $\phi V3$ pulse during interval T2. As a result, the charge accumulated in the $\phi V3$ line shift gate allows memory operations to continue until the $\phi V4$ pulse is input during interval T3. The charge is transferred sequentially to $\phi V4$ to $\phi V7$ and SH and the charge is output during interval T3.

If the sequence of the pulse input to $\phi V1$ to $\phi V7$ and SH is reversed one time, the output is delayed for one cycle.

In other words, reversing the sequence n times delays the output by n cycles in relation to the output in Figure 5.8 (A).

In staggered-type contact sensors, the pixel array dislocation between the odd-numbered and even-numbered chips is four lines, necessitating four reversals of the sequence of pulse input to the line shift gate. Figure 5.9 shows a typical example.





(B) Where \$\phi V3\$ to \$\phi V4\$ input in reverse sequence

Figure 5.8 Change in Output Resulting from Difference in Sequence of Pulse Input to Line Shift Gate

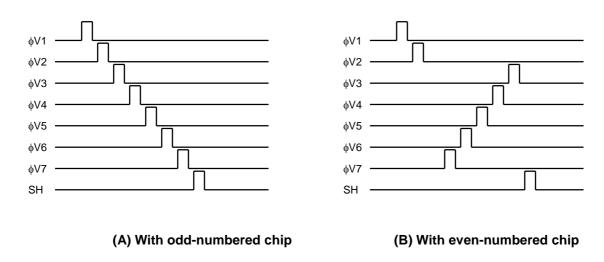


Figure 5.9 Typical Timing of Pulse Input to Line Shift Gate

(2) How to Use Line Memory (2)

Another use of line memory is to separate the interval where the chip reads the image information from the interval where the data are output from the chip.

As two-chip configurations, let us compare a sensor with internal line memory to a sensor with no line memory. Figure 5.10 shows the cross-section potential of both sensors.

Figure 5.11 shows a drive example using a sensor with internal line memory; Figure 5.12, an example using a sensor with no line memory. At the drive timing, the signals output from OSA and OSB (the outputs of the two chips) are multiplexed to obtain the signal SOUT. When a sensor with internal line memory is used, the intervals in which all the chips read the image data can be synchronized. Accordingly, even though the light source flickers at manual scanning or when the quantity of light is excessive, there is no image slippage of the secondary scanning direction at the chip join. In sensors with no line memory, because slippage occurs between the interval when the A chip reads the data and the B chip reads the data, when the sensor and document move in relation to each other, there is slippage in the data reading.

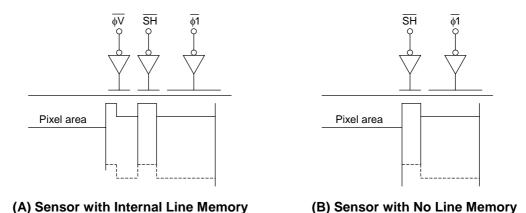


Figure 5.10 Cross-Section Potential of Sensor with Internal Line Memory and Sensor with No Line Memory

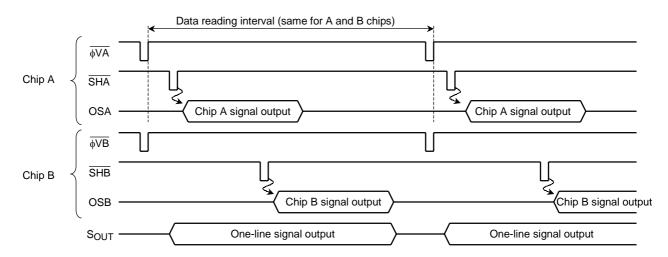


Figure 5.11 Drive Timing for Sensor with Internal Line Memory

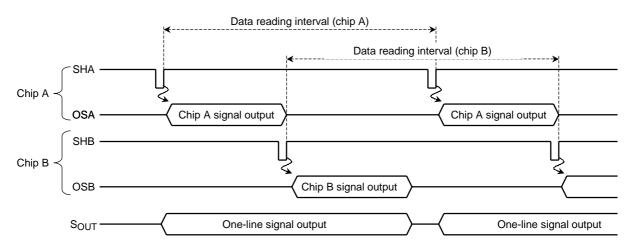


Figure 5.12 Drive Timing for Sensor with No Line Memory

The drive timing in staggered-type sensors is the same as above. Figure 5.13, and Figure 5.14 show the drive timings for parallel and serial output with the TCD118AC. Compared to serial output, parallel output can reduce the optical signal accumulation time but requires a bright light source and multiple signal processors.

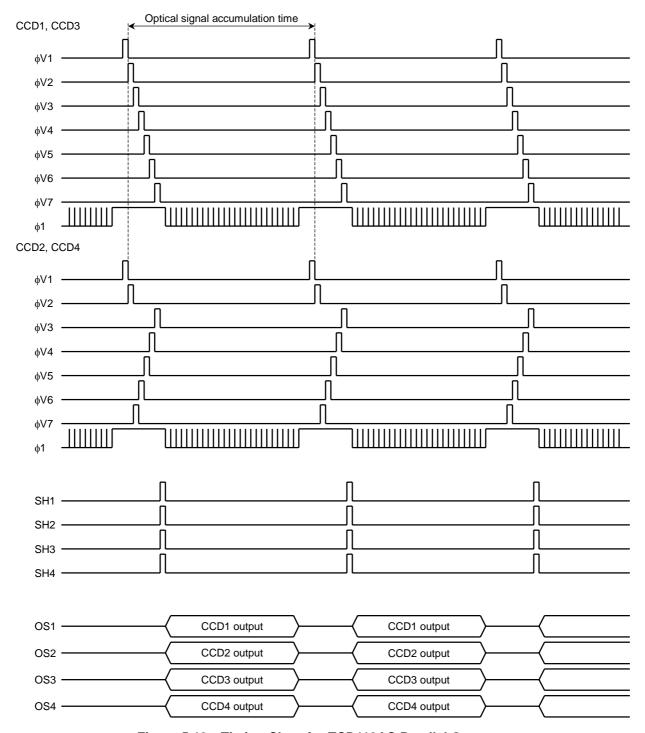


Figure 5.13 Timing Chart for TCD118AC Parallel Output

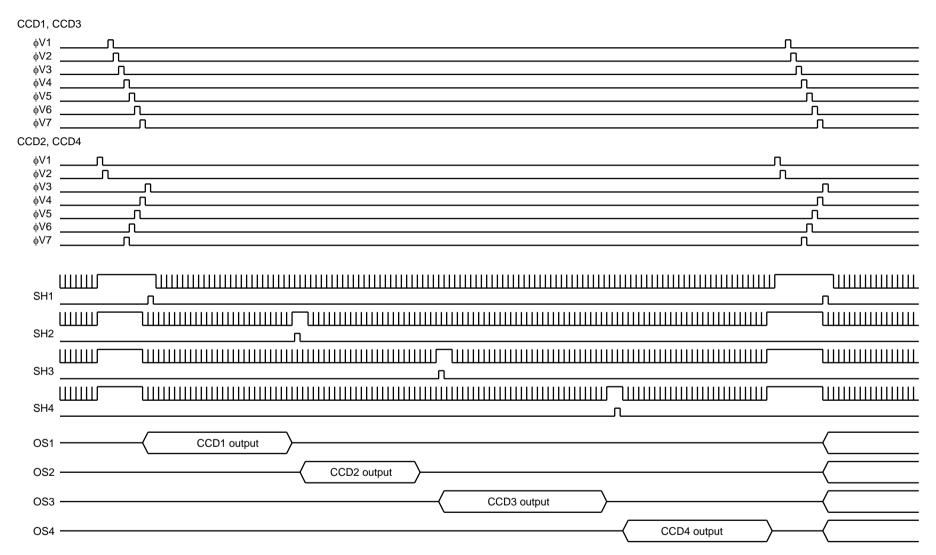


Figure 5.14 Timing Chart for TCD118AC Serial Output

5.4 Attaching Method

The location of the light reception surface of the contact sensor is determined in relation to the substrate surface. Therefore, to ensure the light reception surface of the contact sensor is flat, Toshiba recommend horizontally crimping a ceramic substrate or using a similar mounting method.

As Figure 5.15 shows, it would be convenient to integrate the LED array, rod lens array, and contact sensor in one unit. If such a unit were created, it could also be effective for the development of various types of systems.

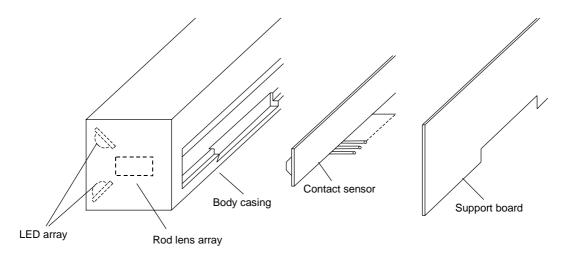


Figure 5.15 Contact Sensor Fixing Method

5.5 Components

The components used with the contact sensor are the LED array and rod lens array.

The LED array features linear light-emitting diodes. When using the array as a light source, one or two LED arrays can be configured. (See Figure 5.16)

When using two LED arrays, the advantage is that even with pasted up documents, there is no shadow. However, whether to use one or two arrays depends on such variables as the sensor's accumulation time, the brightness of the lens, and cost. Using two LED arrays with each array a different color allows a color selection feature to be configured.

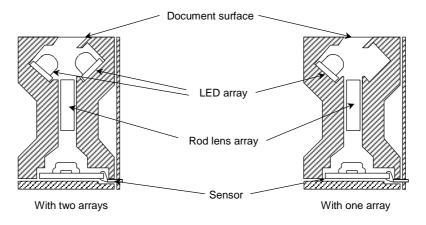


Figure 5.16 Example of LED Array Installation

When the LED array is lit, heat is emitted. This changes the forward voltage of the light-emitting diodes. As a result, when constant voltage E (V) is used to light an LED array with the circuit structure shown in Figure 5.17, the voltage (V_R (= E – V_D)) between each end of the protection resistor changes. This changes the current to the LED and the brightness of the LED array. This variation can be prevented by using a constant current power supply to power the array.

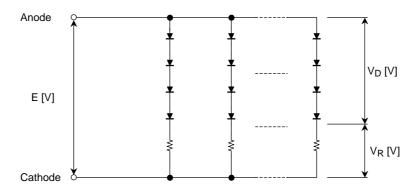


Figure 5.17 LED Array Circuit Structure

6. Contact Sensor Module

6.1 Outline

The contact sensor module is an image reader unit combining an image sensor, lens, light source, and control circuits. The contact sensor module offers the following features.

(1) No optical settings necessary

As the focus is adjusted in advance, the document simply needs to be placed in the focal position for its image to be read.

(2) Easy mechanical adjustment

The only mechanical adjustments are the relative positions of the contact sensor module and the document.

(3) Simple drive and signal processing

To drive the contact sensor module, three pulses are used (in a 5-V system): two pulses and a trigger pulse for the shading compensation reference data.

The picture signal is a digital signal consisting of binary, 8-bit shading-compensated data.

6.2 Structure

The contact sensor module contributes to miniaturization by using a special lens known as a rod lens array. Figure 6.1 shows a cross-section of the module, which has the following five main components.

- Image sensor
- Rod lens array
- LED array
- Control circuit board
- Body casing

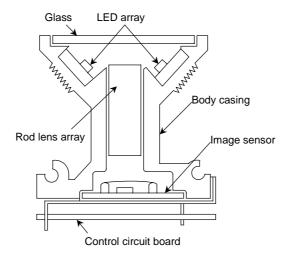


Figure 6.1 Cross-Section

6.3 Contact Sensor Module Drive

Using built-in control circuits, the contact sensor module simplifies system signal input/output. The following describes the drive operation, using the CIPS305MA400 input/output diagram below as an example. (See Figure 6.2 and Figure 6.3.)

(1) Drive pulses

Three drive pulses are supported: the master clock (CLK), the line start (\overline{LST}), and the LED control (\overline{LEDC}). Continuously input CLK and \overline{LST} . Input \overline{LEDC} once when writing shading compensation data.

(2) Signal Output

This is a binary, 8-bit digital shading-compensated output signal. The signal output can be easily sampled because a data clock pulse (\overline{DCLK}) is output synchronously with the signal output.

Sample the signal output on the rising edge of \overline{DCLK} .

(3) Power Supply

The module requires the following power supplies: +15 V, -12 V, and +5 V. The LED comes on at -12 V.

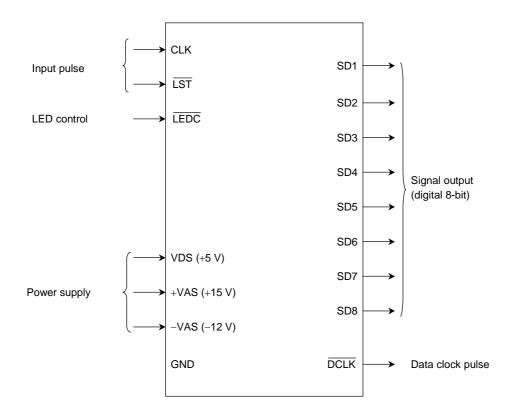


Figure 6.2 Diagram of CIPS305MA400 Input/Output

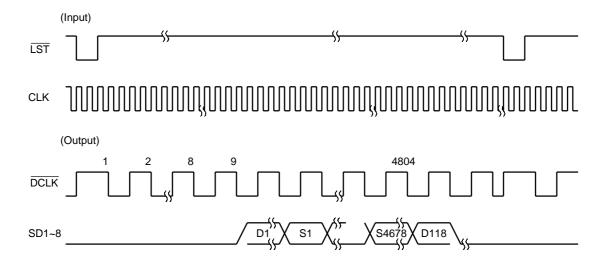


Figure 6.3 Timing Chart for CIPS305MA400 Input/Output

6.4 Block Diagram of Contact Sensor Module

Figure 6.4 shows a block diagram of the contact sensor module.

• Timing generator

This is a circuit to generate pulses, including the sensor array drive pulse.

Driver

This is a circuit to convert the pulse supplied to the sensor array from 5 V to 12 V.

Sensor array

This is a contact image sensor to convert optical signals to electrical signals.

• Clamp circuit

This is a circuit to prepare the picture signal output from the sensor array for A/D conversion.

• A/D converter

This circuit performs A/D conversion on the picture signal.

• Shading compensation circuit

This circuit initially inputs the white and black signals used as reference to memory and uses them to compensate the actual picture signals.

The compensation formula is:

$$SD = \frac{SD' - SB}{SW - SB} \times 255(LSB)$$

Where SD' is the actual picture signal, SW is the white reference signal, and SB is the black reference signal. For the shading compensation method, see section 6.5.

Memory (RAM)

Stores the white and black reference signals.

• LED control circuit

This circuit automatically turns the LED on/off at shading compensation.

LED array

This is the light source for illuminating the document. CIPS305MA400 and CIPS300MA300 use two LED arrays.

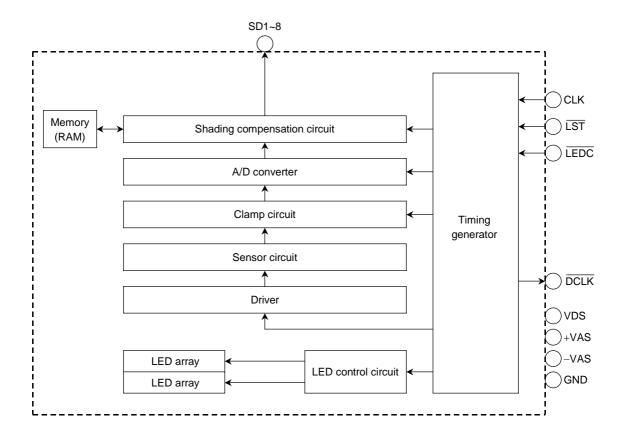


Figure 6.4 CIPS305MA400 Block Diagram

6.5 Shading Compensation

When the contact sensor module reads the document, the white and black shading compensation data must be first written to memory (RAM).

When writing the shading compensation data, place the white document used as reference in the contact sensor module document reading position to block any incident light. The timing chart below shows the timing for the shading compensation. The LED automatically turns on/off according to the CLK, LST, and LEDC input. Shading compensation starts on the LEDC falling edge after the power (VAS, –VAS, VDS) is turned on. When LEDC goes Low, a valid signal is output from the 17th LST.

When rewriting shading compensation data, set LEDC to High for at least 18 LSTs.

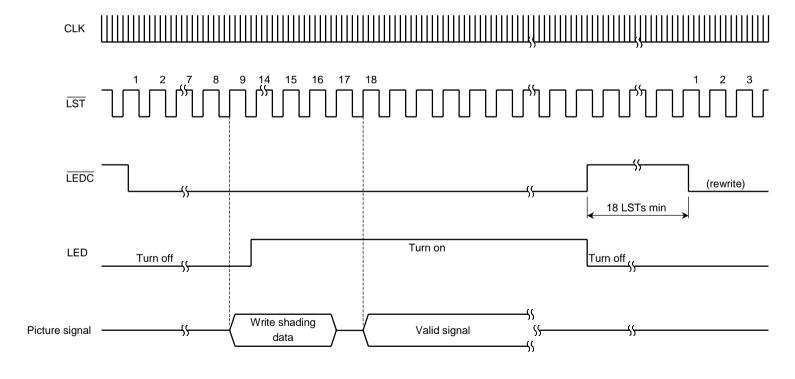


Figure 6.5 Timing Chart for Shading Compensation

7. Peripheral Circuits

7.1 Timing Generator Circuit

The CCD image sensor needs various pulses for its operation that are synchronized with one another; these pulses are cyclic. The diagrams on the following pages are examples of circuitry for the CCD image sensor.

Figure 7.1 shows an example of a timing pulse generator circuit for driving a reduction-type sensor. Figure 7.2 shows the corresponding timing diagram. The master clock is set to an appropriate frequency using SW1 and VR and divided by IC2 to generate the fundamental clock pulses. The operating pulses for the CCD are generated by the fundamental clock pulses. The SW2 and SW3 switches determine the integration time and the pulse width of the shift pulses (SH) respectively.

Figure 7.3 is an example of a timing generator for the contact sensor. The main difference from that in Figure 7.1 is that the timing generator in Figure 7.3 generates pulses for memory gates. The role of SW2 is the same as that in , Figure 7.1. Figure 7.4 is the timing chart for the timing generator shown in Figure 7.3

7.2 CCD Driver Circuit

Normally a pulse voltage of 12 V is required to drive the CCD image sensor (except in some products which have an internal driver). In general, however, a logic circuit uses 5-V logic; thus a circuit for converting 5-V pulses to 12-V pulse is required. The CCD drive circuits shown in Figure 7.5 to Figure 7.9 perform this function. Figure 7.5 shows an example circuit using a DS0026CN manufactured by National Semiconductor Co., suitable for driving the CCD image sensor at high speed, since it is a large capacitive load. Figure 7.6 shows a driver circuit using a DS75365 manufactured by National Semiconductor Co.; Figure 7.7, Figure 7.8 and Figure 7.9 shows one using a TC4049BP, TA8660P and TA8660F by Toshiba. Since these elements have different response times and drive capabilities, factors such as the delay time of the CCD output must be taken into consideration.

7.3 Examples of Sensor Operation

This section describes how drive pulses are supplied to the CCD image sensor. Figure 7.10 shows an example of a connection circuit. If the data rate of the video signals is 1 MHz or less, the connection is adequate for the task.

However, the faster the drive speed, the greater the effect of the delay time between the falling edge of the clock and the output of video signals. The delay time is determined by the speed with which the clock pulse goes low. Hence, the foster the clock pulse goes low, the better. It is difficult to reduce the terminal voltage rapidly because of the clock terminal's high capacitance. However, the problem can be resolved by separating the final-stage electrodes related to output delay (in Figure 2.8, the right-hand electrode pair 1/2) from the other electrodes, and making them independent final-stage clock terminals. Thus, since these final-stage clock terminals, which are independent of the other clock terminals, have a lower capacitance, the terminal voltage fall time is reduced and signal charges are rapidly transfer red from the transfer region to the output region.

Figure 2.8 shows that, whereas, when the well bottom rises slowly, charge is slowly input to the floating capacitor, when the well bottom, rises rapidly, the speed of input of charge into the capacitor is increased and the output delay time is reduced. Although independently driving the final-stage clock reduces the effective delay time of the output, as described above, with high-speed driving, even with separate driving, there is no time to spare for the signal output period itself due to the width of the reset pulse (RS). In that case, separate channel output is effective as shown in Figure 7.12. The signal output period for dual-channel outputs (separate channel output) is about twice that of single-channel outputs (composite channel output).

As a practical example, Figure 7.13 shows intermittent RS driving. This example gives the sum of two pixels, data using a half-frequency RS input. This method handles the 1,024-pixel sensor as a 512-pixel sensor, doubling its sensitivity and outputting the combined charge from two pixels. Remember, however, that the saturation output voltage is the same level as, not twice that of when the RS input is not reduced to half frequency.

7.4 Differential Amplifier Circuit

As described in Section 4-4, some CCD linear image sensor devices are equipped with compensation output (DOS). The differential amplification between the compensation output (DOS) and the signal output (OS) can eliminate reset noise. However, it is impossible to completely cancel out the reset noise with the differential amplifier because of the shift in DC output voltage and reset noise voltage between OS and DOS. A sample-and-hold circuit, as described below, is required to completely cancel the reset noise.

7.5 Sample and Hold Circuit

Figure 7.17 shows an example of a sample-and-hold circuit. For the hold capacitor in the sample-and-hold circuit, the amplification, the capacitance, the width of sampling pulse (SP), etc. must be selected to give sufficient charging and discharging. In addition, since there is an inherent delay time in the circuits operation, attention must be paid to the timing of the sampling pulse.

7.6 Dark Signal Compensation Circuit

The output signal from the CCD image sensor consists of a component that is proportional to the amount of input light and a component which has no relationship to the amount of input light (the dark signal). Differential amplification of the signal output and the dark signal can extract the required component: the one that is proportional to the amount of input light (Figure 7.18).

In the case of the TCD1208AP, this dark signal can be obtained from the pixels D13-D36 as shown in Figure 4.1. For further precise adjustment of the dark signal, with output when a perfect black original is read, individual adjustment is required for each pixel.

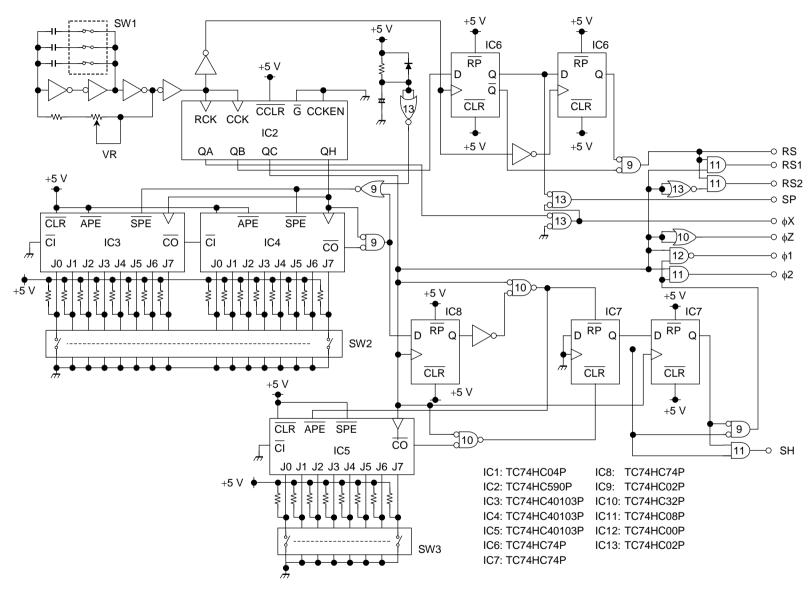


Figure 7.1 Timing Generator Circuit for a Reduction-Type Sensor

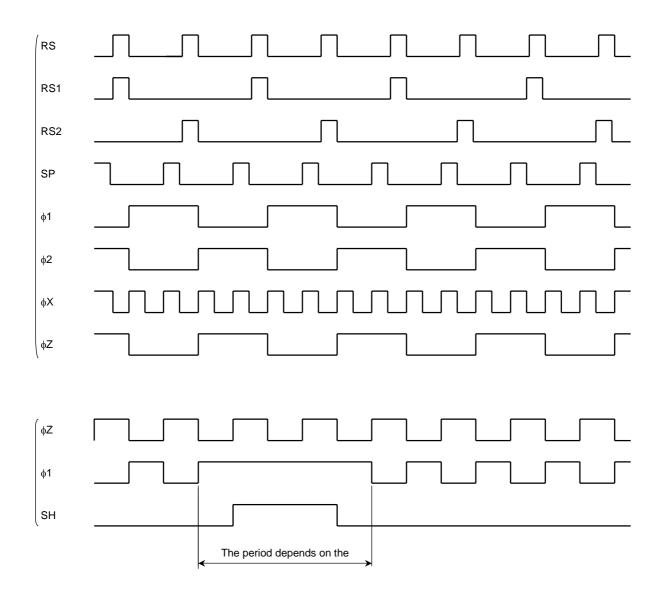


Figure 7.2 Timing Diagram for Figure 7.1

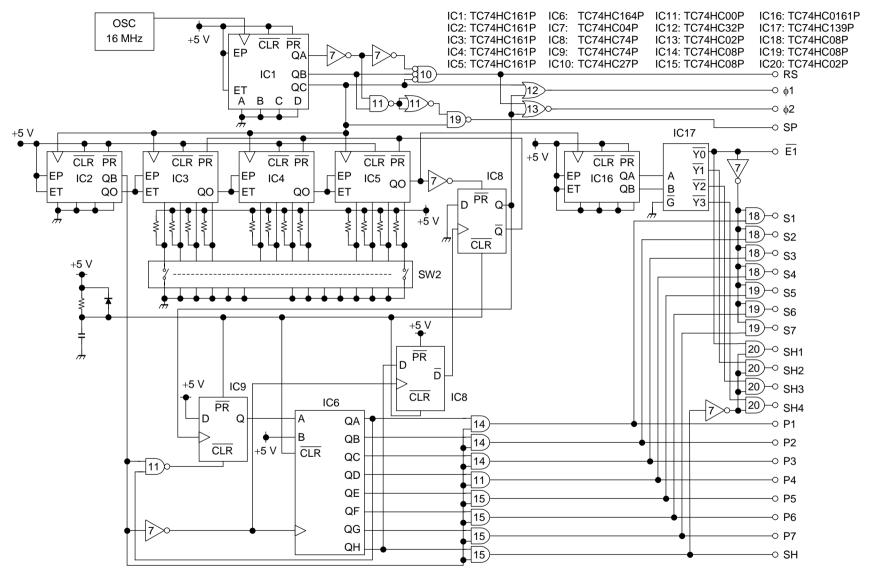


Figure 7.3 Driving Pulse Timing Generator Circuit

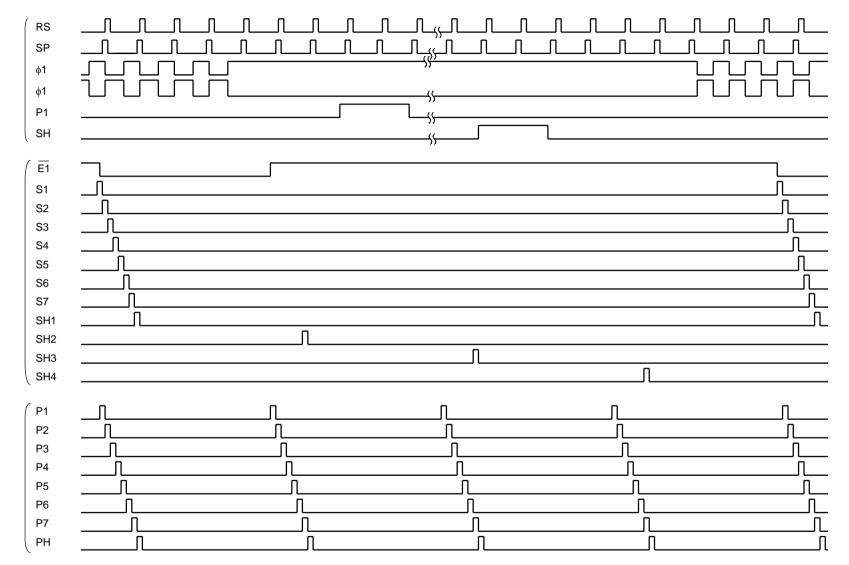


Figure 7.4 Timing Diagram of Timing Generator Circuit

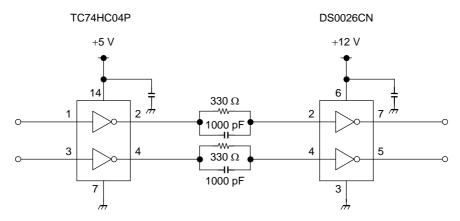


Figure 7.5 CCD Driver Circuit Using a DS0026CN

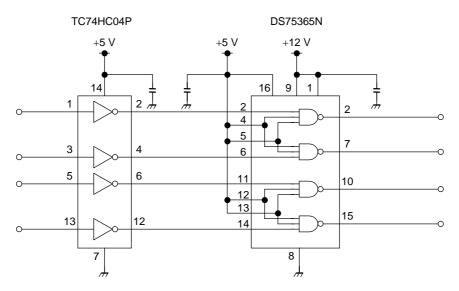


Figure 7.6 CCD Drive Circuit Using a DS75365N

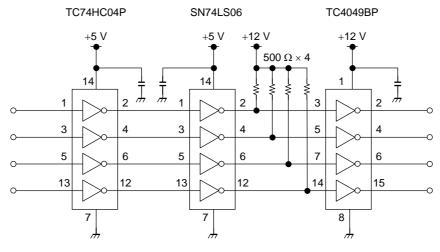


Figure 7.7 CCD Driver Circuit Using a TC4049BP

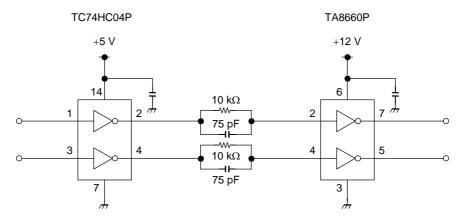


Figure 7.8 CCD Drive Circuit Using a TA8660P

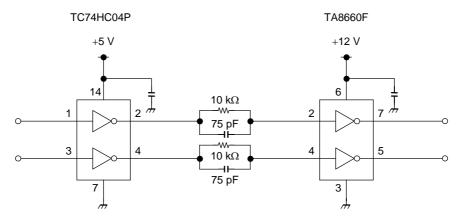


Figure 7.9 CCD Drive Circuit Using a TA8660F

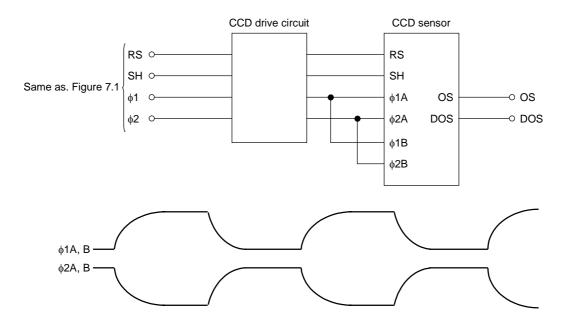


Figure 7.10 Final-Stage Clock Integrated Drive Circuit

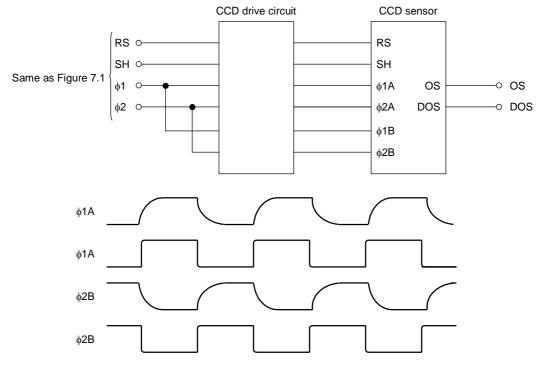
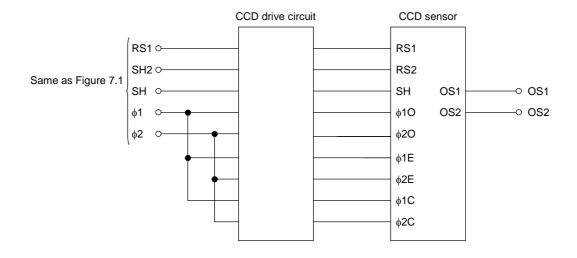


Figure 7.11 Final-Stage Clock Separate Drive Circuit



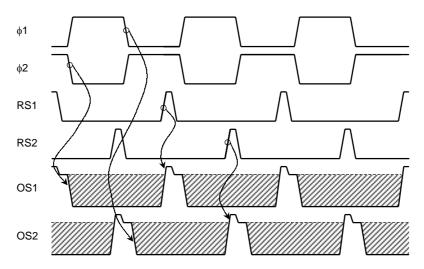


Figure 7.12 Dual-Channel Output Drive Circuit

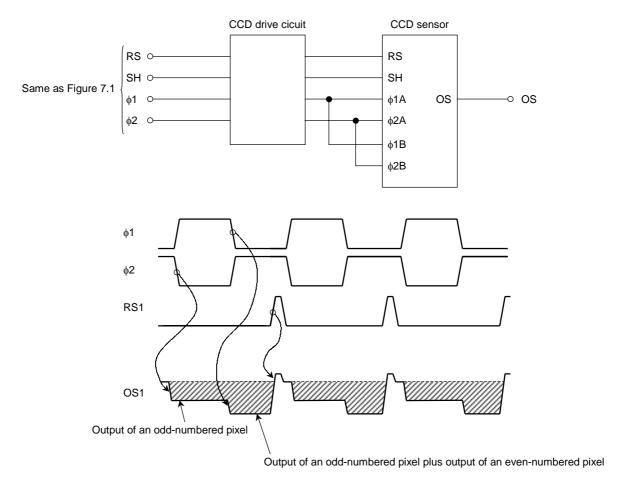


Figure 7.13 Intermittent RS Drive Circuit

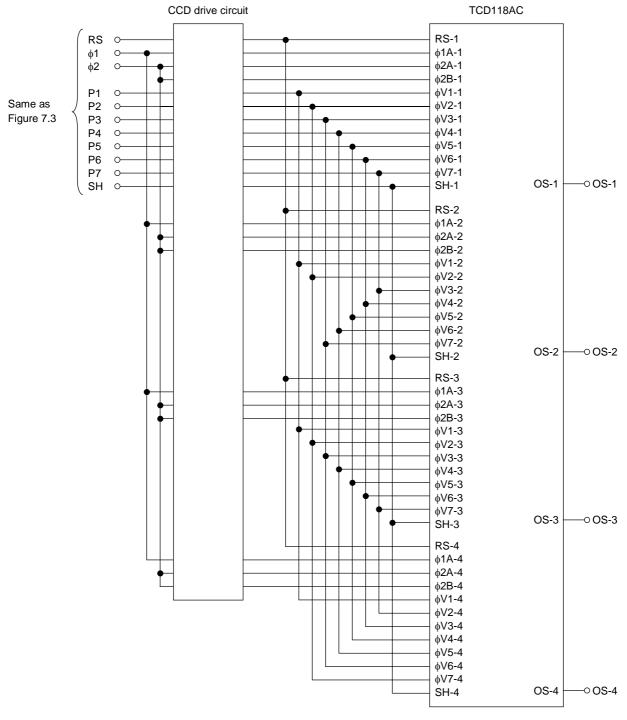


Figure 7.14 Example of Parallel Drive Circuit (for TCD118AC)

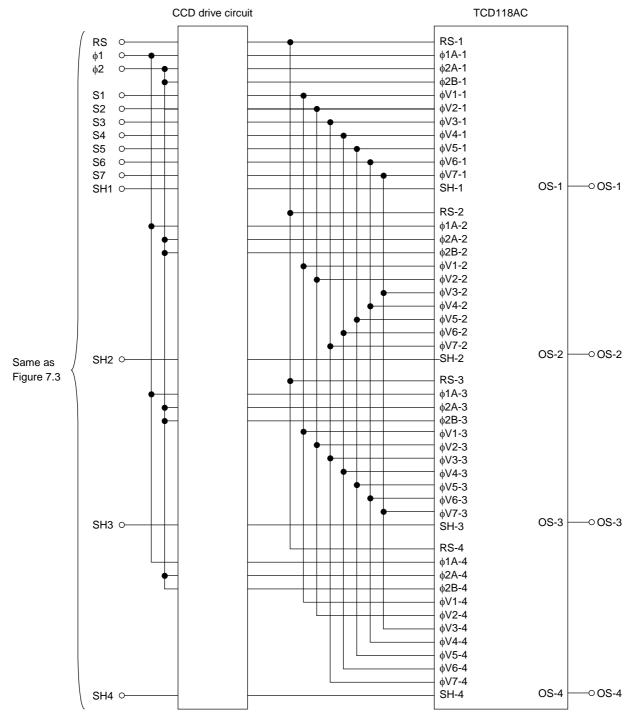


Figure 7.15 Example of Serial Drive Circuit (for TCD118AC)

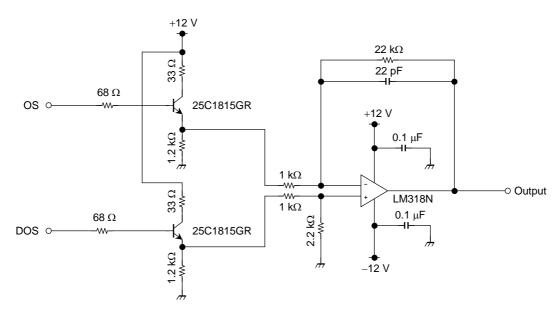


Figure 7.16 Differential Amplifier Circuit

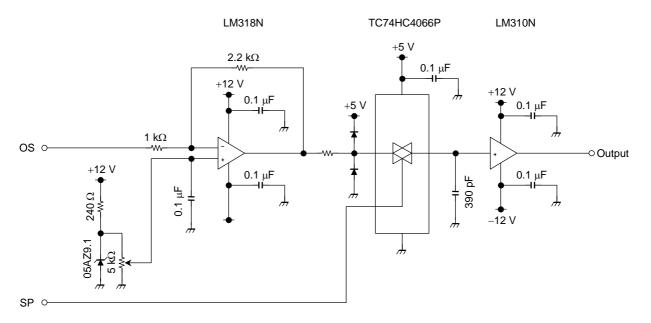


Figure 7.17 Sample-and-Hold Circuit

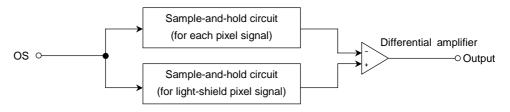


Figure 7.18 Block Diagram for Dark Signal Compensation