MAX66300

DeepCover Secure Authenticator with SHA-256 and RFID Reader

General Description

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible.

The DeepCover Secure Authenticator (MAX66300) combines a highly integrated RFID reader for contactless communication at 13.56MHz and a SHA-256 secure authenticator coprocessor. The RFID IC reader covers the ISO 15693 standard. The authenticator coprocessor's engine is based on the FIPS 180-4 standard and supports secure challenge-and-response authentication when paired with peripherals such as the Maxim MAX66240/MAX66242 family of tag solutions. An embedded host processor can easily interface with the MAX66300 using its UART or SPI interface.

Applications

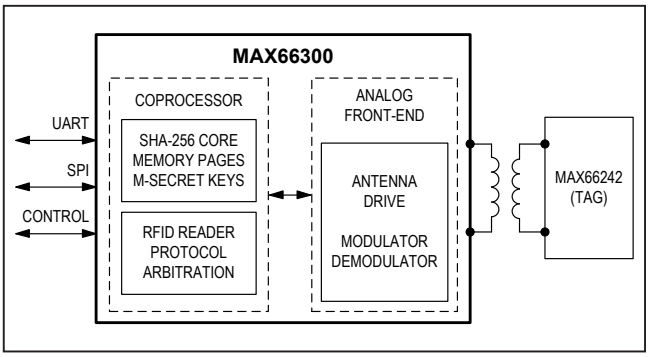
- Secure Access Control
- Asset-Tracking Readers
- Authentication of Consumables
  - Readers in Printers (Ink Cartridge)
  - Blood Glucose Meters/Monitors
- Handheld Reader Modules

Features and Benefits

- Secure, Contactless Host Authenticator
  - ISO/IEC 15693 Standard Compliant
  - SHA-256 Engine to Run a Symmetric Key-Based Bidirectional Secure Authentication
  - Four 32-Byte Pages of User Memory
  - Four Master Secrets with Multiple Programmable Protection Options
  - 76-Byte Scratchpad in SRAM
  - True Hardware Random-Number Generator
  - Unique 64-Bit Serial Number
- Design Flexibility Supports Diverse Applications
  - UART and SPI Interface Ports
  - Power-Down Mode by an Input Pin (Low, Standby Power)
  - Antenna Short-Circuit Protection
  - Compatible with 3.3V or 5V Supply Voltages
  - ±2kV HBM ESD Protection
- Scalable 13.56MHz Analog Front-End Provides Support for Multiple Antenna Configurations
  - Single- or Double-Antenna Driver Using On-Off Keying (OOK) Modulation
  - User-Selectable ASK Uplink Modulations Index Adjustable from 7% Up to 30%
  - High-Output RF Power of Up to 200mW
  - Multiple Receiver Inputs for High-Communication Reliability
  - Built-In Receiver Lowpass-Filter Cutoff Frequencies Selectable Between 400kHz and 1MHz
  - Built-In Receiver Highpass-Filter Cutoff Frequency Selectable Among 100kHz, 200kHz, and 300kHz
  - Selectable Receive Gain from 0dB up to 40dB
  - Multiple Subcarrier Receiving Compatibility
  - (212kHz and 424kHz)
- Antenna Short-Circuit Protection Enhances System Ruggedness

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit



DeepCover is a registered trademark of Maxim Integrated Products, Inc.

219-0045; Rev 1; 10/15

Absolute Maximum Ratings

Continuous Power Dissipation (T_A = +70°C)
TQFN (multilayer board)
(derate 47.6mW/°C above +70°C) 1.9W
Operating Temperature Range..... -40°C to +85°C
Maximum Junction Temperature ..... +110°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection per Method 3015 .....±2kV
(Applies to pins 1 to 32 and 52 to 56)
Voltage Range on V_{DD_CORE}, V_{DDQ} .....-0.3V to +3.6V
Voltage Range on Any Input
or Bidirectional Pin..... -0.3V to the lesser of ((V_{DD_CORE} +3.6V),5.5V) for the max
Voltage Range on HFXIN..... -0.3V to (V_{DD_CORE} + 0.5V)
Continuous Output Current on Any Single I/O Pin.....25mA

(Applies to pins 33 to 51)
Voltage Range on V_{DDA1}, V_{DDA2}, and $V_{DD\_AFE\_DIG}$ .....-0.3V to +6V
Maximum Voltage Range on Any Input or Bidirectional Pin..... $V_{DD\_AFE\_DIG}$ + 0.3V
Minimum Voltage Range on Any input or Bidirectional Pin .....V_{SS} - 0.3V
Maximum Output Current on Any Single I/O pin except ANT1 and ANT2.....10mA
Maximum AC Peak Current on ANT1 and ANT2 .....100mA
Storage Temperature Range (Note 1)..... -55°C to +120°C
ESD Protection per Method 3015 on ANT1 and ANT2.....±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Storage temperature is defined as the temperature of the device when all supply voltage is 0V.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DDQ} = V_{DD_CORE}, limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL (APPLIES TO PINS 1 TO 32 AND 52 TO 56)						
Operating Supply Voltage	V_{DD_CORE}		V_{RST}	3.3	3.6	V
Power-Fail Warning Voltage	V_{RST}	Brownout detection	2.8		3.0	V
Reset Mode Current ($\overline{RESET}$)	I_{DD1}	External 24MHz clock source generates system clock; device in reset		12	20	mA
Supply Current, External Clock Source	I_{DD2}	External 24MHz clock source generates system clock; code running from data memory; CSAM subcommand loop		14.4		mA
Sleep Mode Current (SLEEP)	I_{SLEEP}	T_A = +25°C, V_{DD_CORE} = 3.6V, SLEEP = GND, all other pins disconnected		2.3		mA

Electrical Characteristics (continued)

(V_{DDQ} = V_{DD_CORE}, limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Supply Output High Voltage	V_{DDIOH}	V_{DDIOH} current is the sum of V_{DDIO} current and I_{OH1} of all I/O, I_{OH1} = 20mA	V_{DD_CORE} -0.4		V_{DD_CORE}	V
Input Low Voltage (HFXIN)	V_{IL1}		V_{GND}		0.4	V
Input Low Voltage (Any I/O)	V_{IL2}		V_{GND}		0.2 x V_{DD_CORE}	V
Input High Voltage (HFXIN)	V_{IH1}		0.7 x V_{DDIO}		V_{DD_CORE}	V
Input High Voltage (Any I/O)	V_{IH2}		0.7 x V_{DDIO}		5.5	V
Input Hysteresis (Schmitt)	V_{IHYS}			0.5		V
Output Low Voltage	V_{OL1}	I_{OL1} = 4mA, V_{DDIO} = 3.0V	V_{GND}		0.4	V
Output High Voltage	V_{OH1}	I_{OH1} = -4mA, V_{DDIO} = 3.0V	V_{DDIO} - 0.6		V_{DDIO}	V
Input Crystal Capacitance	C_{IN}	Not production tested		6		pF
Input Leakage Current	I_{LEAK}	$V_{GND} \le V_{IN} \le$ 5.5V (Note 3)	-10		+10	µA
Input Pullup Current (Any I/O)	I_{PU}			-85		µA
Pullup Resistor ($\overline{RESET}$)	R_{PU}		20	40	55	kΩ
VOLTAGE SENSOR						
V_{VDD_CORE} High Reset Overvoltage Threshold	$V_{DD\_CORE\_OV}$		4.0		4.6	V
REG18 Overvoltage Reset Threshold	V_{REG18_OV}			2.6		V
CLOCK SOURCE						
External-Crystal Frequency Between HFXIN and HFXOUT	f_{HFXIN}		23.95	24	24.05	MHz
External-Clock Oscillator Frequency on HFXIN	f_{HFXIN}		23.95	24	24.05	MHz
External-Clock Period Duty Cycle	t_{CLDC}		45		55	%
Clock Rise Time	t_{CR}				3	ns
MEMORY CHARACTERISTICS						
t_{PROG}				27		ms
Write/Erase Cycles				20,000		Cycles
Data Retention		T_A = +25°C		100		Years

Electrical Characteristics (continued)

(V_{DDQ} = V_{DD_CORE}, limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI ELECTRICAL CHARACTERISTICS (Figure 6)						
SPI Slave Operating Frequency	$1/t_{SCK}$	$f_{CK} = f_{HFXIN}$			$f_{CK}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω	8.3		23.6	ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSEL Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns
MOSI Input to SCLK Sample Edge Rise Setup	t_{SIS}		t_{SPI_RF}			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{SPI_RF}			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				$2t_{SPI\_RF}$	ns
SSEL Inactive	t_{SSH}	$f_{CK} = 1/f_{HFXIN}$	$t_{CK} + t_{SPI\_RF}$			ns
SCLK Inactive to SSEL Rising	t_{SD}		t_{SPI_RF}			ns
MISO Output Disabled After SSEL Edge Rise	t_{SLH}	$f_{CK} = 1/f_{HFXIN}$			$2t_{CK} + 2t_{SPI\_RF}$	ns
SSEL Rising to Active BUSY	t_{SAB}		2			µs
SCLK Delay Between Bytes	t_{SDLY}			3		µs
SHA-256 ENGINE						
Computation Time	t_{CSHA}			10		ms
Authentication Time	t_{AUTH}			196		ms

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. **V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$**; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG FRONT-END (APPLIES TO PINS 33 TO 51)						
Supply Voltage	V_{DD}	3.3V	3.3	3.45	3.6	V
		5.0V (Note 4)	4.5	5.0	5.5	
Sleep Mode Current (SLEEP)	I_{PD}			1	5	µA
Supply Current Excluding Antenna Driver Current	I_{ON}	3.3V (Note 5)		8.5	12	mA
		5.0V		12	20	
AGD Level	V_{AGD}	3.3V (Note 5)	0.7	1.3	1.6	V
		5.0V	2.3	2.5	2.7	
Power-On Reset Level	V_{POR}	3.3V		2.1		V
		5.0V	1.4	2.1	3.6	
ANTENNA DRIVERS						
Driver Output Impedance (ANT1 or ANT2)	R_{AD}	3.3V, I_{ANT} = 100mA, 100% modulation index	4	9.3	15	Ω
		3.3V, I_{ANT} = 30mA, 10% modulation index	5	11	20	
		5.0V, I_{ANT} = 100mA, 100% modulation index	3	7	12	
		5.0V, I_{ANT} = 100mA, 10% modulation index	5	10	15	
SPECIAL-PURPOSE PINS (SYSAOUT, SYSBOUT, SYSCOUT, SYSDOUT, SYSEOUT)						
Input Low Voltage	V_{IL}				0.2 x V_{DD}	V
Input High Voltage	V_{IH}		0.8 x V_{DD}			V
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.1 x V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	0.9 x V_{DD}			V
Interface Clock Rate Frequency (SYSCOUT)	f_{MAX}				1	MHz
AM DEMODULATION						
RF Amplitude of RFIN Inputs	V_{RFIN}	3.3V		1.65		V_{PP}
		5.0V		2.5		
RFIN Input Resistance	R_{RFIN}	3.3V, 5.0V	5	15.5	20	kΩ
Receiver Sensitivity at 212kHz	V_{SENS}	3.3V		0.75		mV_{PP}
		5.0V		1.5		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. **V_{DD} = V_{DDA1} = V_{DDA2} = $V_{DD\_AFE\_DIG}$**; V_{SS} = V_{SSA1} = V_{SSA2} = 0V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Sensitivity at 24kHz	V_{SENS}	3.3V		0.8		mV_{P-P}
		5.0V		2.2		
Receiver Sensitivity at 848kHz	V_{SENS}	3.3V		1.95		mV_{P-P}
		5.0V		3.5		
Recovery Time of Reception after Antenna Modulation	t_{REC}				100	µs
XTAL OSCILLATOR (OSCIN, OSCOUT)						
Transconductance	g_M	3.3V, normal mode		0.45		mS
		3.3V, high-oscillator mode		2		
		5.0V, normal mode (Notes 6 and 7)		0.9		
		5.0V, high-oscillator mode (Note 7)		2.7		
Set-Up Time after Power Down	t_{SET}			5	15	ms
Input Crystal Capacitance	C_{INPUT}	Not production tested		22		pF

Note 3: Any tolerant I/O pin, when an input with no internal weak pullup, can reach a peak static current of 45µA (typ) at V_{DD_CORE} + 0.4V.

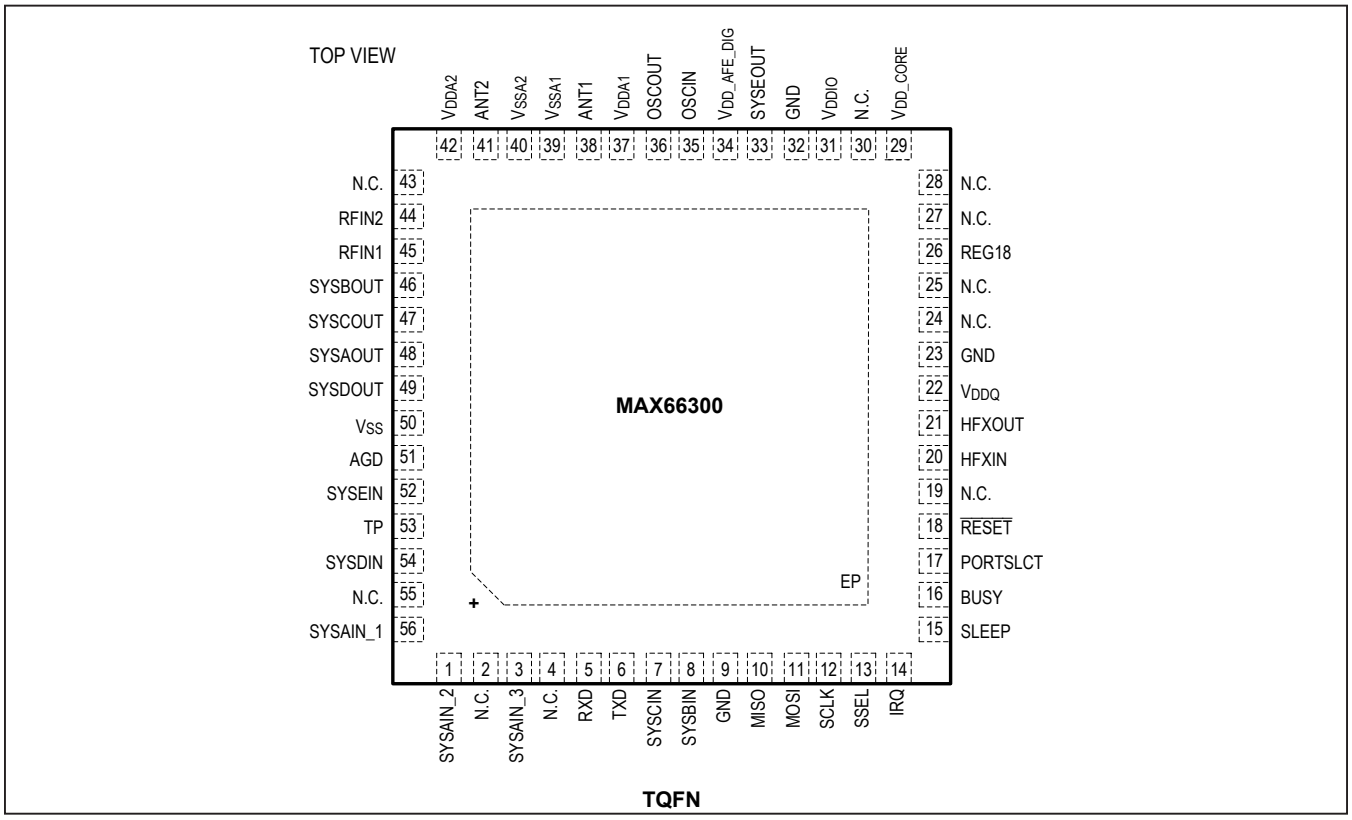
Note 4: Due to the 10kΩ ±5% resistor pullups on pins SYSBIN, SYSCIN, and SYSEIN in 5V operation, V_{DD_CORE} needs to be present at or before $V_{DD\_AFE\_DIG}$.

Note 5: Includes external 1.8kΩ ±5% resistor connected on AGD output to fix a voltage on the pin of 1.3V.

Note 6: Recommended to use the high g_M transconductance (i.e., high oscillator mode).

Note 7: Recommended to use the following crystal electrical parameters: quality factor min of 26,000, series resistance typical of 20Ω, and a static capacitance typical of 2.8pF.

Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	SYSAIN_2	Special-Purpose Pin. Must be connected to SYSAOUT. This pin is 5V tolerant.
2, 4, 19, 24, 25, 27, 28, 30, 43, 55	N.C.	No Connection
3	SYSAIN_3	Special-Purpose Pin. Must be connected to SYSAOUT. This pin is 5V tolerant.
5	RXD	UART Receive. Data input from host. This pin is 5V tolerant.
6	TXD	UART Transmit. Data output to host. This pin is 5V tolerant.
7	SYSCIN	Special-Purpose Pin. This pin must be connected to SYSCOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
8	SYSBIN	Special-Purpose Pin. This pin must be connected to SYSBOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
9	GND	Digital Ground

Pin Description (continued)

PIN	NAME	FUNCTION
10	MISO	Master In-Slave Out. The MISO pin is used to transfer data out of the MAX66300. During a read cycle, data bytes are shifted out on this pin after the falling edge of the serial clock. This pin is 5V tolerant.
11	MOSI	Master Out-Slave In. The MOSI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock. This pin is 5V tolerant.
12	SCLK	Serial Clock. The SCLK pin is used to synchronize the communication between host processor (master) and the MAX66300. Data bytes present on the MOSI pin are latched on the rising edge of the clock input, and data bytes on the MISO pin are updated after the falling edge of the clock input. This pin is 5V tolerant.
13	SSEL	Slave Select. A low level on the SSEL pin selects the device; a high level deselects the device. When the MAX66300 is deselected, MISO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. This pin is 5V tolerant.
14	IRQ	Interrupt Out. This pin drives low when an interrupt has occurred. Otherwise, the pin is in high impedance. This pin is 5V tolerant.
15	SLEEP	Sleep Mode In. This pin is used to put the device into low-power mode when set low. This device comes out of low-power mode and into normal operation within 20ms of transition from low to high logic state. This pin is 5V tolerant.
16	BUSY	Busy Out. This pin indicates a transaction is in progress when driving high and that no messages should be sent to the device. When driving low, the device is ready to accept new messages. Note in UART mode, BUSY in not required since communication is asynchronous.
17	PORTSLCT	Port Select In. After a reset, this pin is sampled within 20ms. If the sample detects logic-low, the UART port is enabled and the SPI port is disabled. If the sample detects logic-high, the SPI port is enabled and the UART port is disabled. This pin is 5V tolerant.
18	$\overline{\text{RESET}}$	Active-Low Reset. This bidirectional pin recognizes external active-low reset inputs and uses an internal pullup resistor to allow for a combination of wired-OR external reset sources. An RC is not required for power-up, as this function is provided internally. This pin also acts as an output when the source of the reset is internal to the device (e.g., exception handling of an incorrect message, etc.). In this case, the pin is low while the processor is in a reset state, and returns high as the processor exits this state. This pin is 5V tolerant.
20	HFXIN	High-Frequency Crystal Input/Output. Connect an external 24MHz crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, if a more accurate external system clock is available, HFXIN can be the input for a 24MHz clock source when HFXOUT is unconnected.
21	HFXOUT	
22	V_{DDQ}	Digital Supply. Connect to V_{DDIO} through a 50Ω 1µF capacitor filter.
23	GND	Digital Ground
26	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.
29	V_{DD_CORE}	Digital Core Supply Voltage. +3.3V nominal supply voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
31	V_{DDIO}	Switched I/O Power Supply (Internally Connected to V_{DD_CORE}). This output pin must be connected to ground through a 1.0µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices or power rail other than the capacitor and V_{DDQ} through a filter should be connected to this pin.
32	GND	Digital Ground
33	SYSEOUT	Special-Purpose Pin. This pin must be connected to SYSEIN.
34	$V_{DD\_AFE\_DIG}$	Digital Supply Voltage for the Analog Front-End. This pin can operate at 3.3V or 5V. This pin has to be the same voltage potential as V_{DDA1} and V_{DDA2}. This pin must be connected to ground through a 0.1µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.
35	OSCIN	Quartz Oscillator Input/Output. These pins are driven by an external crystal oscillator to generate the needed RF frequencies for the analog front-end. These pins require a standard 13.56MHz ±7kHz quartz crystal. A CoG-rated capacitor should be used for loading with a typical value of 22pF for each pin.
36	OSCOUT	
37	V_{DDA1}	Positive Supply for Antenna Driver. This pin is to be separately filtered from any of the digital supplies and lumped together with V_{DDA2}. Variations in this supply voltage directly modulate the antenna driver and effect the receiver's input. The power-supply sensitivity range, for frequency components that are in the receiving bandwidth, is the same as the RFIN sensitivity. The ground pins used for V_{DDA1} and V_{DDA2} of the antenna driver are V_{SSA1} and V_{SSA2} (see note).
38	ANT1	RF Output (10Ω Output Impedance). This pin is the output of the antenna driver. Connect to external antenna components.
39	V_{SSA1}	Negative Supply for Antenna Driver (0V). This pin is the ground pin for the antenna driver. This pin is to be separately filtered from any of the digital supplies and lumped together with V_{SSA2}.
40	V_{SSA2}	Negative Supply for Antenna Driver (0V). See the V_{SSA2} pin description.
41	ANT2	RF Output (10Ω Output Impedance). This pin is the output of the antenna driver. Connect to external antenna circuit.
42	V_{DDA2}	Positive Supply for Antenna Driver. See the V_{DDA1} pin description (see note).
44	RFIN2	RF Input PM (maximum $5V_{P-P}$, DC-coupled to AGD). These two input pins are to be connected with external components to detect the amplitude or phase modulated signals.
45	RFIN1	
46	SYSBOUT	Special-Purpose Pin. This pin must be connected to SYSBIN.
47	SYSCOUT	Special-Purpose Pin. This pin must be connected to SYSCIN.

Pin Description (continued)

PIN	NAME	FUNCTION
48	SYSAOUT	Special-Purpose Pin. Must be connected to SYSAIN_1, SYSAIN_2, and SYSAIN_3.
49	SYSDOUT	Special-Purpose Pin. Must be connected to SYSDIN.
50	V_{SS}	Ground (Analog Ground of RF AFE)
51	AGD	Reference Voltage Output 2.5V. This pin is to be connected to a 0.1µF X7R capacitor to ground when $V_{DD\_AFE\_DIG}$ is 5V. This pin is to be connected to an external resistor to ground to fix the voltage at 1.3V when $V_{DD\_AFE\_DIG}$ is 3.3V.
52	SYSEIN	Special-Purpose Pin. This pin must be connected to SYSEOUT. Also, this pin must be pulled up with a 10kΩ ±5% resistor to the same voltage potential as $V_{DD\_AFE\_DIG}$.
53	TP	Test Pin. This pin is to be pulled up for standard operation to V_{DD_CORE}.
54	SYSDIN	Special-Purpose Pin. Must be connected to SYSDOUT. This pin is 5V tolerant.
56	SYSAIN_1	Special-Purpose Pin. This pin must be connected to SYSAOUT. This pin is 5V tolerant.
—	EP	Exposed Pad

Note: Decouple $V_{DDA1/2}$ to $V_{SS1/2}$ with the following types of capacitors; use C0D ceramic technology (±5%) for the 10nF capacitors, use X7R ceramic technology (±10%) for the 100nF capacitors, and use tantalum electrolytic technology for the 3.3µF capacitors.

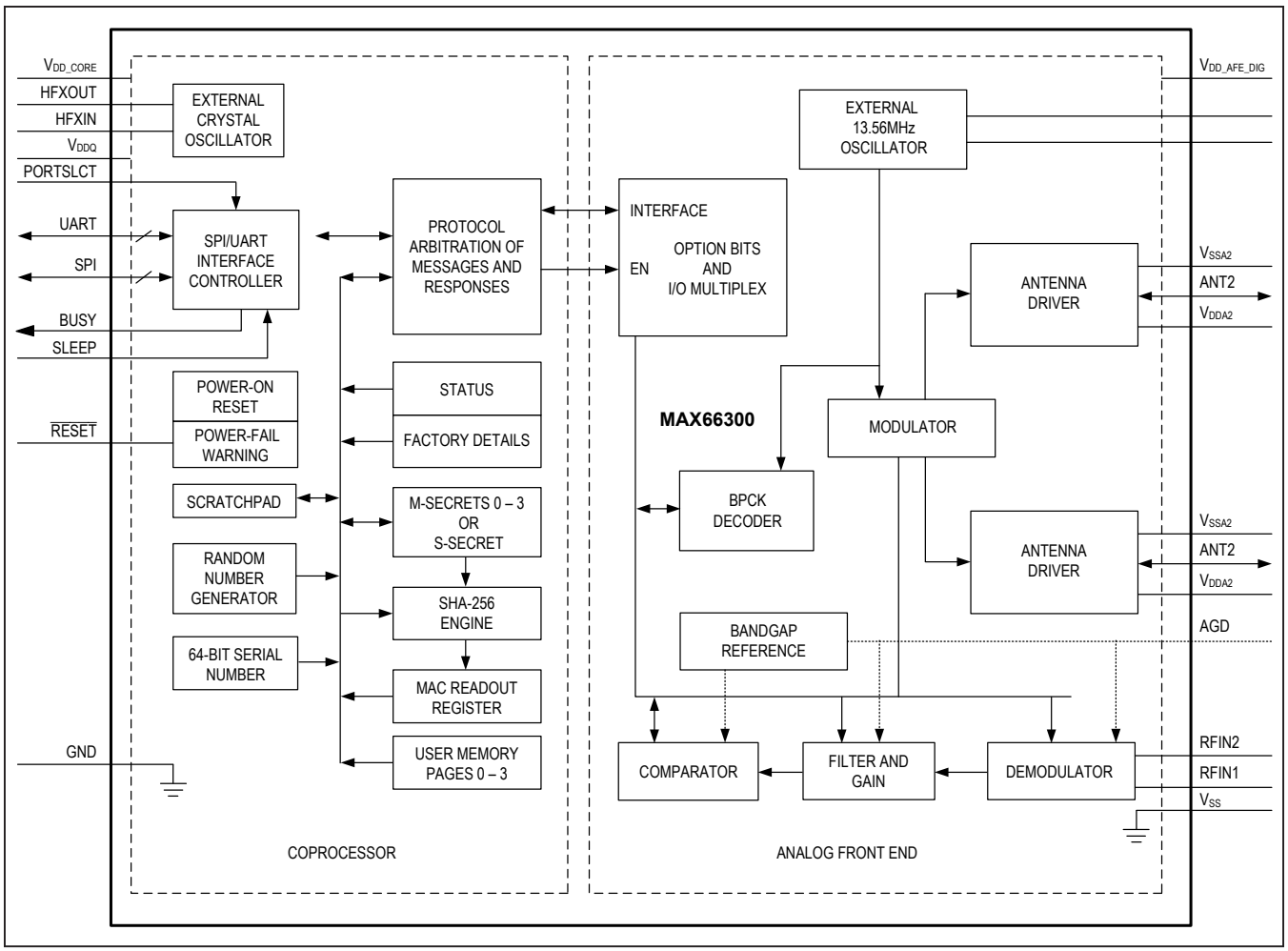


Figure 1. Block Diagram

Detailed Description

The RFID reader's analog front-end (AFE) function is highly integrated into the MAX66300 to support contactless communication at 13.56MHz for compliancy with the ISO/IEC 15693 standard. The host configures this reader with ease and flexibility. This is accomplished through single configuration byte writes to the AFE. The AFE operates at 3.3V or 5V. The reader's push-pull transmitter generates up to 200mW output RF power depending on the antenna configuration design selected. The output stage drivers are capable of on-off keying (OOK) and amplitude shift keying (ASK) modulation from 7% up to 30% of AM modulation. See Figure 1 for a block diagram.

The MAX66300 has a built-in SHA-256 engine and user memory space divided into four pages. Its core operates at 3.3V with 5V tolerant I/O. The device's coprocessor computes a unique slave secret (S-Secret) from any one of four master secrets (M-Secrets) and additional data. Once the S-Secret is computed, the coprocessor computes slave authentication MACs (to verify a tag's authenticity). The same S-Secret in the coprocessor generates slave write MACs. For example, a slave-write MAC permits writing to the memory and protection registers of a secure memory in a tag. If the memory is not write-protected, a new M-Secret can be loaded directly and additional data. In addition, the coprocessor can perform a slave authentication from knowing the MAX66240/42's tag UID with a single message and response, greatly relieving the host's burden. This only requires that both the MAX66300 and MAX66240/42 have been properly set up with secrets. This can be achieved by using Maxim's preprogramming service.

General Message Format

The command and response messages are transmitted and received using either the UART or SPI interface. The MAX66300 periodically analyzes the UART/SPI receive buffer, decodes its content, and then performs the requested action on a valid message. Each request has a corresponding reply. This reply can be a valid response message or an error message if an issue was found with the request message. The reader does not process a new request until it has replied to the currently request. In other words, request messages cannot be intermingled. The SPI data reception performs in a similar fashion, as the UART, except the host, after issuing a message command, must read out the response message before proceeding with the next command message.

Message Format

All command and response messages follow the following structure:

- Byte [0] = STX = 02h
- Byte [1] = Index of Checksum Byte = last -1
- Byte [2] = Command/Response Identification (ID)
- Byte [3..last-2] = Payload (consists of ISO standard)
- Byte [last-1] = XOR Checksum = Byte[1] XOR Byte[2] XOR . . . XOR Byte[Last-2]
- Byte [last] = ETX = 03h

Host to MAX66300—Command Message

STX (02h)	Index of Checksum	Command ID*	Write Payload	Checksum	ETX (03h)

MAX66300 Reader to Host—Response Message

STX (02h)	Index of Checksum	Response ID*	Read Payload	Checksum	ETX (03h)

***Note:** The Command ID and Response ID are normally equal unless a General Error has occurred.*

Acknowledge Status Byte (ACK)

If the ACK is set to 00h, it signalizes a successful execution of the command; otherwise, non-zero ACK values signalize errors or other useful information. Interface UART or SPI port errors are common to all the commands. This indicates a problem during host to/from MAX66300 reader communication or protocol errors.

Table 1. Acknowledge Status Byte (ACK)

ACK	NAME	DESCRIPTION
00h	MESSAGE_OK	All parts (OK)
01h	ERR_ASIC_ANTENNA_FAULT	Reader (timeout during capture process, invoked by watchdog)
:	RFU	Reserved for Future Use
04h	ERR_IF_ERROR_FLAG	Interface UART or SPI (none or wrong STX, parity error)
05h	ERR_OVERFLOW	Interface UART or SPI (receive buffer overflow)
06h	RFU	Reserved for Future Use
07h	ERR_BAD_CRC	Interface SPI or UART (Wrong CHK)
08h	ERR_UNKNOWN_CMD	Interface SPI or UART (Unknown command)
09h	ERR_NO_ETX	Interface SPI or UART (No ETX)
0Ah	ERR_INTERBYTE_ERR	Interface SPI or UART (message length is out of range, message length is wrong with this command)

Table 1. Acknowledge Status Byte (ACK) (continued)

ACK	NAME	DESCRIPTION
0Bh	ERR_WRONG_LEN	Reader (Wrong Response Length, not enough data, wrong demodulation parameters)
0Fh	RFU	Reserved for Future Use
10h	ERR_RAW_DATA	Reader (response contains raw data)
11h	ERR_CAPT_DATA	Reader (response contains captured data pairs)
12h	ERR_NO_TAG	Reader (no UID found)
13h	ERR_BAD_CRC	Reader (bad response CRC)
14h	RFU	Reserved for Future Use
15h	ERR_NO_SOF	Reader (no response received at all)
:	RFU	Reserved for Future Use
50h	ERR_A_GETUID_REQA_FAILED	Reader (Get UID REQA failed)
51h	RFU	Reserved for Future Use
52h	ERR_A_GETUID_SEL0_FAILED	Reader (Get UID – Sel of 1st cascade failed)
53h	ERR_A_GETUID_SEL1_FAILED	Reader (Get UID – Sel of 2nd cascade failed)
54h	ERR_A_GETUID_SEL2_FAILED	Reader (Get UID – Sel of 3rdcascade failed)
55h	ERR_A_GETUID_SELECT0_FAI	Reader (Get UID – Select of 1st cascade failed)
56h	ERR_A_GETUID_SELECT1_FAI	Reader (Get UID – Select of 2nd cascade failed)
57h	ERR_A_GETUID_SELECT2_FAI	Reader (Get UID – Select of 3nd cascade failed)
58h	ERR_A_GETUID_SELECT0_CRC	Reader (Get UID – Select of 1st cascade CRC failed)
59h	ERR_A_GETUID_SELECT1_CRC	Reader (Get UID – Select of 2nd cascade CRC failed)
5Ah	ERR_A_GETUID_SELECT2_CRC	Reader (Get UID – Select of 3rd cascade CRC failed)
:	RFU	Reserved for Future Use
60h	ERR_DATA_PROTECTED	Coprocessor (Memory is protected and cannot be written)
61h	ERR_NOT_AUTH	Coprocessor determined the MAX66240/42 tag to not be authentic
62h	ERR_AUTH_INCOMPLETE	Coprocessor authentication of MAX66240/42 tag not complete
63h	ERR_WRONG_PB	Wrong Parameter Byte used
:	RFU	Reserved for Future Use
FEh	INVENTORY_FINISHED	Reader (No other tags – 1TS Inventory algorithm finished)
FFh	RFU	Reserved for Future Use

Coprocessor Commands and Response Messages

Each command sent by the MAX66300 to the tag is initialized by the host application. The MAX66300 supports two command/response sets of the following groups or protocol standards:

- ISO 15693 commands/responses
- Reader control commands and responses (i.e., includes SHA-256 subcommands used with MAX66240/42)

The MAX66300 can utilize the arbitrary data field portion (i.e., data byte items) of the command to further perform a specific operation (e.g., the flag byte is always used in ISO 15693 commands, the command byte and other special information).

Communication Protocol—Color Codes

Host to MAX66300	MAX66300 to Host	Common between Host and MAX66300	Host waits (MAX66300 busy)

Table 2. Message Communication Protocol—Legend

COMMON TO COMMAND/RESPONSE MESSAGES	
STX	Start of Message Transmission, 02h
ICK	Index of Checksum
ACK	Acknowledge – Typically is a Message OK (00h) or other useful information.
ACKE	Acknowledge Error – ACK Byte that indicates an error has occurred.
CHK	Checksum of Message response by MAX66300
ETX	End of Message, 03h
COMMAND/RESPONSE IDENTIFICATION	
ISO 15693 COMMANDS	
INVST	1TS Inventory with Self-Tuning, 80h
INVRSTST	1TS Inventory with RF Reset with Self-Tuning, 81h
INVRST	1TS Inventory with RF Reset, 82h
INV	1TS Inventory, 83h
SQT	Stay Quiet, 85h
GRD	General Read, 88h
GWR	General Write, 90h
READER CONTROL COMMANDS	
CPW	Coprocessor Write command, E0h
CPR	Coprocessor Read command, E1h
RFR	RF Reset, F0h
AFEW	AFE Write, F1h
AFEWR	AFE Write with RF Reset, F2h
SDD	Send Debug Data, F6h
GRD	Get Raw Data, F7h
GCD	Get Capture Data, F8h
TDM	Toggle Debug Mode, F9h
RS	Reader Status, FDh
SCOF	Switch Coil On/Off, FEh
GERR	General Error, (Response ID field will be 00h)
ADDITIONAL PAYLOAD AFTER COMMAND/RESPONSE ID THAT ARE NOT SUBCOMMANDS	
CP	Command Parameter for Command IDs
$CFGW_n$	Configuration Word (Option bits) for AFE (n = 0–3)
$CFGW_n$	Configuration Word (Option bits) for AFE (n = 0–3)

Table 3. ISO 15693 Communication Protocol—Legend

AFI	Application Family Identifier
UID_n	Unique Identifier byte of the Tag per ISO/IEC 15693-3 Section 4.1 (n = 0–7)
UID_k	Unique Identifier of all 8 bytes(LSB first) of the Tags (k = 0–7 UIDs)
DSFID	Data Storage Format Identifier – 8 bits
CRC16	Cyclic Redundancy Check (2 bytes with LSB first) per ISO 13239
SOF	Start Of Frame

Table 4. Coprocessor Subcommands—Legend

COPROCESSOR SUBCOMMAND CODES	
ADM	Subcommand for “Access Data Memory”, 5Ah
CSS	Subcommand for “Compute S-Secret”, 4Bh
CSAM	Subcommand for “Compute Slave Authentication MAC”, 3Ch
CSWM	Subcommand for “Compute Slave Write MAC”, 2Dh
CNMS	Subcommand for “Compute Next M-Secret”, 69h
SPR	Subcommand for “Set Protection”, 1Eh
PRS	Subcommand for “Protection Status”, 0Fh
RFD	Subcommand for “Read Factory Details”, F0h
AUTH	Subcommand for “Authenticate Tag (MAX66220/42)”, E1h
GRN	Subcommand for “Get Random Number”, D2h
GSN	Subcommand for “Get 64-bit Serial Number”, C3
CPM	Subcommand for “Coprocessor Manager”, B2
ADDITIONAL PAYLOAD AFTER SUBCOMMAND	
PB	Parameter byte, always follows the subcommand abbreviation
UID_n	Unique Identifier byte of the Tag per ISO/IEC 15693-3 Section 4.1 (n = 0–7)
MAC_0	First byte of Message Authentication Code (H_7[0–7]) sent by the device
MAC_{31}	Last byte of Message Authentication Code (H_0[24–31]) sent by the device
MPS_n	Memory Protection Status byte sent by the device (n = 0–3)
RB_n	Random Byte sent by the device (n = 0–255)
SN_n	Serial Number byte sent by device (n = 0–7)

Table 5. UART Communication Protocol—Legend

$BYTE_0$	First byte of multibyte data sent by the host
$BYTE_n$	Last byte of multibyte data sent by the host (n = specific # if possible)
$BYTE_0$	First byte of multibyte data response by the device
$BYTE_n$	Last byte of multibyte data response by the device (n = specific # if possible)

Table 6. SPI Communication Protocol—Legend

SSEL	Slave Select Asserted by the host
DSEL	De-asserted Slave Select by the host
$BYTE_0$	First byte of multibyte data sent by the host
$BYTE_n$	Last byte of multibyte data sent by the host (n = specific # if possible)
$BYTE_0$	First byte of multibyte data response by the device
$BYTE_n$	Last byte of multibyte data response by the device (n = specific # if possible)

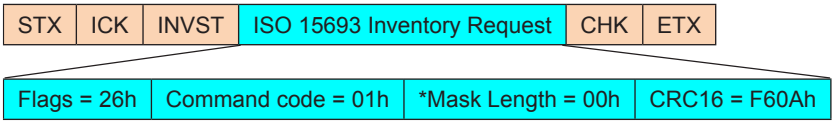
ISO 15563 Commands

1TS Inventory with Self-Tuning	
Command/Response ID	80h
Usage	The 1TS Inventory with Self-Tuning command is an implementation of the 1TS Inventory command (83h) with an additional feature that adjusts the Configuration Word for improved RF Field tuning. A one time slot inventory algorithm is used to search for active tags present in the RF Field while improving on tag reception if needed during the search.
Command Parameter	None
Requires	The ISO 15693 inventory request format requires the Flags field to have the inventory flag set. The MAX66300 requires the Mask Length field (i.e., mask_length) equal '0'. Therefore, the Mask Value field is not present in the ISO 15693 inventory request format sent to MAX66300. The AFI field is optional.
Other Notes	1TS Inventory with Self-Tuning routine is started with the default AFE Configuration word. During the routine loop (see Figure 2), if the aux_nothing counter value exceeds its limit or if the noise is detected, the AFE Configuration Word is changed to one of three AFE constants by calling the self-tuning subroutine. These three AFE Configuration Words were selected to have the best data reception level either for ISO card sized tags or for small sized tags. At the end of the routine, the default (i.e., before this command was ever called) AFE Configuration Word is restored. The result is that each response contains the actual AFE Configuration Word that found the particular tag followed by its UID and an additional last response containing ACK = FEh that indicates the inventory search is finish. The responses received are usually one of the following results: 1. All the tags were found with a single (default) Configuration Word – no action is necessary 2. All the tags were found with a single (nondefault) Configuration Word – the received configuration word has to be used (See AFE Write, F1h) to communicate with these tags. 3. All the tags were found with more than one Configuration Word – the inventory process encountered a low reception level during the communication with all the tags. It is recommended to remove some tags from the RF field and repeat the inventory process with self-tuning. 4. No tag was found – no information can be stated. It is important for the host to properly take action as to handle these responses. The derivation of the actual three AFE Configuration Words used for self-tuning differ in only the Gain settings so the most feasible reception settings are configured during the inventory process. By means of such derivation, either the OOK or the ASK uplink modulation can be achieved.
Command Restrictions	One time slot ASK is supported only. Inventory routine is not based on a detection of the collision position. It performs a binary tree search.
ACK Error Conditions (Error Response)	INVENTORY_FINISHED (FEh)
Accessed Items	Flag byte, AFI value
UART/SPI Busy Duration	None

ISO 15693 Inventory with Self-Tuning

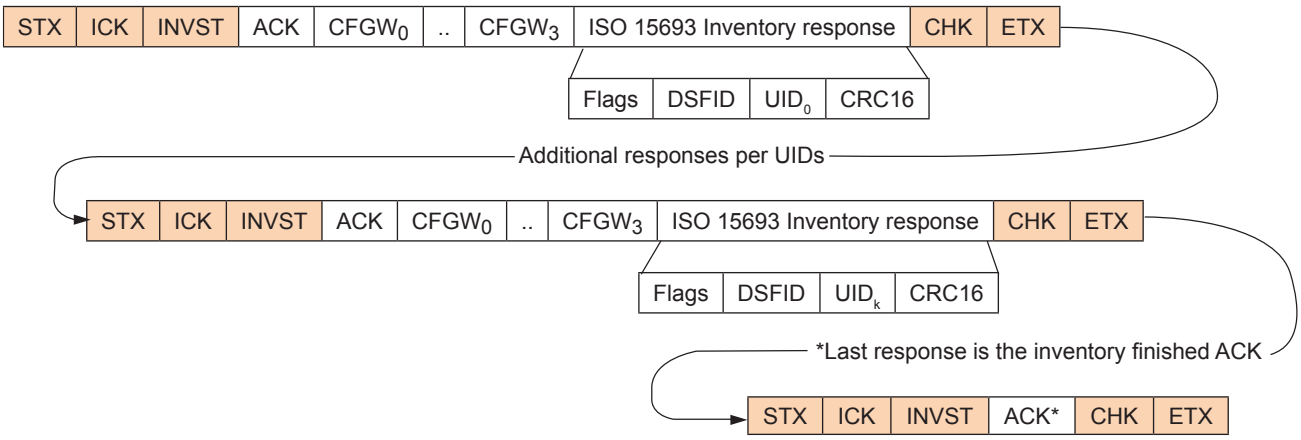
UART:

(Request)



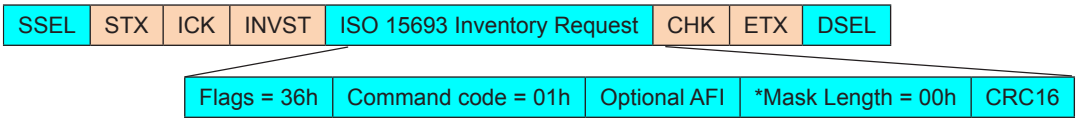
*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



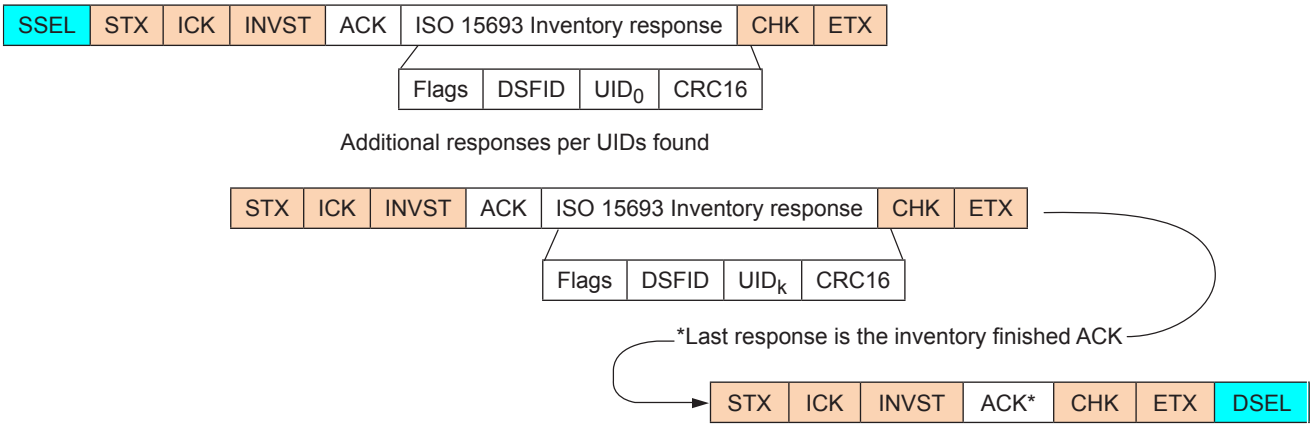
SPI (assume MOSI = FFh during MISO output):

(Request)



Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



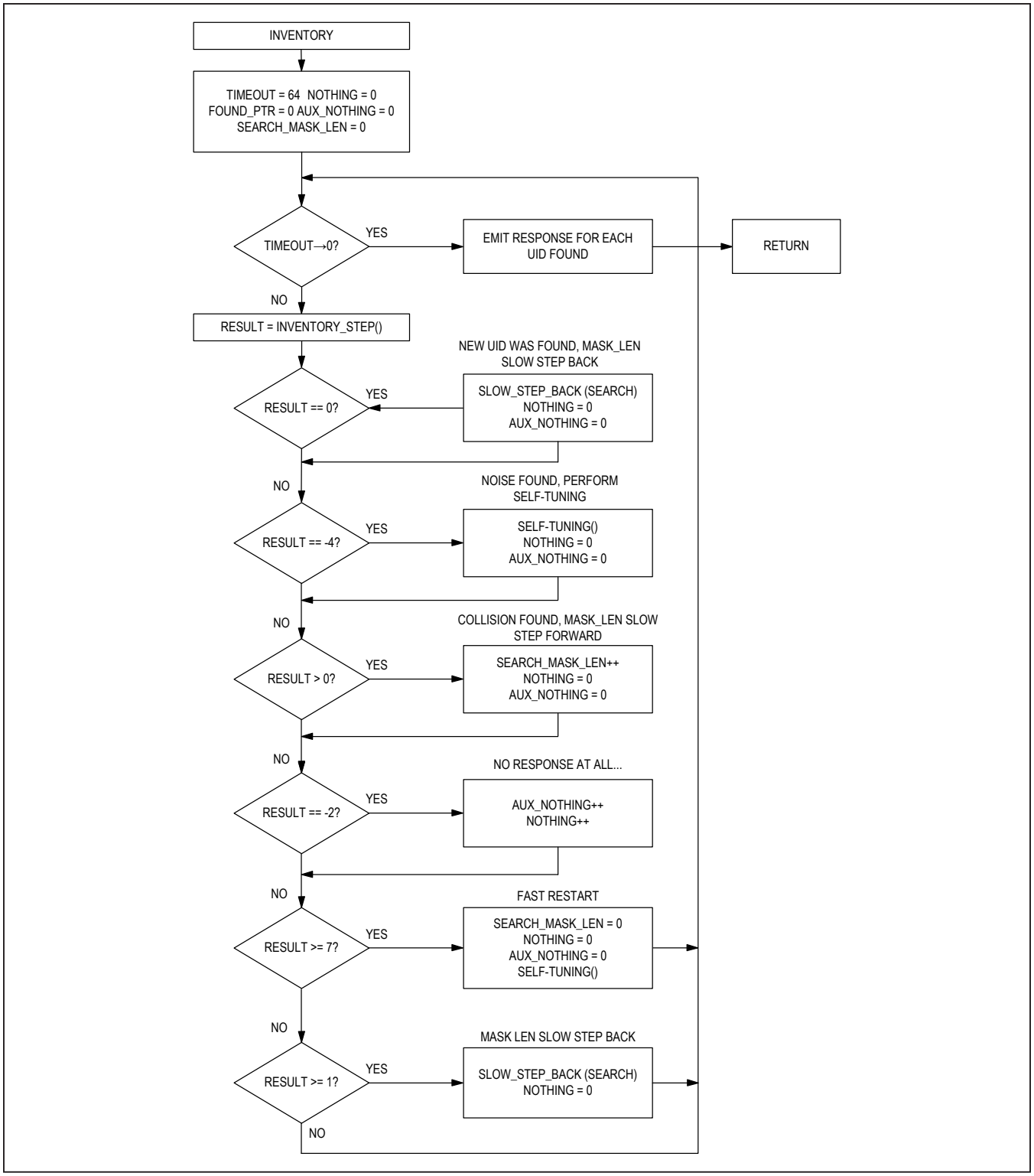


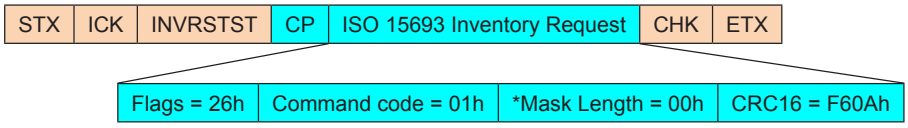
Figure 2. Inventory with Self-Tuning Flow

1TS Inventory with RF Reset and Self-Tuning	
Command/Response ID	81h
Usage	The 1TS Inventory with RF Reset and Self-Tuning command is a combined command implementation of 1TS Inventory with Self-Tuning (80h) and RF Reset (F0h) commands. This is used to first reset the RF field and then, with the one time slot inventory algorithm, search for active tags present in the RF Field and improve on tag reception if needed.
Command Parameter	RF Reset, sets the time interval. See the RF Reset (F0h) command for details on time interval increments (Table 17).
Requires	The ISO 15693 inventory request format requires the Flags field to have the inventory flag set. The MAX66300 requires the Mask Length field (i.e., mask_length) equal 0. Therefore, the Mask Value field is not present in the ISO 15693 inventory request format sent to MAX66300. The AFI field is optional.
Other Notes	See 1TS Inventory with self-tuning (80h) command for details of the Inventory routine used after the RF Reset sets the tag to the Ready state.
Command Restrictions	One time slot ASK is supported only. Inventory routine is not based on a detection of the collision position. It performs a binary tree search.
ACK Error Conditions (Error Response)	INVENTORY_FINISHED (FEh)
Accessed Items	Flag byte, AFI value
UART/SPI Busy Duration	None

ISO 15693 Inventory with RF Reset and Self-Tuning

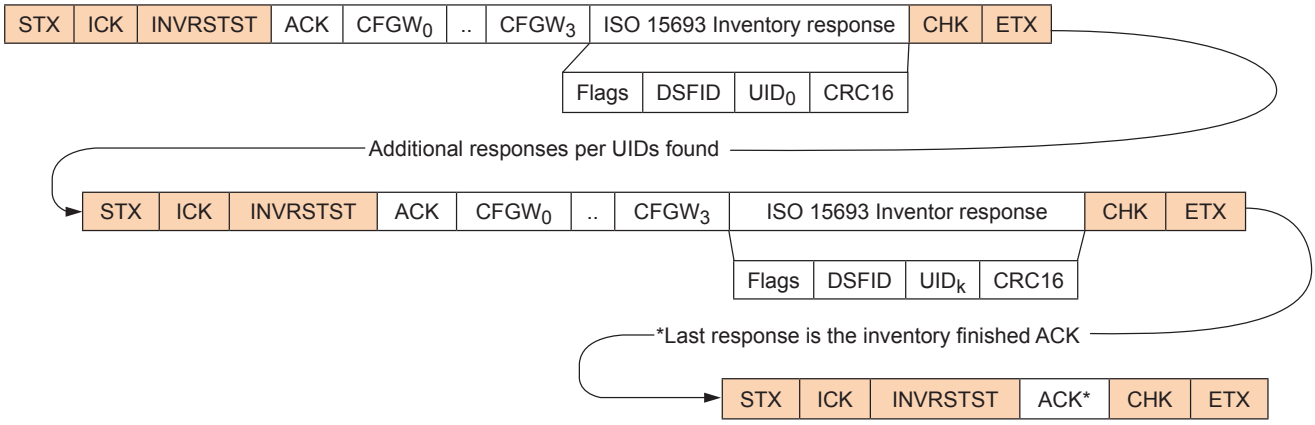
UART:

(Request)



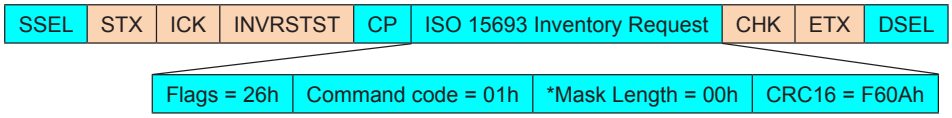
*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



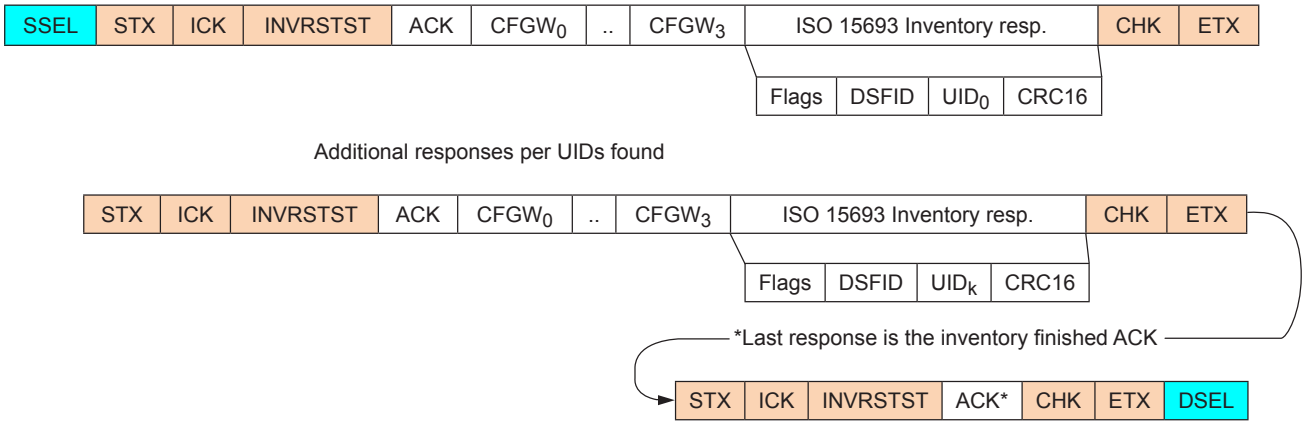
SPI (assume MOSI = FFh during MISO output):

(Request)



*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)

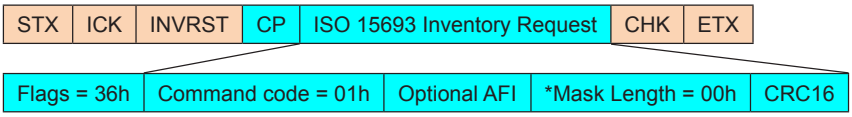


1TS Inventory with RF Reset	
Command/Response ID	82h
Usage	First, the RF Reset is performed so that all the tags are switched to the Ready state due to the loss of power for a time interval. Next, the one time slot inventory algorithm is used to search for active tags present in the RF Field. Response of the command contains one tag UID (actually the response of Inventory command), data item is valid only if ACK = 0. If two or more tags are detected successfully, the same number of responses is generated. The last response contains ACK = FEh only.
Command Parameter	RF Reset, sets the time interval. See RF Reset (F0h) command for details on time interval increments (Table 17).
Requires	The ISO 15693 inventory request format requires the Flags field to have the inventory flag set. The MAX66300 requires the Mask Length field (i.e., mask_length) equal ‘0’. Therefore, the Mask Value field is not present in the ISO 15693 inventory request format sent to MAX66300. The AFI field is optional.
Other Notes	See 1TS Inventory (83h) command for details of the Inventory routine used after the RF Reset sets the tag to the Ready state.
Command Restrictions	One time slot ASK is supported only (one single sub-carrier mode). Inventory routine is not based on a detection of the collision position. It performs a binary tree search.
ACK Error Conditions (Error Response)	INVENTORY_FINISHED (FEh)
Accessed Items	Flag byte, AFI value
UART/SPI Busy Duration	None

ISO 15693 Inventory with RF Reset and AFI Present

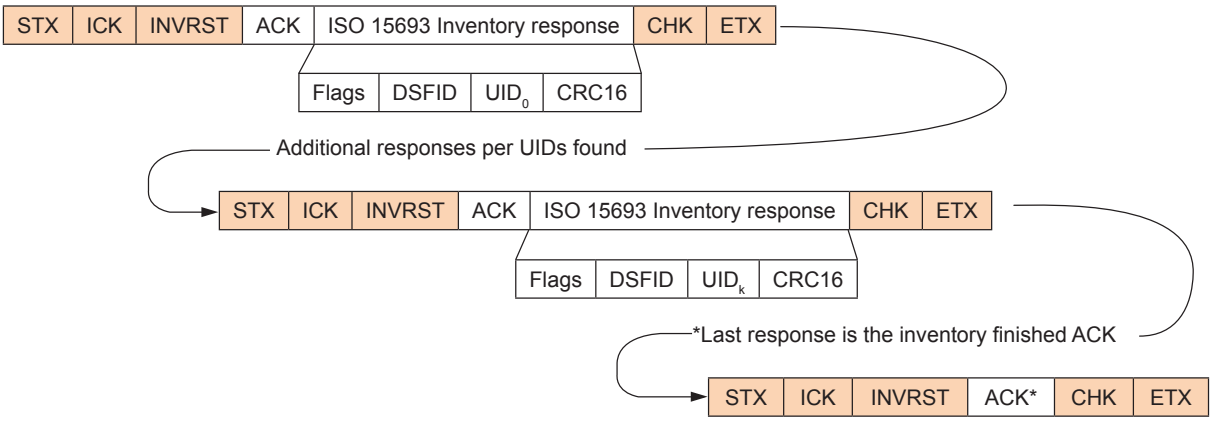
UART:

(Request)



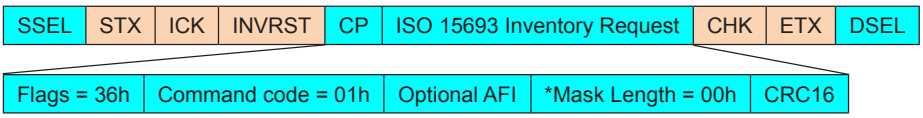
*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



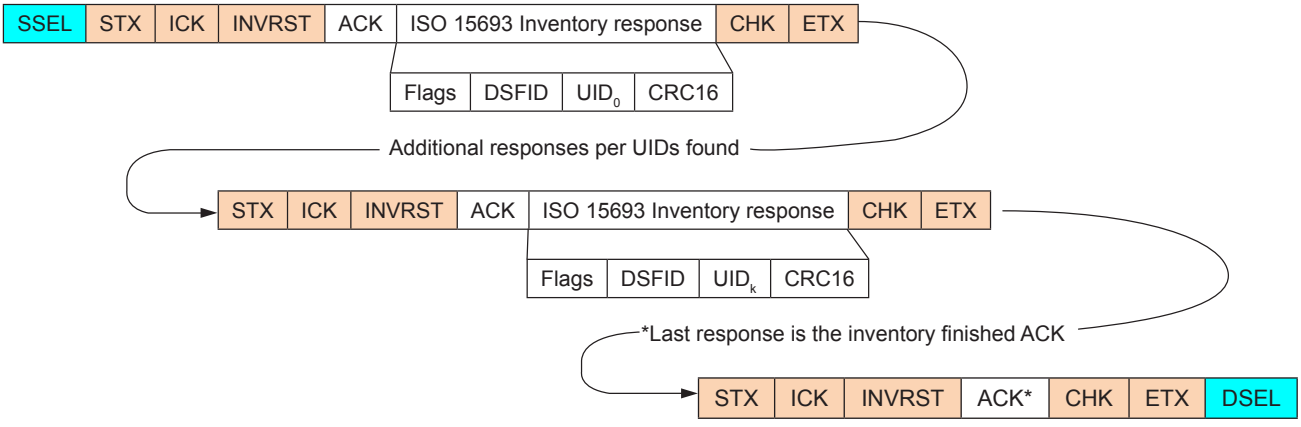
SPI (assume MOSI = FFh during MISO output):

(Request)



*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)

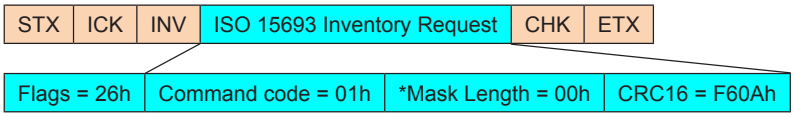


1TS Inventory	
Command/Response ID	83h
Usage	The 1TS Inventory command has a one time slot inventory algorithm used to search for active tags present in the RF Field. Response of the command contains one tag UID (actually the response of Inventory command), data item is valid only if ACK = 0. If two or more tags are detected successfully, the same number of responses is generated. The last response contains ACK = FEh indicating the inventory search is finished.
Requires	The ISO 15693 inventory request format requires the Flags field to have the inventory flag set. The MAX66300 requires the Mask Length field (i.e., mask_length) equal '0'. Therefore, the Mask Value field is not present in the ISO 15693 inventory request format sent to MAX66300. The AFI field is optional.
Other Notes	Inventory routine starts with zero mask length. The routine sends ISO 15693 Inventory request with current mask and mask length settings. According to the result of the response received, the routine updates the mask and the mask length until timeout is reached. 1. If a single UID is found, mask is "stepped back". 2. If a collision is found, mask is "stepped forward" by 1 and additional Inventory commands are sent. UID stack storage buffer is dimensioned for 8 UIDs. 3. If no response is received, mask is "stepped back". If no response is received for all 7 times, the mask length is zeroed causing the search to "fast restart". For more information, refer to the higher level Inventory routine diagram in Figure 3. There are three operations over the mask and mask length used: 1. "Slow step back" is a modification of current mask and mask length so that all branches are traversed. If the last mask bit is 0, it is toggled to 1. Otherwise, (the last mask bit is 1), mask length is decremented by 1 and "slow step back" is repeated. 2. "Slow step forward" is a modification of current mask and mask length so that all the '0' sub-tree is traversed first. The mask length is incremented by 1 and this last mask bit is set to 0. 3. "Fast restart" is a reset of mask length to 0. Inventory_step routine performs a single inventory query. Inventory_step routine builds an ISO 15693 Inventory command according to the current flag byte, AFI value, mask and mask length. It sends it to the tags in the RF field and receives a response. If a clean single tag UID is received, it stores the tag UID into the array of found UIDs, builds and sends a Stay Quiet command to this tag.
Command Restrictions	One time slot ASK is supported only (one single sub-carrier mode). Inventory routine is not based on a detection of the collision position. It performs a binary tree search.
ACK Error Conditions (Error Response)	INVENTORY_FINISHED (FEh)
Accessed Items	Flag byte, AFI value
UART/SPI Busy Duration	None

ISO 15693 Inventory

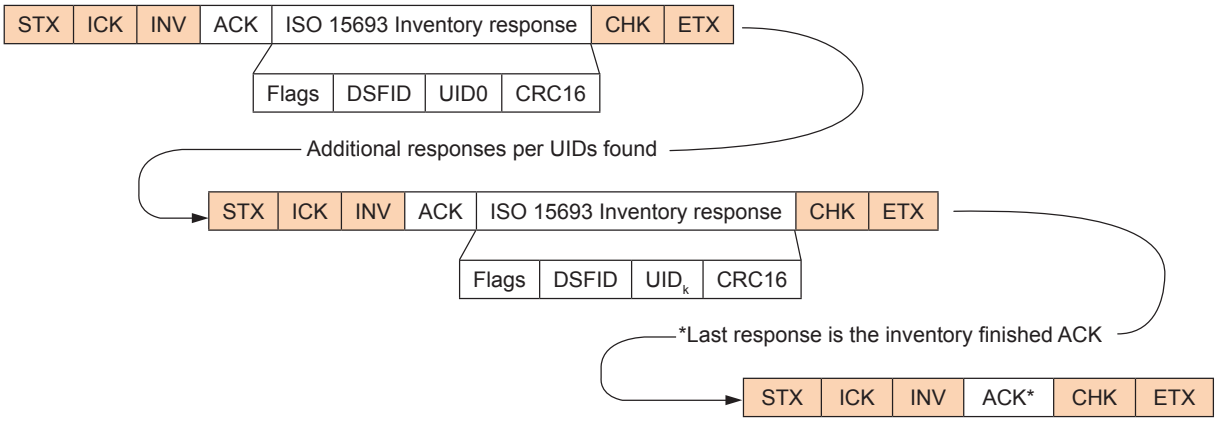
UART:

(Request)



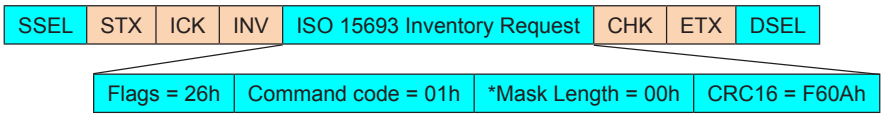
*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



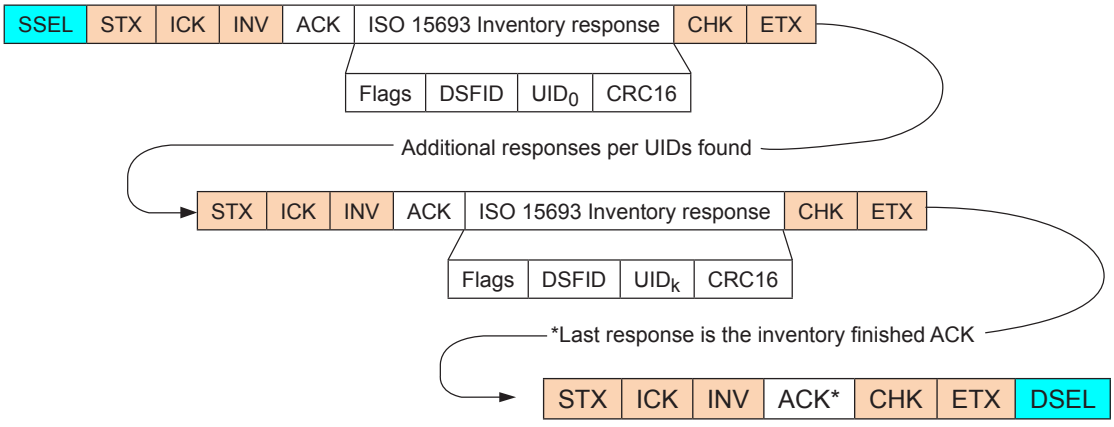
SPI (assume MOSI = FFh during MISO output):

(Request)



*Only Mask Length of 00h is supported. MAX66300 will automatically find up to 8 UIDs by performing a binary tree search.

(Response)



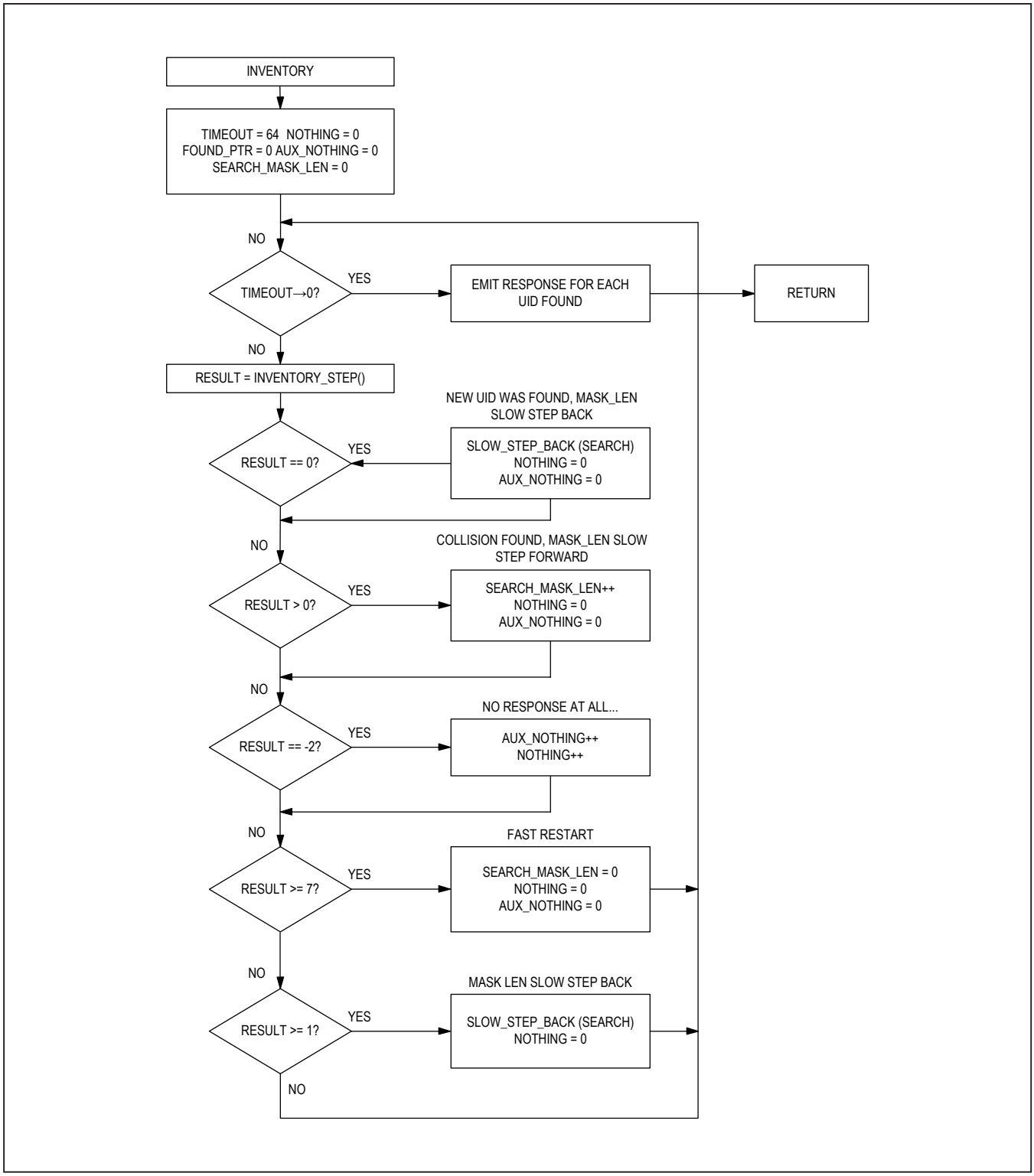


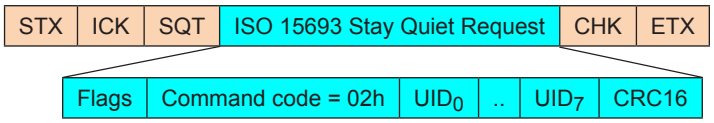
Figure 3. Inventory Flow

Stay Quiet	
Command/Response ID	85h
Usage	The Stay Quiet command places a tag that is in the select state or ready state into the quiet state using the UID. Also, if a tag is already in the quiet state this command will be accepted by the tag and the tag will again be placed in the quiet state.
Command Parameter	None
Requires	The Stay Quiet command is executed in ISO 15693 Addressed mode (i.e., select_flag is set to '0' and address_flag is set to 1). Also, ISO 15693 requires a command code (i.e., 02h) and a UID field used to set the appropriate tag into the quiet state.
Other Notes	When an ISO 15693 tag receives the Stay Quiet command, the tag enters the quiet state and does not send a returning response. The MAX66300 will only return a response ID indicating that whatever I/F (i.e., UART/SPI) ACK is OK.
Command Restrictions	The command will not process a valid message to any tag when the Inventory_flag is set and where the Address_flag is not set as per ISO 15693 standard.
ACK Error Conditions (Error Response)	None
Accessed Items	None
UART/SPI Busy Duration	None

Set Tags to Quiet State

UART:

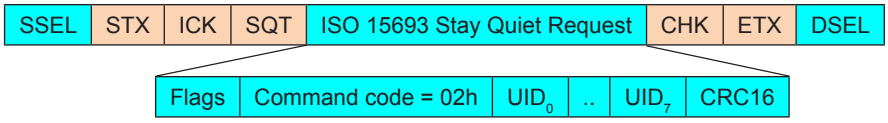
(Request)



(Response)

SPI (assume MOSI = FFh during MISO output):

(Request)



(Response)

General Read	
Command/Response ID	88h
Usage	The General Read command sends the provided formed message from the host to the tag and waits a time t1 of ~318µs (i.e., per ISO 15693-3 section 9) before trying to capture the response. This command is typically used for ISO 15693 Read single block and Read multiple blocks.
Command Parameter	Expected response length in number of bytes per Table 7.
Requires	The host forms the sending message and checks the format, data and CRC as needed per ISO 15693.
Other Notes	The General Read process is the following: 1. MAX66300 sends the formed message provided by the host with this command; waits for time t1 to expire and begins trying to capture the response from the tag. 2. If there is no response from a tag, the ACK error ERR_NO_SOF (15h) will return in the response from the MAX66300 to the host. 3. If no ERR_NO_SOF error, MAX66300 will continue to find and extract the decoded data. 4. If the response contains more than four bytes (i.e., Flags, Error code, CRC16 fields) and the Flags field (i.e., first byte) is not zero, consider the error message is not per the ISO 15593 standard. MAX66300 will return the ACK error ERR_ISO_ERROR_MSG (0Eh) along with the response data to the host. 5. If the number of response data bytes is less than expected from the response length; the MAX66300 returns an ACK error ERR_WRONG_LEN (0Bh) and the decoded response data. 6. If the response is limited to the expected response length number of bytes boundary then MAX66300 returns an ACK equal to zero and the response data to the host.
Command Restrictions	Only supports reading up to 128 bytes.
ACK Error Conditions (Error Response)	ERR_WRONG_LEN (0Bh) ERR_ISO_ERROR_MSG (0Eh) ERR_RAW_DATA (10h) ERR_CAPT_DATA (11h) ERR_NO_SOF (15h)
Accessed Items	Flag byte, command byte
UART/SPI Busy Duration	A time t1 of ~318µs. The tag's response of expected response length is analyzed after the time t1.

Table 7. Command Parameter Byte Bitmap for Response Length

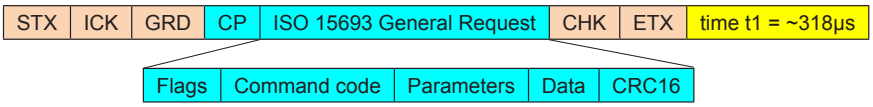
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSPL							

Bits 7:0: Response Length (RSPL). These bits specify the length in number of bytes of the expected response; the value can be from 0 to 80h (i.e., 81h–FFh is RFU). All expected ISO response field bytes are to be included in the response length or an ACK error occurs.

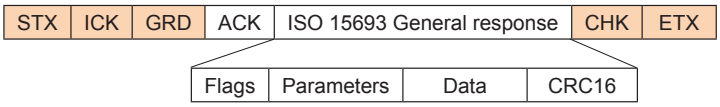
ISO 15693 General Read Command Format

UART:

(Request)

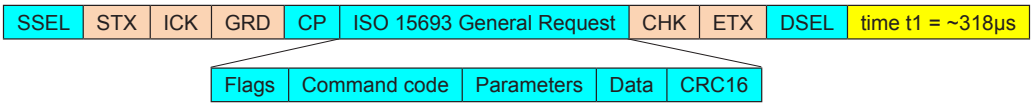


(Response)

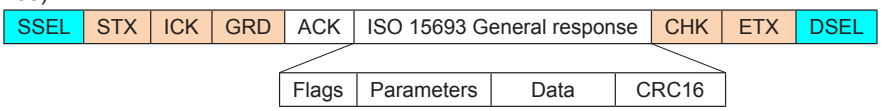


SPI (assume MOSI = FFh during MISO output):

(Request)



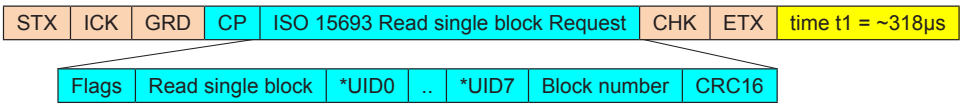
(Response)



ISO 15693 Read Single Block with General Read Command

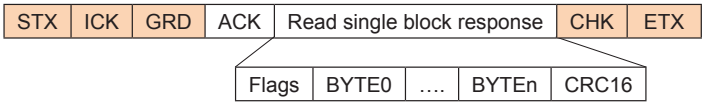
UART:

(Request)



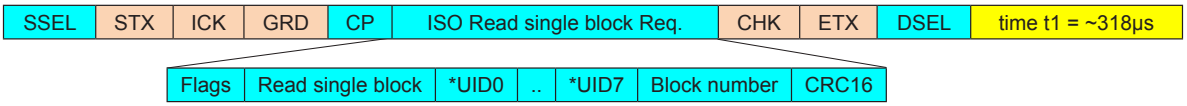
*Optional

(Response)



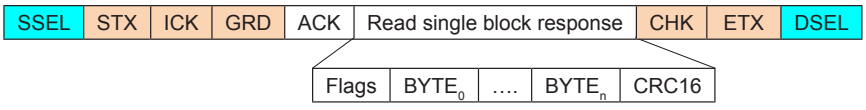
SPI (assume MOSI = FFh during MISO output):

(Request)



*Optional

(Response)



General Write	
Command/Response ID	90h
Usage	The General Write command sends the provided formed message from the host to the tag and waits a time t1 of ~318µs before trying to capture the response for the delay time duration (i.e., defined by the Delay time). This command is typically used for ISO 15693 Write single block, Lock block and Write AFI.
Command Parameter	Expected response length in number of bytes per Table 7.
Requires	The host forms the sending message and checks the format, data and CRC as needed per ISO 15693.
Other Notes	The General Write process is the following: The host forms and sends this command to the MAX66300. If the Option_flag and the command code of a Write block, Lock block or Write AFI are detected to be set, then the MAX66300 waits for the Delay time provided followed by sending a single EOF, and captures the response; else, the MAX66300 waits the time t1 and captures the response during the Delay time provided. If there is no response from a tag, the ACK error ERR_NO_SOF (15h) will return in the response from MAX66300 to the host. If no ERR_NO_SOF error, the MAX66300 will continue to find and extract the decoded data. If the response contains more than four bytes (i.e., Flags, Error code, CRC16 fields) and the Flags field (i.e., 1st byte) is not zero consider the error message is not per the ISO 15593 standard. The MAX66300 will return the ACK error ERR_ISO_ERROR_MSG (0Eh) along with the response data to the host. If the number of response data bytes is less than expected from the response length; MAX66300 returns an ACK error ERR_WRONG_LEN (0Bh) and the decoded response data. If the response is limited to the expected response length number of bytes boundary then the MAX66300 returns an ACK equal to zero and the response data to the host.
Command Restrictions	Only supports reading up to 128 bytes per the response length limit.
ACK Error Conditions (Error Response)	ERR_WRONG_LEN (0Bh) ERR_ISO_ERROR_MSG (0Eh) ERR_RAW_DATA (10h) ERR_CAPT_DATA (11h) ERR_NO_SOF (15h)
Accessed Items	flag byte, command byte
UART/SPI Busy Duration	A time t1 of ~318µs and the timeout duration (i.e., typically tag programming time) specified by the two delay time bytes.

Transmission Sequence of the Delay Time for General Write

LSB(Byte)	
Byte 1	Byte 2
DTL	DTH
	MSB(Byte)

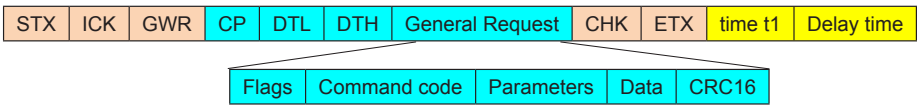
Legend:

DTL	Delay time LSB	Delay time = timeout(f_{CK}/320)
DTH	Delay time MSB	

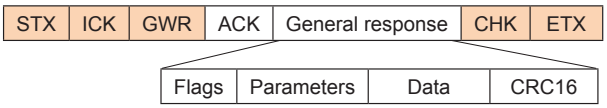
ISO 15693 General Write Command Format

UART:

(Request)

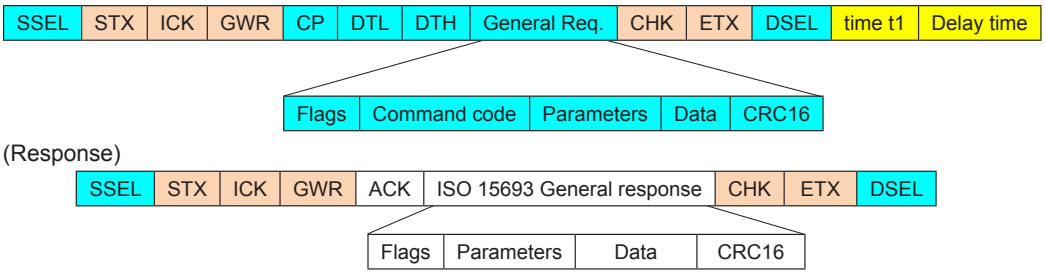


(Response)



SPI (assume MOSI = FFh during MISO output):

(Request)

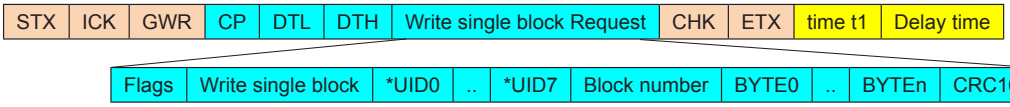


(Response)

ISO 15693 Write Single Block with General Write Command

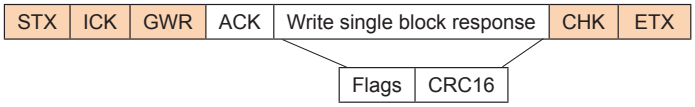
UART:

(Request)



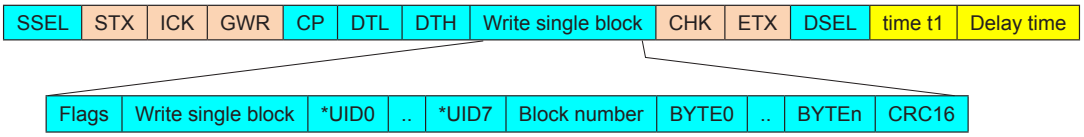
*Optional

(Response)



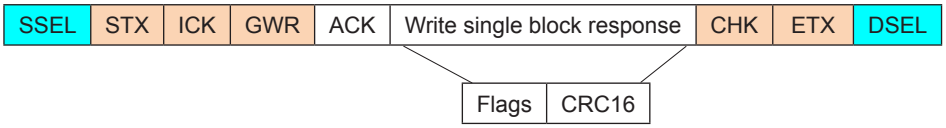
SPI (assume MOSI = FFh during MISO output):

(Request)



*Optional

(Response)



Reader Control Commands

This section describes the Reader Control commands and responses used to control the MAX66300, which are listed in Table 4. These commands and responses together can directly control the coprocessor integrated in the MAX66300. The key functions include SHA-256 tag authentication. This command also represents the means to set various configurations in the AFE to tweak the RF field as desired by the user application.

Coprocessor (Reader) Write/Read Commands	
Command/Response ID	E0h (CPW), E1 (CPR)
Usage	The Coprocessor Write/Read Commands are used to control the command flow and access of resources for the SHA-256 authentication applications.
Command Parameter	See subcommands that use this field.
Other Notes	None
Command Restrictions	Requires both a subcommand and a parameter byte.
ACK Error Conditions (Error Response)	See subcommand specific ACK field.
UART/SPI Busy Duration	See subcommand for busy duration.

SHA-256 Coprocessor Write/Read Subcommands

This subsection describes the SHA-256 coprocessor write/read memory access subcommands, as well as the SHA-256 functions. The coprocessor write/read commands use a subcommand and a parameter byte to control the command flow and gain access of resources for the SHA-256 authentication applications. Attempting to read a page that is read-protected results in the ACK error condition ERR_DATA_PROTECTED. If the page is only one-half read-protected, then that portion of the page is replaced with FFh bytes in the return data with not error condition indicated.

Access Data Memory	
Subcommand	5Ah
Parameter Byte	Data destination
Usage	Transferring data in message to user memory pages. Installs the master secrets in the device. Writes to the scratchpad in the device. Reads data from memory pages. Reads data from the scratchpad.
Other Notes	None
Command Restrictions	The target memory must not be write-protected (locked).
ACK Error Conditions (Error Response)	ERR_DATA_PROTECTED, 60h
MAC Notes	See Table 8 for the mapping of message data to M-Secret.
UART/SPI Busy Duration	For a CPW; t_{PROG}
Calling Commands and Responses	CPW and CPR

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOU	SP	X	X	X	X	TT	

Bit 7: Secret or User Memory (SOU). This bit specifies whether the data is to be copied into secret memory or into a user memory page. If SOU is 0, message data is copied to the secret memory space specified by the TT bits. If SOU is 1, message data is copied to the user memory page specified by the TT bits.

Bit 6: Scratchpad (SP). This bit specifies data to be written to a 76-byte scratchpad in SRAM when set. If this bit is 0 then SOU bit applies.

Bits 1:0: Target (TT). These bits specify the user memory page number (SOU = 1) to which the message data is to be copied.

For SOU = 0, the assignments are:

00 M-Secret 0 (256 bits, used for SHA-256 by default)

01 M-Secret 1 (256 bits, used for SHA-256 if selected)

10 M-Secret 2 (256 bits, used for SHA-256 if selected)

11 M-Secret 3 (256 bits, used for SHA-256 if selected)

For SOU = 1, the assignments are:

00 User memory page 0 (32 bytes, may be used for binding data)

01 User memory page 1 (32 bytes, may be used for binding data or partial secret)

10 User memory page 2 (32 bytes, may be used for binding data)

11 User memory page 3 (32 bytes, may be used for binding data)

Table 8. Mapping of Message to M-Secret

(MS+0) := $BYTE_0$	(MS+1):= $BYTE_1$	(MS+2):= $BYTE_2$	(MS+3):= $BYTE_3$
(MS+4):= $BYTE_4$	(MS+5):= $BYTE_5$	(MS+6):= $BYTE_6$	(MS+7):= $BYTE_7$
(MS+8):= $BYTE_8$	(MS+9):= $BYTE_9$	(MS+10):= $BYTE_{10}$	(MS+11):= $BYTE_{11}$
(MS+12):= $BYTE_{12}$	(MS+13):= $BYTE_{13}$	(MS+14):= $BYTE_{14}$	(MS+15):= $BYTE_{15}$
(MS+16):= $BYTE_{16}$	(MS+17):= $BYTE_{17}$	(MS+18):= $BYTE_{18}$	(MS+19):= $BYTE_{19}$
(MS+20):= $BYTE_{20}$	(MS+21):= $BYTE_{21}$	(MS+22):= $BYTE_{22}$	(MS+23):= $BYTE_{23}$
(MS+24):= $BYTE_{24}$	(MS+25):= $BYTE_{25}$	(MS+26):= $BYTE_{26}$	(MS+27):= $BYTE_{27}$
(MS+28):= $BYTE_{28}$	(MS+29):= $BYTE_{29}$	(MS+30):= $BYTE_{30}$	(MS+31):= $BYTE_{31}$

Loading the Secret Into Memory

UART:

STX	ICK	CPW	ADM	PB	$BYTE_0$	..	$BYTE_{31}$	CHK	ETX	t_{PROG}

STX	ICK	CPW	ACK	CHK	ETX

- OR -

STX	ICK	CPW	ACKE	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPW	ADM	PB	$BYTE_0$	..	$BYTE_{31}$	CHK	ETX	DSEL	t_{PROG}

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPW	ACKE	CHK	ETX	DSEL

Loading the Scratchpad Into Memory

UART:

STX	ICK	CPW	ADM	PB	$BYTE_0$	..	$BYTE_{75}$	CHK	ETX

STX	ICK	CPW	ACK	CHK	ETX

- OR -

STX	ICK	CPW	ACKE	CHK	ETX

SPI (assume MOSI=FFh during MISO output):

SSEL	STX	ICK	CPW	ADM	PB	$BYTE_0$	..	$BYTE_{75}$	CHK	ETX	DSEL

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPW	ACKE	CHK	ETX	DSEL

Reading a Page from Memory (Secret Cannot Be Read Out)

UART:

STX	ICK	CPR	ADM	PB	CHK	ETX

STX	ICK	CPR	ACK	$BYTE_0$	..	$BYTE_{31}$	CHK	ETX

- OR -

STX	ICK	CPR	ACKE	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPR	ADM	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPR	ACK	$BYTE_0$	..	$BYTE_{31}$	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPR	ACKE	CHK	ETX	DSEL

Compute S-Secret	
Subcommand	4Bh
Parameter Byte	SHA-256 message input selection of M-Secret and memory pages as needed.
Usage	Re-creating or rolling a unique slave secret in the coprocessor from an existing one.
Other Notes	The computed MAX66300's S-Secret must match the memory slave's unique secret.
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	See Table 8 and Table 9 for the message input used for computing the MAC, as well as the mapping of the MAC to the secret.
UART/SPI Busy Duration	For a CPW; 2 x t_{CSHA}
Calling Command/Response ID	CPW only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	ID			MS		PR	

Bits 6:4: Input Data (ID). These bits specify if data from the coprocessor's user memory is to be swapped in for M0 to M7 in the first block (SHA-256 mode). As well if selected, specifies what memory page is to be swapped-in. The swap is necessary if the memory in the tag is read protected. Valid codes are:

0XX = no swapping, take input data from scratchpad (X = don't care)

100 = swap-in data from user memory page 0

101 = swap-in data from user memory page 1

110 = swap-in data from user memory page 2

111 = swap-in data from user memory page 3

Bits 3:2: Master Secret (MS). These bits specify which master secret from the coprocessor's user memory is to be swapped in for M0 to M7 in the second block (SHA-256 mode). The swap is necessary if the M-Secret is desired to support four different groups of tags. The assignments are:

00 = M-Secret 0 (256 bits, used for SHA-256 by default)

01 = M-Secret 1 (256 bits, used for SHA-256 if selected)

10 = M-Secret 2 (256 bits, used for SHA-256 if selected)

11 = M-Secret 3 (256 bits, used for SHA-256 if selected)

Bits 1:0: Page Region (PR). Valid codes are:

00 = Undefined or RFU

01 = First one-half of page in selected ID is loaded into M0 to M3 (Second one-half is not swapped.)

10 = Second one-half of page in selected ID is loaded into M4 to M7 (First one-half is not swapped.)

11 = Entire page in selected ID is loaded into M0 to M7

Table 9. Computing a Unique Slave Secret

Message, First Block			
M0[1][31:24] = (IP+3)	M0[1][23:16] = (IP+2)	M0[1][15:8] = (IP+1)	M0[1][7:0] = (IP+0)
M1[1][31:24] = (IP+7)	M1[1][23:16] = (IP+6)	M1[1][15:8] = (IP+5)	M1[1][7:0] = (IP+4)
M2[1][31:24] = (IP+11)	M2[1][23:16] = (IP+10)	M2[1][15:8] = (IP+9)	M2[1][7:0] = (IP+8)
M3[1][31:24] = (IP+15)	M3[1][23:16] = (IP+14)	M3[1][15:8] = (IP+13)	M3[1][7:0] = (IP+12)
M4[1][31:24] = (IP+19)	M4[1][23:16] = (IP+18)	M4[1][15:8] = (IP+17)	M4[1][7:0] = (IP+16)
M5[1][31:24] = (IP+23)	M5[1][23:16] = (IP+22)	M5[1][15:8] = (IP+21)	M5[1][7:0] = (IP+20)
M6[1][31:24] = (IP+27)	M6[1][23:16] = (IP+26)	M6[1][15:8] = (IP+25)	M6[1][7:0] = (IP+24)
M7[1][31:24] = (IP+31)	M7[1][23:16] = (IP+30)	M7[1][15:8] = (IP+29)	M7[1][7:0] = (IP+28)
M8[1][31:24] = (SP+35)	M8[1][23:16] = (SP+34)	M8[1][15:8] = (SP+33)	M8[1][7:0] = (SP+32)
M9[1][31:24] = (SP+39)	M9[1][23:16] = (SP+38)	M9[1][15:8] = (SP+37)	M9[1][7:0] = (SP+36)
M10[1][31:24] = (SP+43)	M10[1][23:16] = (SP+42)	M10[1][15:8] = (SP+41)	M10[1][7:0] = (SP+40)
M11[1][31:24] = (SP+47)	M11[1][23:16] = (SP+46)	M11[1][15:8] = (SP+45)	M11[1][7:0] = (SP+44)
M12[1][31:24] = (SP+51)	M12[1][23:16] = (SP+50)	M12[1][15:8] = (SP+49)	M12[1][7:0] = (SP+48)
M13[1][31:24] = (SP+55)	M13[1][23:16] = (SP+54)	M13[1][15:8] = (SP+53)	M13[1][7:0] = (SP+52)
M14[1][31:24] = (SP+59)	M14[1][23:16] = (SP+58)	M14[1][15:8] = (SP+57)	M14[1][7:0] = (SP+56)
M15[1][31:24] = (SP+63)	M15[1][23:16] = (SP+62)	M15[1][15:8] = (SP+61)	M15[1][7:0] = (SP+60)
Message, Second Block			
M0[2][31:24] = (MS+3)	M0[2][23:16] = (MS+2)	M0[2][15:8] = (MS+1)	M0[2][7:0] = (MS+0)
M1[2][31:24] = (MS+7)	M1[2][23:16] = (MS+6)	M1[2][15:8] = (MS+5)	M1[2][7:0] = (MS+4)
M2[2][31:24] = (MS+11)	M2[2][23:16] = (MS+10)	M2[2][15:8] = (MS+9)	M2[2][7:0] = (MS+8)
M3[2][31:24] = (MS+15)	M3[2][23:16] = (MS+14)	M3[2][15:8] = (MS+13)	M3[2][7:0] = (MS+12)
M4[2][31:24] = (MS+19)	M4[2][23:16] = (MS+18)	M4[2][15:8] = (MS+17)	M4[2][7:0] = (MS+16)
M5[2][31:24] = (MS+23)	M5[2][23:16] = (MS+22)	M5[2][15:8] = (MS+21)	M5[2][7:0] = (MS+20)
M6[2][31:24] = (MS+27)	M6[2][23:16] = (MS+26)	M6[2][15:8] = (MS+25)	M6[2][7:0] = (MS+24)
M7[2][31:24] = (MS+31)	M7[2][23:16] = (MS+30)	M7[2][15:8] = (MS+29)	M7[2][7:0] = (MS+28)
M8[2][31:24] = (SP+67)	M8[2][23:16] = (SP+66)	M8[2][15:8] = (SP+65)	M8[2][7:0] = (SP+64)
M9[2][31:24] = (SP+71)	M9[2][23:16] = (SP+70)	M9[2][15:8] = (SP+69)	M9[2][7:0] = (SP+68)
M10[2][31:24] = (SP+75)	M10[2][23:16] = (SP+74)	M10[2][15:8] = (SP+73)	M10[2][7:0] = (SP+72)
M11[2][31:24] = 00h	M11[2][23:16] = 00h	M11[2][15:8] = 00h	M11[2][7:0] = 00h
M12[2][31:24] = 00h	M12[2][23:16] = 00h	M12[2][15:8] = 00h	M12[2][7:0] = 00h
M13[2][31:24] = 00h	M13[2][23:16] = 00h	M13[2][15:8] = 00h	M13[2][7:0] = 80h
M14[2][31:24] = 00h	M14[2][23:16] = 00h	M14[2][15:8] = 00h	M14[2][7:0] = 00h
M15[2][31:24] = 00h	M15[2][23:16] = 00h	M15[2][15:8] = 03h	M15[2][7:0] = B8h

IP: Either SP or UP (swapped in user memory page).

Legend:	
Mt	Input buffer of SHA engine; 0 ≤ t ≤ 15; 32-bit words.
(IP + N)	Byte N swapped in memory page or from the scratchpad.
(SP + N)	Byte N of scratchpad.
(MS + N)	Byte N swapped in from M-Secret 0-3; 0 ≤ N ≤ 31 for SHA-256.
	Constant data.

Table 10. Mapping of MAC to S-Secret

(SS+0) := H_7[7:0]	(SS+1):= H_7[15:8]	(SS+2):= H_7[23:16]	(SS+3):= H_7[31:24]
(SS+4):= H_6[7:0]	(SS+5):= H_6[15:8]	(SS+6):= H_6[23:16]	(SS+7):= H_6[31:24]
(SS+8):= H_5[7:0]	(SS+9):= H_5[15:8]	(SS+10):= H_5[23:16]	(SS+11):= H_5[31:24]
(SS+12):= H_4[7:0]	(SS+13):= H_4[15:8]	(SS+14):= H_4[23:16]	(SS+15):= H_4[31:24]
(SS+16):= H_3[7:0]	(SS+17):= H_3[15:8]	(SS+18):= H_3[23:16]	(SS+19):= H_3[31:24]
(SS+20):= H_2[7:0]	(SS+21):= H_2[15:8]	(SS+22):= H_2[23:16]	(SS+23):= H_2[31:24]
(SS+24):= H_1[7:0]	(SS+25):= H_1[15:8]	(SS+26):= H_1[23:16]	(SS+27):= H_1[31:24]
(SS+28):= H_0[7:0]	(SS+29):= H_0[15:8]	(SS+30):= H_0[23:16]	(SS+31):= H_0[31:24]

Computing S-Secret

UART:

STX	ICK	CPW	CSS	PB	CHK	ETX	2 × t_{CSHA}

STX	ICK	CPW	ACK	CHK	ETX

- OR -

STX	ICK	CPW	ACKE	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPW	CSS	PB	CHK	ETX	DSEL	2 × t_{CSHA}

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

Compute Slave Authentication MAC	
Subcommand	3Ch
Parameter Byte	Page size, page swapping flags
Usage	Verification of a tag's MAC from Read Authenticated Page or equivalent command.
Other Notes	This command always uses the S-Secret, which must first be computed before it can be used for tag authentication MACs or write MACs. The MAC is read from the MAC Readout register. The MAC comparison is done by the host.
Command Restrictions	The message containing this command must be followed by a wait time of 2 x t_{CSHA}. The device will respond with a valid MAC immediately after this wait time.
ACK Error Conditions (Error Response)	None
MAC Notes	See Table 11 and Table 12 for the message input that is used for computing the MAC and the MAC read-out byte sequence.
UART/SPI Busy Duration	For a CPR; 2 × t_{CSHA}
Calling Command/Response ID	CPR only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ID			0	0	PR	

Bits 6:4: Input Data (ID). These bits specify whether data from the coprocessor's user memory is to be swapped in for M0 to M7 in the first block (SHA-256 mode) and if yes, which page to swap. The swap-in is necessary if the memory in the slave to be authenticated is read protected. Valid codes are:

0XX = no swapping, take input data from scratchpad (X = don't care)

100 = swap-in data from user memory page 0

101 = swap-in data from user memory page 1

110 = swap-in data from user memory page 2

111 = swap-in data from user memory page 3

Bits 1:0: Page Region (PR). Valid codes are:

00 = undefined or RFU

01 = First one-half of page in selected ID is loaded into M0 to M3 (Second one-half is not swapped.)

10 = Second one-half of page in selected ID is loaded into M4 to M7 (First one-half is not swapped.)

11 = Entire page in selected ID is loaded into M0 to M7

Table 11. Computing a Slave Authentication MAC

Message, First Block			
M0[1][31:24] = (IP+3)	M0[1][23:16] = (IP+2)	M0[1][15:8] = (IP+1)	M0[1][7:0] = (IP+0)
M1[1][31:24] = (IP+7)	M1[1][23:16] = (IP+6)	M1[1][15:8] = (IP+5)	M1[1][7:0] = (IP+4)
M2[1][31:24] = (IP+11)	M2[1][23:16] = (IP+10)	M2[1][15:8] = (IP+9)	M2[1][7:0] = (IP+8)
M3[1][31:24] = (IP+15)	M3[1][23:16] = (IP+14)	M3[1][15:8] = (IP+13)	M3[1][7:0] = (IP+12)
M4[1][31:24] = (IP+19)	M4[1][23:16] = (IP+18)	M4[1][15:8] = (IP+17)	M4[1][7:0] = (IP+16)
M5[1][31:24] = (IP+23)	M5[1][23:16] = (IP+22)	M5[1][15:8] = (IP+21)	M5[1][7:0] = (IP+20)
M6[1][31:24] = (IP+27)	M6[1][23:16] = (IP+26)	M6[1][15:8] = (IP+25)	M6[1][7:0] = (IP+24)
M7[1][31:24] = (IP+31)	M7[1][23:16] = (IP+30)	M7[1][15:8] = (IP+29)	M7[1][7:0] = (IP+28)
M8[1][31:24] = (SP+35)	M8[1][23:16] = (SP+34)	M8[1][15:8] = (SP+33)	M8[1][7:0] = (SP+32)
M9[1][31:24] = (SP+39)	M9[1][23:16] = (SP+38)	M9[1][15:8] = (SP+37)	M9[1][7:0] = (SP+36)
M10[1][31:24] = (SP+43)	M10[1][23:16] = (SP+42)	M10[1][15:8] = (SP+41)	M10[1][7:0] = (SP+40)
M11[1][31:24] = (SP+47)	M11[1][23:16] = (SP+46)	M11[1][15:8] = (SP+45)	M11[1][7:0] = (SP+44)
M12[1][31:24] = (SP+51)	M12[1][23:16] = (SP+50)	M12[1][15:8] = (SP+49)	M12[1][7:0] = (SP+48)
M13[1][31:24] = (SP+55)	M13[1][23:16] = (SP+54)	M13[1][15:8] = (SP+53)	M13[1][7:0] = (SP+52)
M14[1][31:24] = (SP+59)	M14[1][23:16] = (SP+58)	M14[1][15:8] = (SP+57)	M14[1][7:0] = (SP+56)
M15[1][31:24] = (SP+63)	M15[1][23:16] = (SP+62)	M15[1][15:8] = (SP+61)	M15[1][7:0] = (SP+60)
Message, Second Block			
M0[2][31:24] = (SS+3)	M0[2][23:16] = (SS+2)	M0[2][15:8] = (SS+1)	M0[2][7:0] = (SS+0)
M1[2][31:24] = (SS+7)	M1[2][23:16] = (SS+6)	M1[2][15:8] = (SS+5)	M1[2][7:0] = (SS+4)
M2[2][31:24] = (SS+11)	M2[2][23:16] = (SS+10)	M2[2][15:8] = (SS+9)	M2[2][7:0] = (SS+8)
M3[2][31:24] = (SS+15)	M3[2][23:16] = (SS+14)	M3[2][15:8] = (SS+13)	M3[2][7:0] = (SS+12)
M4[2][31:24] = (SS+19)	M4[2][23:16] = (SS+18)	M4[2][15:8] = (SS+17)	M4[2][7:0] = (SS+16)
M5[2][31:24] = (SS+23)	M5[2][23:16] = (SS+22)	M5[2][15:8] = (SS+21)	M5[2][7:0] = (SS+20)
M6[2][31:24] = (SS+27)	M6[2][23:16] = (SS+26)	M6[2][15:8] = (SS+25)	M6[2][7:0] = (SS+24)
M7[2][31:24] = (SS+31)	M7[2][23:16] = (SS+30)	M7[2][15:8] = (SS+29)	M7[2][7:0] = (SS+28)
M8[2][31:24] = (SP+67)	M8[2][23:16] = (SP+66)	M8[2][15:8] = (SP+65)	M8[2][7:0] = (SP+64)
M9[2][31:24] = (SP+71)	M9[2][23:16] = (SP+70)	M9[2][15:8] = (SP+69)	M9[2][7:0] = (SP+68)
M10[2][31:24] = (SP+75)	M10[2][23:16] = (SP+74)	M10[2][15:8] = (SP+73)	M10[2][7:0] = (SP+72)
M11[2][31:24] = 00h	M11[2][23:16] = 00h	M11[2][15:8] = 00h	M11[2][7:0] = 00h
M12[2][31:24] = 00h	M12[2][23:16] = 00h	M12[2][15:8] = 00h	M12[2][7:0] = 00h
M13[2][31:24] = 00h	M13[2][23:16] = 00h	M13[2][15:8] = 00h	M13[2][7:0] = 80h
M14[2][31:24] = 00h	M14[2][23:16] = 00h	M14[2][15:8] = 00h	M14[2][7:0] = 00h
M15[2][31:24] = 00h	M15[2][23:16] = 00h	M15[2][15:8] = 03h	M15[2][7:0] = B8h

Legend:	
Mt	Input buffer of SHA engine; 0 ≤ t ≤ 15; 32-bit words.
(IP + N)	Byte N of swapped in memory page or from the scratchpad.
(SP + N)	Byte N of scratchpad.
(SS + N)	Byte N of S-Secret; 0 ≤ N ≤ 31 for SHA-256.
	Constant data.

Table 12. MAC Readout Byte Sequence

(MB+0) := H_7[7:0]	(MB+1):= H_7[15:8]	(MB+2):= H_7[23:16]	(MB+3):= H_7[31:24]
(MB+4):= H_6[7:0]	(MB+5):= H_6[15:8]	(MB+6):= H_6[23:16]	(MB+7):= H_6[31:24]
(MB+8):= H_5[7:0]	(MB+9):= H_5[15:8]	(MB+10):= H_5[23:16]	(MB+11):= H_5[31:24]
(MB+12):= H_4[7:0]	(MB+13):= H_4[15:8]	(MB+14):= H_4[23:16]	(MB+15):= H_4[31:24]
(MB+16):= H_3[7:0]	(MB+17):= H_3[15:8]	(MB+18):= H_3[23:16]	(MB+19):= H_3[31:24]
(MB+20):=H_2[27:0]	(MB+21):= H_2[15:8]	(MB+22):= H_2[23:16]	(MB+23):= H_2[31:24]
(MB+24):= H_1[7:0]	(MB+25):= H_1[15:8]	(MB+26):= H_1[23:16]	(MB+27):= H_1[31:24]
(MB+28):= H_0[7:0]	(MB+29):= H_0[15:8]	(MB+30):= H_0[23:16]	(MB+31):= H_0[31:24]

Computing a Slave Authentication MAC

UART:

STX	ICK	CPR	CSAM	PB	CHK	ETX	2 × t_{CSHA}

STX	ICK	CPR	ACK	MAC_0	..	MAC_{31}	CHK	ETX

SPI (assume MOSI=FFh during MISO output):

SSEL	STX	ICK	CPR	CSAM	PB	CHK	ETX	DSEL	2 × t_{CSHA}

SSEL	STX	ICK	CPR	ACK	MAC_0	..	MAC_{31}	CHK	ETX	DSEL

Compute Slave Write MAC	
Subcommand	2Dh
Parameter Byte	None (i.e., set to zero)
Usage	This computes the MAC needed when performing subsequent authenticated write accesses to a tag.
Other Notes	This command always uses the S-Secret, which must first be computed before it can be used for tag authentication MACs or write MACs. The MAC can be read from the MAC Readout register and then re-transmitted using the General Read command.
Command Restrictions	The message, containing this command, must be followed by a wait time of 1 × t_{CSHA}. The device will respond with a valid MAC immediately after this wait time.
Error Conditions (Error Response)	None
MAC Notes	See Table 13 for the message input that is used for computing the MAC. The MAC transmission byte sequence is the same as is Table 12.
UART/SPI Busy Duration	For a CPR; 1 x t_{CSHA}
Calling Command/Response ID	CPR only

Table 13. Computing a Slave Write MAC for Authenticated Write Memory or Page Protection

M0[31:24] = (SS+3)	M0[23:16] = (SS+2)	M0[15:8] = (SS+1)	M0[7:0] = (SS+0)
M1[31:24] = (SS+7)	M1[23:16] = (SS+6)	M1[15:8] = (SS+5)	M1[7:0] = (SS+4)
M2[31:24] = (SS+11)	M2[23:16] = (SS+10)	M2[15:8] = (SS+9)	M2[7:0] = (SS+8)
M3[31:24] = (SS+15)	M3[23:16] = (SS+14)	M3[15:8] = (SS+13)	M3[7:0] = (SS+12)
M4[31:24] = (SS+19)	M4[23:16] = (SS+18)	M4[15:8] = (SS+17)	M4[7:0] = (SS+16)
M5[31:24] = (SS+23)	M5[23:16] = (SS+22)	M5[15:8] = (SS+21)	M5[7:0] = (SS+20)
M6[31:24] = (SS+27)	M6[23:16] = (SS+26)	M6[15:8] = (SS+25)	M6[7:0] = (SS+24)
M7[31:24] = (SS+31)	M7[23:16] = (SS+30)	M7[15:8] = (SS+29)	M7[7:0] = (SS+28)
M8[31:24] = (SP+3)	M8[23:16] = (SP+2)	M8[15:8] = (SP+1)	M8[7:0] = (SP+0)
M9[31:24] = (SP+7)	M9[23:16] = (SP+6)	M9[15:8] = (SP+5)	M9[7:0] = (SP+4)
M10[31:24] = (SP+11)	M10[23:16] = (SP+10)	M10[15:8] = (SP+9)	M10[7:0] = (SP+8)
M11[31:24] = (SP+15)	M11[23:16] = (SP+14)	M11[15:8] = (SP+13)	M11[7:0] = (SP+12)
M12[31:24] = (SP+19)	M12[23:16] = (SP+18)	M12[15:8] = (SP+17)	M12[7:0] = (SP+16)
M13[31:24] = 00h	M13[23:16] = 00h	M13[15:8] = 00h	M13[7:0] = 80h
M14[31:24] = 00h	M14[23:16] = 00h	M14[15:8] = 00h	M14[7:0] = 00h
M15[31:24] = 00h	M15[23:16] = 00h	M15[15:8] = 01h	M15[7:0] = B8h

Legend:	
Mt	Input buffer of SHA engine; 0 ≤ t ≤ 15; 32-bit words.
(SP + N)	Byte N of scratchpad.
(SS + N)	Byte N of S-Secret; 0 ≤ N ≤ 31 for SHA-256.
	Constant data.

Computing a Slave Write MAC

UART:

STX	ICK	CPR	CSWM	PB	CHK	ETX	1 × t_{CSHA}

STX	ICK	CPR	ACK	MAC_0	..	MAC_{31}	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPR	CSWM	PB	CHK	ETX	DSEL	1 × t_{CSHA}

SSEL	STX	ICK	CPR	ACK	MAC_0	..	MAC_{31}	CHK	ETX	DSEL

Compute Next M-Secret	
Subcommand	69h
Parameter Byte	Input data, master secret, and swap flags.
Usage	Computing a new M-Secret from the current M-Secret and then replaces the current M-Secret with the new M-Secret.
Other Notes	If the current M-Secret is locked, this command cannot complete successfully.
Command Restrictions	None
ACK Error Conditions (Error Response)	ERR_DATA_PROTECTED, 60h
MAC Notes	See Table 8 and Table 9 for the message input that is used for computing the MAC and see Table 14 for the mapping of the MAC to the M-secret.
UART/SPI Busy Duration	For a CPW; 2 x t_{CSHA} + t_{PROG}
Calling Command/Response ID	CPW only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	ID			MS		PR	

Bits 6:4: Input Data (ID). These bits specify whether data from the coprocessor's user memory is to be swapped in for M0 to M7 in the first block (SHA-256 mode). And if this is the case, which user memory page data to swap in. The swap is necessary if the memory in the tag is read protected. Valid codes are:

0XX = no swapping, take input data from scratchpad (X = don't care)

100 = swap-in data from user memory page 0

101 = swap-in data from user memory page 1

110 = swap-in data from user memory page 2

111 = swap-in data from user memory page 3

Bits 3:2: Master Secret (MS). These bits specify which master secret from the coprocessor's user memory is to be swapped in for M0 to M7 in the second block (SHA-256 mode). The swap is necessary if the M-Secret is desired to support four different groups of tag slaves. The assignments are:

00 = M-Secret 0 (256 bits, used for SHA-256 by default)

01 = M-Secret 1 (256 bits, used for SHA-256 if selected)

10 = M-Secret 2 (256 bits, used for SHA-256 if selected)

11 = M-Secret 3 (256 bits, used for SHA-256 if selected)

Bits 1:0: Page Region (PR). Valid codes are:

00 = undefined or RFU

01 = First one-half of page in selected ID is loaded into M0 to M3 (Second one-half is not swapped.)

10 = Second one-half of page in selected ID is loaded into M4 to M7 (First one-half is not swapped.)

11 = Entire page in selected ID is loaded into M0 to M7

Table 14. MAC Mapping (i.e., new M-Secret) to the Location of the Current M-Secret

(MS+0) := H_7[7:0]	(MS+1):= H_7[15:8]	(MS+2):= H_7[23:16]	(MS+3):= H_7[31:24]
(MS+4):= H_6[7:0]	(MS+5):= H_6[15:8]	(MS+6):= H_6[23:16]	(MS+7):= H_6[31:24]
(MS+8):= H_5[7:0]	(MS+9):= H_5[15:8]	(MS+10):= H_5[23:16]	(MS+11):= H_5[31:24]
(MS+12):= H_4[7:0]	(MS+13):= H_4[15:8]	(MS+14):= H_4[23:16]	(MS+15):= H_4[31:24]
(MS+16):= H_3[7:0]	(MS+17):= H_3[15:8]	(MS+18):= H_3[23:16]	(MS+19):= H_3[31:24]
(MS+20):= H_2[7:0]	(MS+21):= H_2[15:8]	(MS+22):= H_2[23:16]	(MS+23):= H_2[31:24]
(MS+24):= H_1[7:0]	(MS+25):= H_1[15:8]	(MS+26):= H_1[23:16]	(MS+27):= H_1[31:24]
(MS+28):= H_0[7:0]	(MS+29):= H_0[15:8]	(MS+30):= H_0[23:16]	(MS+31):= H_0[31:24]

Computing Next M-Secret

UART:

STX	ICK	CPW	CNMS	PB	CHK	ETX	2 × t_{CSHA} + t_{PROG}

STX	ICK	CPW	ACK	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPW	CNMS	PB	CHK	ETX	DSEL	2 × t_{CSHA} + t_{PROG}

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPW	ACKE	CHK	ETX	DSEL

Set Protection	
Subcommand	1Eh
Parameter Byte	Protection mode, target selection
Usage	Sets the write protection of a secret memory or user memory page, sets read protection for a user memory page
Other Notes	Secrets are read protected by hardware design. The protection for a user memory page can be set in stages: first write protection bits, then read protection bits (or reverse sequence). One can also set both protections simultaneously.
Command Restrictions	Once set, the protection cannot be reversed.
ACK Error Conditions (Error Response)	ERR_DATA_PROTECTED, 60h
MAC Notes	N/A
UART/SPI Busy Duration	For a CPW; t_{PROG}
Calling Command/Response ID	CPW only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RP	WP	PR		0	TS		

Bits 7:6: Protection Settings (RP:WP). These bits specify the type of protection to be activated (set). For user memory, valid codes are:

01b (set write protection only),

10b (set read protection only),

11b (set both, read and write protection at the same time).

To write protect a secret, either code 01b and 11b is valid.

Bits 5:4: Page Region (PR): (Not valid for M-secret.) Valid codes are:

00 = undefined or RFU

01 = First half of page

10 = Second half of page

11 = Entire page

Bits 2:0: Target Selection (TS). These bits specify the memory type and/or page for which the protection is to be set. Valid codes are:

000 = M-Secret 0

001 = M-Secret 1

010 = M-Secret 2

011 = M-Secret 3

100 = User memory page 0

101 = User memory page 1

110 = User memory page 2

111 = User memory page 3

Set Protection

UART:

STX	ICK	CPW	SPR	PB	CHK	ETX	t_{PROG}

STX	ICK	CPW	ACK	CHK	ETX

- OR -

STX	ICK	CPW	ACKE	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPW	SPR	PB	CHK	ETX	DSEL	t_{PROG}

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPW	ACKE	CHK	ETX	DSEL

Protection Status	
Subcommand	0Fh
Parameter Byte	Protection mode, status selection
Usage	The Protection Status command allows the host to read the current protection status setting (Table 15). The secret and the user memory pages can be write-protected. The secret is read-protected by hardware design. If desired, the user memory pages can also be read-protected. The protection is activated using the Set Protection command.
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	N/A
UART/SPI Busy Duration	N/A
Calling Command/Response ID	CPR only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	TA	TSS	

Bit 2: Target All (TA). When this bit is set, it reveals all four protection status bytes in the response. When logic low, the TSS bits will determine the byte response.

Bits 1:0: Target Status Selection (TSS). These bits select which memory location will have its protection status byte revealed in the response. This only works as described below if the TA bit is 0. Valid codes are:

00 = User memory page 0 and M-Secret 0 (MPS0)

01 = User memory page 1 and M-Secret 1 (MPS1)

10 = User memory page 2 and M-Secret 2 (MPS2)

11 = User memory page 3 and M-Secret 3 (MPS3)

Table 15. Memory Protection Status Bit Assignment

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MPS_n	RP1	WP1	RP0	WP0	1	1	1	SL

Bit 7: User Memory Read Protection (RP1). This bit specifies whether the upper half of the selected user memory page n (n = 0–3) is read protected. If RP1 is 0 (factory default), the memory is read accessible. If RP1 is 1, the memory is read-protected and its data can only be accessible for use with the SHA engine.

Bit 6: User Memory Write Protection (WP1). This bit specifies whether the upper half of the selected user memory page n (n = 0–3) is write protected. If WP1 is 0 (factory default), the memory is not protected and can be rewritten. If WP1 is 1, the memory is write protected and its data cannot be changed.

Bit 5: User Memory Read Protection (RP0). This bit specifies whether the lower half of the selected user memory page n (n = 0–3) is read protected. If RP0 is 0 (factory default), the memory is read accessible. If RP0 is 1, the memory is read-protected and its data can only be accessible for use with the SHA engine.

Bit 4: User Memory Write Protection (WP0). This bit specifies whether the lower half of the selected user memory page n (n = 0–3) is write protected. If WP0 is 0 (factory default), the memory is not protected and can be rewritten. If WP0 is 1, the memory is write protected and its data cannot be changed.

Bit 0: Secret Locking (SL). This bit specifies whether the selected M-Secret n (n = 0–3) is locked (write-protected). If SL is 0 (factory default), the secret is not protected and can be rewritten. If SL is 1, the secret is write-protected and its data cannot be changed.

Protection Status

UART:

STX	ICK	CPR	PRS	PB	CHK	ETX

STX	ICK	CPR	ACK	MPS_0	..	MPS_3	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPR	PRS	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPR	ACK	MPS_0	..	MPS_3	CHK	ETX	DSEL

Read Factory Details	
Subcommand	F0h
Parameter Byte	Set Number of Bytes to read
Usage	The Read Factory Details command allows the host to read the Coprocessor's Factory byte, Personality byte, and the Manufacturer ID bytes (Table 16). These bytes are set during manufacturing and can't be changed by the host. The factory details are: Factory Byte – This byte reads 55h. Personality Byte – This byte reads 00h. Manufacturer ID – These two bytes read 0000h unless the device is programmed with customer specific data using the factory preprogramming service.
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	N/A
UART/SPI Busy Duration	N/A
Calling Command/Response ID	CPR only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	SNB		

Bits 1:0: Set Number of Bytes (SNB). These bits select the number of bytes from 1 to 4 bytes to be placed in the response. Typical valid codes are:

000 = Byte 1 only (FB)

001 = Byte 2 only (PSB)

010 = Byte 3 only (MAN_ID0)

011 = Byte 4 only (MAN_ID1)

1XXh = All 4 bytes

Table 16. Transmission Sequence of the Factory Details

LSB(Byte)			
Byte 1	Byte 2	Byte 3	Byte 4
FB	PSB	MAN_ID_0	MAN_ID_1
			MSB(Byte)

Legend:	
FB	Factory Byte
PSB	Personality Byte
MAN_ID_0	Manufacturing ID LSB
MAN_ID_1	Manufacturing ID MSB

Read Factory Details

UART:

STX	ICK	CPR	RFD	PB	CHK	ETX

STX	ICK	CPR	ACK	FB	PSB	MAN_ID_0	MAN_ID_1	CHK	ETX

SPI (assume MOSI=FFh during MISO output):

SSEL	STX	ICK	CPR	RFD	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPR	ACK	FB	PSB	MAN_ID_0	MAN_ID_1	CHK	ETX	DSEL

Authenticate Tag (MAX66240/42)	
Subcommand	E1h
Parameter Byte 1	Sets what will be used for the ‘Compute S-Secret” operation.
Parameter Byte 2	Sets what will be used for the ‘Compute Slave Authenticate MAC’ operation.
Parameter Byte 3	Sets what target page of the MAX66240/42 Tag will be used.
Usage	Authentication of MAX66240/42 Tag. The UID to be used for the Authentication must be provided LSB first after the parameter bytes. If the MAX66240/42 tag is authentic then the ACK returned will be OK. If the MAX66240/42 tag is not authentic then an ACK error will occur.

Other Notes	Both the MAX66300 and the MAX66240/42 must be preprogrammed. For a unique secret the operation would be: 1. Find the tag UID. 2. Write scratchpad with 'Compute S-secret' input values. 3. Call 'Authenticate Tag' command. For a fixed M-Secret the operation would be: 1. Find the tag UID. 2. Call 'Authenticate Tag' command.
Command Restrictions	The host must know the UID of the MAX66240/42 tag. The message, containing this command, must be followed by a wait time of t_{AUTH}. The device will respond with a response message immediately after this wait time.
ACK Error Conditions (Error Response)	ERR_NOT_AUTH, 61h ERR_AUTH_INCOMPLETE, 62h
MAC Notes	MAC from the MAX66240/42 and the MAX66300 are compared.
UART/SPI Busy Duration	For a CPR; t_{AUTH}
Calling Command/Response ID	CPR only

Parameter Byte 1 Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	ID			MS		PR	

Bits 6:4: Input Data (ID). These bits specify if data from the coprocessor's user memory is to be swapped in for M0 to M7 in the first block (SHA-256 mode). As well if selected, specifies what memory page is to be swapped-in. The swap is necessary if the memory in the tag is read protected. Valid codes are:

0XX = no swapping, take input data from scratchpad (X = don't care)

100 = swap-in data from user memory page 0

101 = swap-in data from user memory page 1

110 = swap-in data from user memory page 2

111 = swap-in data from user memory page 3

Bits 3:2: Master Secret (MS). These bits specify which master secret from the coprocessor's user memory is to be swapped in for M0 to M7 in the second block (SHA-256 mode). The swap is necessary if the M-Secret is desired to support four different groups of tags. The assignments are:

00 = M-Secret 0 (256 bits, used for SHA-256 by default)

01 = M-Secret 1 (256 bits, used for SHA-256 if selected)

10 = M-Secret 2 (256 bits, used for SHA-256 if selected)

11 = M-Secret 3 (256 bits, used for SHA-256 if selected)

Bits 1:0: Page Region (PR). Valid codes are:

00 = Undefined or RFU

01 = First half of page in selected ID is loaded into M0 to M3 (Second half is not swapped.)

10 = Second half of page in selected ID is loaded into M4 to M7 (First half is not swapped.)

11 = Entire page in selected ID is loaded into M0 to M7

Parameter Byte 2 Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
M/S	ID			MSS		PR	

Bits 7: M-Secret or S-Secret (M/S). When this bit is set, the Authenticate tag command uses a fix M-Secret for authentication. When this bit is logic-low, the Authenticate tag command uses the S-Secret operation for authentication.

Bits 6:4: Input Data (ID). These bits specify whether data from the coprocessor's user memory is to be swapped in for M0 to M7 in the first block (SHA-256 mode) and if yes, which page to swap. The swap-in is necessary if the memory in the slave to be authenticated is read protected. Valid codes are:

0XX = no swapping, take input data from scratchpad (X = don't care)
100 = swap-in data from user memory page 0
101 = swap-in data from user memory page 1
110 = swap-in data from user memory page 2
111 = swap-in data from user memory page 3

Bit 3:2: Master Secret Select (MSS). These bits select the MSS to be used for the MAC generation when M/S bit is 1. Otherwise, these bits are ignored. The assignments are:

00 = M-Secret 0 (256 bits, used for SHA-256 by default)
01 = M-Secret 1 (256 bits, used for SHA-256 if selected)
10 = M-Secret 2 (256 bits, used for SHA-256 if selected)
11 = M-Secret 3 (256 bits, used for SHA-256 if selected)

Bits 1:0: Page Region (PR). Valid codes are:

00 = undefined or RFU
01 = First half of page in selected ID is loaded into M0 to M3 (Second half is not swapped.)
10 = Second half of page in selected ID is loaded into M4 to M7 (First half is not swapped.)
11 = Entire page in selected ID is loaded into M0 to M7

Parameter Byte 3 Bitmap

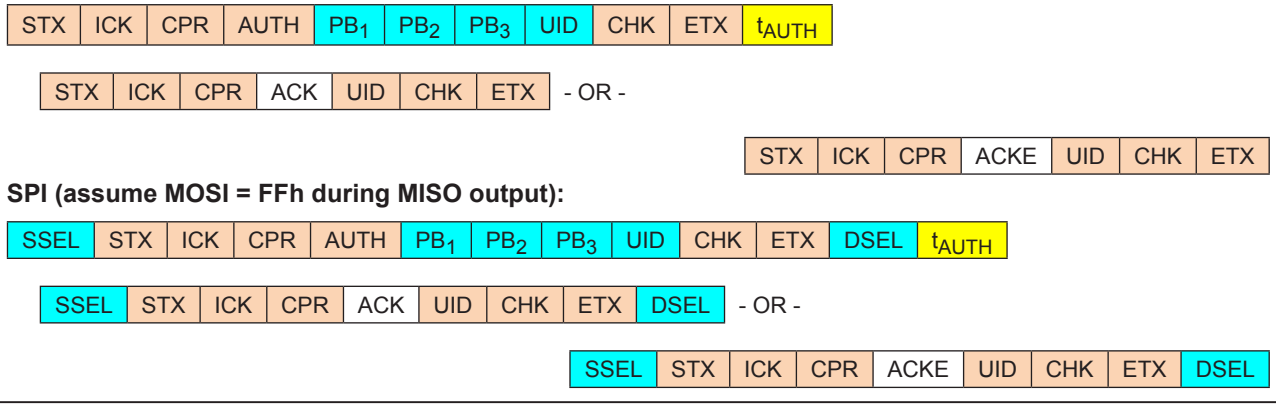
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU				TTP			

Bits 7:4: Reserved for Future Use (RFU). Set to 0000b for MAX66240/2 tag.

Bits 3:0: Target Tag Page (TTP). These bits select the target tag page of the MAX66240/2 tag to use for the read page authentication. Valid target tag page numbers are 0000b (page 0) to 1111b (page 15).

Authenticate the MAX66240/42 Tag

UART:



SPI (assume MOSI = FFh during MISO output):

Get Random Number	
Subcommand	D2h
Parameter Byte	Set the Number of Random bytes to generate
Usage	This random number can be used in the generation of a master secret, binding data, and partial secret randomly which is usually needed during the setup of the Coprocessor at the factory. Used to generate the 256-bit challenge during an authentication of a tag
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	N/A
UART/SPI Busy Duration	N/A
Calling Command/Response ID	CPR only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NRB							

Bits 7:0: Number of Random Bytes (NRB). These bits select the number of random bytes from 1 to 251 bytes to be placed in the response. Typical valid codes are:

00h = 1 random byte number

1Fh = 32 random byte numbers (common for 256-bit challenge)

3Fh = 64 random byte numbers

7Fh = 128 random byte numbers

EFh = 240 random byte numbers

FBh–FFh = RFU

Get Random Number of Bytes

UART:

STX	ICK	CPR	GRN	PB	CHK	ETX

STX	ICK	CPR	ACK	RB_0	..	RB_{31}	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPR	GRN	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPR	ACK	RB_0	..	RB_{31}	CHK	ETX	DSEL

Get 64-Bit Serial Number	
Subcommand	C3h
Parameter Byte	Set Number of SN Bytes to read.
Usage	Returns an absolute unique number stored in the ROM of the MAX66300. This unique number can serve as an electronic serial number within an application.
Other Notes	This is not the same as the UID used in the tag inventory process or the 64-bit ROM ID in the MAX66240/42 tag
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	N/A
UART/SPI Busy Duration	N/A
Calling Command/Response ID	CPR only

Parameter Byte Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	SNB			

Bits 3:0: Set Number of Bytes (SNB). These bits select the number of bytes from 1 to 8 bytes or all 8 bytes to be placed in the response payload. Typical valid codes are:

0000 = SN0 only
0001 = SN1 only
0010 = SN2 only
0011 = SN3 only
0100 = SN4 only
0101 = SN5 only
0110 = SN6 only
0111 = SN7 only
1XXX = All 64 bits of the SN0-7 in the payload

Get 64-Bit Serial Number

UART:

STX	ICK	CPR	GSN	PB	CHK	ETX

STX	ICK	CPR	ACK	SN_0	..	SN_7	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPR	GRN	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPR	ACK	SN_0	..	SN_7	CHK	ETX	DSEL

Coprocessor Manager	
Subcommand	B2h
Parameter Byte	Set Manager
Usage	Used to globally manage the coprocessor.
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
MAC Notes	None
UART/SPI Busy Duration	None
Calling Commands and Responses	CPW

Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	X	X	PP	AR2V

Bit 0: Add Round 2 Variables (AR2V). When 0 (factory default), this bit does not add the second round SHA-256 variables to the final hash result. This bit when 1 does add the second round SHA-256 variables to the final hash result. Factory default is to be used for MAX66240/42 tags. Different secure vendor tags need this bit set.

Bit 1: Push Pull (PP). When this bit is 0 (factory default), the SYSBIN, SYSCIN, and SYSEIN pins require an external 10k pullup for either 3.3V or 5V AFE operation. When 1, this bit enables push-pull drive for the SYSBIN, SYSCIN, and SYSEIN pins and no external 10k pullups are required for 3.3V AFE operation. Never set this bit to 1 when the AFE is in 5V operation.

Coprocessor Manager

UART:

STX	ICK	CPW	CPM	PB	CHK	ETX

STX	ICK	CPW	ACK	CHL	ETX

- OR -

STX	ICK	CPW	ACKE	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	CPW	CPM	PB	CHK	ETX	DSEL

SSEL	STX	ICK	CPW	ACK	CHK	ETX	DSEL

- OR -

SSEL	STX	ICK	CPW	ACKE	CHK	ETX	DSEL

RF Reset	
Command/Response ID	F0h
Usage	The RF Reset command switches the RF field off for a specified time interval according to Table 17, placing the analog circuitry to a power-down state.
Command Parameter	RF Reset, sets the time interval
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	RFRD value x 32.7ms

Table 17. Command Parameter Byte Bitmap for RF Reset

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFRD							

Turn off RF Field for a Given Duration

UART:

STX	ICK	RFR	CP	CHK	ETX	RFRD value x 32.7ms

STX	ICK	RFR	ACK	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	RFR	CP	CHK	ETX	DSEL	RFRD value x 32.7ms

SSEL	STX	ICK	RFR	ACK	CHK	ETX	DSEL

AFE Write	
Command/Response ID	F1h
Usage	The AFE Write command sends the configuration word containing 32 bits of data. This configuration word, in Table 18, is stored internally and it is used for the RF field on/off operations.
Command Parameter	None
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Table 18. Configuration Word (Option Bits)

NAME	BIT [x:y]	DESCRIPTION
PUF	[0]	Power Up Flag 0 = Power down 1 = Power up
ODC	[3:1]	Output Driver Configuration
	[3:1]	Modulation Index 0 = 10% ASK typ 1 = OOK 2 = ASK decrease 3% 3 = ASK decrease 1.5% 4 = ASK increase 3% 5 = ASK increase 6% 6 = ASK increase 12% 7 = ASK increase 20%
SCP	[4]	Short-Circuit Protection 0 = Short-circuit protection disabled 1 = Short-circuit protection enabled
SDRFDS	[5]	Single or Dual RF Driver Selection 0 = ANT1 only 1 = ANT1 and ANT2
DDPPO	[6]	Dual Driver in Phase or Phase Opposite 0 = In phase driving 1 = Differential driving

Table 18. Configuration Word (Option Bits) (continued)

NAME	BIT [x:y]	DESCRIPTION
RCC	[12:7]	Receiving Chain Configuration
	[8:7]	Filter Zero Selection 0 = High int. zero (~300kHz) 1 = Medium int. zero (~200kHz) 2 = Low int. zero (100kHz)
	[9]	Filter Lowpass Selection 400kHz 0 = High cutoff frequency (~1MHz) 1 = Low cutoff frequency (~400kHz)
	[12:10]	Receive Gain Selection 000b = Nominal gain 001b = Gain decreased for 5.7dB 010b = Gain decreased for 11.4dB 100b = Gain decreased for 22.8dB
AGC	[20:13]	AGC System
	[13]	AM/PM Input Channel Selection 0 = RFIN1 input selected 1 = RFIN2 input selected
	[14]	AGC On/Off Selection 0 = AGC off 1 = AGC on
	[15]	AGC Attack Mode Selection 0 = Attack always 1 = First pulse not attacked
	[16]	AGC Decay Mode Selection 0 = Fast decay 1 = Slow decay
	[18:17]	AGC Attack Rate 00b = ~19dB/µs (average) 01b = ~9.5dB/µs (average) 10b = ~4.7dB/µs (average)
	[20:19]	AGC Decay Wait 00b = ~44µs 01b = ~88µs 10b = ~176µs
BPSKD	[22:21]	BPSK Decoder
	[21]	Output Selection Direct Sub-carrier or BPSK 848kHz 0 = Sub-carrier 1 = Enabled
	[22]	BPSK Automatic Frequency Adjust 0 = Disabled 1 = Enabled

Table 18. Configuration Word (Option Bits) (continued)

NAME	BIT [x:y]	DESCRIPTION
OSA	[24:23]	Output Selection Analog
	[23]	Analog Disable or Enable 0 = Disabled 1 = Enabled
	[24]	Hold Delay After Modulation 0 = ~5µs 1 = ~15µs
OSC	[26:25]	Oscillator
	[25]	Oscillator Gain Selection 0 = Low g_M 1 = High g_M. The oscillator startup time can be decreased with the additional gain.
	[26]	External Oscillator Selection 0 = Internal quartz oscillator. OSCIN/OSCOUT require an external quartz crystal. 1 = External oscillator on. OSCIN input can be driven by an external clock source.
Reserved	[31:27]	Must be set to 0.
Note: It is recommended to set option bits 15 up to bit 20 and option bits 22, 24 to 0. Bit 25 should be set to 1.		

Setting RF Field On/Off Operations

UART:

STX	ICK	AFEW	$CFGW_0$	..	$CFGW_3$	CHK	ETX

STX	ICK	AFEW	ACK	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	AFEW	$CFGW_0$	..	$CFGW_3$	CHK	ETX	DSEL

SSEL	STX	ICK	AFEW	ACK	CHK	ETX	DSEL

AFE Write with RF Reset	
Command/Response ID	F2h
Usage	The AFE Write with RF Reset command sends the configuration word containing 32 bits of data and switches the RF field off for a specified time interval according to Table 17. This configuration word is defined in Table 18. In essence, this is combining RF Reset (F0h) and AFE Write (F1h) command IDs into one command ID.
Command Parameter	RF Reset, sets the time interval
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Setting RF Field On/Off Operations with RF Reset

UART:

STX	ICK	AFEWR	CP	$CFGW_0$	..	$CFGW_3$	CHK	ETX	RFRD x 32.7ms

STX	ICK	AFEWR	ACK	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	AFEWR	CP	$CFGW_0$	..	$CFGW_3$	CHK	ETX	DSEL	RFRD x 32.7ms

SSEL	STX	ICK	AFEWR	ACK	CHK	ETX	DSEL

Reader Status	
Command/Response ID	FDh
Usage	Reader Status command response contains Version (family), Release, and Release date of the MAX66300. See Table 19 for specific details.
Command Parameter	None
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Table 19. Transmission Sequence of the Reader Status

LSB(Byte)			
Byte 1	Byte 2	Byte 3	Byte 4
RLS	RLSD		VRS
			MSB(Byte)

VRS	Version (Family)
RLS	Release - coded in “BCD” format (e.g. 0Dh => release 0.13)
RLSD	Release Date – coded in format: year [15:10], month [9:6], day [5:0]. The value of “year” starts with year 2000 as 0.

Reader Status Response

UART:

STX	ICK	RS	CHK	ETX

STX	ICK	RS	ACK	RLS	RLSD	VRS	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	RS	CHK	ETX	DSEL

SSEL	STX	ICK	RS	ACK	RLS	RLSD	VRS	CHK	ETX	DSEL

Send Debug Data	
Command/Response ID	F6h
Usage	This Send Debug Data command is used to return the contents of the last raw data bit stream buffer. This is intended for test engineering only.
Command Parameter	None
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Send Debug Data

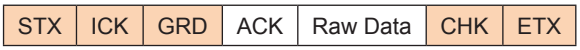
UART:

SPI (assume MOSI = FFh during MISO output):

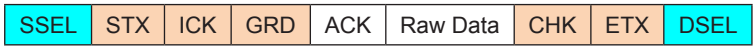
Get Raw Data	
Command/Response ID	F7h
Usage	This Get Raw Data command is used to return the contents of the last raw data bit stream buffer. This is intended for test engineering only.
Command Parameter	None
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Get Raw Data

UART:



SPI (assume MOSI = FFh during MISO output):



Get Capture Data	
Command/Response ID	F8h
Usage	This Get Capture Data command is used to return the contents of the last decoded bit stream. This is intended for test engineering only.
Command Parameter	None
Other Notes	If the debug mode is Normal or Decoded, then the response data contains two binary arrays of the same length. The first array contains the demodulated data bits, the second array contains each demodulated data bit validity (if present). If there is no bit captured at all, the two arrays are zero length. If the debug mode is Raw the response data contains single array of raw captured data.
Command Restrictions	None
ACK Error Conditions (Error Response)	Not applicable
UART/SPI Busy Duration	None

Get Capture Data

XX	The Command/Response ID
YY	00h for XX = F8h, 11h for others
Data bits	Example: FF AA 05 50 = 11111111 _10101010_00000101_01010000*
Valid bits	Example: 80 00 04 00 = 10000000_0000000_00000100_00000000*
***Note:** This result, in that the 0th and the 22nd data bit positions, was rejected by the decoding routine.	

UART:

STX	ICK	GCD	CHK	ETX

STX	0Ch	XX	YY	Data bits	Valid bits	CHK	ETX

SPI (assume MOSI=FFh during MISO output):

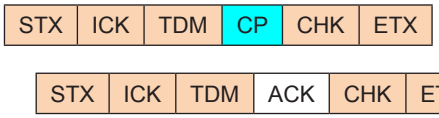
SSEL	STX	ICK	GCD	CHK	ETX	DSEL

SSEL	STX	0Ch	XX	YY	Data bits	Valid bits	CHK	ETX	DSEL

Toggle Debug Mode	
Command/Response ID	F9h
Usage	This Toggle Debug Mode checks demodulation routines. Read and write tag memory commands can return either raw pulse lengths (DBG = 1) or decoded bit stream (DBG = 2). This is intended for test engineering only.
Command Parameter	Debug Mode (DBG) is 00h for Off, 01h for Raw Mode, and 02h for Decoded Mode.
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Toggle Debug Mode

UART:

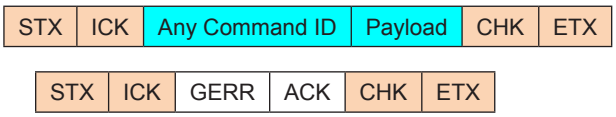


SPI (assume MOSI=FFh during MISO output):

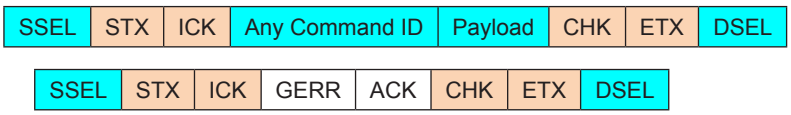
General Error	
Command/Response ID	00h (Response ID only)
Usage	A General Error response can occur when any Command ID has an error and no specific ACK error handling is available in Table 1.
Command Parameter	None
Other Notes	This typically occurs for Invalid Command IDs.
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

General Error

UART:



SPI (assume MOSI=FFh during MISO output):



Switch Coil On/Off	
Command/Response ID	FEh
Usage	Switch Coil On/Off. Toggles the coil to either standard operation of on or standby operation of off.
Command Parameter	None
Other Notes	None
Command Restrictions	None
ACK Error Conditions (Error Response)	None
UART/SPI Busy Duration	None

Command Parameter Byte Bitmap for Coil Value

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
COIL							

Bits 7:0: RF Reset Duration (RFRD). These bits specify the duration the RF field will be off; the value can be from 0 to 255 of the time interval in approximately 32.7ms steps.

Bits 7:0: Coil Value (COIL). These bits select if the coil is on or off. Typical valid codes are the following:

01h = Off – standby operation

Switch Coil On

UART:

STX	ICK	SCOF	02h	CHK	ETX

STX	ICK	SCOF	ACK	CHK	ETX

SPI (assume MOSI = FFh during MISO output):

SSEL	STX	ICK	SCOF	02h	CHK	ETX	DSEL

SSEL	STX	ICK	SCOF	ACK	CHK	ETX	DSEL

02h = On – standard operation
Xxh = All other values are invalid

Functional Description

Coprocessor

The MAX66300 coprocessor analyzes command IDs and payload received from the host. Next, the coprocessor communicates with the AFE to send and capture data from a tag. The coprocessor then returns the proper responses and payload to the host after it has analyzed the received data bytes. The ISO 15693 uplink encoding supported in the MAX66300 is the “1 out of 4” pulse position encoding scheme. The other encoding scheme supported on the ISO 15693 standard, “1 out of 256,” is not supported in the MAX66300. Additionally, the coprocessor also performs all the SHA-256 computations necessary for all secure transactions. Doing so helps to reduce host processing time during a tag authentication session. The coprocessor operates a 3.3V and requires a clock running at 24MHz with an external crystal for greater accuracy.

AFE Power-Supply Considerations

The MAX66300 AFE can operate at 3.3V or 5V. The supply voltages to power the AFE must be the same on both the analog and digital input lines ($V_{DD\_AFE\_DIG}$, V_{DDA1}, V_{DDA2}). It is strongly recommended to use a regulated supply. Power-supply ripples and noise inside the receiver frequency range degrade the overall performance of the system. An external resistor must be added to the AGD output to use the AFE at 3.3V. Doing so fixes the voltage level on AGD to 1.3V. For power efficiency reasons, the external resistor can be switched off (using for example a microcontroller I/O) when the MAX66300 is not used or is in the sleep mode.

Power Management

There are two available power modes. The selection of these two modes is done by setting the PUF bit to logic-low. Here are the two modes:

- Reset the power-up flag in the configuration word (option bit 0), which turns off the AFE only. The coprocessor and UART/SPI interface continues to run.
- Apply a low level on the SLEEP pin input. In this case, the AFE goes to sleep and the coprocessor, including the UART/SPI, goes to sleep mode.

When the SLEEP pin input is changed to high (i.e., PUF is high), the MAX66300 goes immediately to the mode in which it was before the SLEEP pin went to a low level.

Bandgap Reference

A reference voltage (2.5V) is generated internally by a bandgap reference and uses an external capacitor for blocking.

Antenna Drivers

The antenna driver produces the RF signal from the oscillator output. The pMOS and nMOS driver sides are fed by nonoverlapping signals (3ns) to minimize the power consumption. The output resistance of each antenna driver is typically 7Ω. The two integrated antenna drivers can be used in three possible configurations, depending on the output power level desired. When a single driver configuration is selected, the output power level on the 50Ω load is 100mW. For a 200mW output power, both drivers must be used in a parallel configuration fashion to double the output power (option bit 5). The drivers can operate in a push-pull configuration (option bit 6). This mode can used in case of a direct antenna connection configuration. In that configuration, the reader's antenna is connected to the output drivers through a resonant

capacitor (LC tank adjusted to 13.56MHz). In the direct antenna configuration, the user can achieve an RF output power above 200mW. To be compliant with emissions regulation in certain countries (e.g., FCC in the U.S.), it could be necessary to add a filtering structure between the device output state drivers and the antenna. The short protection circuit (option bit 4) prevents damage to the output driver when the ANT pin is shorted to ground or to the AFE's power supply.

Modulator

The modulator enables OOK or ASK modulation of the RF signal on the antenna outputs (ANT1 and ANT2). The reader can cause a low field (ASK modulation index as in Figure 5) or a field-stop (OOK modulation as in Figure 4). The selection between OOK and ASK modulation depth is done using configuration word (option bits 1, 2, and 3). The field modulation index can be adjusted from 7% up to 30% covering all the ISO standard air interface requirements. Before and after a modulation phase, the receiver input is disconnected from the antenna circuitry to preserve DC operating point setting. For high-quality factor systems, it may be necessary to prolong (option bit 24) the hold time after modulation to allow settling of the resonant circuit.

Receiver

The receiver senses the envelope of the signal present on the inputs RFIN1 or RFIN2 (option bit 13). These two inputs, used with external components, permit the detection of amplitude or phase modulated signals. Any RF frequency components still present in the envelope signal are removed by a second-order lowpass filter. The received signal DC component is removed by the highpass filter, which has selectable corner frequency (option bits 7 and 8). The signal is amplified and further processed by the lowpass filtering stage, which corner frequency is selectable (option bit 9). The gain selection (option bits 10, 11, and 12) should be chosen according to the reader system parameters. Modifying the signal bandwidth changes noise level and results in different input sensitivity.

AGC System

The integrated AGC system can be activated by the configuration word (option bit 14). The AGC amplifier has a 40dB gain correction depth. The AGC system is adapted to all RFID communication protocols. Before the tag starts to emit the data, the receiver gain is set to maximum (option bits 10, 11, 12). When the reader detects a tag signal that is above the attack threshold the receiver gain is rapidly reduced (option bits 17 and 18) to fit the signal into a linear range of the receiver. The gain remains unchanged as long as the signal level is above the decay threshold. When the received signal falls below the decay threshold for a period of time set by option bits 19 and 20, the reader logic establishes that the communication with one tag is finished and makes a fast decay to return to the maximum gain. The receiver is ready to demodulate the emission of the next tag, which can be far away from the reader antenna. This feature is necessary for anti-collision purposes. With tags that have a modulation DC level shift significantly higher than modulation sub-carrier AC level the AGC can

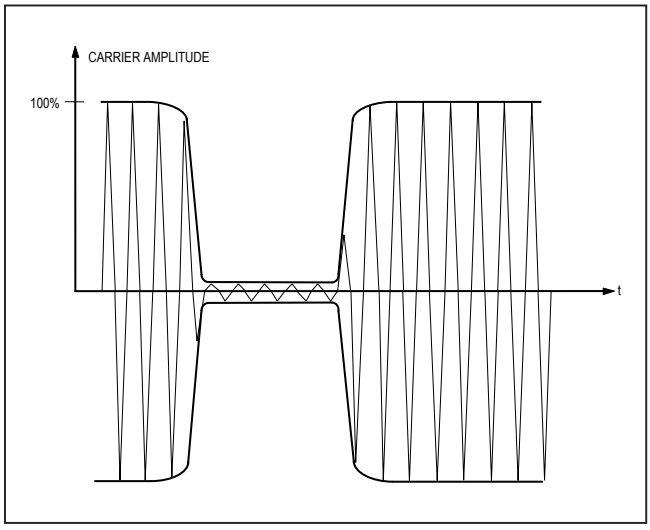


Figure 4. Transmitter Field on ANT1 for Modulation Set to OOK (100% AM)

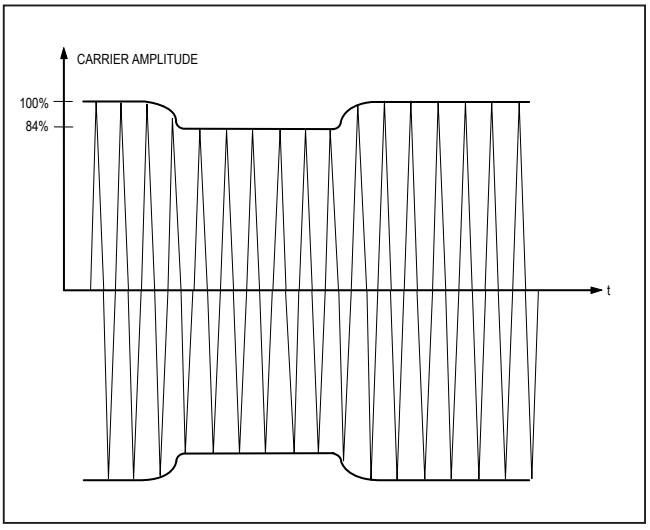


Figure 5. Transmitter Field for ANT1 for Modulation Set to ASK (16% AM)

react on DC shift and decrease the system gain too much. It is possible not to attack the first pulse (option bit 15) in a burst (for OOK modulation) to allow the DC level to settle before AGC action. The time after which the first pulse in a burst is not attacked (shortest sub-carrier stop in OOK modulation is 1/10 of the time) is set by option bits 19, 20 as decay wait time. It is also possible to use slow decay mode (option bit 16). The slow decay is started when the received signal falls below the decay threshold. The decay rate is one gain step per time defined by option bits 19 and 20. When AGC system is disabled the receiver gain is directly controlled by option bits 10, 11, 12.

True Random-Number Generator

A true hardware random-number generator is included for key generation and challenge generation. As an example, during a SHA-256 authentication of a tag, it is required to have a 256-bit challenge. If a system only has a pseudo random-number generator, hackers who know how the random number is generated can compromise a system. By using true hardware to generate a random number, a higher level of security is achieved.

UART

The universal asynchronous receiver-transmitter (UART) interface provides transmit and receive signals to communicate with PCs, modems, and other similar interfaces when paired with an external RS-232 line driver/receive. This device provides asynchronous, full-duplex communication (i.e., Baud rate: 38400, Data: 8 bit, Parity: none, Stop: 1 bit, Flow control: none).

SPI Interface

The MAX66300 is a slave device that communicates with its master—a microcontroller—through the serial SPI interface. This interface uses the signals SSEL, SCLK, MOSI, and MISO.

The SPI protocol defines communication in full bytes with the most significant bit being transmitted first. Every SPI communication sequence begins with at least 1 byte written to the slave device. The first byte that the slave receives from the master is understood as the beginning of the message. Depending on the first few message bytes the slave may need more bytes, e.g., more message data to complete the message; for a read function, after having received the beginning response message bytes, the slave starts sending data to the master.

The SPI protocol knows four communication modes, which differ in the polarity and phase of the SCLK signal. The MAX66300 supports MODE (0/0). See the timing specification in Figure 6.

The read timing of these graphics begins with the first bit that the MAX66300 transmits to the master and ends when the master ends the communication by deactivating SSEL (low to high transition). The data on the MOSI is latched (i.e., sampled) on the SCLK's rising edge and data on the MISO is updated (i.e., shifted out) on a falling edge of SCLK. Also, the first bit on the MOSI is latched on the first leading rising edge of SCLK. So data on the MOSI needs to be stable for at least a t_{SIS} before the first SCLK cycle for MAX66300. Therefore, the first bit transmitted from the MISO is updated at least a half cycle before the first SCLK cycle to meet the master's setup time.

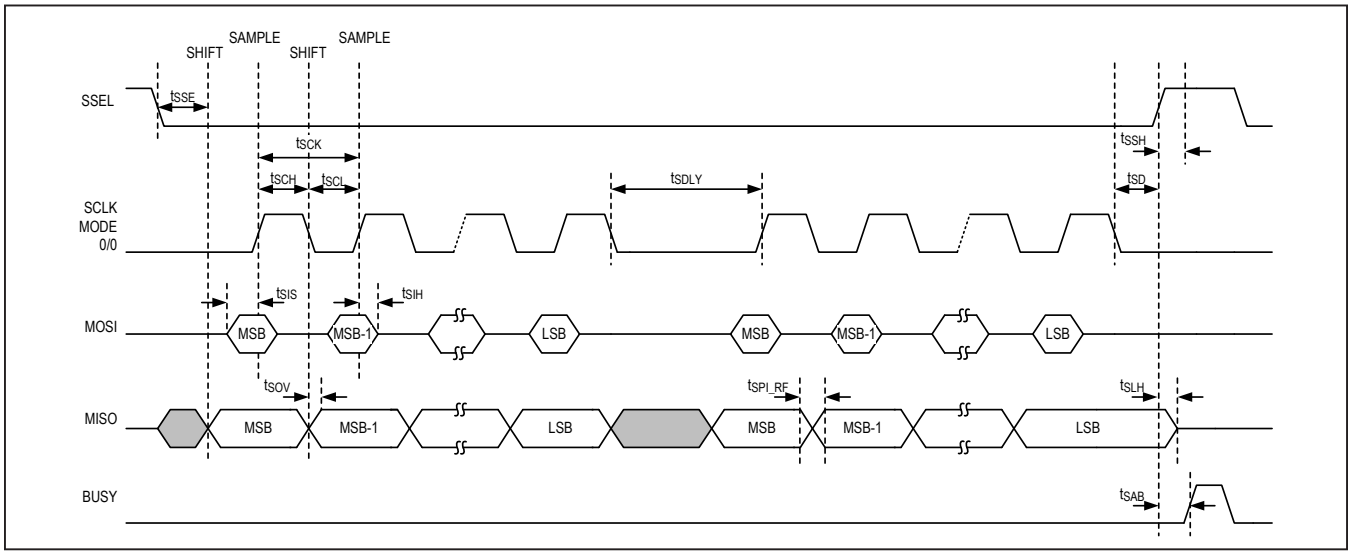


Figure 6. SPI Timing Specification

Applications Information

AFE Oscillator

The frequency range allowed by the regulations is 13.56MHz ±7kHz. The correct load capacitance has to be chosen according to the manufacturer's guideline. A temperature coefficent of type C0G capacitors should be used. It is not recommended to connect any components except quartz crystal and load capacitors to the oscillator's pins since any interference or noise injected into the oscillator corrupts the system performance. When an external clock source is used, the phase noise of the clock has to be kept low since it also corrupts the system performances.

Antenna Driver

The correct load impedance for a single output driver (100mW) is 7Ω resistive. The correct load impedance for a double parallel output driver (option bit 5, 200mW) is 3.5Ω resistive. The load impedance for a push-pull driver (option bits 5 and 6) must be at least 14Ω resistive. In this configuration, the consideration of chip power dissipation and junction temperature is necessary. It is also possible to use this configuration for low power systems with a direct antenna connection if a load impedance higher than 14Ω is used. Since the ASK modulation index is dependent on the load, it differs from those listed in Table 18.

Receiver

Systems using a 212kHz sub-carrier modulation should use the medium filter selection and systems using a 424kHz or 848kHz sub-carrier should use the high frequency filter selection. When a 424kHz or 848kHz system with on/off sub-carrier coding is used, the higher frequency zero enables very fast response of the receiver to the pulse burst with high DC level shift. When a BPSK system is used, lower frequency zero decreases phase distortion of the BPSK signal. System option bits control the receiver gain. Different receiver bandwidths result in different noise levels therefore enabling different gain and sensitivity levels. The combination of filter selection and gain selection allows the system designer to choose the best combination for the RFID reader.

Configuration Word (Option Bits) Selection Depending on Tag IC

The MAX66300 is compliant with almost all 13.56MHz tag ICs by setting the AFE by the use of Table 18. The large combinations offered by the MAX66300 option bits permit to adapt the reader IC to the tag communication protocol. Table 20 gives the ISO typical suggested option bit configuration depending on the tag IC used.

Table 20. Option Bit Configuration for ISO 15693 Standard

OPTION BIT	SUGGESTED VALUE	CONFIGURATION
0	1	Power up
1, 2, 3	1, 0, 0	OOK modulation
4	1	Short circuit enabled
5, 6	1, 1	Two drivers in differential
7, 8	0, 0	300kHz
9	0	1MHz
10, 11, 12	1, 0, 0	Gain decreased for 5.7dB
13	0	RFIN1 selected
14	1	AGC activated
15 to 20	0, 0, 0, 0, 0, 0	Standard configuration
21	0	Sub-carrier mode
22	0	BPSK not used
23	0	Analog output disable
24	0	Hold delay set to 5µs
25	1	High g_M
26	0	Internal quartz
27 to 31	0, 0, 0, 0, 0	Normal IC mode

Tag subcarrier: 424kHz or 484kHz

Modulation index: 100%

Reception bandwidth: 300kHz to 1MHz

AGC: Nominal gain

Configuration word value: (MSB) 02h 00h 44h 73h (LSB)

Antenna Configurations and Decoupling

The theoretical antenna configurations and typical decoupling are shown in Figure 7, Figure 8, and Figure 9. Since the LC tank values needed for tuning of the antenna are subject to a larger dialogue, this information is available in Application Note 5912: *Designing an Antenna for the MAX66300*.

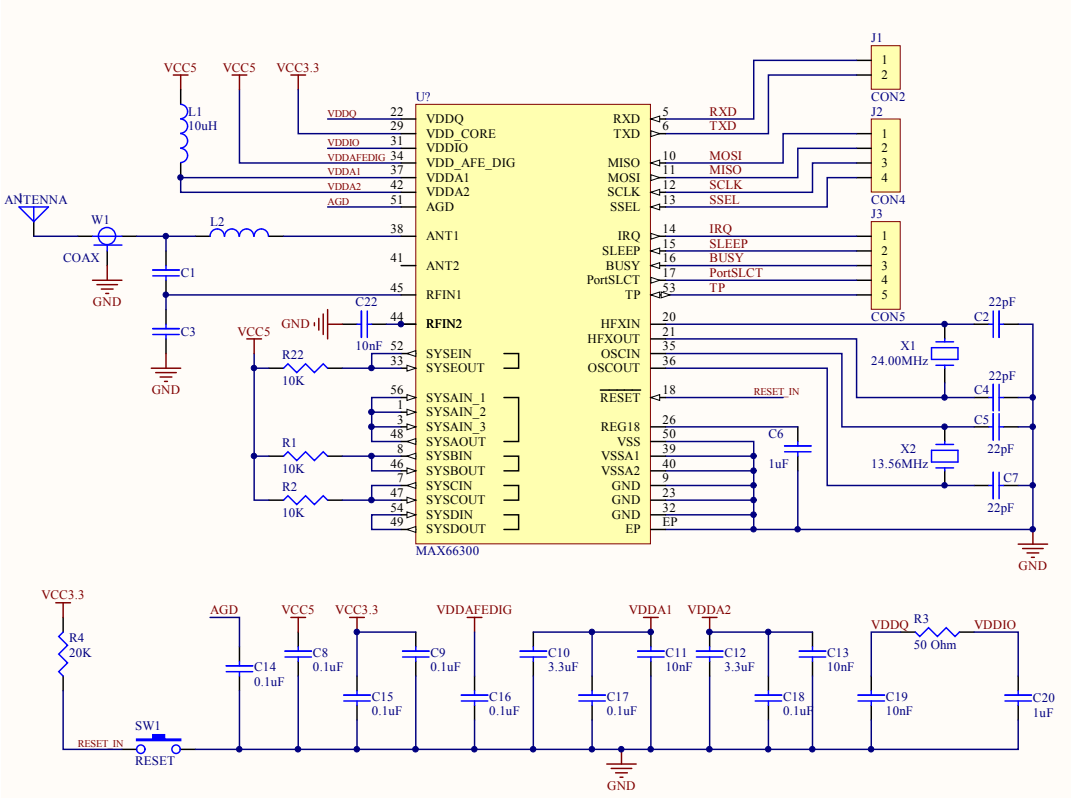


Figure 7. Single Output Driver (100mW)

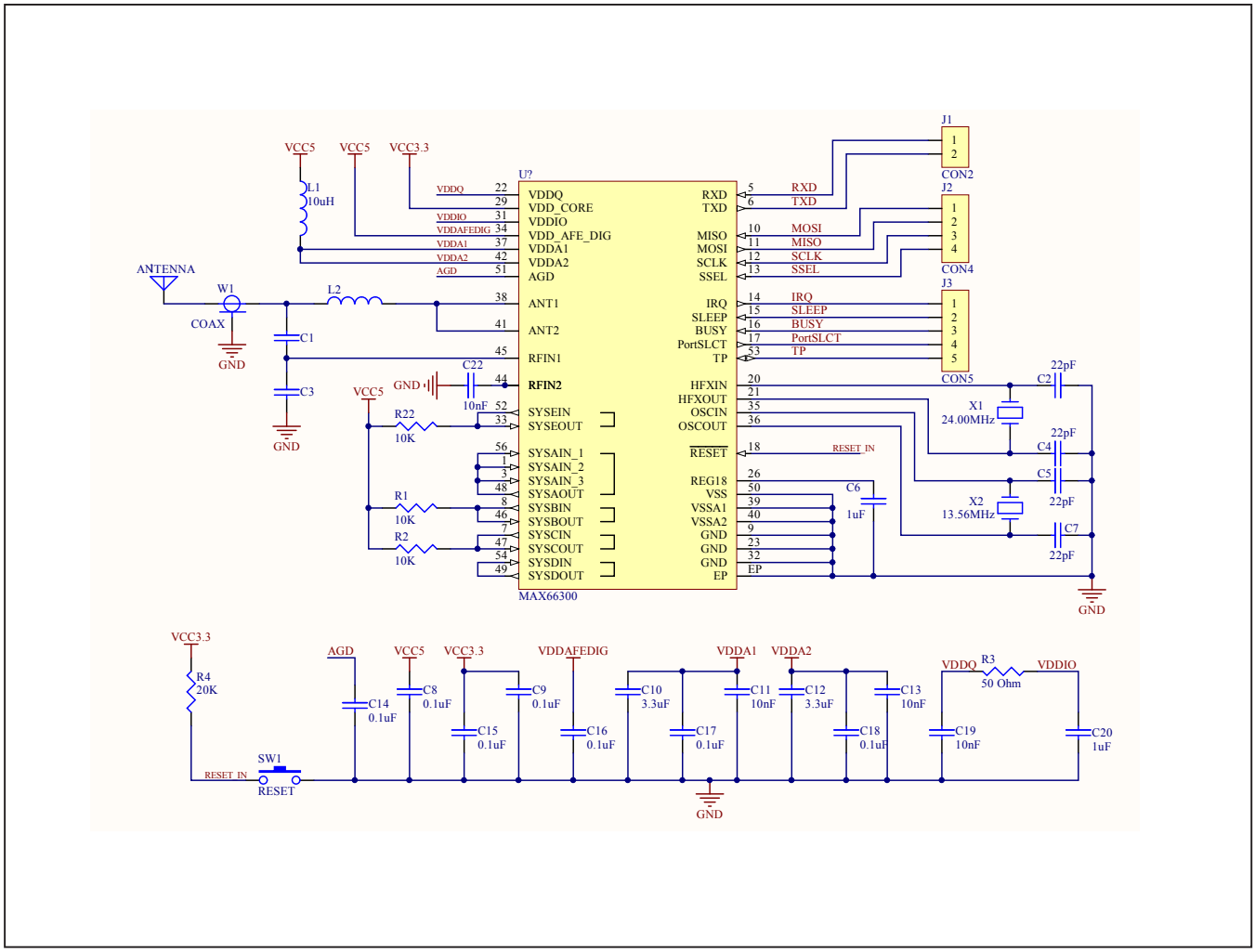


Figure 8. Double Parallel Output Driver (Options Bit 5, 200mW)

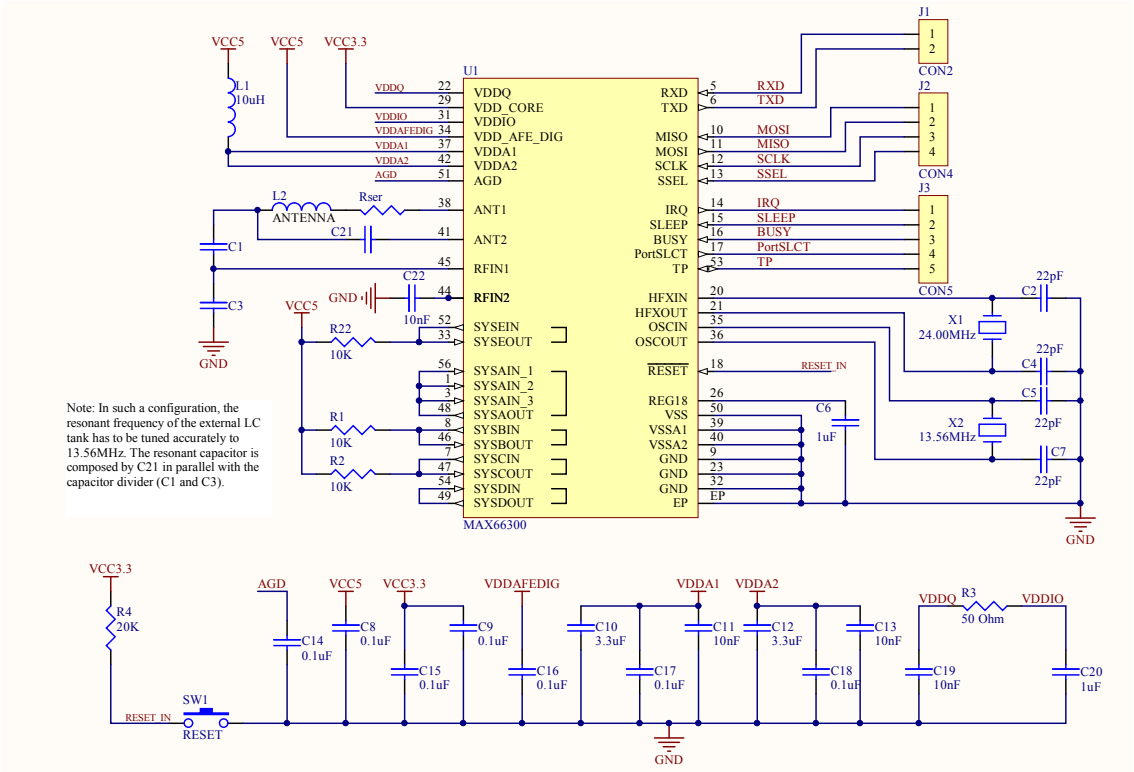


Figure 9. Configuration for Lower Power Systems with Direct Antenna Connections

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX66300ETN+	-40°C to +85°C	56 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688M+3	21-0135	90-0047

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	10/15	Removed M/S and MSS parameter fields	37, 38

