



AKD4499-B

AK4499 Evaluation Board Rev.0

1. General Description

The AKD4499-B is an evaluation board for the AK4499 (Premium Switched Resistor 4ch DAC) that supports Network-Audios, USB-DAC, Car-Audio Systems. It integrates differential output low pass filters, allowing quick evaluation with digital audio interface.

■ Ordering Guide

AKD4499-B -- Evaluation Board for the AK4499

(A USB I/F board for IBM-AT compatible computers and control software are included in this package.)

2. Function

- 10-pin Header for Serial Control
- Low Pass Filters (LPF) for Pre-amplifier Outputs
- Digital Audio Interface (AK4118A)
- Sample Rate Converter (AK4137)

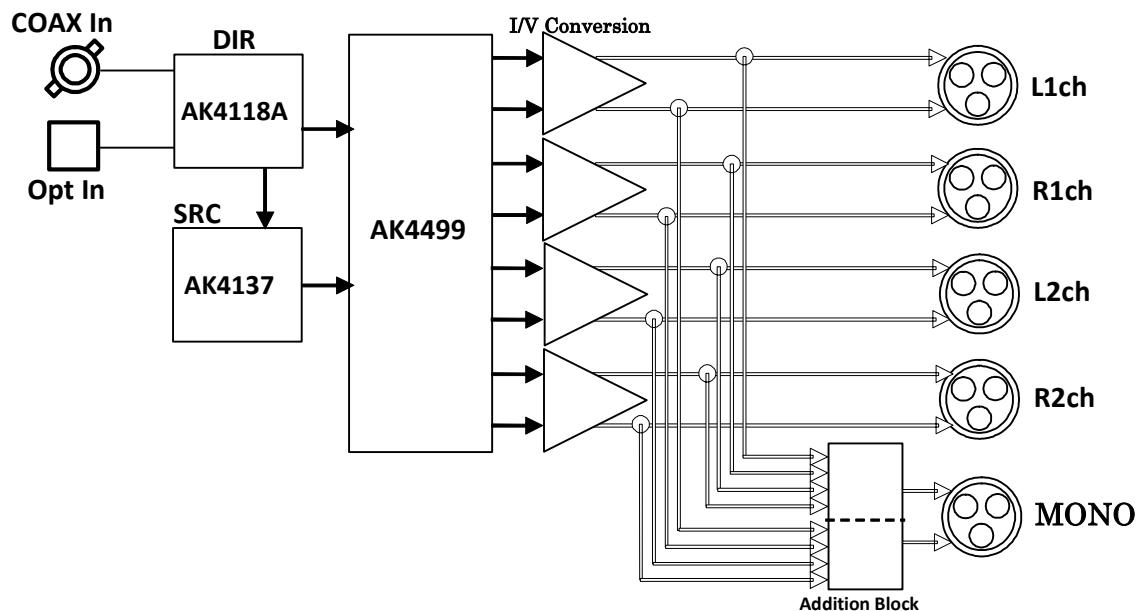


Figure 1. AKD4499-B Block Diagram ([Note 1](#))

Note 1. Circuit schematics are attached at the end of this document.

3. Board Appearance

■ Appearance Diagram

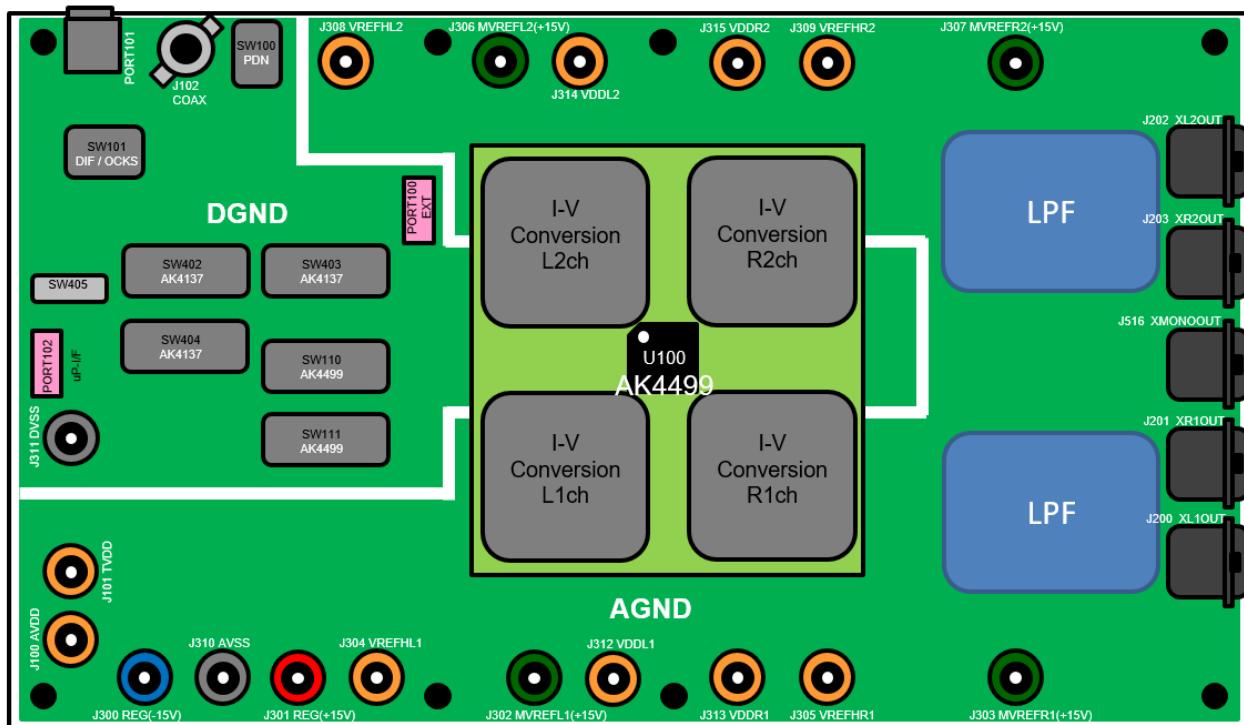


Figure 2. AKD4499-B Outline View

■ Description

- (1) Connectors for Power Supply and GND
(REG(+15V), REG(-15V), AVDD, TVDD, VDDL, VDDR, VREFHL, VREFHR, AGND, DGND)
Connectors for power supply and the ground
Refer to the “Power Supply Connections” for details.
- (2) SPDIF Input Connectors (J102/BNC Connector, PORT101/Optical Connector)
Input a SPDIF signal to the AK4118A.
Set the JP102 jumper pin to “BNC” side when using the J102 (BNC Connector) jack.
Set the JP102 jumper pin to “OPT” side when using the PORT101 (Optical Connector).
- (3) Analog Output Terminals (J200 / J201 / J202 / J203, XLR Connector)
Differential Analog Output Connector
- (4) Analog Differential MONO Output Terminals (J516, XLR Connector)
Differential MONO Analog Output Connector

(5) EXT1 PORT (PORT100)

10-pin Header for External Interfacing

External digital audio devices are interfaced to this port.

Set the JP110, JP111, JP112 JP113 and JP114 jumper pins to “EXT” side when using the PORT100 (EXT1).

Pin	I/O	Function	Pin	I/O	Function
1	I	MCLK	7	P	GND
2	I	BICK / BCK / DCLK	8	P	GND
3	I	SDATA1 / DINL1 / DSDL1	9	P	GND
4	I	LRCK / DINR1 / DSDR1	10	P	GND
5	I	SDATA2 / DIN2 / DSDL2	11	P	GND
6	I	DINR2 / DSDR2	12	P	GND

Table 1. PORT100 (EXT1) Pin Assignments

(6) AK4499 (U100)

The AK4499 is a premium switched resistor 4ch DAC.

(7) AK4118A (U101)

The AK4118A is a digital audio transceiver.

It is used when evaluating sound quality of the AK4499 by SPDIF signals.

(8) AK4137 (U400)

The AK4137 is a 2channels input/output Digital Sample Rate Converter (SRC).

(9) μP-IF PORT (PORT102)

10-pin Header for the USB I/F board

Connect the USB I/F board for IBM-AT compatible computers to this port for a connection to a USB port of a PC. Refer to the “Serial Control Mode” for details.

(10) Slide Switch and DIP Switches (SW405 / SW101 / SW110 / SW111 / SW402 / SW403 / SW404)

Setting Switches for the AK4499 and the AK4137.

Slide Switch : Left side is Serial Control Mode and Right side is Parallel Control Mode.

DIP Switches : Upside is “H” (ON) and Downside is “L” (OFF).

Refer to “■ Jumper Pin and DIP Switch Settings” for details.

(11) Toggle Switch (SW100)

Setting Switches for the AK4499, the AK4118A and the AK4137.

Upside is “L” (OFF) and Downside is “H” (ON).

4. Operation Sequence

■ Operation sequence

- 1). Power Supply Connections
- 2). Evaluation Mode
- 3). Jumper Pin and DIP Switch Settings
- 4). Power-up

■ Power Supply Connections

No.	Name	Color	Voltage	Content	Note	Default Setting
J301	+15V	Red	+10 to +15V	MVDD+ (AK4499), Op-Amp	This jack is always needed.	+15V
J300	-15V	Blue	-10 to -15V	Op-Amp	This jack is always needed.	-15V
J302	MVREFL1(+15V)	Green	+10 to +15V	MVREFL1 (AK4499)	This jack is always needed. These are used when supplying MVREFL/R(+15V) from a MVREF connector for a regulator.	+15V
J303	MVREFR1(+15V)	Green	+10 to +15V	MVREFR1 (AK4499)	Set the JP309, JP310, JP311 and JP312 jumper pins to "MVREF" side.	+15V
J306	MVREFL2(+15V)	Green	+10 to +15V	MVREFL2 (AK4499)		+15V
J307	MVREFR2(+15V)	Green	+10 to +15V	MVREFR2 (AK4499)		+15V
J101	TVDD	Orange	+2.7 to +3.6V	TVDD (AK4499)	These are used when supplying TVDD, AVDD, VDDL and VDDR from a +3V or a +5V connector without a regulator. Set the JP101 jumper pin to "+3V" side and the JP100, JP305, JP306, JP307 and JP308 jumper pins to "+5V" side.	Open
J100	AVDD	Orange	+4.75 to +5.25V	AVDD (AK4499)		Open
J312	VDDL1	Orange	+4.75 to +5.25V	VDDL1 (AK4499)		Open
J313	VDDR1	Orange	+4.75 to +5.25V	VDDR1 (AK4499)		Open
J314	VDDL2	Orange	+4.75 to +5.25V	VDDL2 (AK4499)		Open
J315	VDDR2	Orange	+4.75 to +5.25V	VDDR2 (AK4499)		Open
J304	VREFHL1	Orange	+4.75 to +5.25V	VREFHL1 (AK4499)	This jack is always needed. These are used when supplying VREFHL/R from a +5V connector without a regulator. Set the JP301, JP302, JP303 and JP304 jumper pins to "+5V" side.	Open
J305	VREFHR1	Orange	+4.75 to +5.25V	VREFHR1 (AK4499)		Open
J308	VREFHL2	Orange	+4.75 to +5.25V	VREFHL2 (AK4499)		Open
J309	VREFHR2	Orange	+4.75 to +5.25V	VREFHR2 (AK4499)		Open
J310	AVSS	Black	0V	Analog Ground	This jack is always needed.	0V
J311	DVSS	Black	0V	Digital Ground	This jack is always needed.	0V

Table 2. Power Supply Connections ([Note 2](#))

Note 2. Each power supply line should be distributed separately from the power supply unit.

■ Evaluation Mode

(1) Evaluation with a DIR (COAX) < Default >

The J102 (COAX) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the J102 (COAX) connector.

Set the JP102 (RX-SEL) jumper pin to “BNC”(3pin), and set the JP110 (MCLK), JP111 (BICK), JP112 (DATA1), JP113 (LRCK) and JP114 (DATA2) jumper pins to “DIR”, and set the JP400 (MCLK-SEL), JP402 (DATASEL) jumper pins to “DIR”.

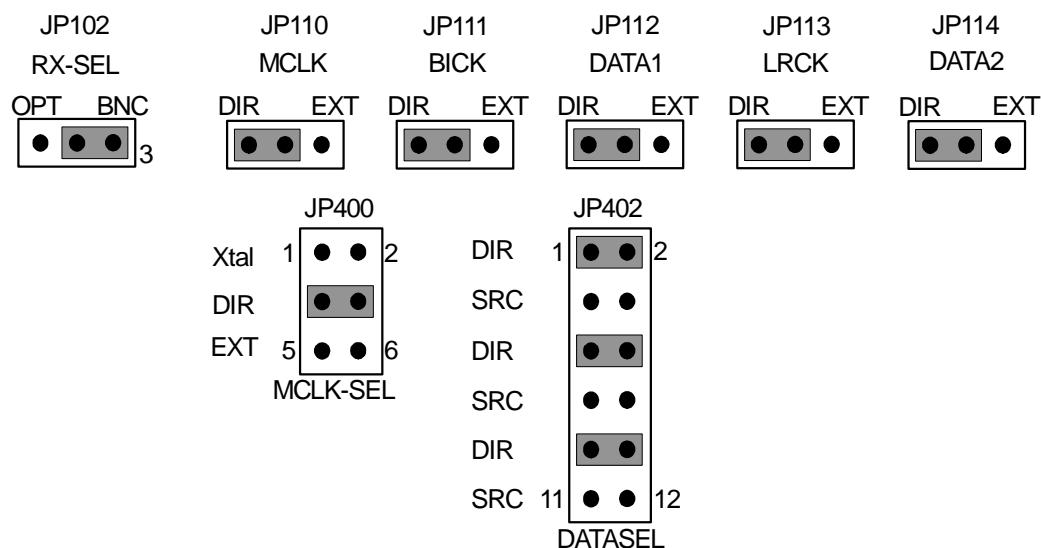


Figure 3. Jumper Pin Settings with DIR

(2) Evaluation with a DIR (OPTICAL)

The J102 (OPTICAL) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the input data of the PORT101 (OPTICAL) connector.

Set the JP102 (RX-SEL) jumper pin to “OPT”(1pin), and set the JP110 (MCLK), JP111 (BICK), JP112 (DATA1), JP113 (LRCK) and JP114 (DATA2) jumper pins to “DIR”, and set the JP400 (MCLK-SEL), JP402 (DATASEL) jumper pins to “DIR”.

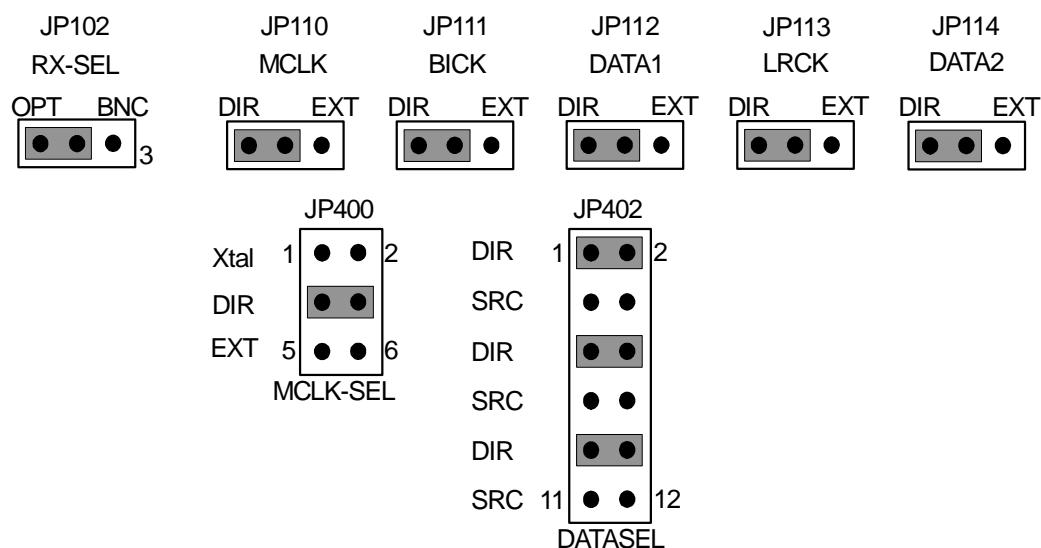


Figure 4. Jumper Pin Settings with DIR

(3) In the case that all interface clocks including the master clock are input externally. (PORT100)

Input all interface clocks including the master clock to the PORT100 (DSP).

The PORT100 (EXT1) port is used in this mode. MCLK, BICK, LRCK, SDATA1 and SDATA2 from the input data of the PORT100 (EXT1) 12pin-port connector.

Set the JP110 (MCLK), JP111 (BICK), JP112 (DATA1), JP113 (LRCK) and JP114 (DATA2) jumper pins to "EXT".

External data and clock input :

PORT100 : EXT1

Signal	Pin No.		Signal
GND	7	1	MCLK
GND	8	2	BICK / BCK / DCLK
GND	9	3	SDATA1 / DINL1 / DSDL1
GND	10	4	LRCK / DINR1 / DSRR1
GND	11	5	SDATA2 / DINL2 / DSDL2
GND	12	6	DINR2 / DSRR2

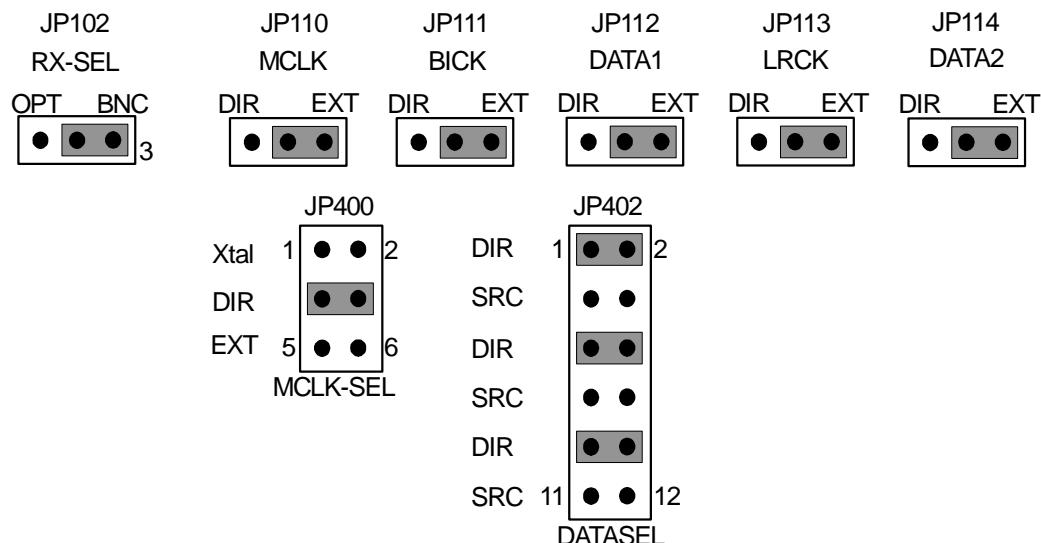


Figure 5. Jumper Pin Settings with External Clocks

■ Jumper Pin and DIP Switch Settings

(1) Jumper Pin Settings

Table 3-1. Jumper Settings for power supply

No.	Name	Content	Default Setting
JP100	AVDD	AVDD pin input select REG: The AVDD pin is supplied from the T100 regulator. +5V: The AVDD pin is supplied from the J100 (AVDD) connector.	REG
JP101	TVDD	TVDD pin input select REG: The TVDD pin is supplied from the T101 regulator. +3V: The TVDD pin is supplied from the J101 (TVDD) connector.	REG
JP301	VREFHL1	VREFHL1 pin input select REG: The VREFHL1 pin is supplied from the VREFHL1 regulator. +5V: The VREFHL1 pin is supplied from the J304 (VREFHL1) connector.	REG
JP302	VREFHR1	VREFHR1 pin input select REG: The VREFHR1 pin is supplied from the VREFHR1 regulator. +5V: The VREFHR1 pin is supplied from the J305 (VREFHR1) connector.	REG
JP303	VREFHL2	VREFHL2 pin input select REG: The VREFHL2 pin is supplied from the VREFHL2 regulator. +5V: The VREFHL2 pin is supplied from the J308 (VREFHL2) connector.	REG
JP304	VREFHR2	VREFHR2 pin input select REG: The VREFHR2 pin is supplied from the VREFHR2 regulator. +5V: The VREFHR2 pin is supplied from the J309 (VREFHR2) connector.	REG
JP309	MVREFL1	MVREFL1 power supply for VREFHL1 regulator input select MVDD+: The power supply (MVREFL1) for VREFHL1 regulator is supplied from the J301 (+15V) connector. MVREF: The power supply (MVREFL1) for VREFHL1 regulator is supplied from the J302 (MVREFL1(+15V)) connector.	MVREF
JP310	MVREFR1	MVREFR1 power supply for VREFHR1 regulator input select MVDD+: The power supply (MVREFR1) for VREFHR1 regulator is supplied from the J301 (+15V) connector. MVREF: The power supply (MVREFR1) for VREFHR1 regulator is supplied from the J303 (MVREFR1(+15V)) connector.	MVREF
JP311	MVREFL2	MVREFL2 power supply for VREFHL2 regulator input select MVDD+: The power supply (MVREFL2) for VREFHL2 regulator is supplied from the J301 (+15V) connector. MVREF: The power supply (MVREFL2) for VREFHL2 regulator is supplied from the J306 (MVREFL2(+15V)) connector.	MVREF
JP312	MVREFR2	MVREFR2 power supply for VREFHR2 regulator input select MVDD+: The power supply (MVREFR2) for VREFHR2 regulator is supplied from the J301 (+15V) connector. MVREF: The power supply (MVREFR2) for VREFHR2 regulator is supplied from the J307 (MVREFR2(+15V)) connector.	MVREF
JP305	VDDL1	VDDL1 pin input select REG: The VDDL1 pin is supplied from the T300 regulator. +5V: The VDDL1 pin is supplied from the J312 (VDDL1) connector.	REG
JP306	VDDR1	VDDR1 pin input select REG: The VDDR1 pin is supplied from the T301 regulator. +5V: The VDDR1 pin is supplied from the J313 (VDDR1) connector.	REG

JP307	VDDL2	VDDL2 pin input select REG: The VDDL2 pin is supplied from the T302 regulator. +5V: The VDDL2 pin is supplied from the J314 (VDDL2) connector.	REG
JP308	VDDR2	VDDR2 pin input select REG: The VDDR2 pin is supplied from the T303 regulator. +5V: The VDDR2 pin is supplied from the J315 (VDDR2) connector.	REG
JP300	VSS-SEL1	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	short
JP320	VSS-SEL2	Connection between Analog VSS pattern and Digital VSS pattern. short: Connect Analog VSS pattern and Digital VSS pattern. open: Detach Analog VSS pattern and Digital VSS pattern.	short

Table 3-2. Jumper Settings for data & clock

No.	Name	Content	Default Setting
JP102	RX-SEL	SPDIF signal for AK4115 BNC(3pin): SPDIF signal is supplied from the J102 (COAX) connector. OPT(1pin): SPDIF signal is supplied from the PORT101 (Optical) connector.	BNC (3pin)
JP110	MCLK	MCLK pin input select DIR: MCLK signal is supplied from the DIR (AK4118A). EXT: MCLK signal is supplied from the PORT100 (EXT1).	DIR
JP111	BICK	BICK pin input select DIR: BICK signal is supplied from the DIR (AK4118A). EXT: BICK signal is supplied from the PORT100 (EXT1).	DIR
JP113	LRCK	LRCK pin input select DIR: LRCK signal is supplied from the DIR (AK4118A). EXT: LRCK signal is supplied from the PORT100 (EXT1).	DIR
JP112	DATA1	SDATA1 pin input select DIR: SDATA1 signal is supplied from the DIR (AK4118A). EXT: SDATA1 signal is supplied from the PORT100 (EXT1).	DIR
JP114	DATA2	SDATA2 pin input select DIR: SDATA2 signal is supplied from the DIR (AK4118A). EXT: SDATA2 signal is supplied from the PORT100 (EXT1).	DIR
JP400	MCLK-SEL	MCLK input source select Xtal: This setting is for used Xtal (X400) clock. DIR: This setting is for used DIR(AK4118A) Output MCLK. EXT: This setting is for used External clock.	DIR short
JP402	DADASEL	BICK/LRCK/SDATA input source select DIR: This setting is for used DIR (AK4118A) Output signals. SRC: This setting is for used SRC (AK4137) Output signals.	DIR short
JP115	DEM0/DSDL1	DEM0/DSDL1 pin input select DEM0: This setting is for Parallel Control Mode. (DEM0 setting by SW111) DVSS(3pin): This pin is for DSD Data (DSDL1) Input.	DEM0
JP116	DSDR1/TSTO4	DSDR1/TSTO4 pin input/output select DSDR1(1pin): This pin is for DSD Data (DSDR1) Input or TEST Data (TSTO4) Output. DVSS(2pin): This pin is DVSS pin for DSD Data Input Mode or TEST Data Output Mode.	open

JP117	TDM0/DCLK	TDM0/DCLK pin input select TDM0: This setting is for Parallel Control Mode. (TDM0 setting by SW111) DVSS(3pin): This pin is for DSD Data (DCLK) Input Mode.	TDM0
JP118	TDM1/DSDL2	TDM1/DSDL2 pin input select TDM1: This setting is for Parallel Control Mode. (TDM1 setting by SW111) DVSS(3pin): This pin is for DSD Data (DSDL2) Input Mode.	TDM1
JP119	DCHAIN/DSDR2	DCHAIN/DSDR2 pin input select DCHAIN: This setting is for Parallel Control Mode. (DCHAIN setting by SW111) DVSS(3pin): This pin is for DSD Data (DSDR2) Input Mode.	DCHAIN
JP120	TDM0/TSTO3	TDM0/TSTO3 pin input/output select TDM0(1pin): This pin is for TDM Data (TDM0) Output or TEST Data (TSTO3) Output. DVSS(2pin): This pin is DVSS pin for TDM Data Output Mode or TEST Data Output Mode.	open
JP121	SSLOW/WCK	SSLOW/WCK pin input select SSLOW: This setting is for Parallel Control Mode. (SSLOW setting by SW110) DVSS(3pin): This pin is for Data (WCK) Input Mode.	SSLOW

Table 3-3. Jumper Settings for control signal

No.	Name	Content	Default Setting
JP122	PS1 CSN/SMUTE	CSN/SMUTE pin input select CSN: This setting is for Serial Control Mode. SMUTE: This setting is for Parallel Control Mode. (SMUTE setting by SW110)	CSN
JP123	PS2 CCLK/SCL/SD	CCLK/SCL/SD pin input select CCLK/SCL: This setting is for Serial Control Mode. SD: This setting is for Parallel Control Mode. (SD setting by SW110)	CCLK/SCL
JP124	PS3 CDTI/SDA/SLOW	CDTI/SDA/SLOW pin input select CDTI/SDA: This setting is for Serial Control Mode. SLOW: This setting is for Parallel Control Mode. (SLOW setting by SW110)	CDTI/SDA
JP125	DIF0/DZFL/TSTO1	DIF0/DZFL/TSTO1 pin input select DIF0: This setting is for Parallel Control Mode. (DIF0 setting by SW110) DVSS: This setting is for Serial Control Mode. (DZFL: Output, TSTO1: Output)	open
JP126	DIF1/DZFR/TSTO2	DIF1/DZFR/TSTO1 pin input select DIF1: This setting is for Parallel Control Mode. (DIF1 setting by SW110) DVSS: This setting is for Serial Control Mode. (DZFR: Output, TSTO2: Output)	open

(2) DIP Switch Setting

Upside is ON ("H"), and Downside is OFF ("L").

AK4118A Settings :

[SW101]: Setting of the AK4118A

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	Audio I/F Format for AK4118A Refer to Table 4-2.		H
2	DIF1			L
3	DIF0			L
4	OCKS1	Master Clock setting for AK4118A Refer to Table 4-3.		L
5	OCKS0			L

Table 4-1. SW101 Setting (AK4118A)

Mode	DIF2 pin	DIF1 pin	DIF0 pin	SDTO	LRCK	BICK	
0	L	L	L	16bit Right justified	H/L	O	64fs
1	L	L	H	18bit Right justified	H/L	O	64fs
2	L	H	L	20bit Right justified	H/L	O	64fs
3	L	H	H	24bit Right justified	H/L	O	64fs
4	H	L	L	24bit Left justified	H/L	O	64fs
5	H	L	H	24bit I2S	L/H	O	64fs
6	H	H	L	24bit Left justified	H/L	I	64-128fs
7	H	H	H	24bit I2S	L/H	I	64-128fs

Table 4-2. Audio I/F Format of the AK4118A

< Default >

Mode	OCKS1	OCKS0	MCK01	fs (max)
0	L	L	256fs	96 kHz
1	L	H	256fs	96 kHz
2	H	L	512fs	48 kHz
3	H	H	128fs	192 kHz

< Default >

Table 4-3. Master Clock Setting of the AK4118A

AK4499 Settings :

[SW110]: Setting of the AK4499

No.	Name	ON ("H")	OFF ("L")	Default
1	LDOE	LDO "ON"	LDO "OFF"	H
2	SMUTE	Mute "ON"	Mute "OFF"	L
3	SSLOW	Digital Filter Setting Refer to Table 5-2. (In Parallel Control Mode)		
4	SD			
5	SLOW			
6	DIF0	Audio I/F Format for AK4499 Refer to Table 5-3. (In Parallel Control Mode)		
7	DIF1	Audio I/F Format for AK4499 Refer to Table 5-3. (In Parallel Control Mode)		
8	DIF2 /CAD0	Audio I/F Format for AK4499 Refer to Table 5-3. (In Parallel Control Mode)		
		CAD0 pin= "H"	CAD0 pin= "L"	
9	ACKS /CAD1	Auto Setting Mode (In Parallel Control Mode)	Manual Setting Mode	
		CAD1 pin= "H"	CAD1 pin= "L"	
10	VTSEL	VIH/L level select of MCLK pin. VTSEL pin = "H" VIH=2.2V, VIL=0.8V		
		VTSEL pin = "L" VIH=1.36V, VIL=0.34V		

Table 5-1. SW110 Setting (AK4499)

SSLOW	SD	SLOW	Mode
L	L	L	Sharp roll-off filter
L	L	H	Slow roll-off filter
L	H	L	Short delay sharp roll-off filter
L	H	H	Short delay slow roll-off filter
H	L	L	Super Slow roll-off filter
H	L	H	Reserved
H	H	L	Low dispersion Shot Delay filter / Programable FIR filter
H	H	H	

< Default >

Table 5-2. Digital Filter Setting of the AK4499

Mode	DIF2 pin	DIF1 pin	DIF0 pin	Input Format	BICK
0	L	L	L	16bit LSB justified	$\geq 32fs$
1	L	L	H	20bit LSB justified	$\geq 48fs$
2	L	H	L	24bit MSB justified	$\geq 48fs$
3	L	H	H	24bit I ² S Compatible	$\geq 48fs$
4	H	L	L	24bit LSB justified	$\geq 48fs$
5	H	L	H	32bit LSB justified	$\geq 64fs$
6	H	H	L	32bit MSB justified	$\geq 64fs$
7	H	H	H	32bit I ² Compatible	$\geq 64fs$

< Default >

Table 5-3. Audio I/F Format of the AK4499

[SW111]: Setting of the AK4499

No.	Name	ON ("H")	OFF ("L")	Default
1	PSN	Parallel Control Mode	Serial Control Mode	L
2	DEM0	De-emphasis Control Refer to Table 5-5 . (In Parallel Control Mode)		H
3	TDM0	Audio I/F Format for AK4499 Refer to Table 5-6 . (In Parallel Control Mode)		L
4	TDM1			L
5	DCHAIN	Daisy Chain Mode (In Parallel Control Mode)	Normal mode	L
6	INVR/I2C	Rch Signal Invert (In Parallel Control Mode)	Normal	H
		I2C-Bus Control Mode (In Serial Control Mode)	3-wire Control Mode	
7	TESTE	Test Mode	Normal Mode	L
8	NC		-	L
9	NC		-	L
10	NC		-	L

Table 5-4. SW111 Setting (AK4499)

DEM0	Mode
L	44.1kHz
H	OFF

< Default >

Table 5-5. De-emphasis Control of the AK4499

Mode	TDM1 pin	TDM0 pin	Input Format Mode	< Default >
0	L	L	Normal Mode	
1	L	H	TDM128 Mode	
2	H	L	TDM256 Mode	
3	H	H	TDM512 Mode	

Table 5-6. Audio I/F Format of the AK4499

AK4137 Settings :

[SW402]: Setting of the AK4137

No.	Name	ON ("H")	OFF ("L")	Default
1	PSN	Parallel Control Mode	Serial Control Mode	H
2	I2C	I2C-Bus Control Mode (In Serial Control Mode)	4-wire Control Mode	H
3	SD			L
4	SLOW	Digital Filter select in parallel control mode.		L
5	CM3			L
6	CM2			L
7	CM1	Clock select or Mode setting.		L
8	CM0			L
9	DEM1			L
10	DEMO	De-emphasis Control in Parallel control mode.		H

Table 6-1. SW402 Setting (AK4137)

[SW403]: Setting of the AK4137

No.	Name	ON ("H")	OFF ("L")	Default
1	IDIF2			L
2	IDIF1	Digital Input Format in Parallel control mode.		H
3	IDIFO			L
4	TEST1	TEST1 pin setting.		L
5	TEST0	TEST0 pin setting.		L
6	ODIF1			H
7	ODIFO	Audio Interface Format for Output PORT.		L
8	DITHER	Dither ON	Dither OFF	L
9	SMSEMI	Soft Mute: Semi Auto mode	Manual mode	L
10	VSEL	Digital Power select DV18 is Power supply	DV18 is Output	H

Table 6-2. SW403 Setting (AK4137)

[SW404]: Setting of the AK4137

No.	Name	ON ("H")	OFF ("L")	Default
1	SMT1			L
2	SMT0	Soft Mute Timer select		L
3	TDM	TDM Format select TDM mode for output (connected to DVDD)	Stereo mode (connected to DVSS)	L
4	CLKMODE	Master clock select External master clock or TDM="H" (connected to DVDD)	X'tal mode (connected to DVSS)	H
5	OBIT1			L
6	OBIT0	Bit Length select for Output PORT.		L
7	NC	-		L
8	NC	-		L
9	NC	-		L
10	NC	-		L

Table 6-3. SW404 Setting (AK4137)

■ Resistor Settings

(1) Resistor Settings

Table 7-1. Resistor Settings for Mono Mode Outputs

No.	Name	Content	Default Setting
R240 R241 R242 R243	XMONOOUT_P	Resistors for Analog Differential Mono Mode Positive Output Connector pin. (J516, XLR Connector) Connection (620ohm) : Mono Mode Output. Open : Single Mode Output	Open
R244 R245 R246 R247	XMONOOUT_N	Resistors for Analog Differential Mono Mode Negative Output Connector pin. (J516, XLR Connector) Connection (620ohm) : Mono Mode Output. Open: Single Mode Output	Open

■ Power-up

Upside is OFF (“L”), and Downside is ON (“H”).

[SW100] (PDN): DAC Reset control. It must be set to “H” during operation.

After power-up, the AKD4499-B must be reset once.

To reset the AKD4499-B, set the SW100 toggle switch to “L” and power down the AK4499, AK4137 and the AK4118A.

Then, release the power-down by setting back the SW100 to “H”.

■ Serial Control Mode

The AKD4499-B should be connected to a PC (IBM-AT compatible) via a USB control box (AKDUSBIF-B) included in this package. The USB control box is connected to a PC with a USB cable and the AKD4499-B with a 10-pin flat cable. ([Note.4](#), [Note.5](#))

Note 3. The AKD4499-B accepts only one AKDUSBIF-B at one time. It does not operate if two or more AKDUSBIF-Bs are connected.

Note 4. Connect the 10pin Flat Cable as the red line of the cable is connected to the 1 pin of the 10pin Header of the board.

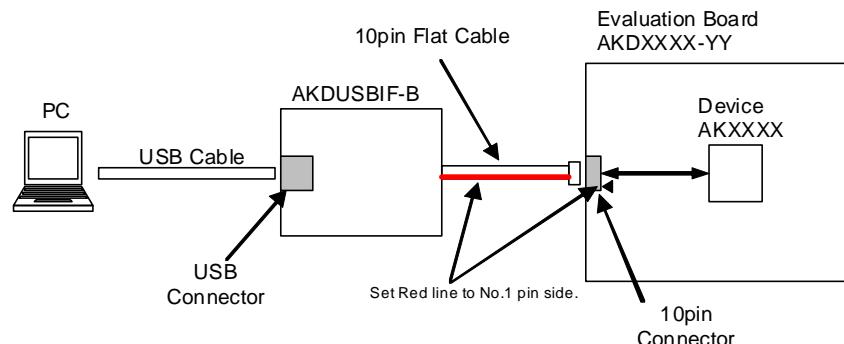


Figure 10. AKDUSBIF-B Connection

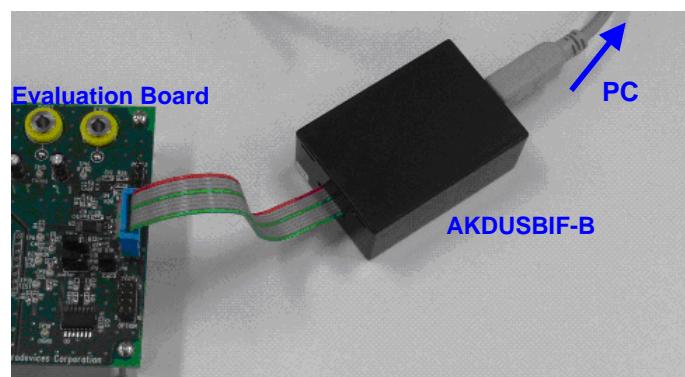


Figure 11. AKDUSBIF-B

Set up the jumper pins.

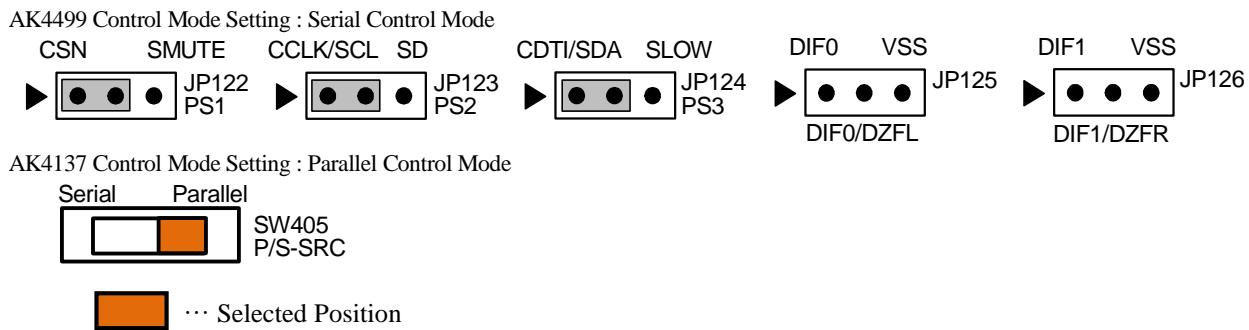
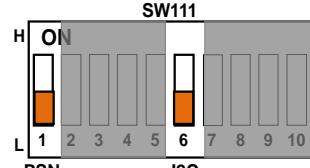
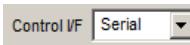
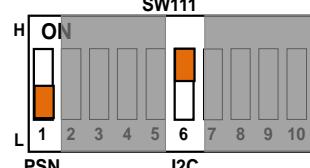
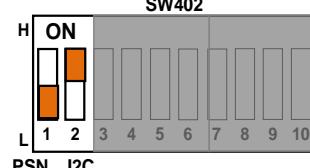


Figure 12. Jumper pin and Slide Switch setting

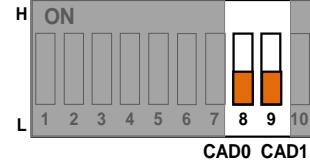
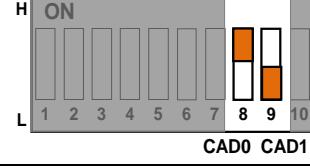
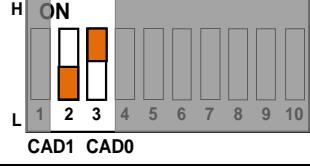
Other settings.

Serial Control Mode	SW111 (AK4499) (No.1: PSN, No.6: I2C)	SW402 (AK4137) (No.1: PSN, No.2: I2C)	Control Software (Control I/F)
3-wire			
I ² C-Bus			

 ... Selected Position

Table 12-1. Serial control mode setting

When using this evaluation board in serial control mode, settings of the CAD1 pin and the CAD0 pin on the board must match the Chip Address settings of the control software.

Chip Address	SW110 (AK4499) (No.8: CAD0, No.9: CAD1)	SW403 (AK4137) (No.3: CAD0, No.2: CAD1)	Control Software (Chip Address)
"00"			
"01"			

"10"	<p>SW110 H ON L 1 2 3 4 5 6 7 8 9 10 CAD0 CAD1</p>	<p>SW403 H ON L 1 2 3 4 5 6 7 8 9 10 CAD1 CAD0</p>	<p>Chip Address 10</p>
"11"	<p>SW110 H ON L 1 2 3 4 5 6 7 8 9 10 CAD0 CAD1</p>	<p>SW403 H ON L 1 2 3 4 5 6 7 8 9 10 CAD1 CAD0</p>	<p>Chip Address 11</p>



... Selected Position

Table 12-2. "Chip Address" setting

Control Software Manual

■ Evaluation Board and Control Software Manual

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB cable.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD4499-B Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “AKD4499-B.exe” to open the control program.
6. Begin evaluation by following the procedure below.

[Supported OS]

Windows XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
64bit OS is not supported.



Figure 13-1. Control Program Window

■ Operation Overview

Register map is controlled by this control software.

Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Box” section for details of each dialog box setting.

1.[Port Reset]: Reset connection to PC

Click this button after the control software starts up and the evaluation board is connected to the PC via USB cable.

2.[Write Default]: Register Initialization

Use this button to initialize the registers when the device is reset by a hardware reset.

3.[All Write]: Execute write command for all registers displayed.

4.[All Read]: Execute read command for all registers displayed. ([Note 5](#))

5.[Save]: Save current register settings to a file.

6.[Load]: Execute data write from a saved file.

7.[All Reg Write]: [All Reg Write] dialog box pops up.

8.[Data R/W]: [Data R/W] dialog box pops up.

9.[Sequence]: [Sequence] dialog box pops up.

10.[Sequence(File)]: [Sequence(File)] dialog box pops up.

Note 5. The [All Read] button is only valid when the interface mode for register control is in I²C bus control mode.

When input dummy command settings to AK4499 and the connection error by the evaluation board to a PC with USB cable, the following No Ack error message will pop up. Click “OK”.

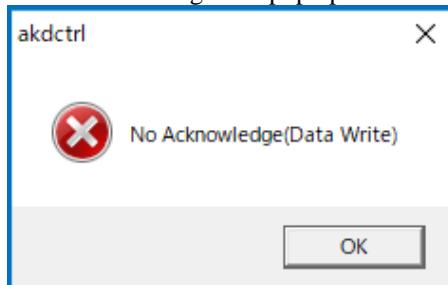


Figure 13-2. No ack message window

■ Tab Functions

1. [REG] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch.

Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).

Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)

Grayed out registers are Read-Only registers. They cannot be controlled.

The registers which are not defined on the datasheet are indicated as “---”.

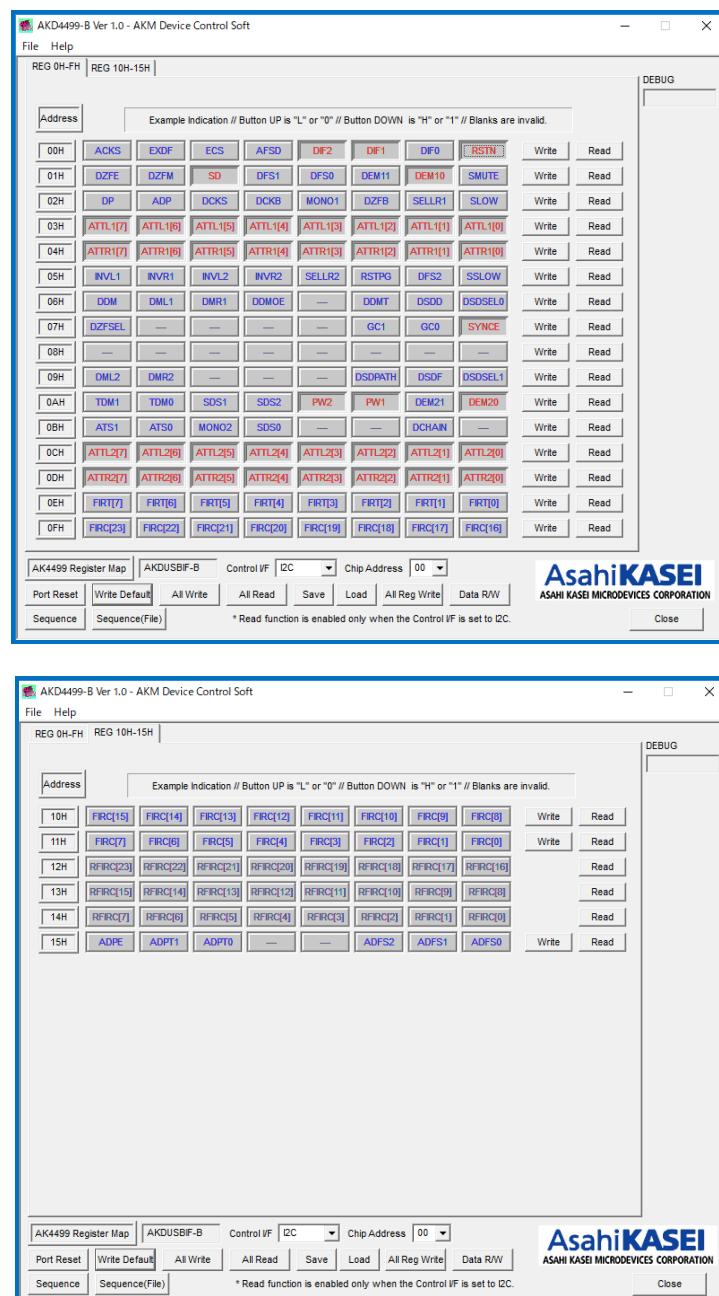


Figure 14. REG Window

[Write] button: Data Write Dialog

Select the [Write] button located on the right of the each corresponding address when changing two or more bits on the same address simultaneously.

Click the [Write] button for the register pop-up dialog box shown below.

When the checkbox next to the register is checked, the data will become “1”. When the checkbox is not checked, the data will become “0”. Click [OK] to write the set values to the registers, or click [Cancel] to cancel this setting.

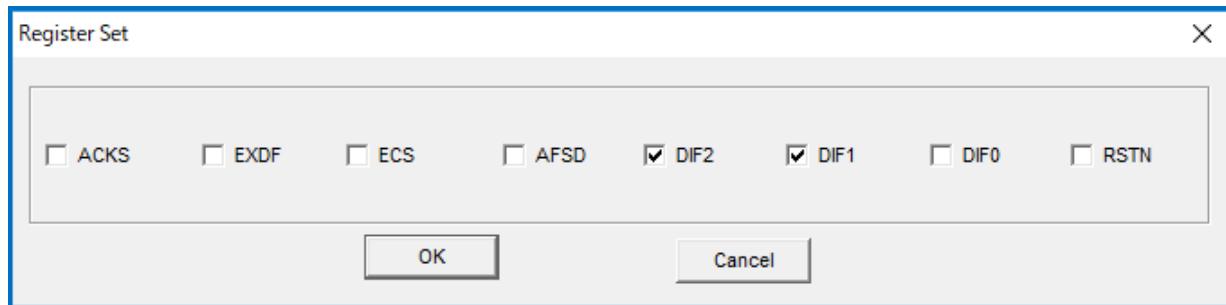


Figure 15. Register Set Window

[Read] button: Data Read (Only in I²C-bus Control Mode)

Click the [Read] button located on the right of the each corresponding address to execute a register read.

The current register value will be displayed in the register window as well as in the upper right hand DEBUG window.

Button Down indicates “1” and the bit name is shown in red (when read only the bit name is shown in dark red). Button Up indicates “0” and the bit name is shown in blue (when read only the bit name is shown in gray)

■ Dialog Box

1. [All Reg Write]: All Register Write dialog box

Click [All Reg Write] button in the main window to open register setting file window shown below. Register setting files saved by [SAVE] button may be applied.

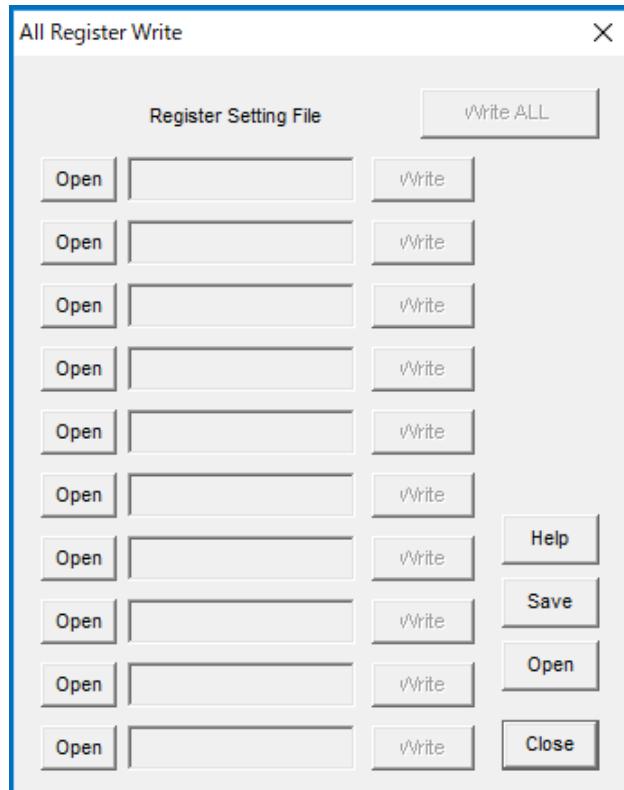


Figure 16. [All Reg Write] Window

[Open (left)]: Select a register setting file (*.akr).

[Write]: Execute register write with selected setting file.

[Write All]: Execute register write with all selected setting files.

Selected files are executed in descending order.

[Help]: Open help window.

[Save]: Save register setting file assignment. File name is “*.mar”.

[Open (right)]: Open saved register setting file assignment “*.mar”.

[Close]: Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
2. When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data is written to the specified address.

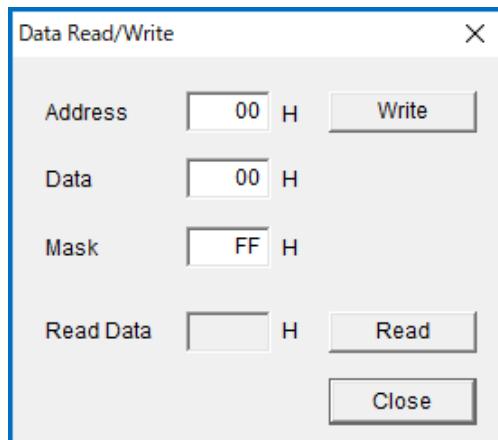


Figure 17. [Data R/W] Window

[Address] Box: Input data write address in hexadecimal numbers.

[Data] Box: Input write data in hexadecimal numbers.

[Mask] Box: Input mask data in hexadecimal numbers.

This value “ANDed” with the write data becomes the input data.

[Write]: Write data generated from Data and Mask value is written to the address specified in “Address” box.

([Note 6](#))

[Read]: Read data from the address specified in “Address” box. ([Note 7](#))

[Close]: Close dialog box and finish process.

Data write will not be executed unless [Write] is clicked.

Note 6. The register map will be updated after executing the [Write] command.

Note 7. The [Read] button is only valid when the interface mode for register control is in I²C bus control mode.

3. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

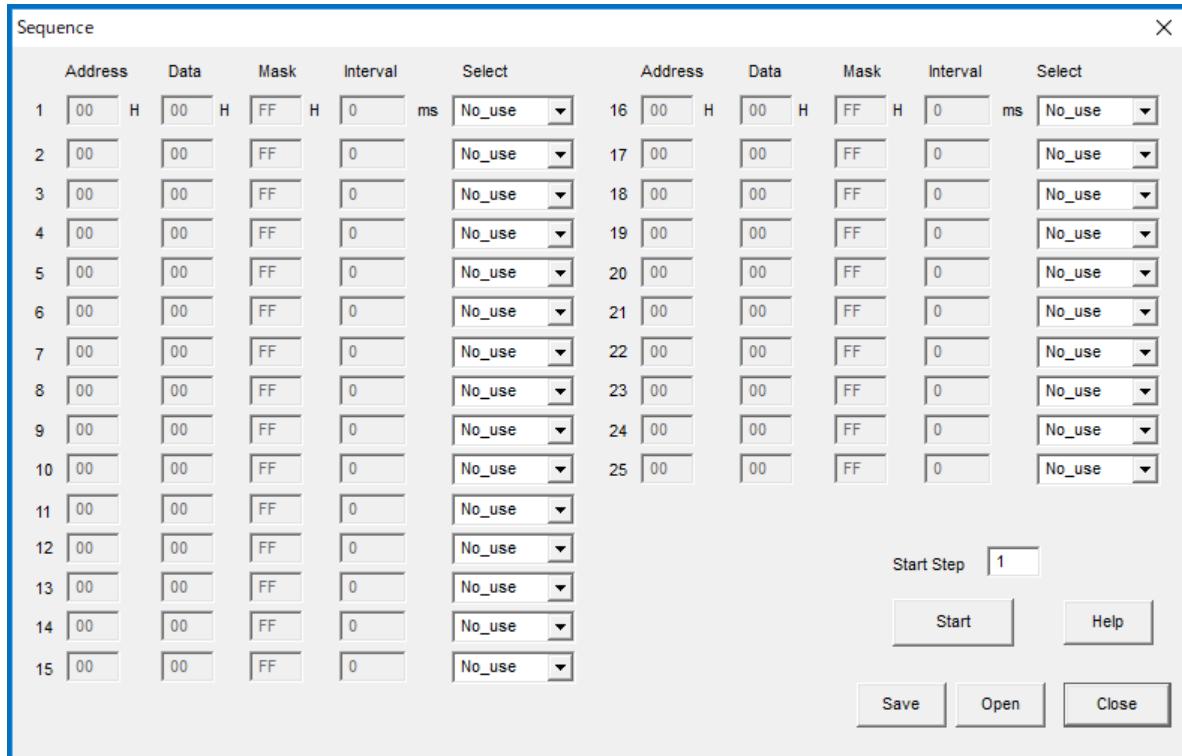


Figure 18. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

Use [Select] pull-down box to choose commands.
Corresponding input boxes will be valid.

<Combo Box>

- No_use: Not using this address
- Register: Register write
- Reg(Mask): Register write (Masked)
- Interval: Take an interval
- Stop: Pause the sequence
- End: End the sequence

2. Input Sequence

[Address]: Data Address

[Data]: Write Data

[Mask]: Mask

This value “ANDed” with the write data becomes the input data.

When Mask = 0x00, current setting is hold.

When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.

When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.

Upper 4bit is hold to current setting.

[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

- [Start] button : Execute the sequence.
- [Help] button : Open a help window.
- [Save] button : Save sequence settings as a file. The file name is “*.aks”.
- [Open] button : Open a sequence setting file “*.aks”.
- [Close] button : Close the dialog box and finishes the process.

Stop Sequence

When “Stop” command is selected in the sequence, the process is paused at this step. It is resumed by clicking the [Start] button. The process starts from the step shown in [Start Step] box. This step number returns to “1” when the sequence is executed until the end. Input arbitrary step number to the [Start Step] box to start the process from the middle of sequence.

The process sequence can be restarted from the beginning by writing “1” to the [Start Step] box and click the [Start] button during the process.

4. [Sequence(File)]: Sequence(File) Dialog

Click the [Sequence(File)] button to open sequence setting file dialog box shown below.
Files saved in the “Sequence setting dialog” can be applied in this dialog.

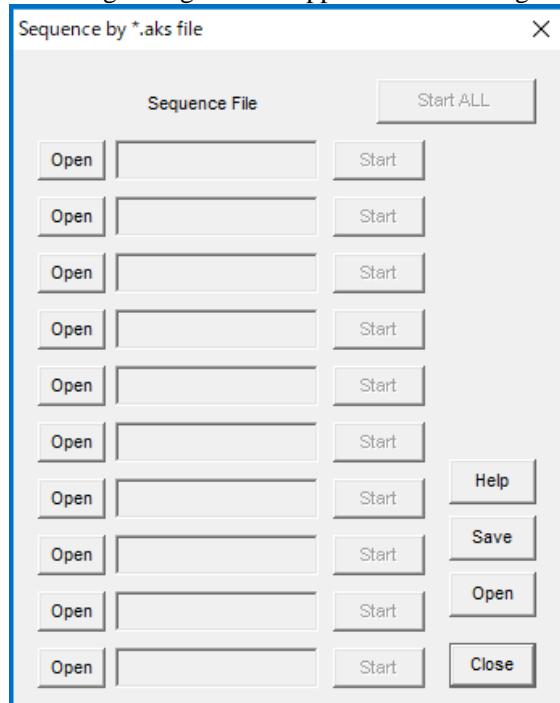


Figure 19-1. [Sequence (File)] Window

[Open (left)] button: Select a sequence setting file (*.aks)

[Start] button: Execute the sequence by the setting of selected file.

[Start All] button: Execute sequence with all selected setting files.

Selected files are executed in descending order.

[Help] button: Open help window.

[Save] button: Save register setting file assignment. File name is “*.mas”.

[Open (right)] button: Open saved sequence setting file assignment “*. mas”.

[Close] button: Close dialog box and finish process.

~ Operating Suggestions ~

1. Files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
2. When “Stop” command is selected in the sequence, the process is paused at this step and a message shown below pops up. The sequence is resumed by clicking “OK” button.

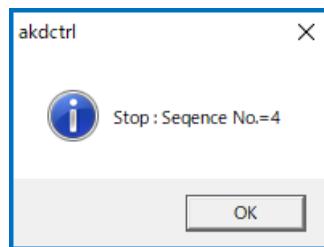


Figure 19-2. Sequence Pause Window

5. Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision APX555 audio analyzer (APX555)
- MCLK : 256fs (44.1 kHz), 256fs (96 kHz), 128fs (192 kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : AVDD=5V, TVDD=3.3V, DVDD=LDO,
VDDL1/R1/L2/R2=5V, VREFHL1/R1/L2/R1=5V
- Pass : DIR → AK4499 → Cannon Connector
- Interface : Internal DIR (44.1 kHz, 96 kHz, 192 kHz)
- Temperature : Room Temperature
- Operational Amplifiers : OPA1612

fs=44.1kHz

Parameter	Input signal	Measurement filter	Results					
			L1ch	/	R1ch	L2ch	/	R2ch
THD	1kHz, 0dB	20kHz LPF	125.2 dB	/	123.7 dB	126.7 dB	/	123.3 dB
DR	1kHz, -60dB		129.4 dB	/	129.4 dB	129.2 dB	/	129.1 dB
S/N	“0” data	A-weighted	131.6 dB	/	131.6 dB	131.8 dB	/	131.4 dB
		20kHz LPF	131.8 dB	/	131.1 dB	130.9 dB	/	131.2 dB
		A-weighted						

fs=96kHz

Parameter	Input signal	Measurement filter	Results					
			L1ch	/	R1ch	L2ch	/	R2ch
THD	1kHz, 0dB	40kHz LPF	124.9 dB	/	123.2 dB	129.9 dB	/	122.2 dB
DR	1kHz, -60dB		123.7 dB	/	123.5 dB	123.8 dB	/	123.8 dB
S/N	“0” data	A-weighted	128.5 dB	/	128.6 dB	128.6 dB	/	128.6 dB
		40kHz LPF	130.5 dB	/	130.7 dB	130.6 dB	/	131.0 dB
		A-weighted						

fs=192kHz

Parameter	Input signal	Measurement filter	Results					
			L1ch	/	R1ch	L2ch	/	R2ch
THD	1kHz, 0dB	80kHz LPF	124.2 dB	/	123.1 dB	126.9 dB	/	123.0 dB
DR	1kHz, -60dB		123.5 dB	/	122.9 dB	123.7 dB	/	123.5 dB
S/N	“0” data	A-weighted	131.6 dB	/	131.4 dB	131.6 dB	/	131.5 dB
		80kHz LPF	131.4 dB	/	131.5 dB	131.4 dB	/	131.9 dB
		A-weighted						

■ Capacitance between the VREFH pin and the VREFL pin

Distortion at lower frequency can be improved by increasing the capacitance of a capacitor between the VREFH pin and the VREFL pin. Applicable capacitors are C90, C6, C35 and C14 in the circuit schematic.
 (R64, R14_4, R18, R14_2, R60, R14_3, R14, R14_1 = 10ohm (The series resistances for the VREFH/L pin.))

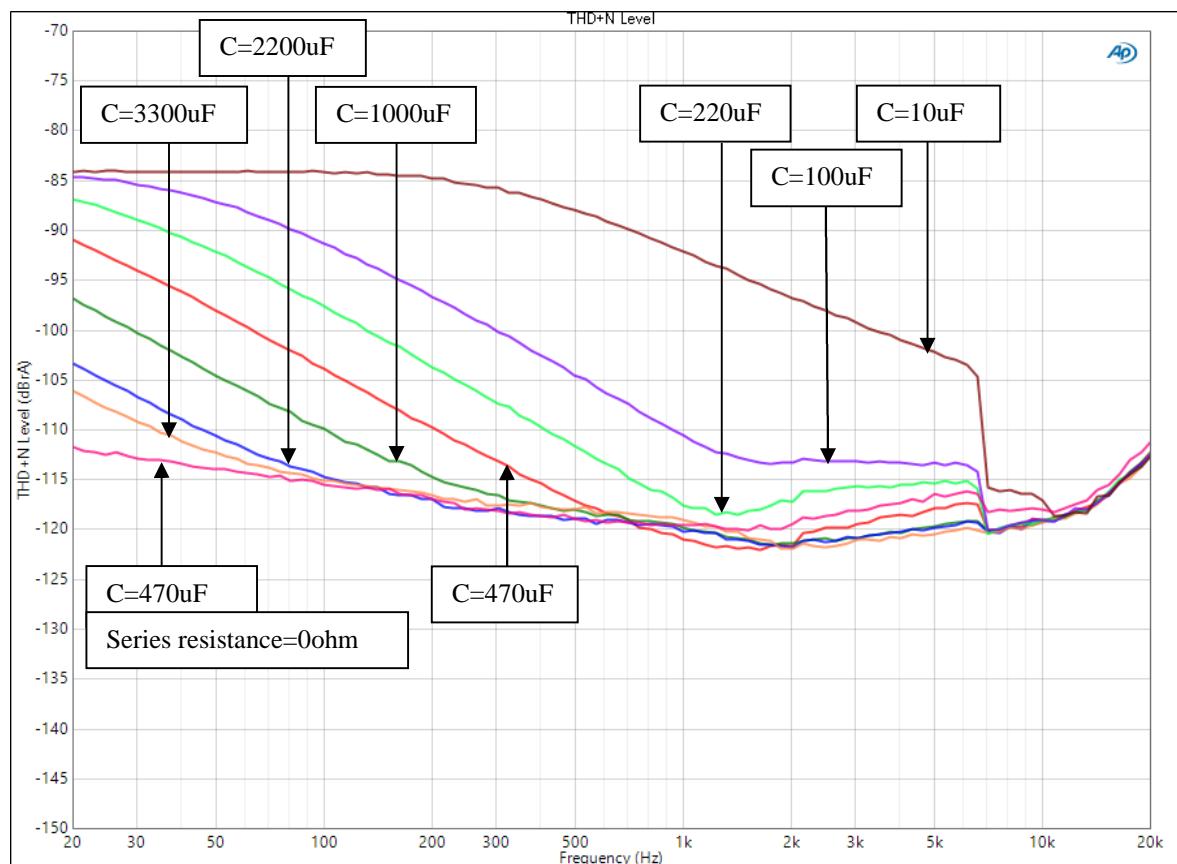


Figure. THD+N vs. Input Frequency Comparison by Capacitance

[Plots]

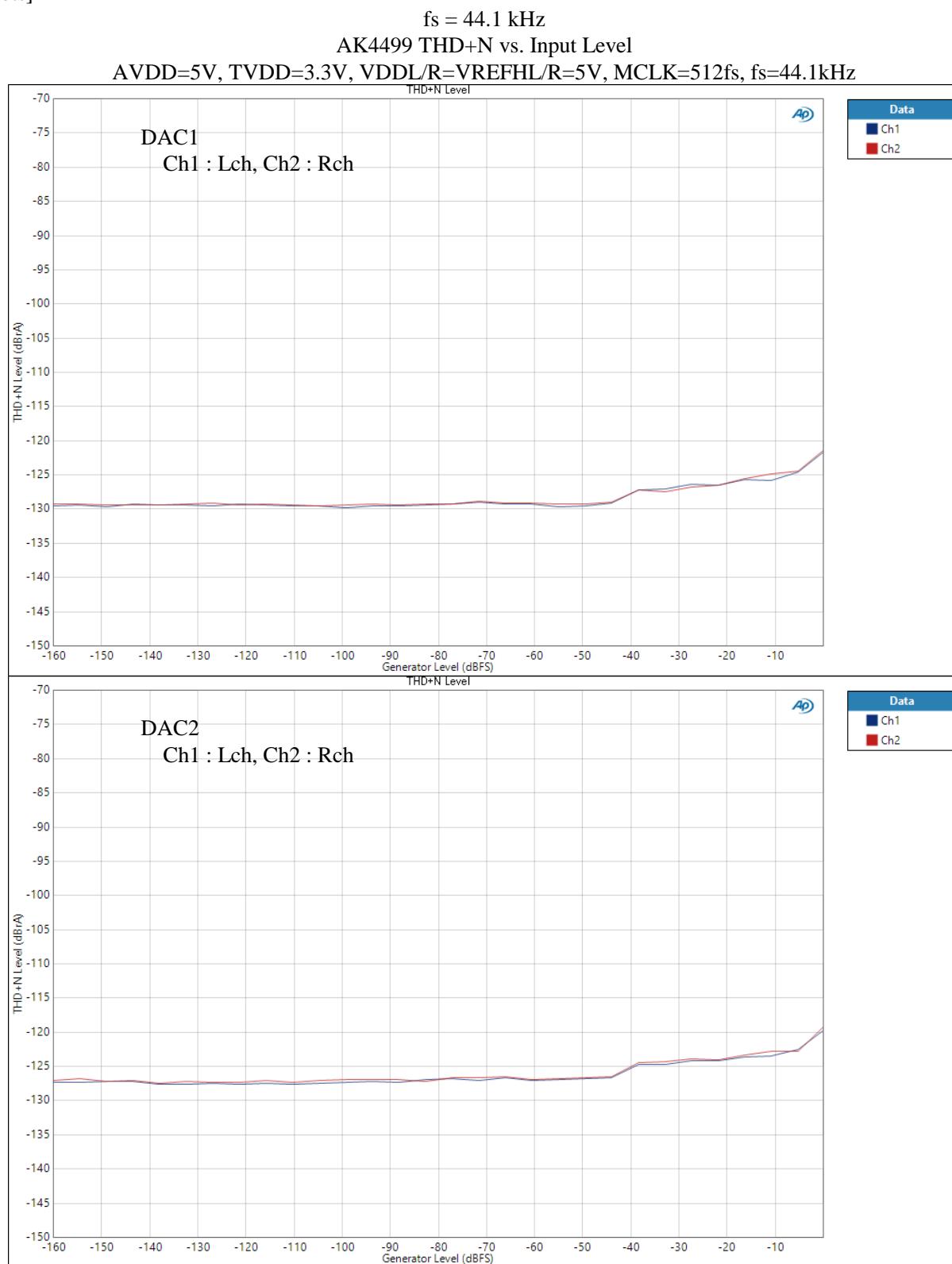


Figure 20. THD+N vs. Input Level

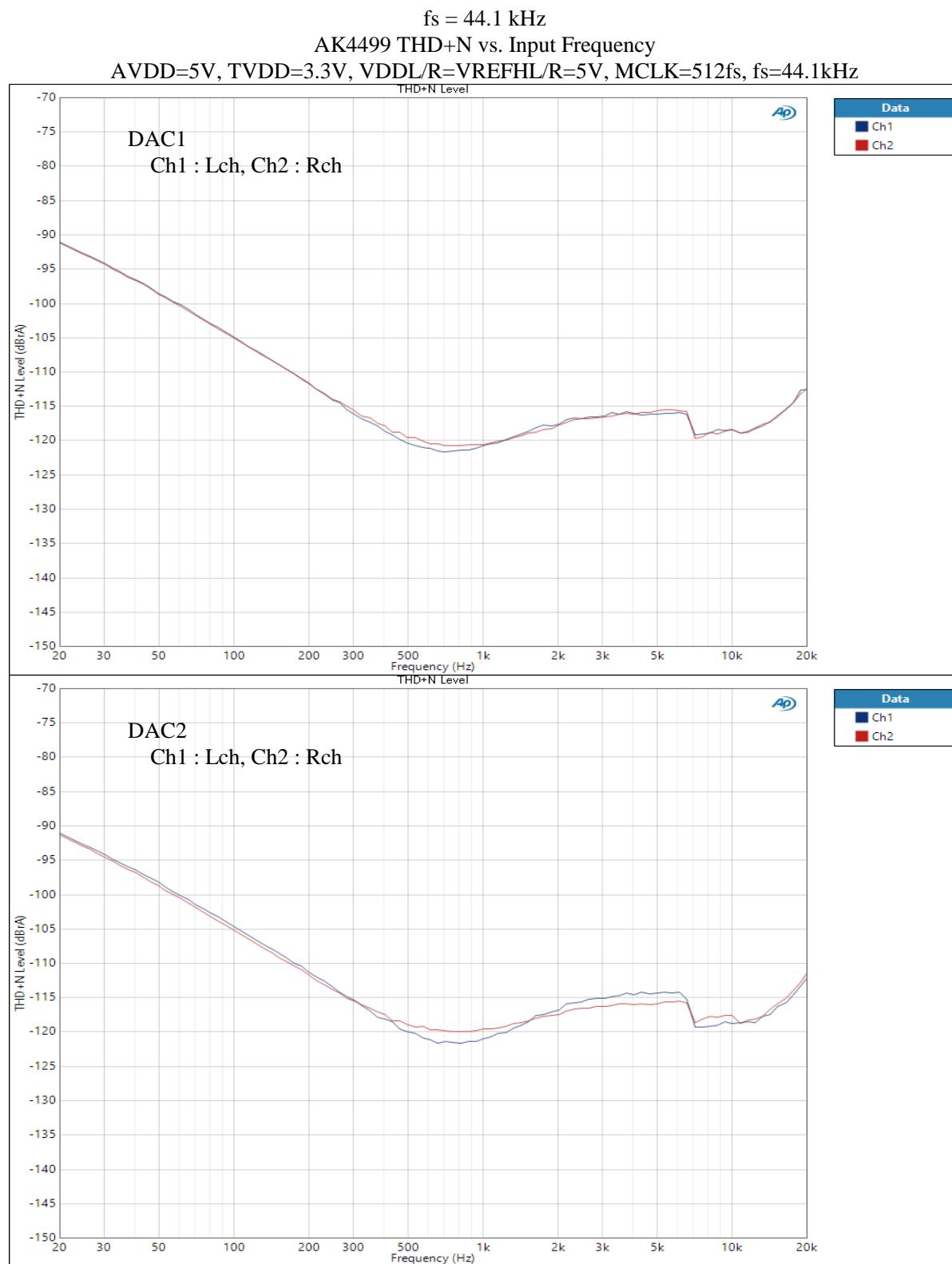


Figure 21. THD+N vs. Input Frequency

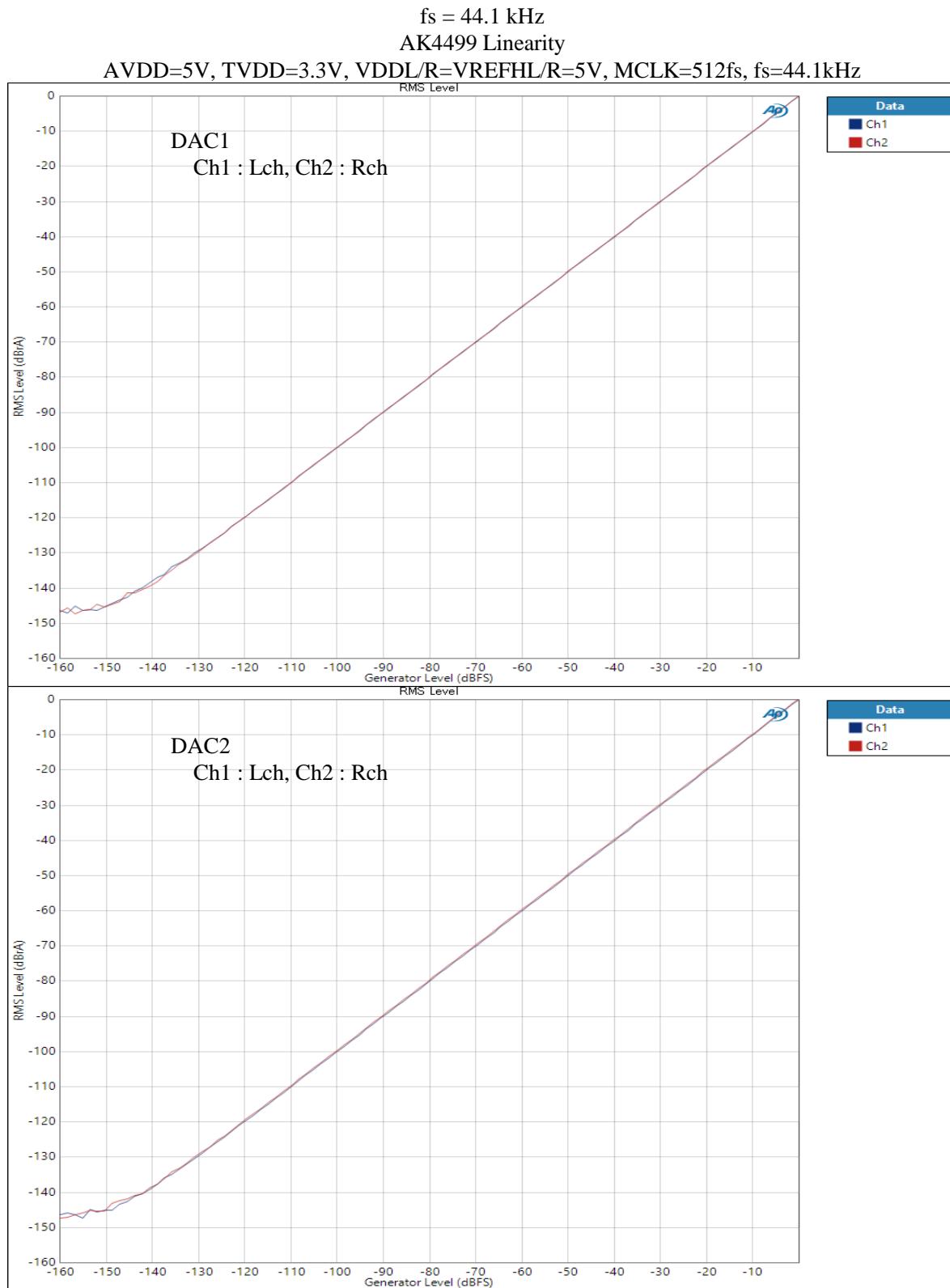


Figure 22. Linearity

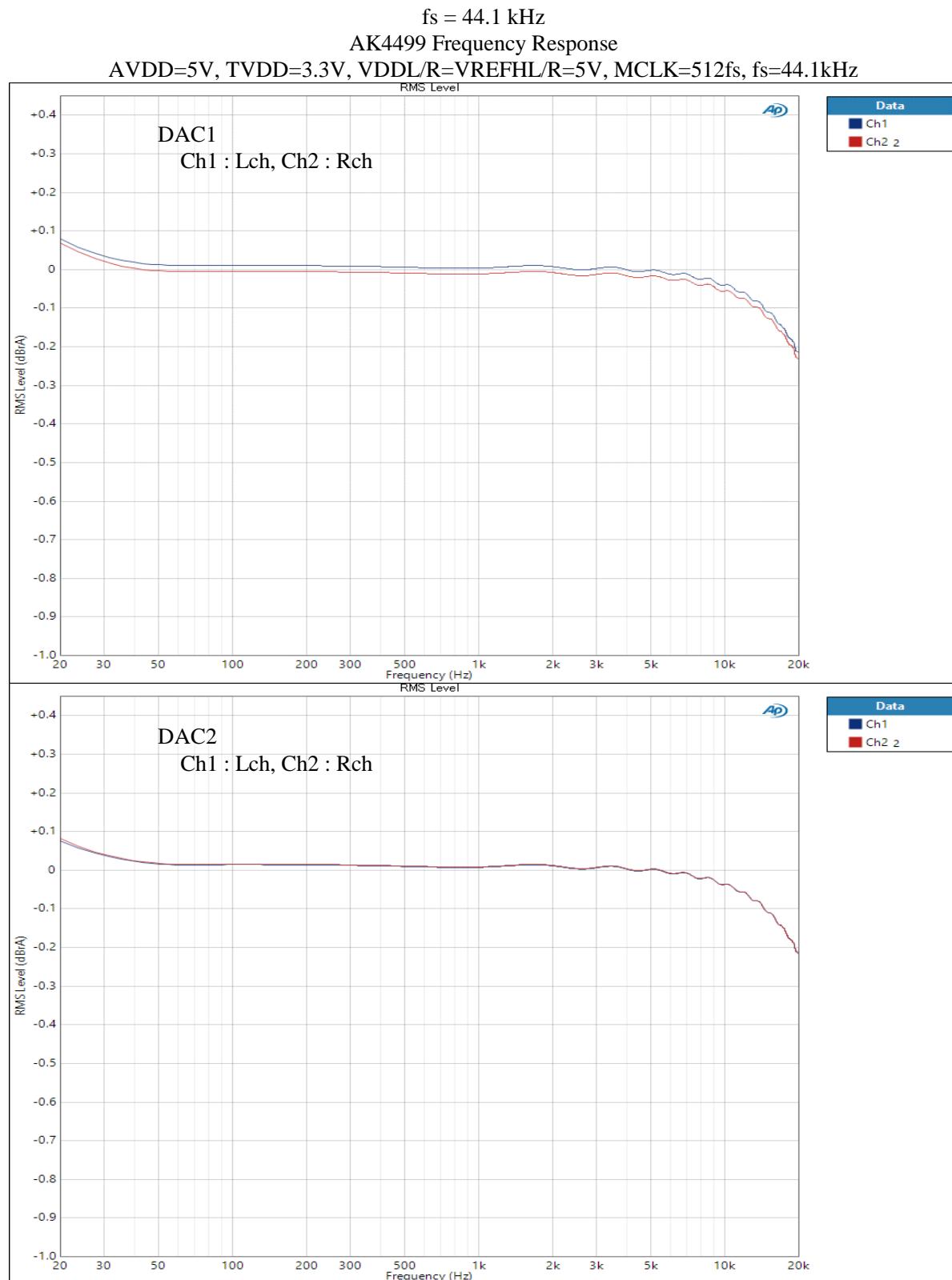


Figure 23. Frequency Response

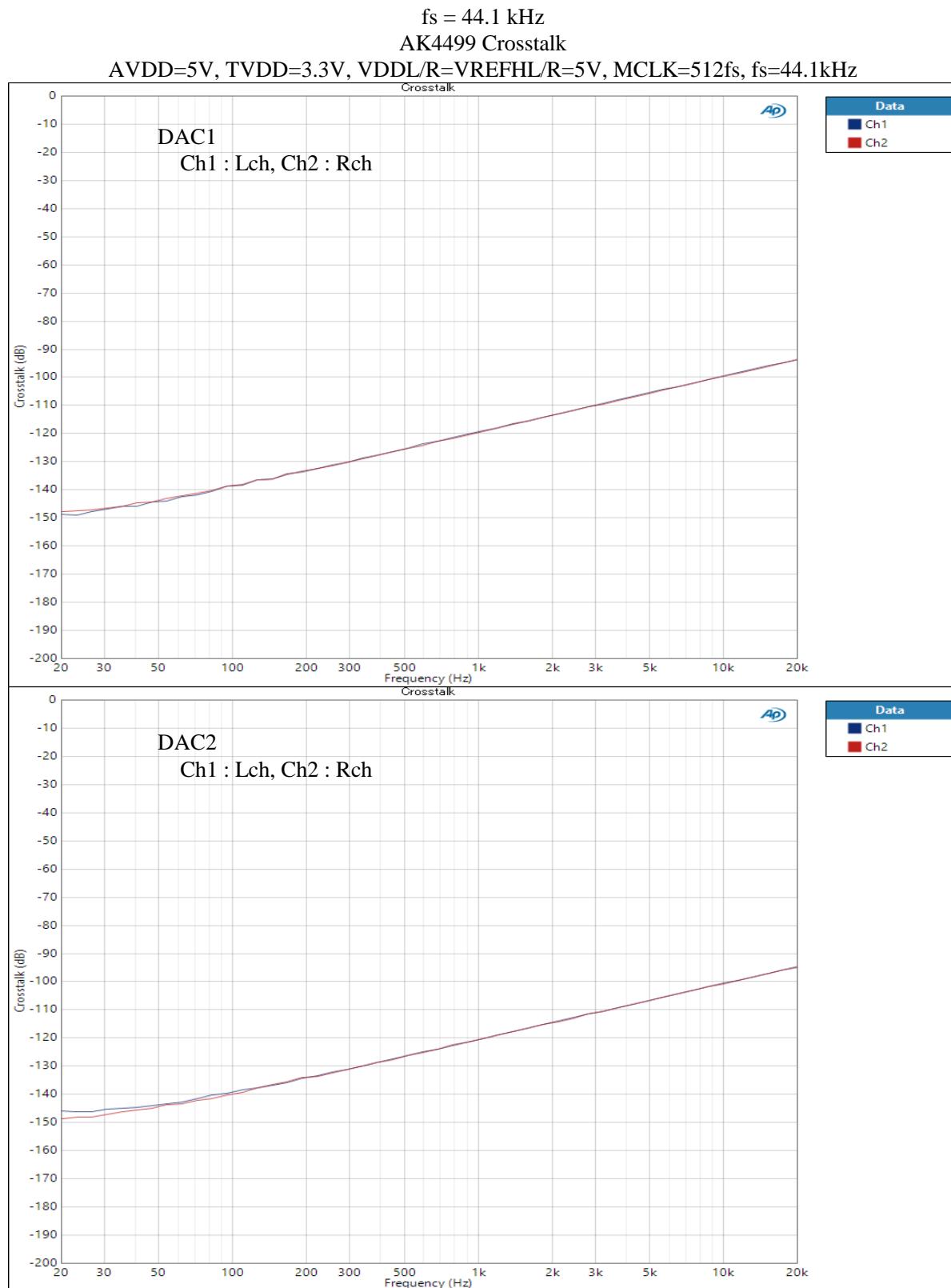


Figure 24. Crosstalk

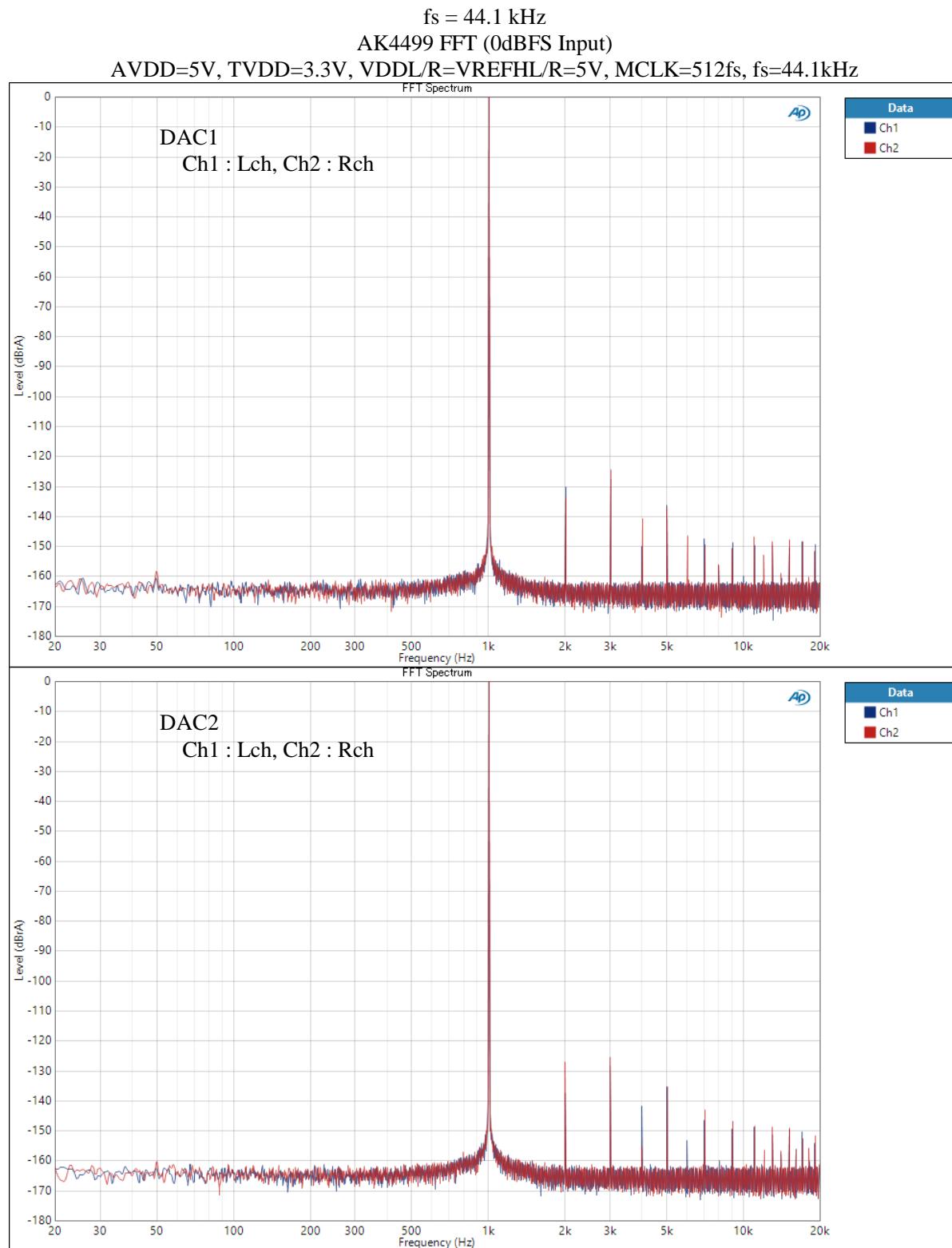


Figure 25. FFT (0dBFS Input)

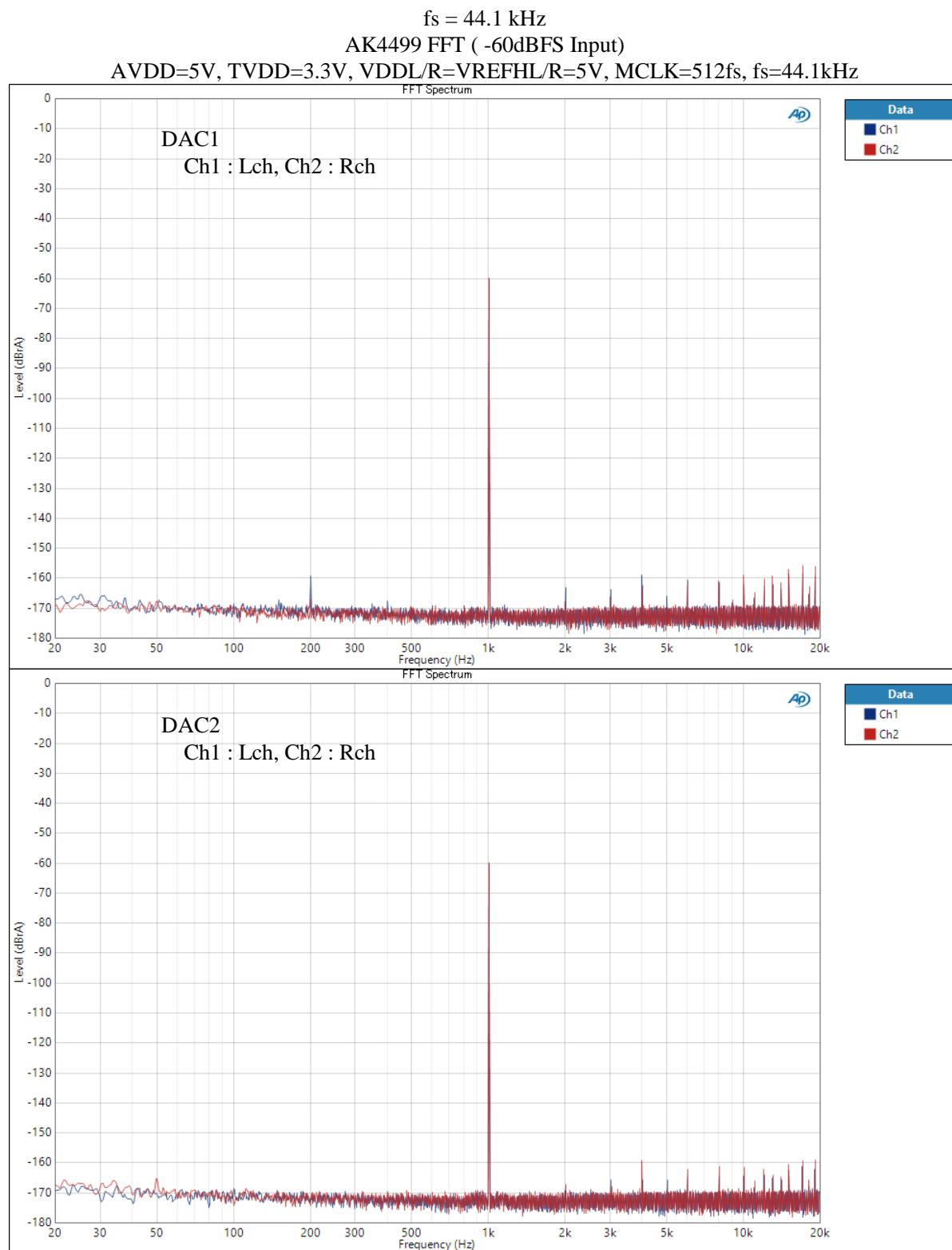


Figure 26. FFT (-60dBFS Input)

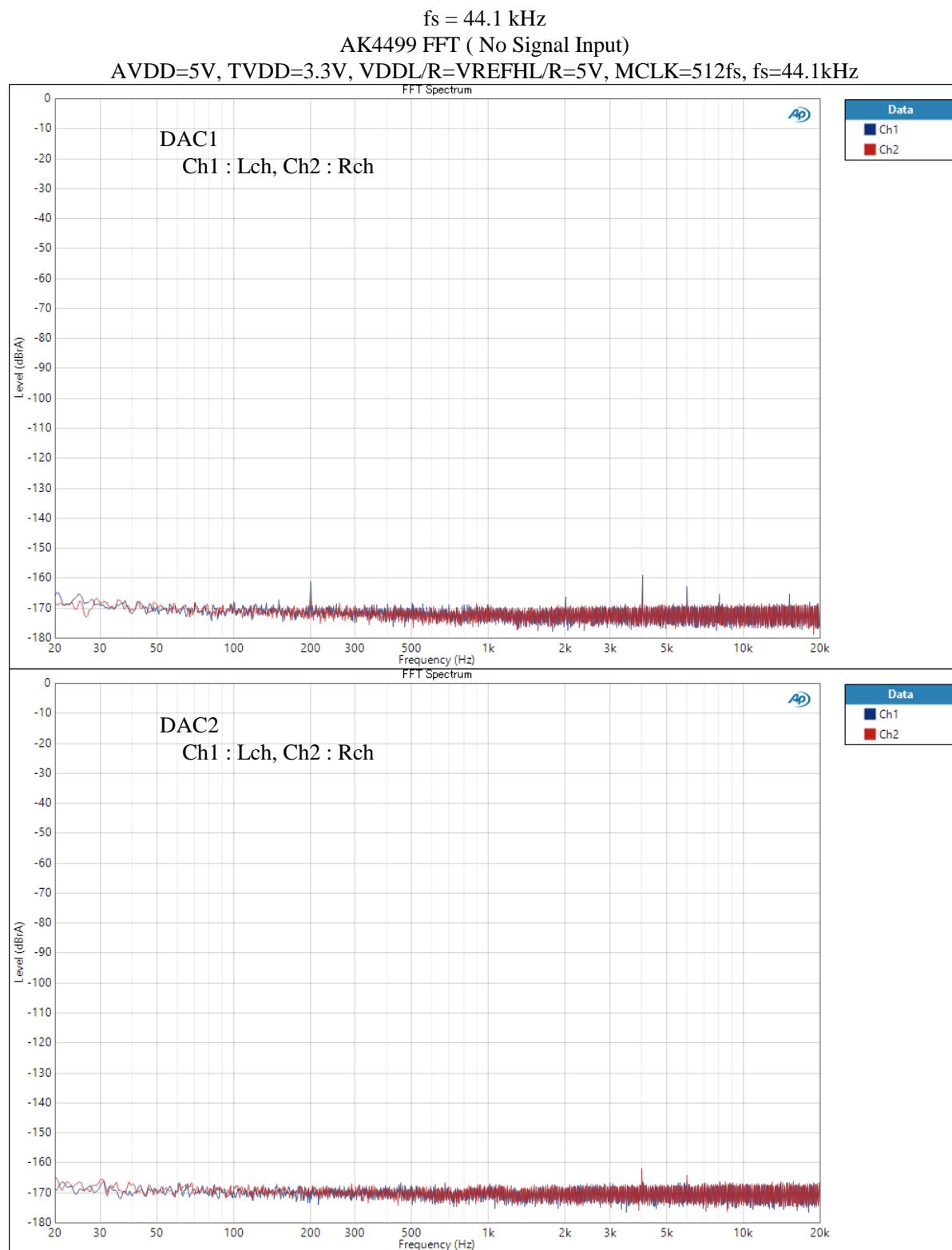


Figure 27. FFT (No Signal Input)

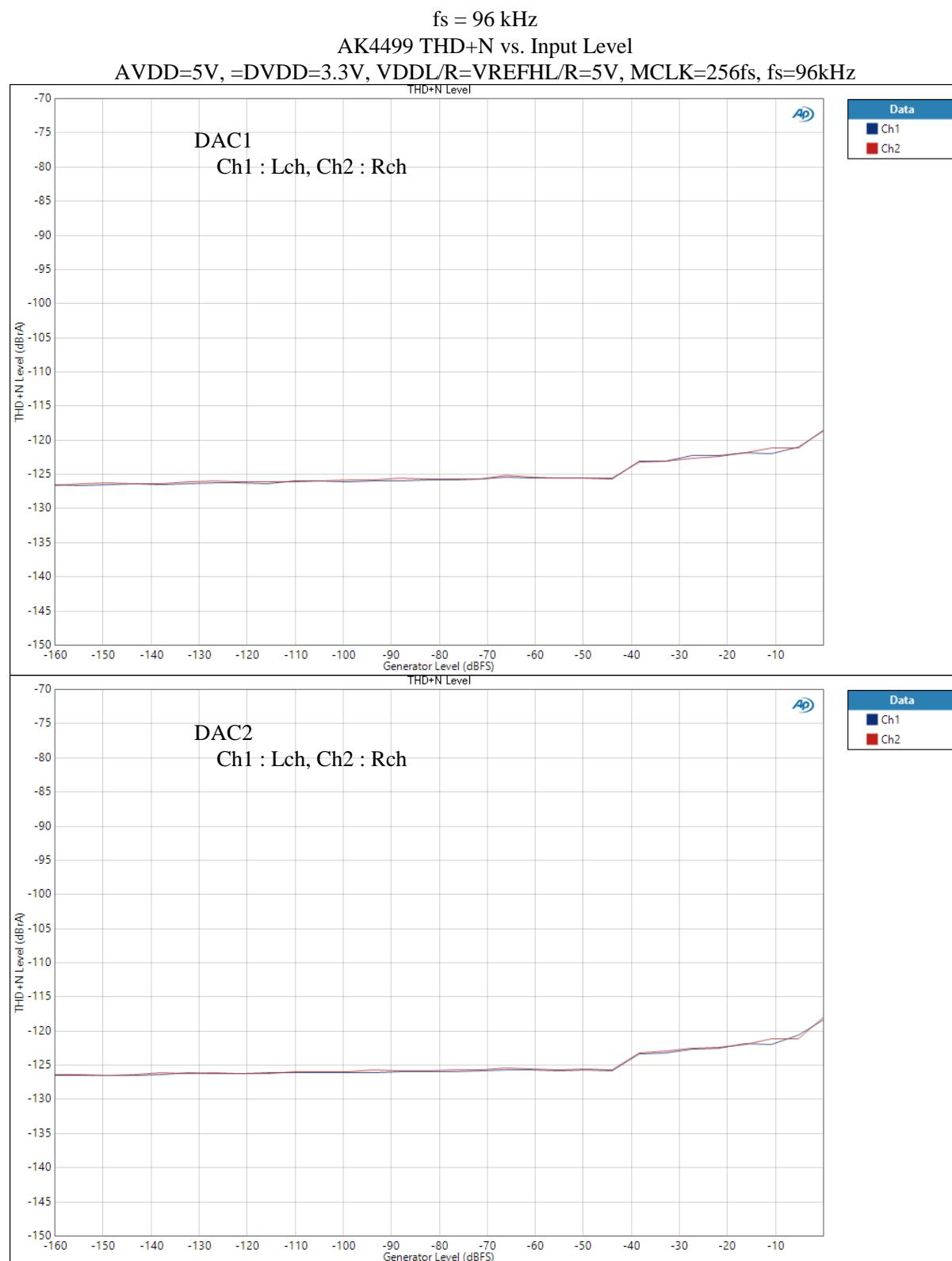


Figure 28. THD+N vs. Input Level

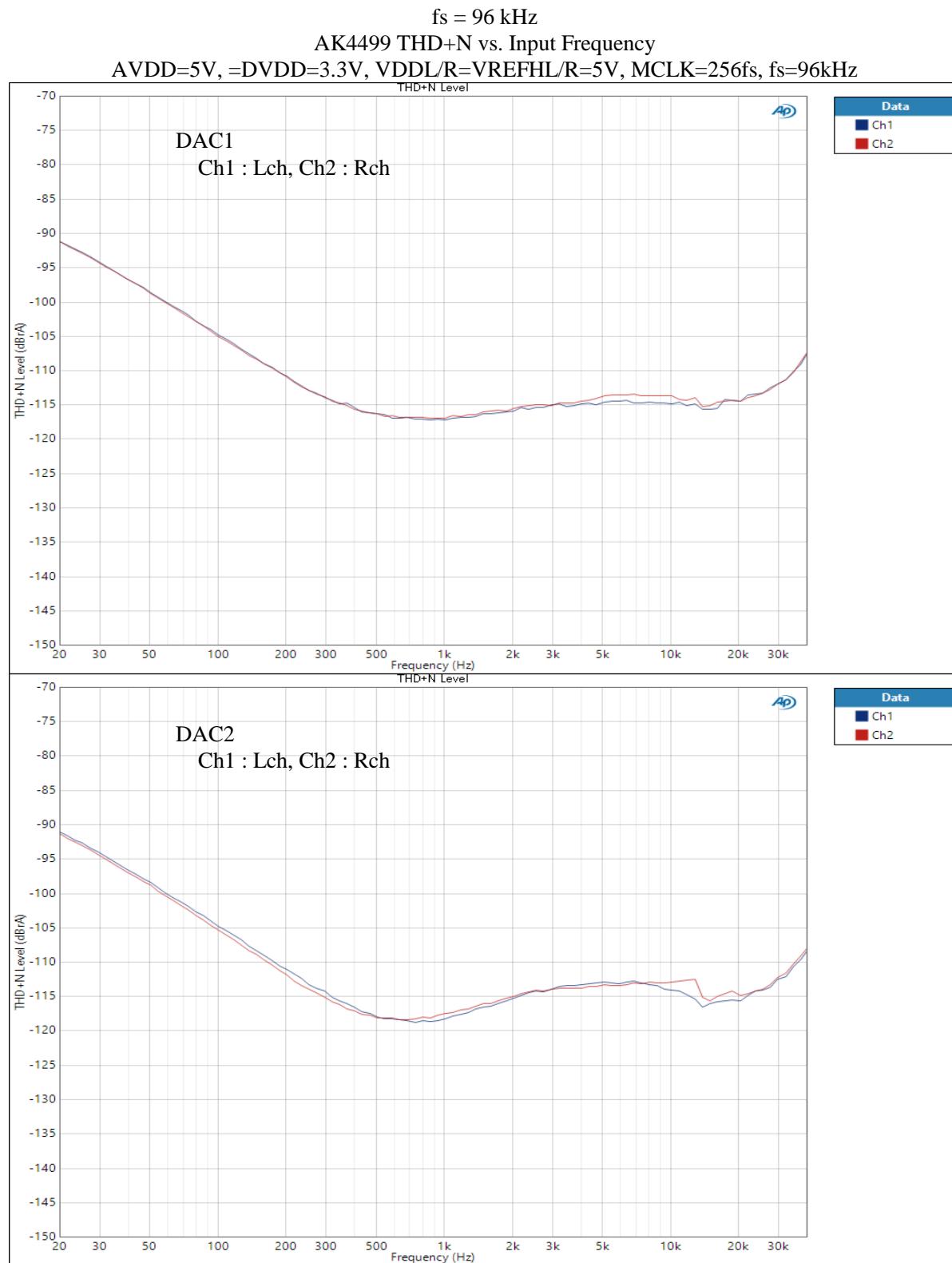


Figure 29. THD+N vs. Input Frequency

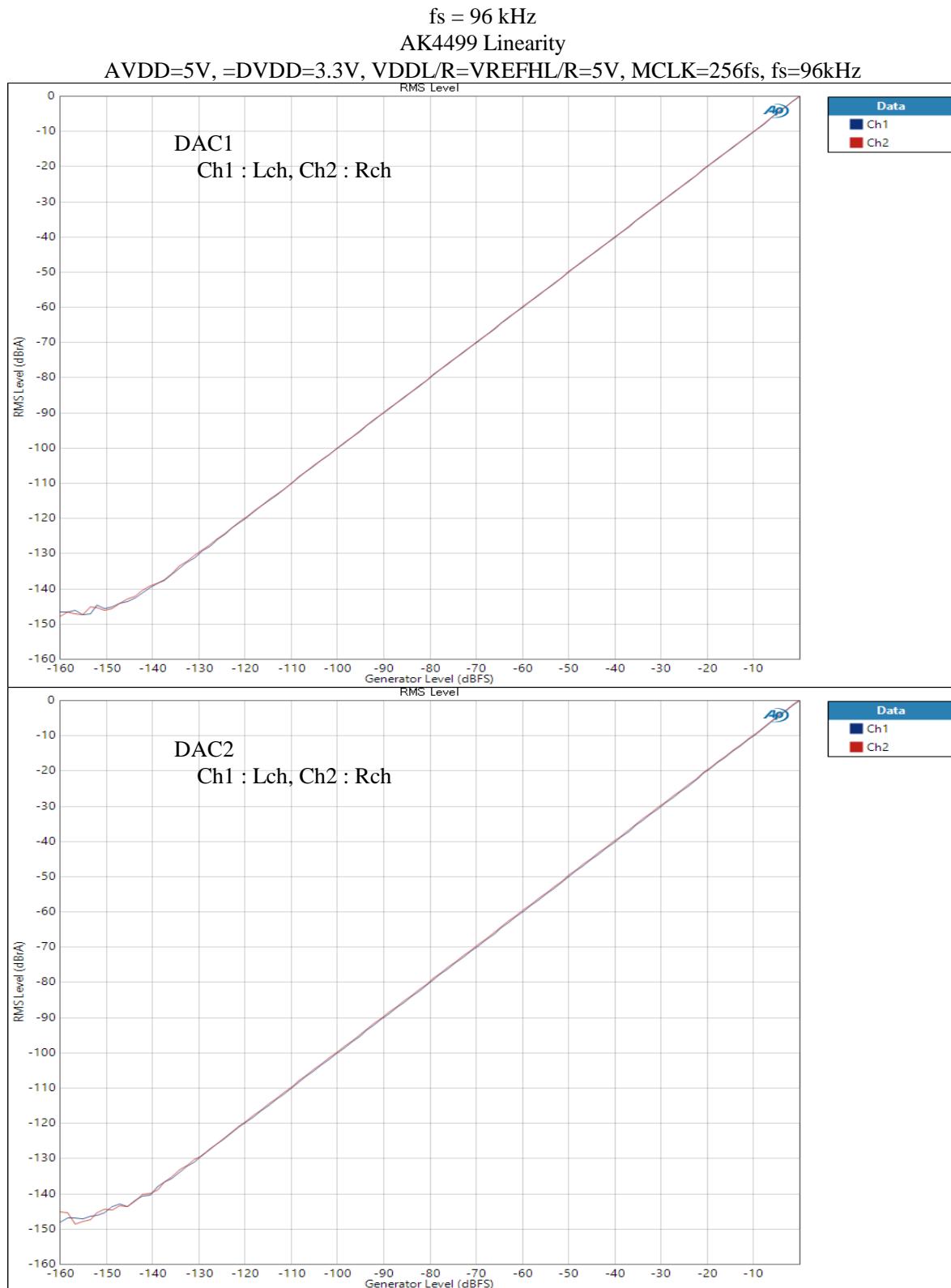


Figure 30. Linearity

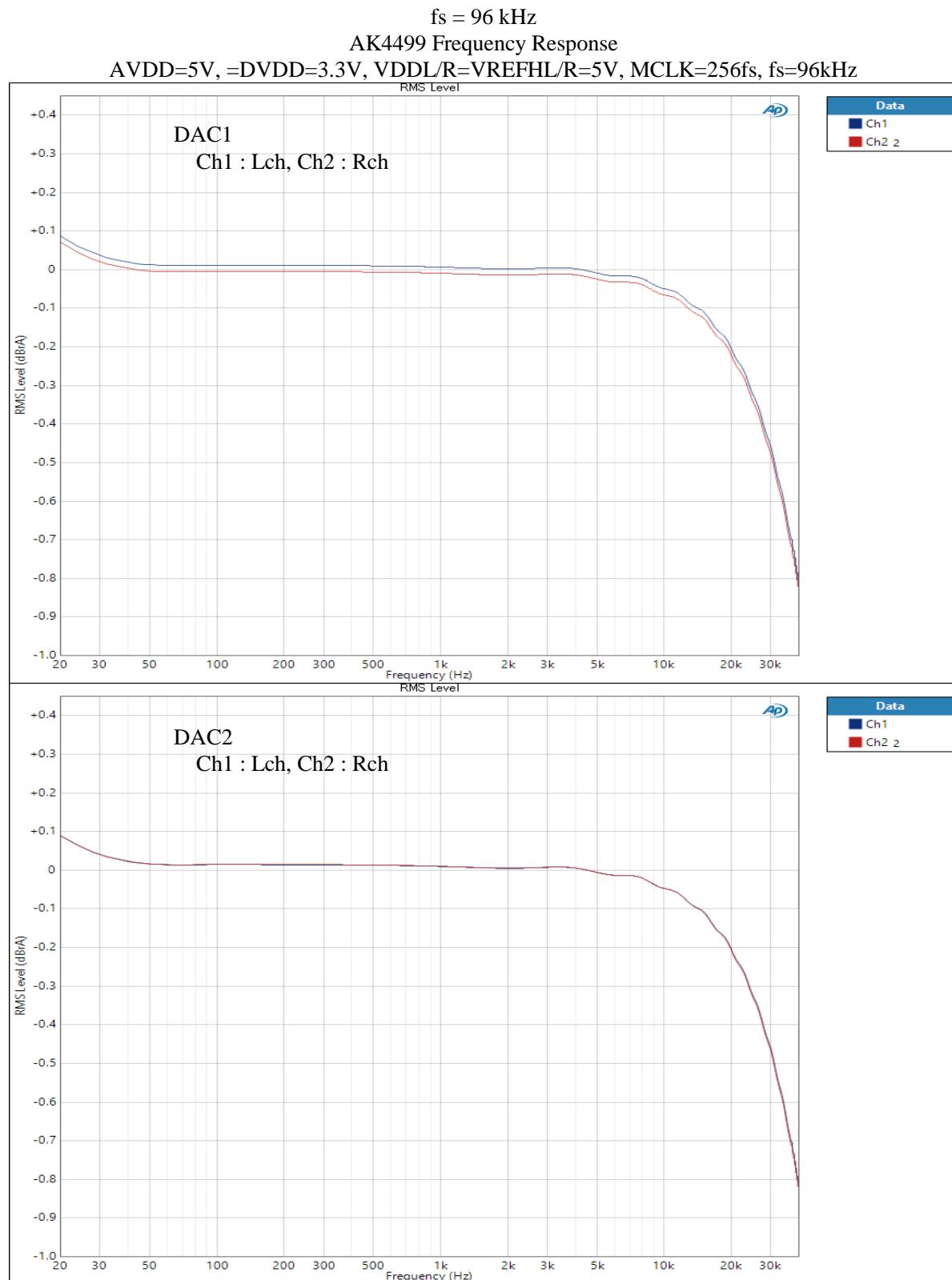


Figure 31. Frequency Response

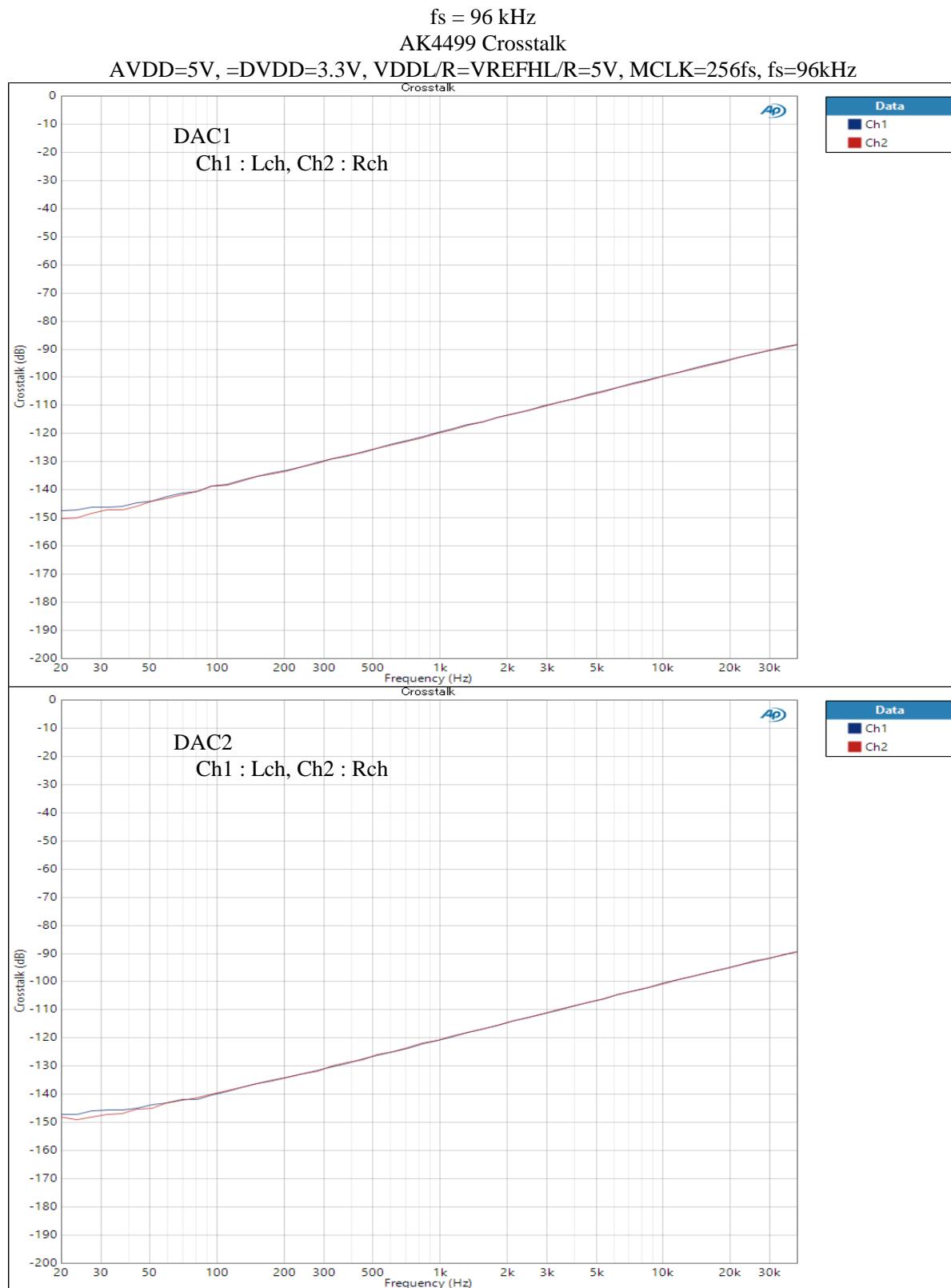


Figure 32. Crosstalk

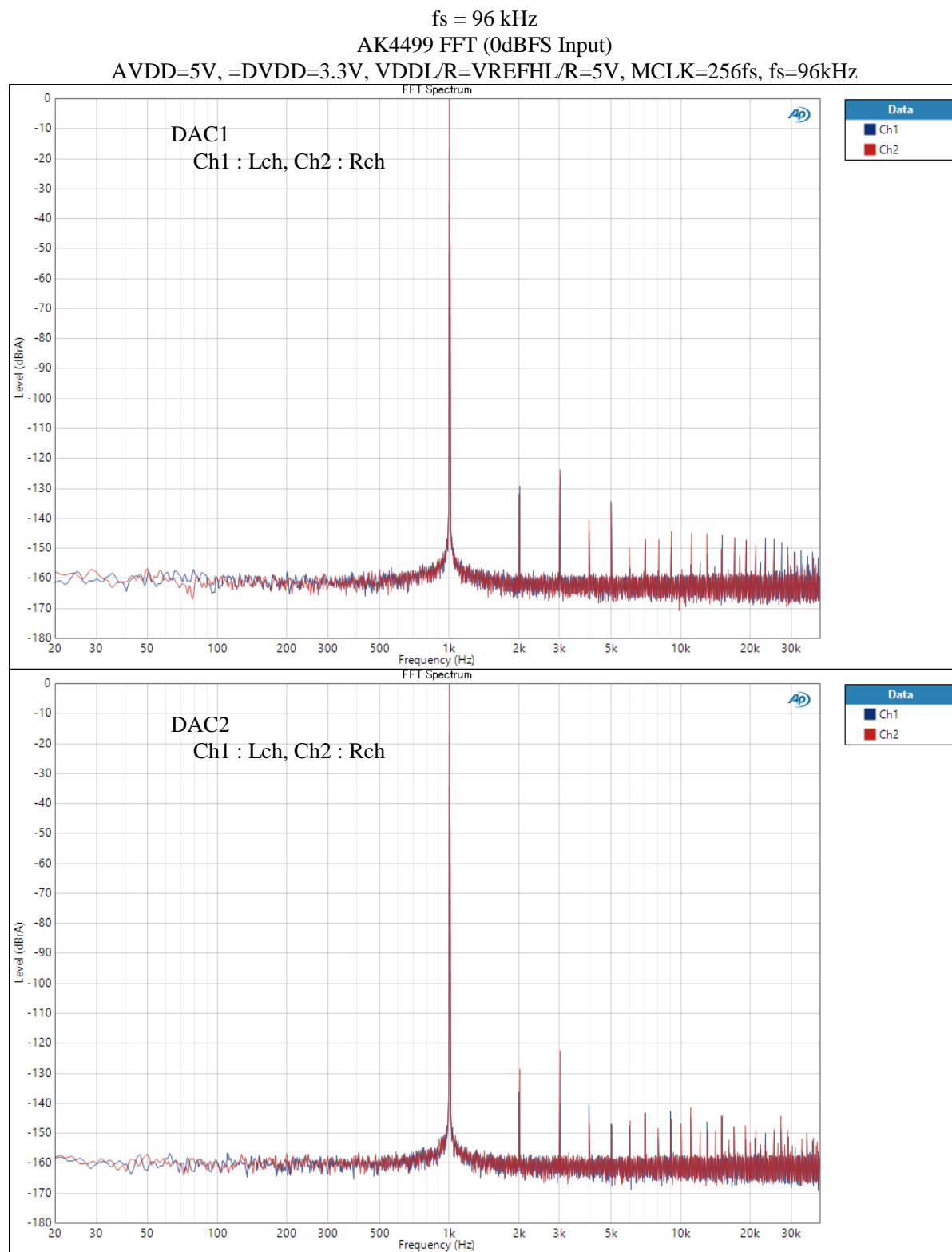


Figure 33. FFT (0dBFS Input)

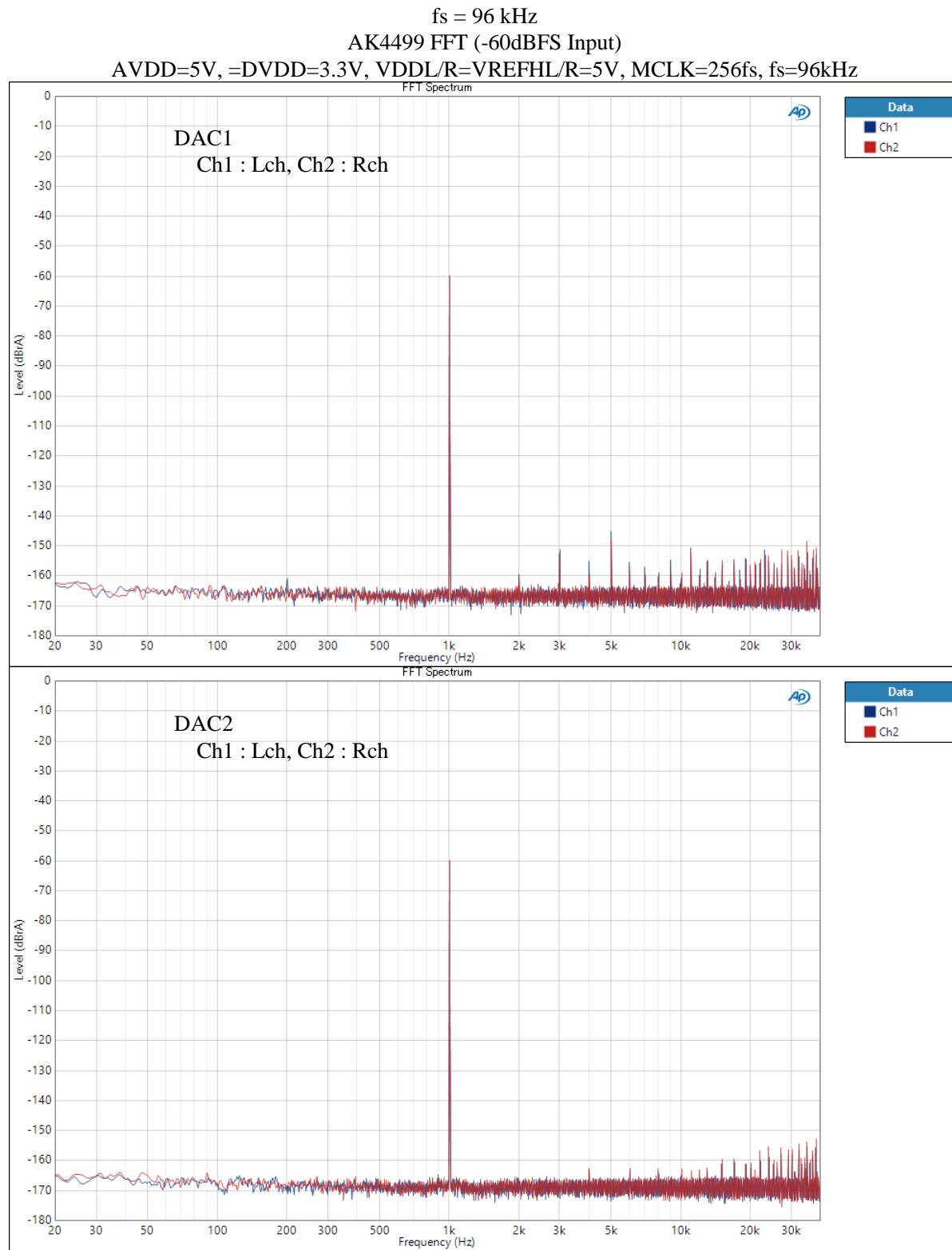


Figure 34. FFT (-60dBFS Input)

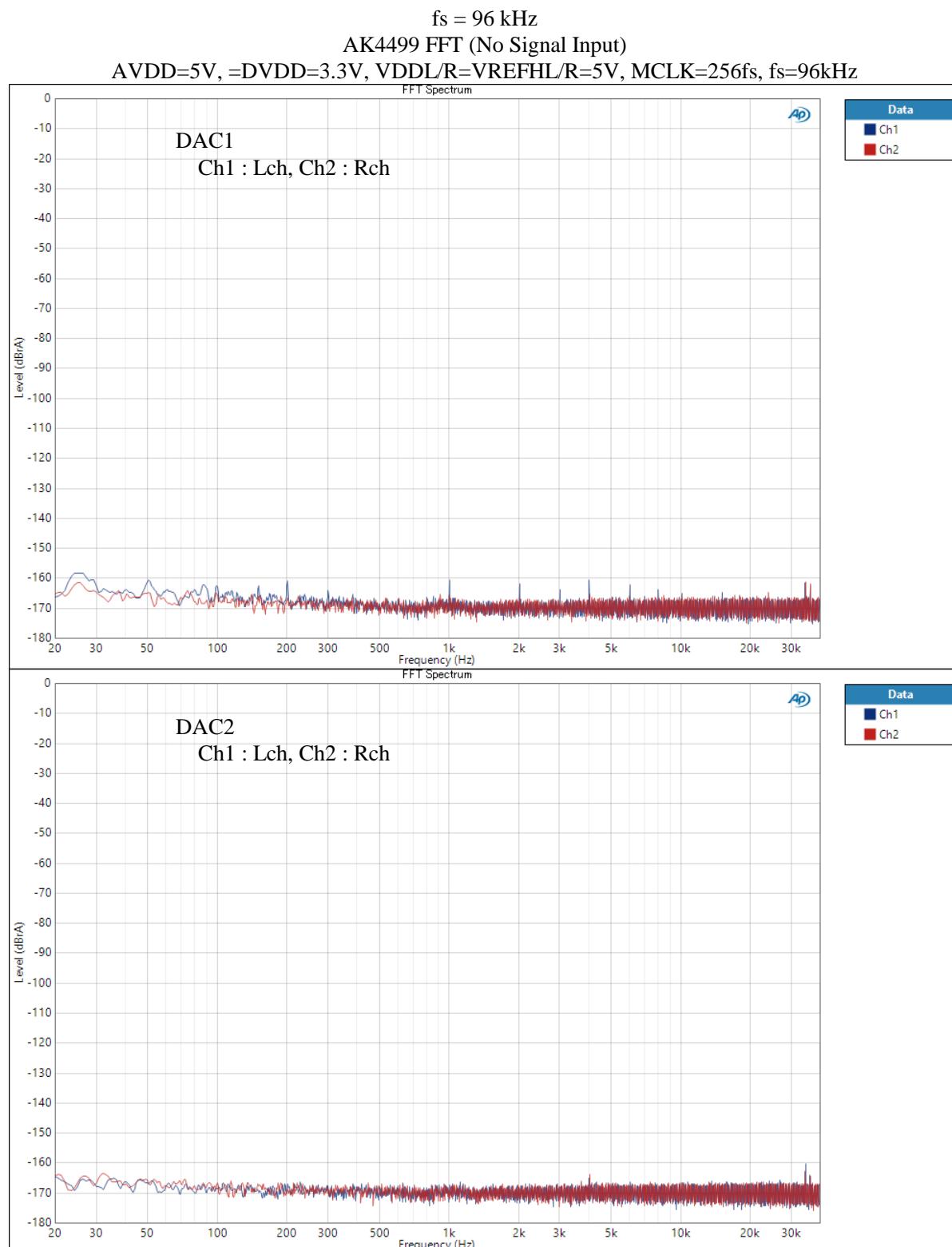


Figure 35. FFT (No Signal Input)

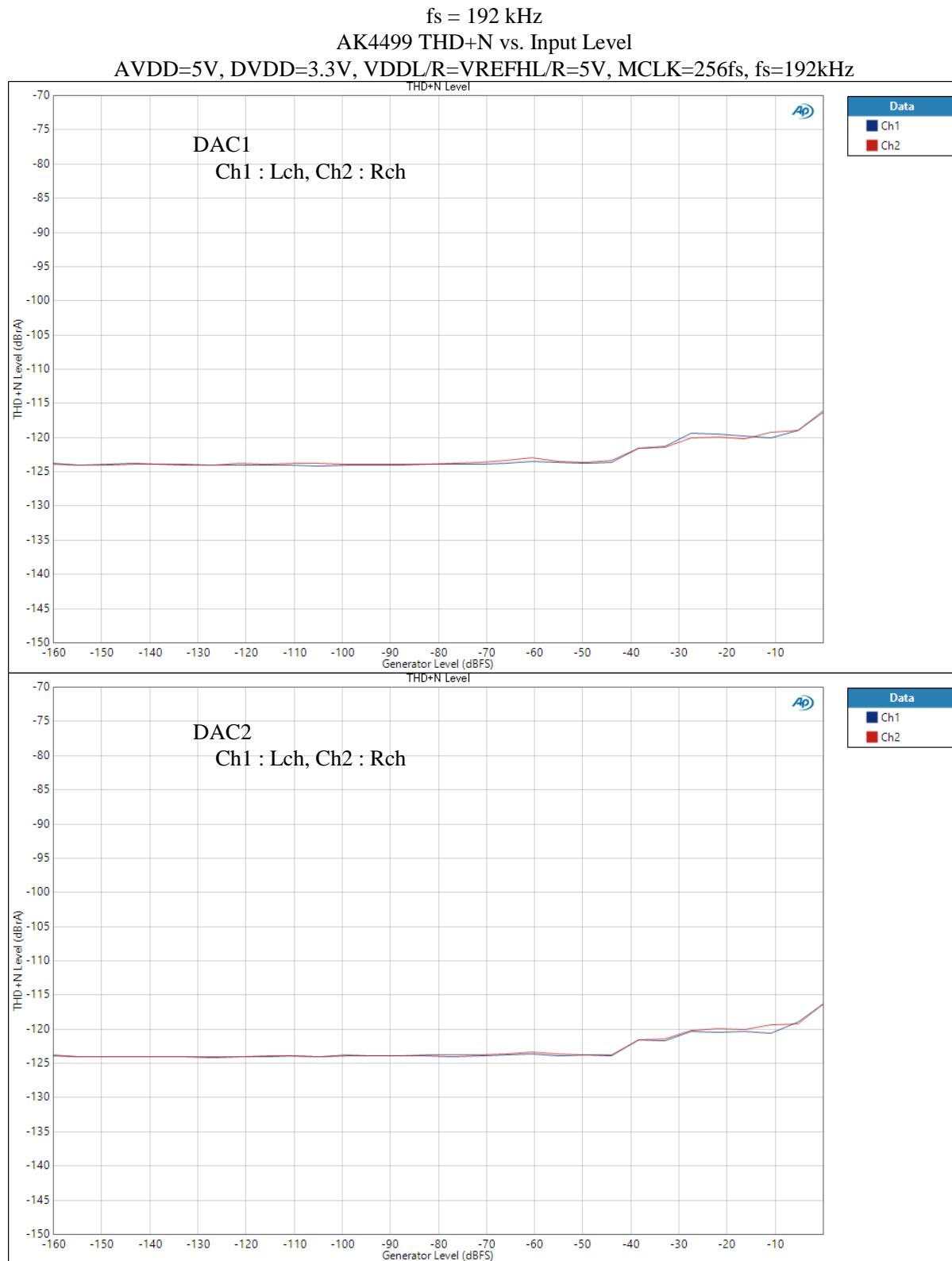


Figure 36. THD+N vs. Input Level

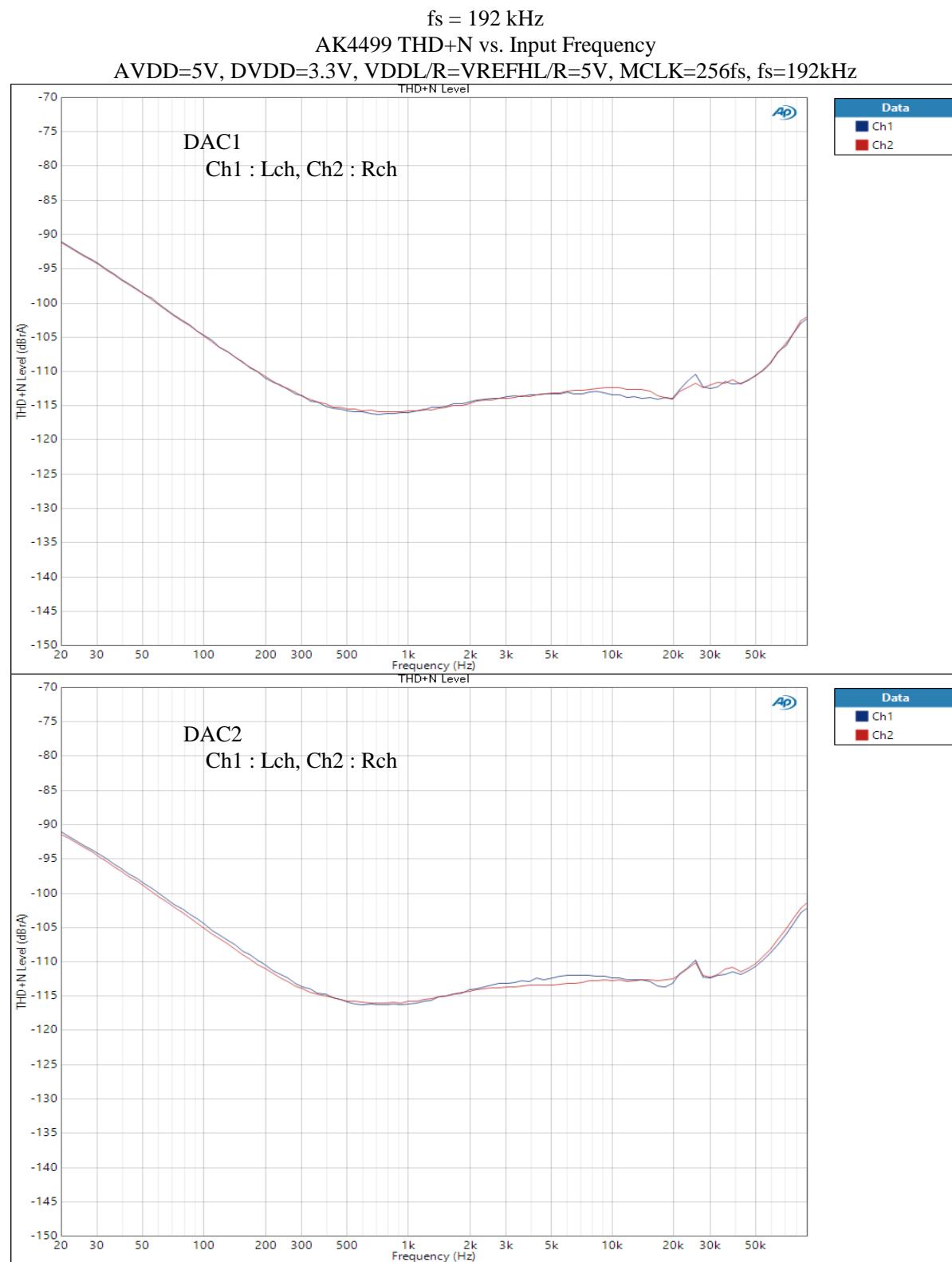


Figure 37. THD+N vs. Input Frequency

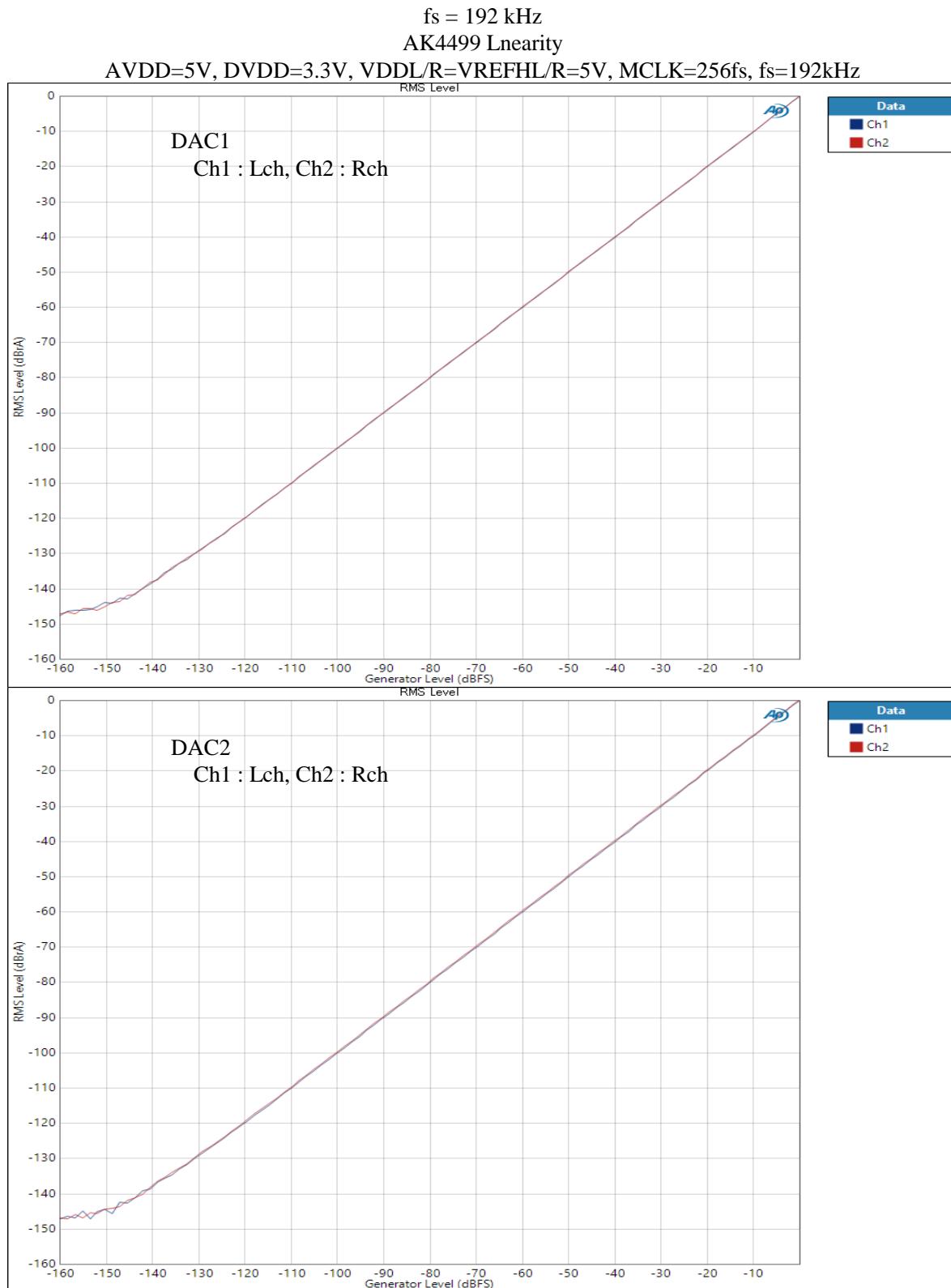


Figure 38. Linearity

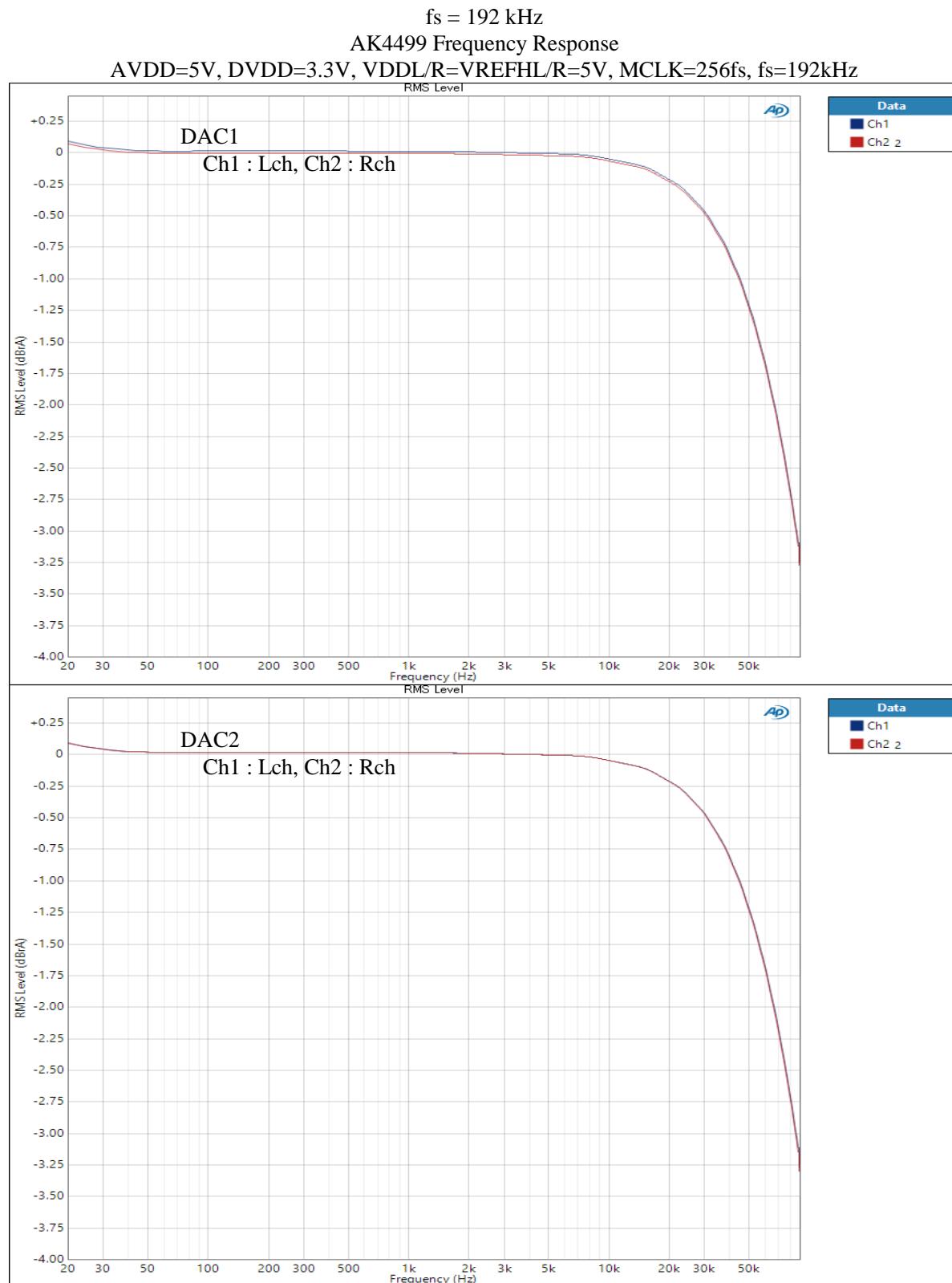


Figure 39. Frequency Response

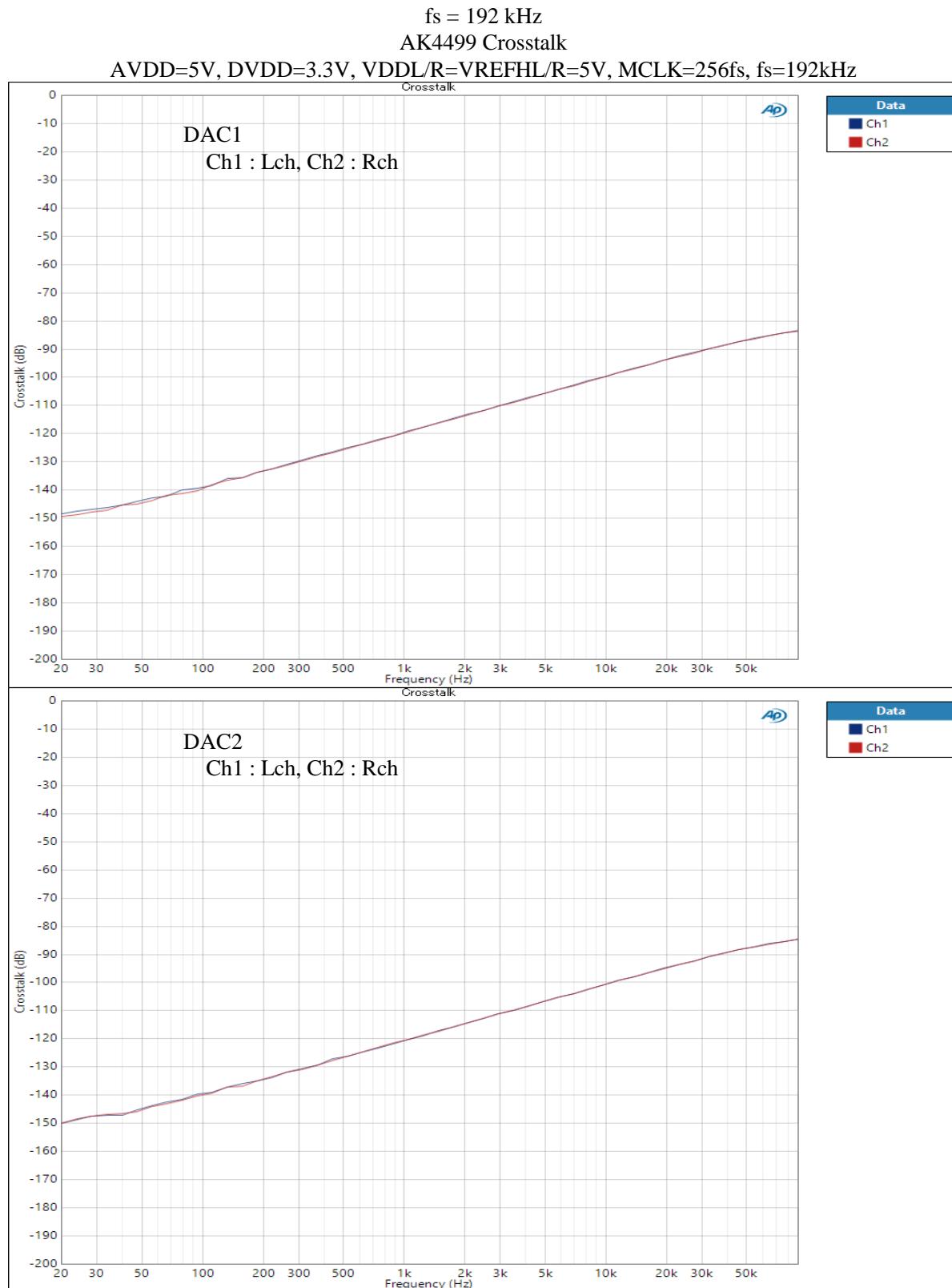


Figure 40. Crosstalk

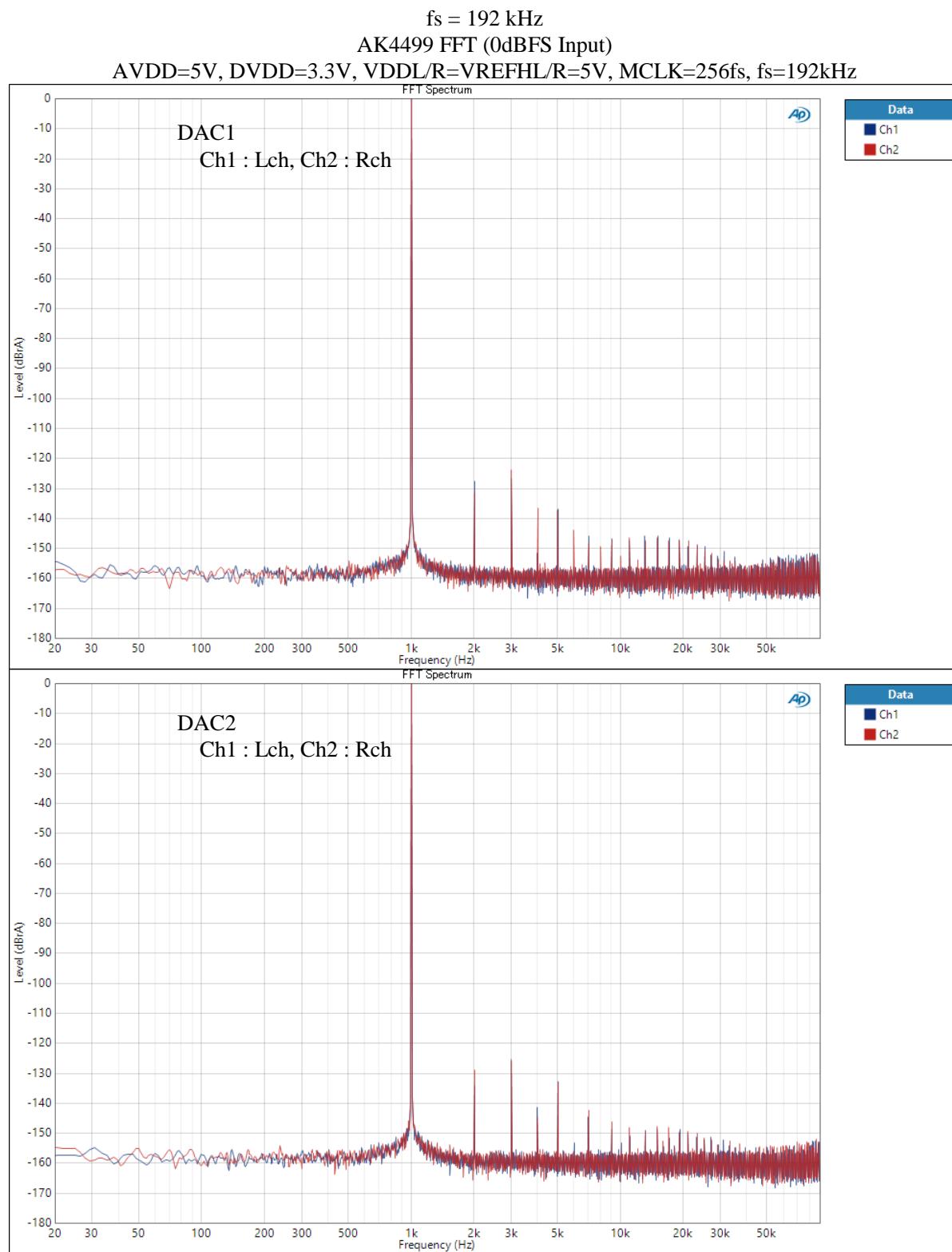


Figure 41. FFT (0dBFS Input)

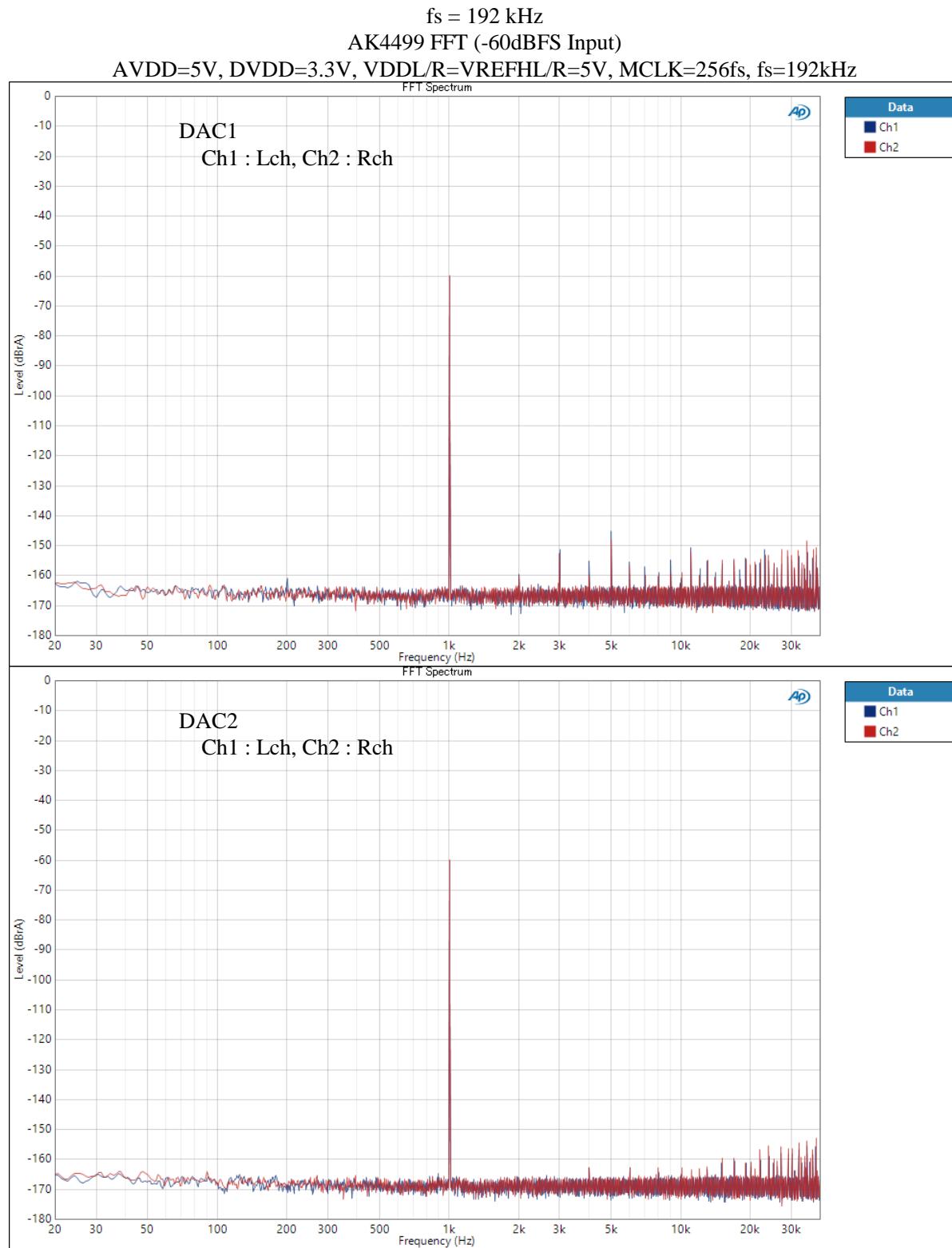


Figure 42. FFT (-60dBFS Input)

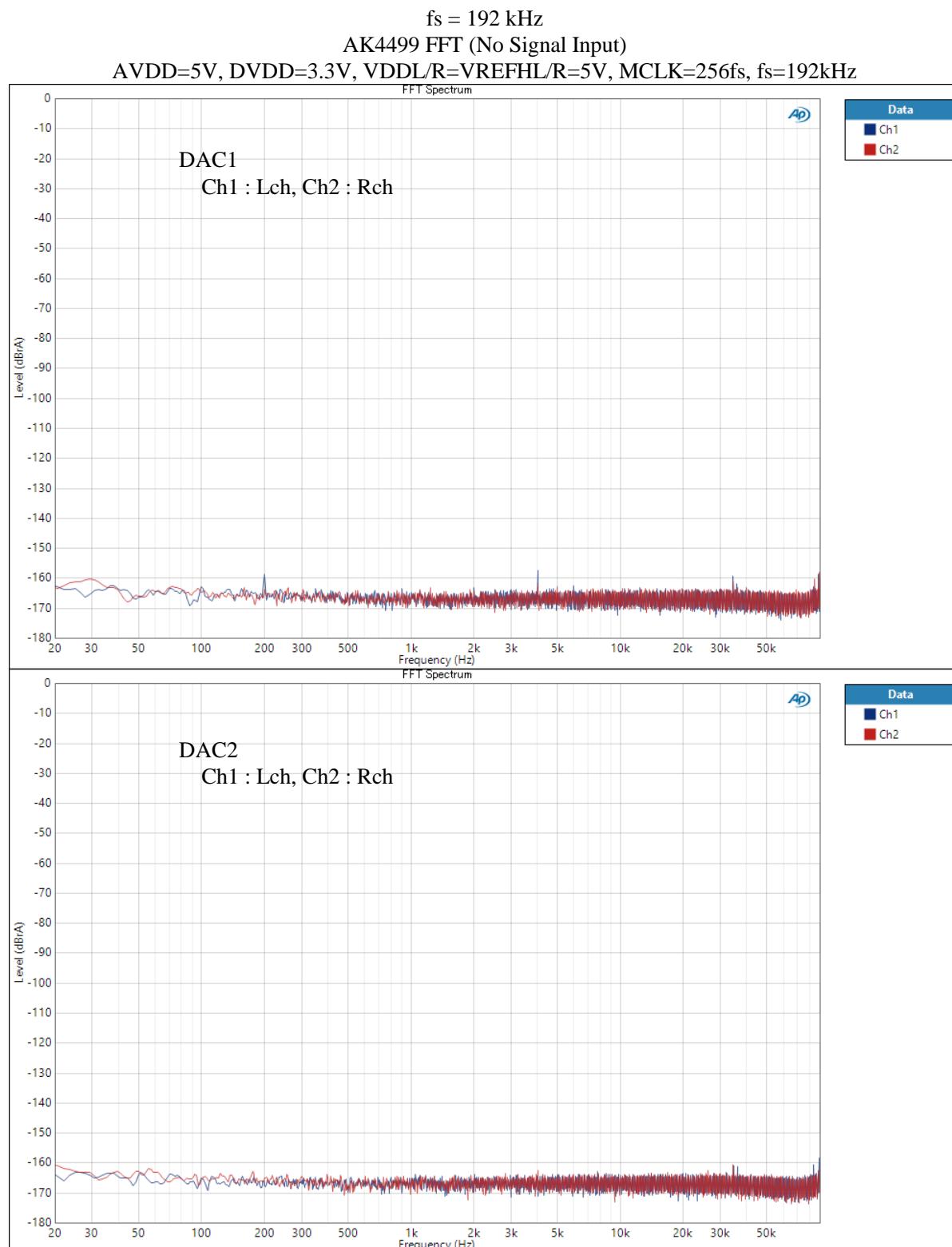


Figure 43. FFT (No Signal Input)

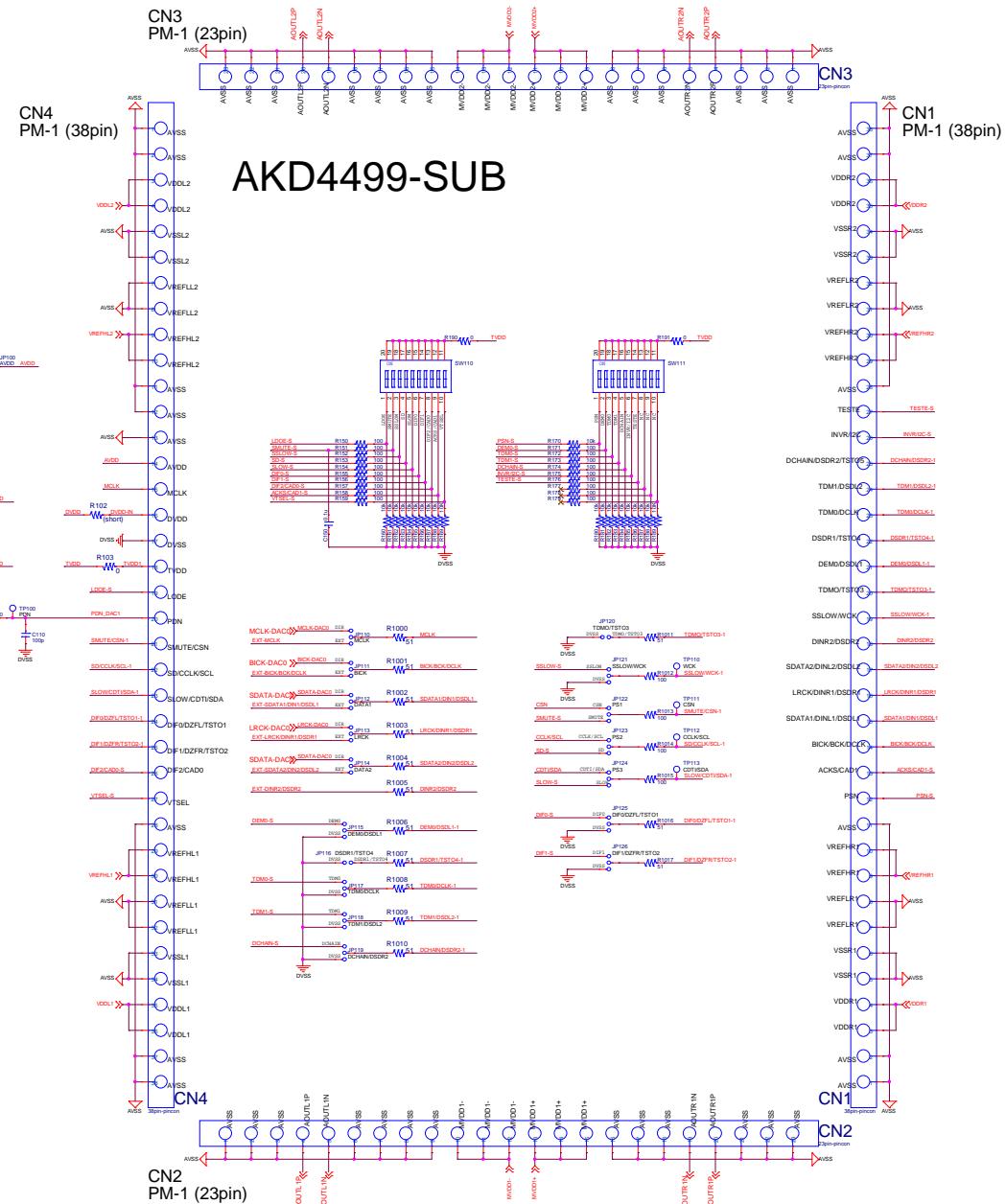
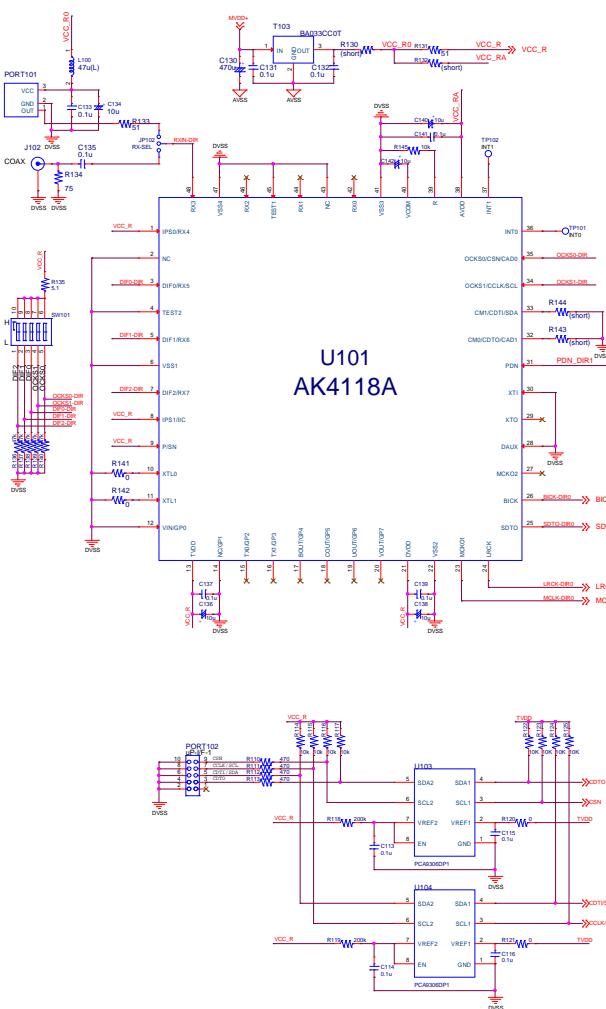
6. Revision History

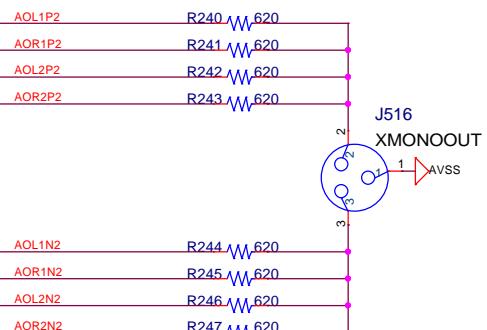
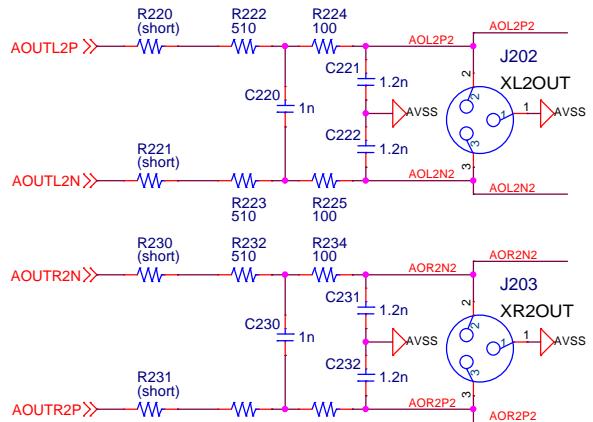
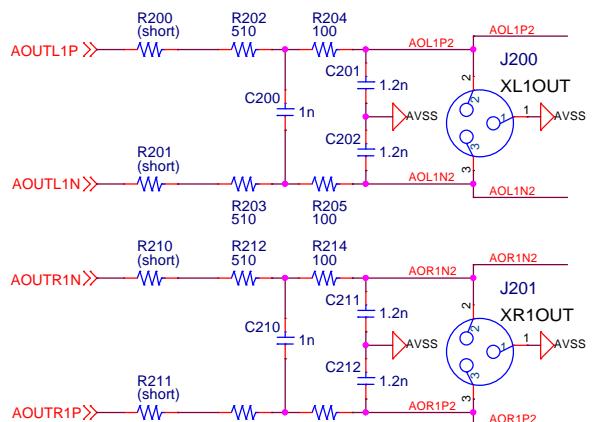
Date (y/m/d)	Manual Revision	Board Revision	Reason	Page	Contents
19/01/15	KM131500	0	First Edition	-	-
19/05/16	KM131501	0	Add Drawing	-	Add drawing. Figure. THD+N vs. Input Frequency Comparison by Capacitance

IMPORTANT NOTICE

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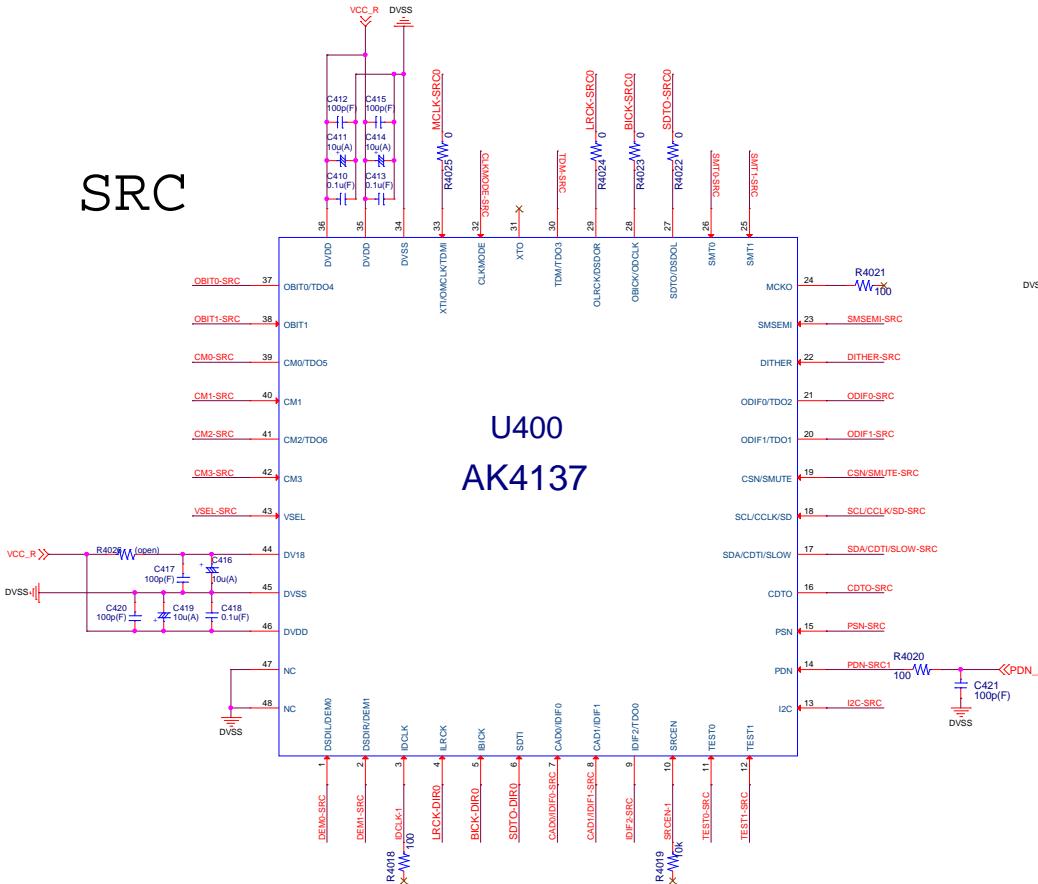
Rev.1





SRC

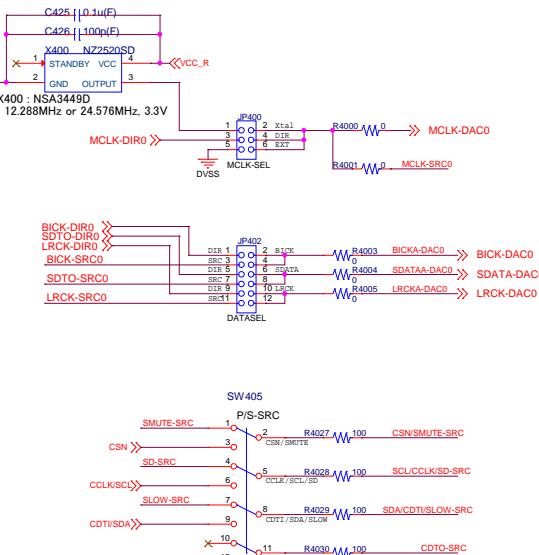
U400
AK4137

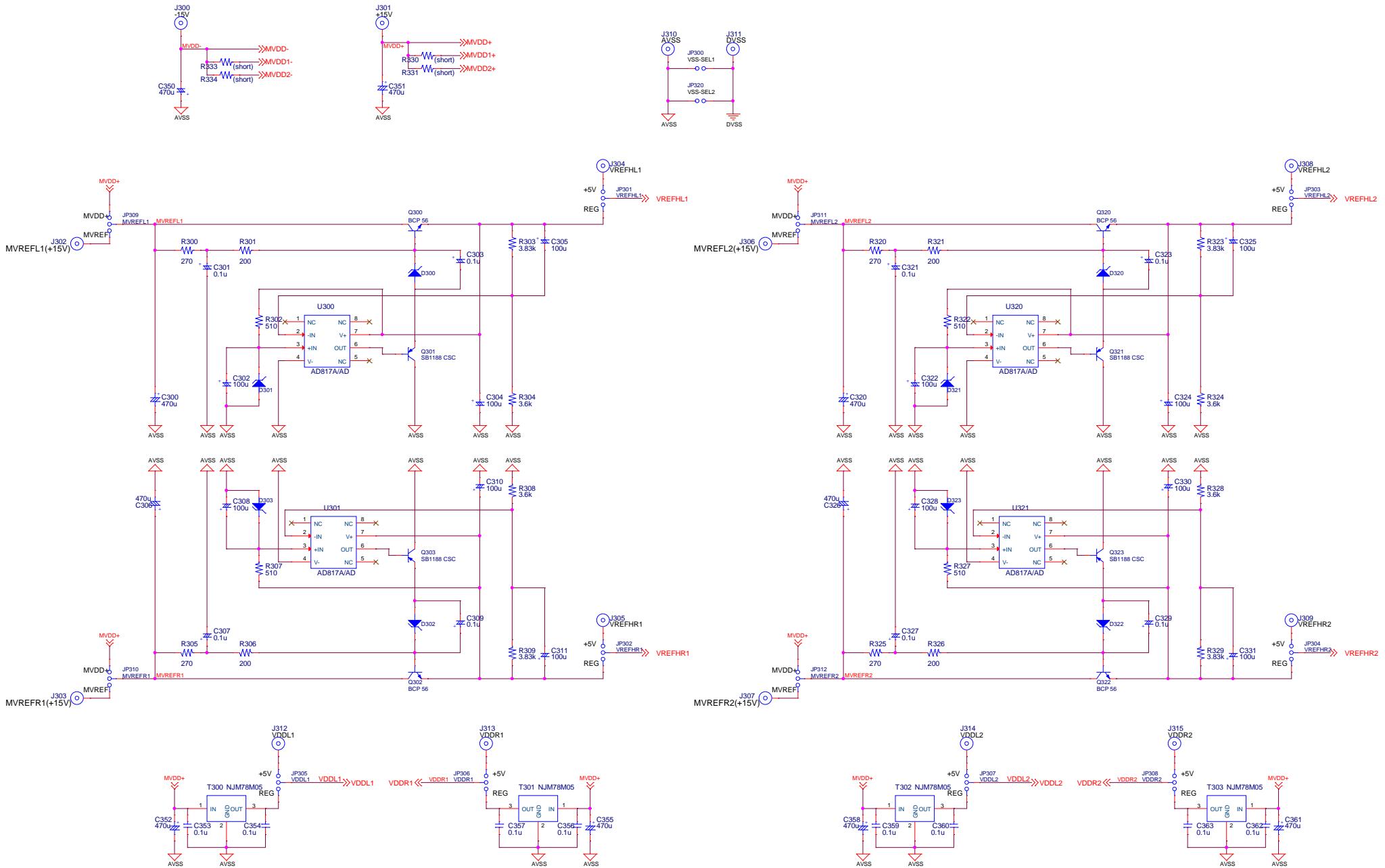


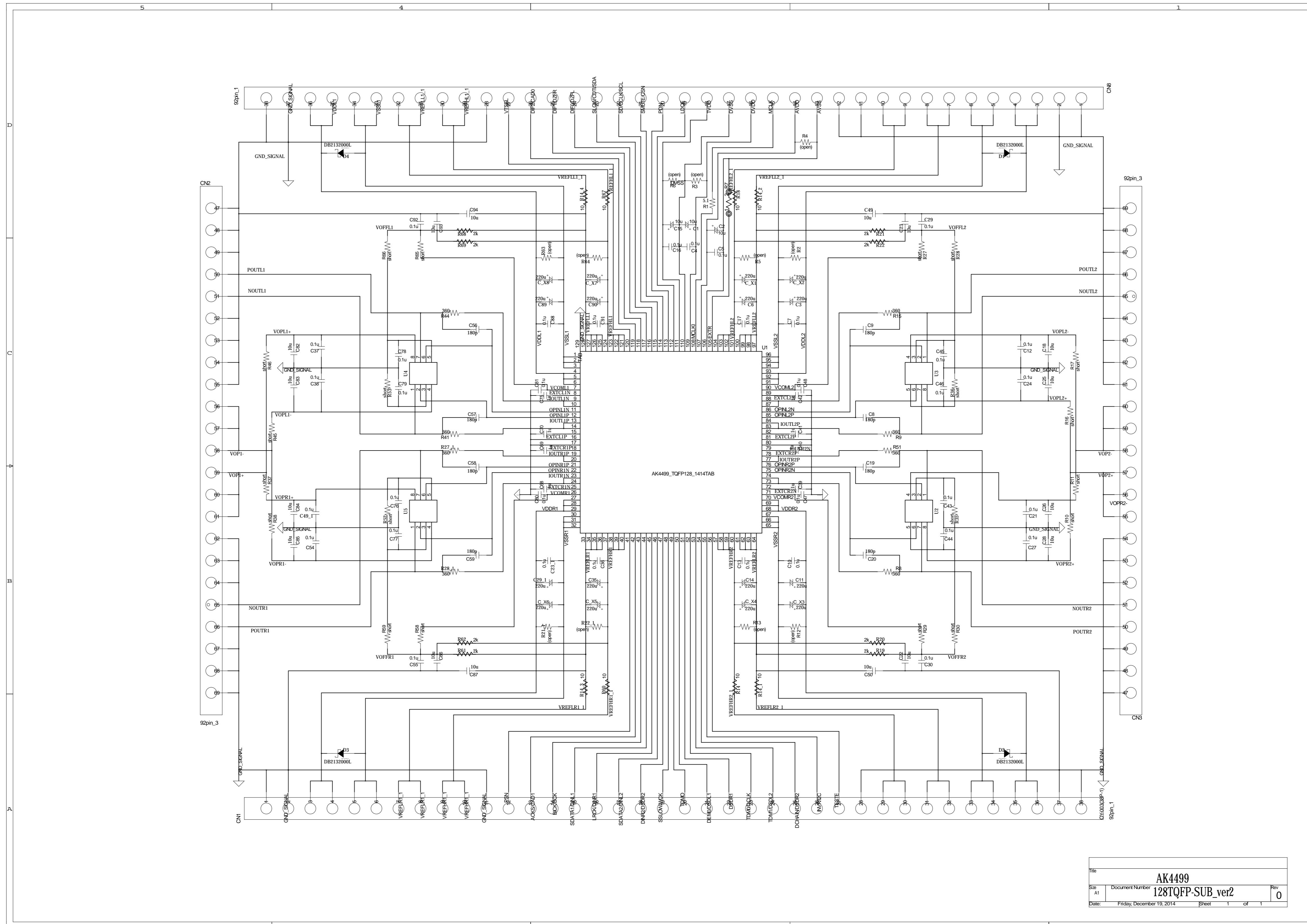
*Default Setting

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I2C=H
SD=H
SLOW=L
CM3=H
CM2=L
CM1=L
CM0=L
DEM1=L
DEM2=L
DEM1=L
IDF2=L
CAD1/IDF1=H
CAD0/IDF0=L
TEST1=L
TEST0=L
ODIF1=H
ODIF0=L
DITHER=L
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SMT0=L
TDM=L
CLKMODE=L
OBIT1=L
OBIT0=L
  
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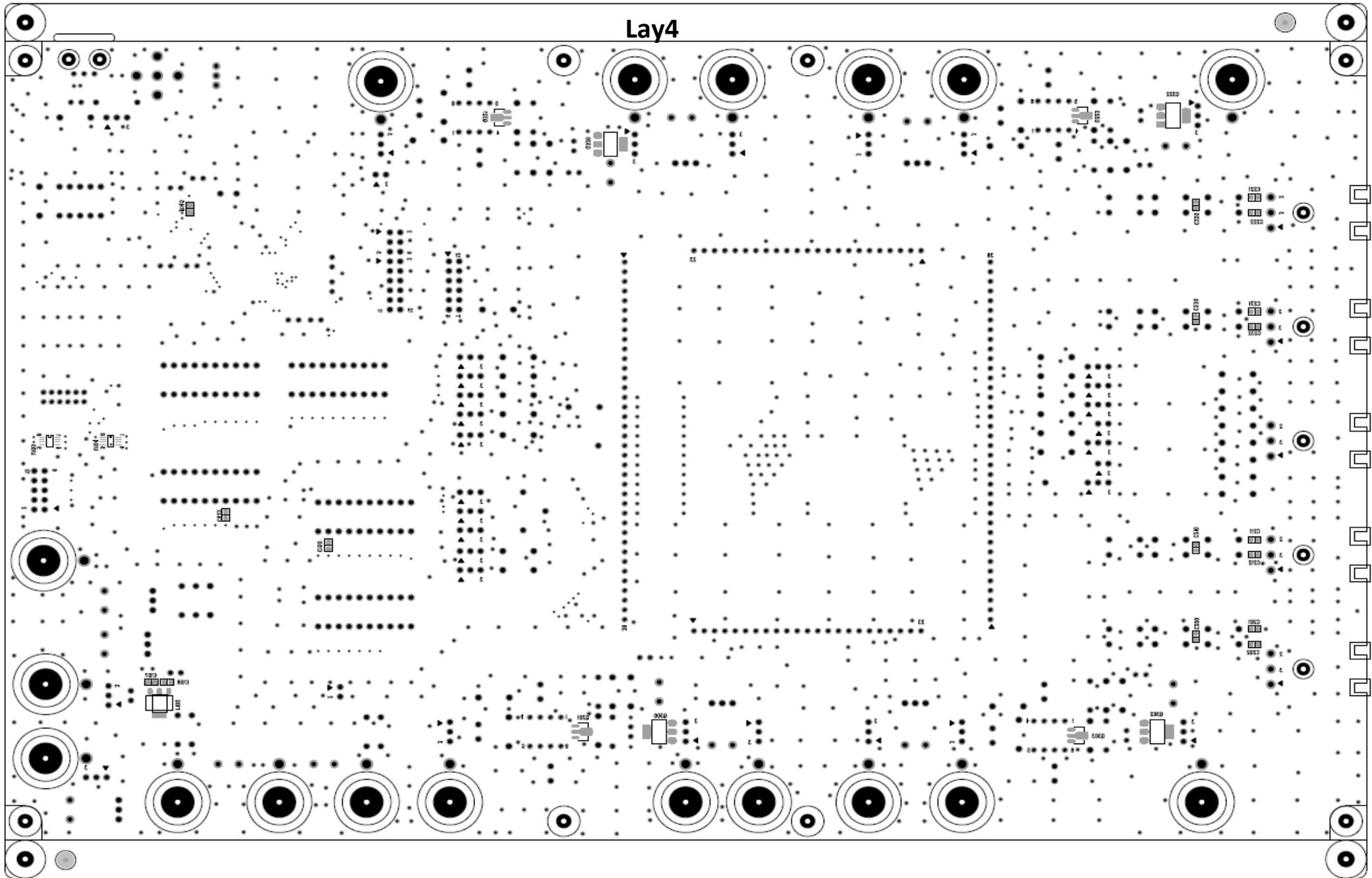


Lay1

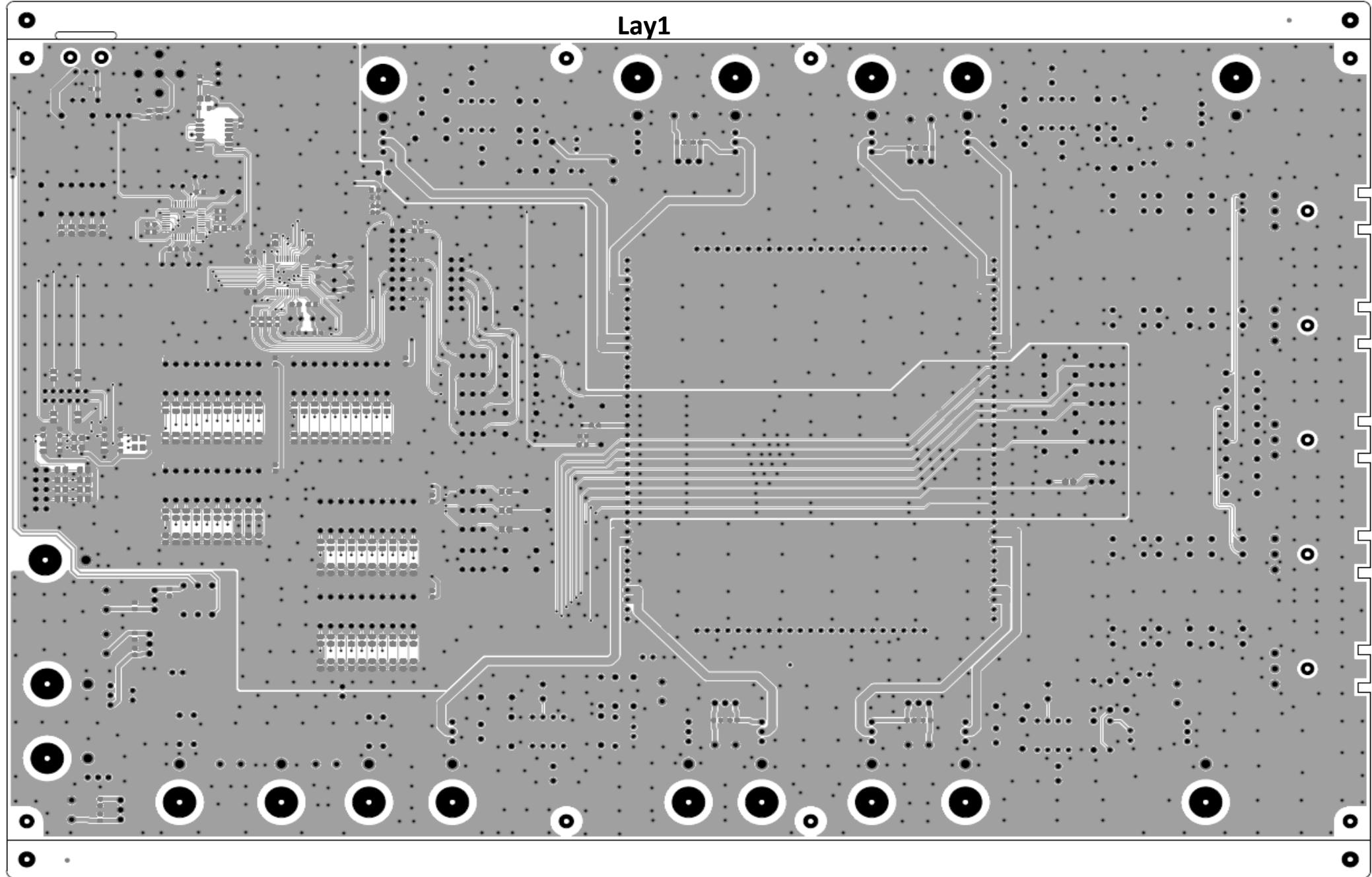
AKD4499-AZ1-MAIN, Rev.0
Evaluation Board



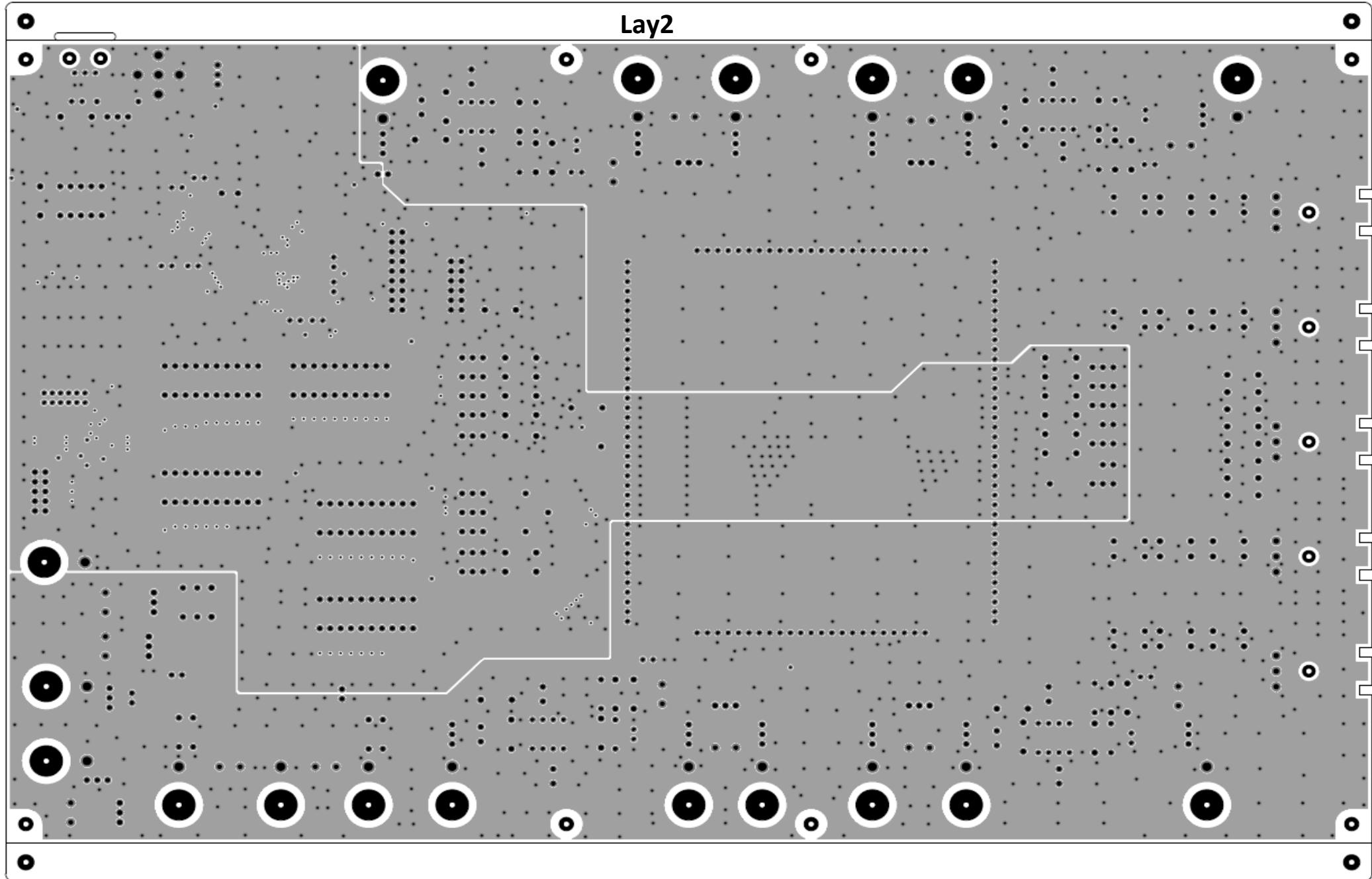
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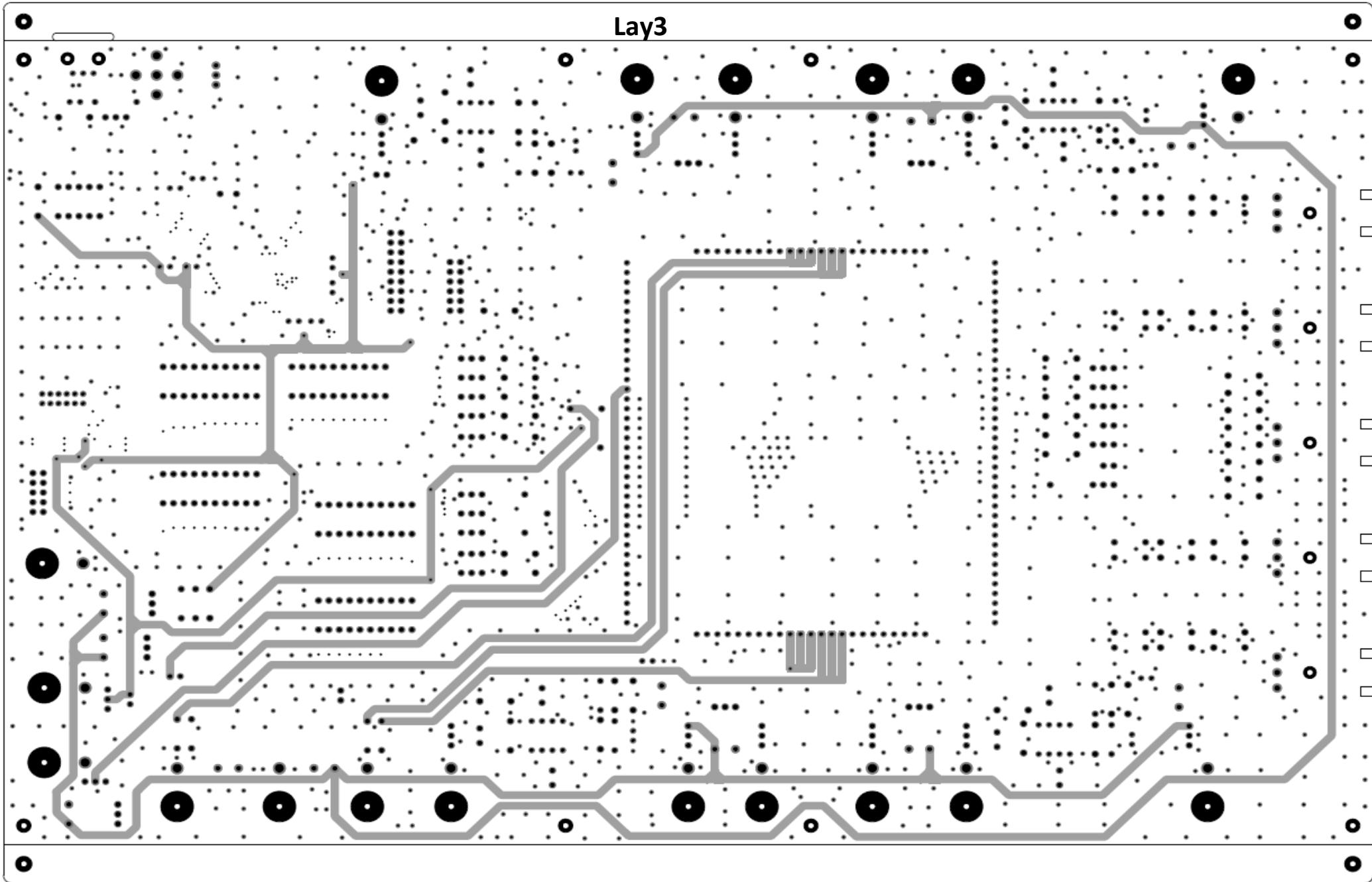
Lay1



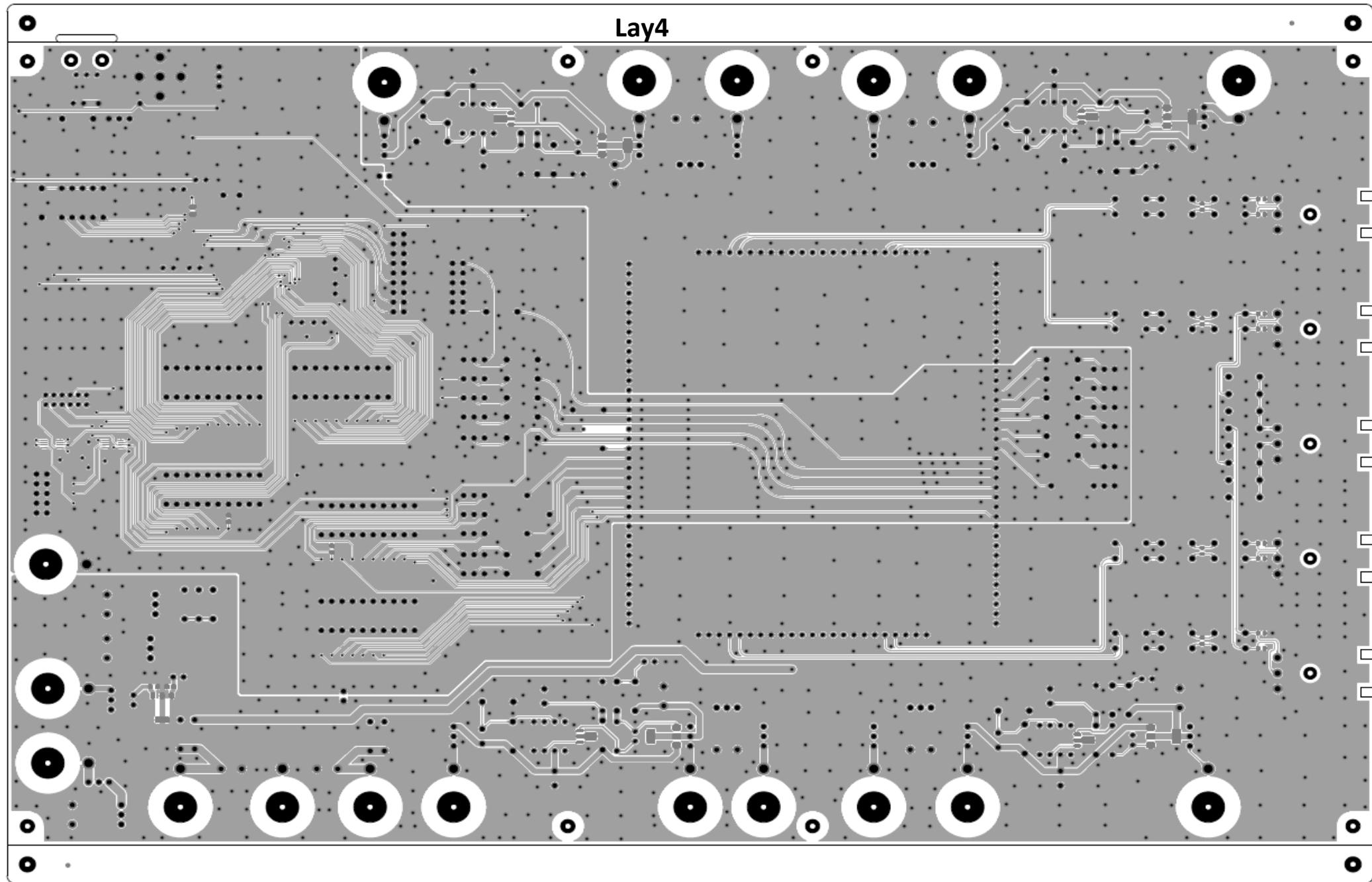
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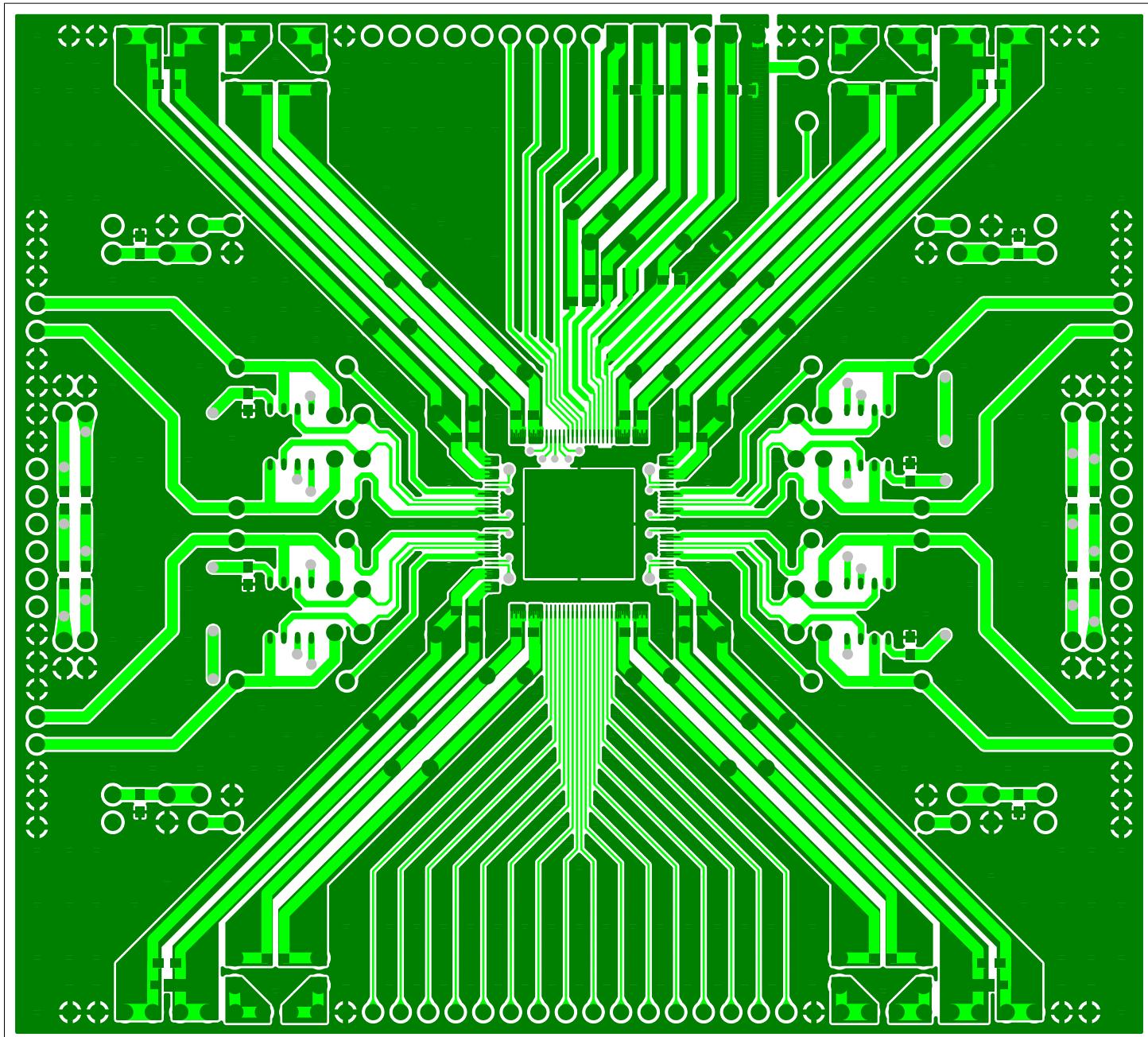


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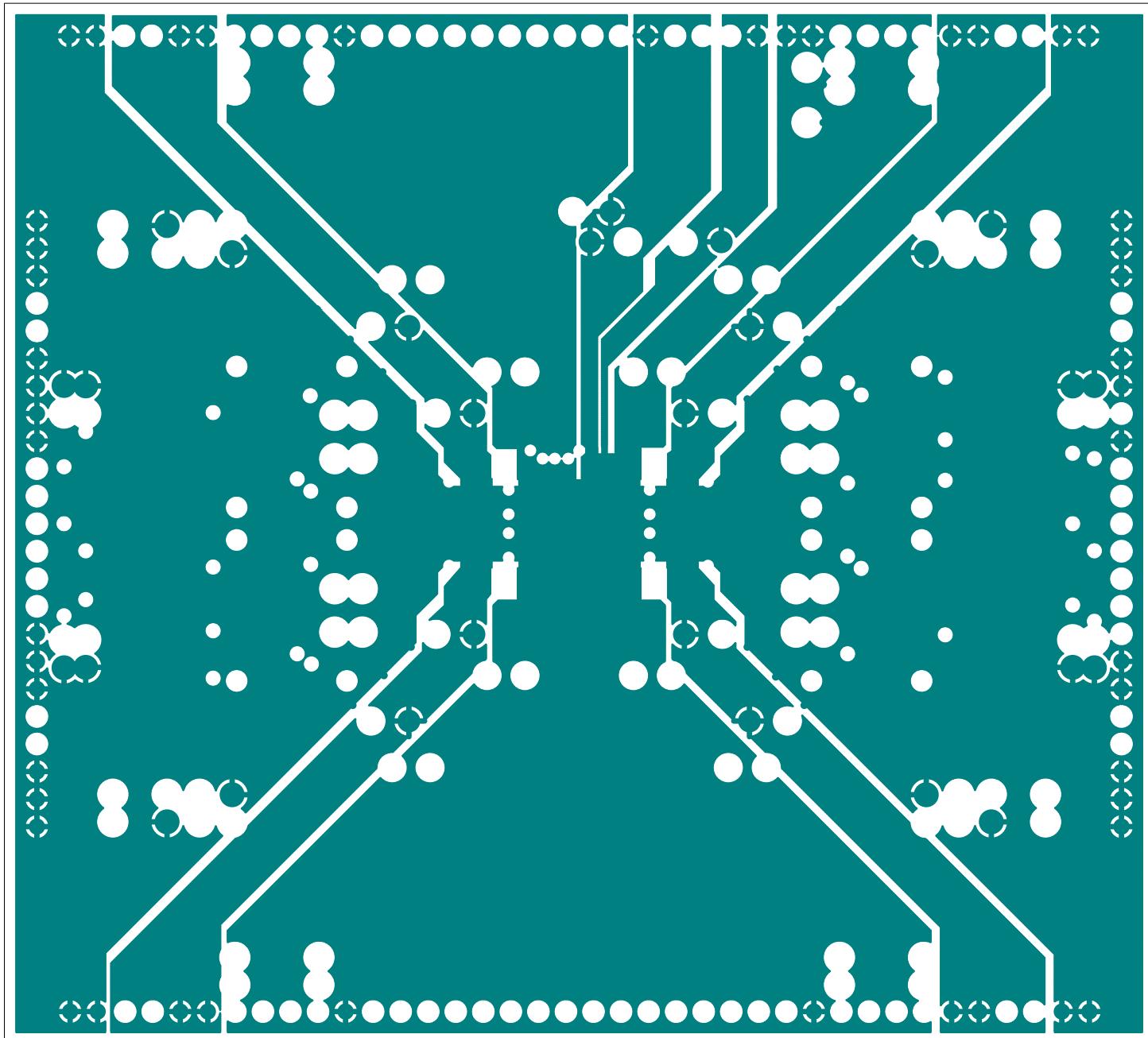


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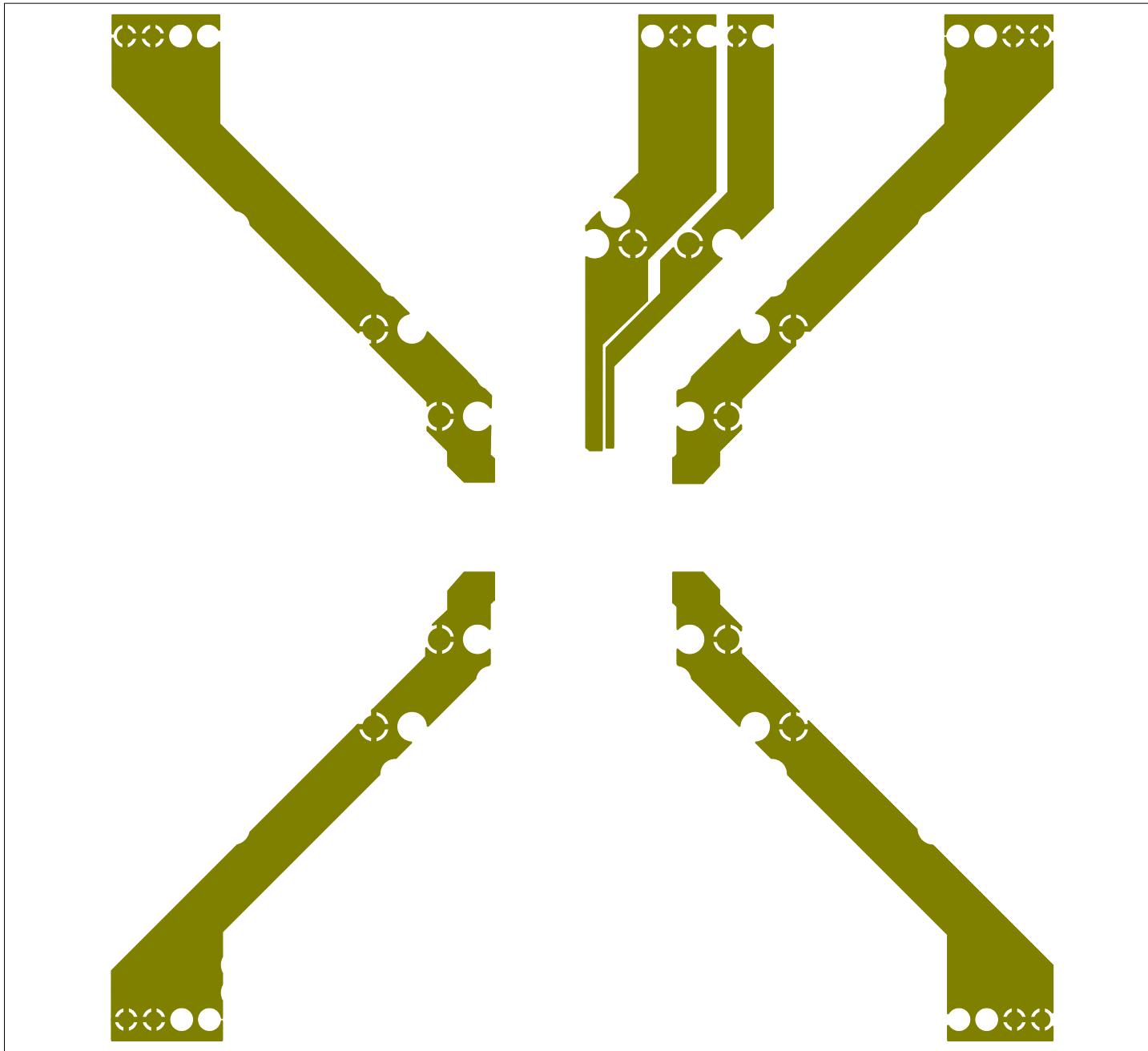




AK4499
Lay1



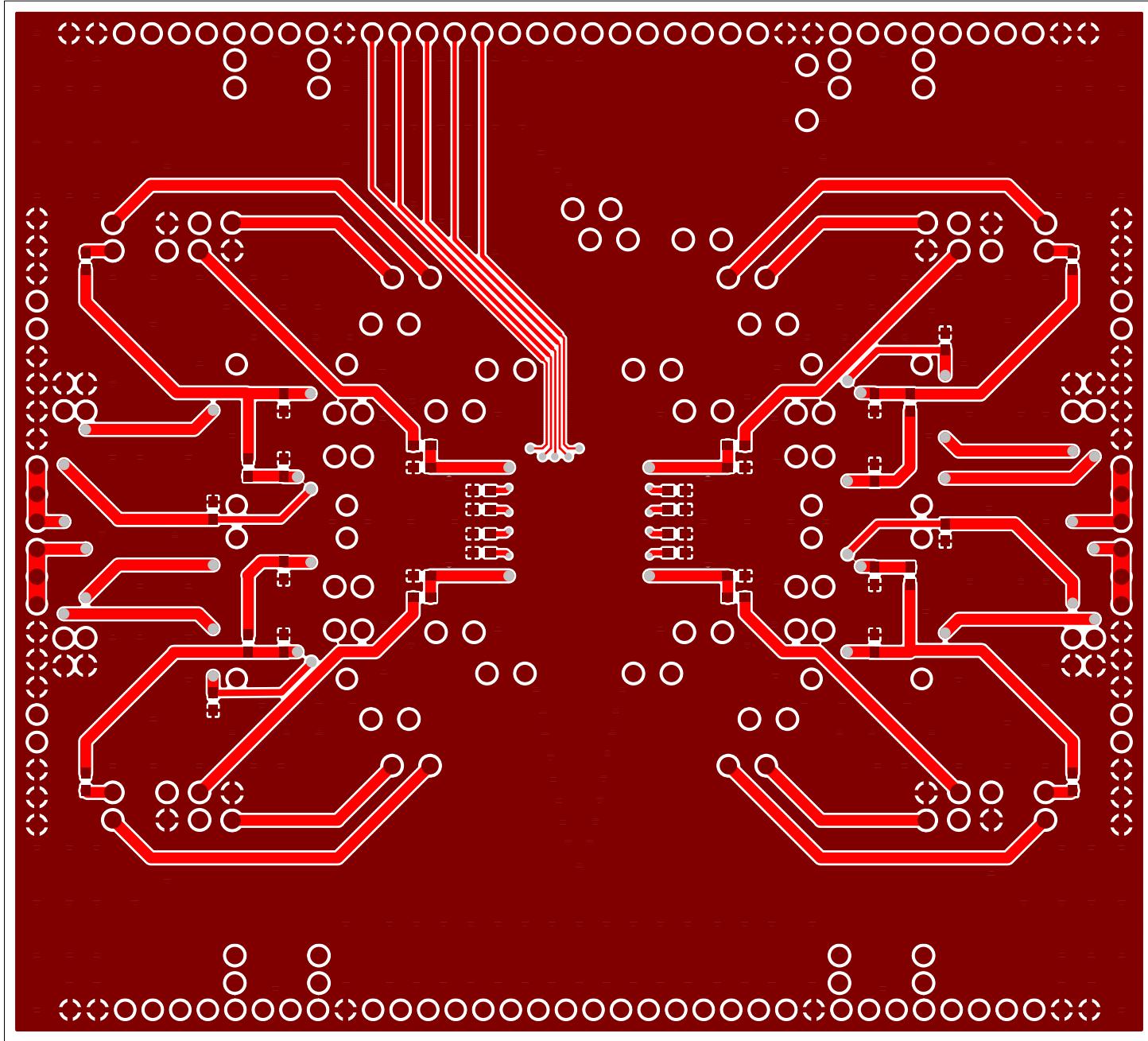
AK4499
Lay2



AK4499

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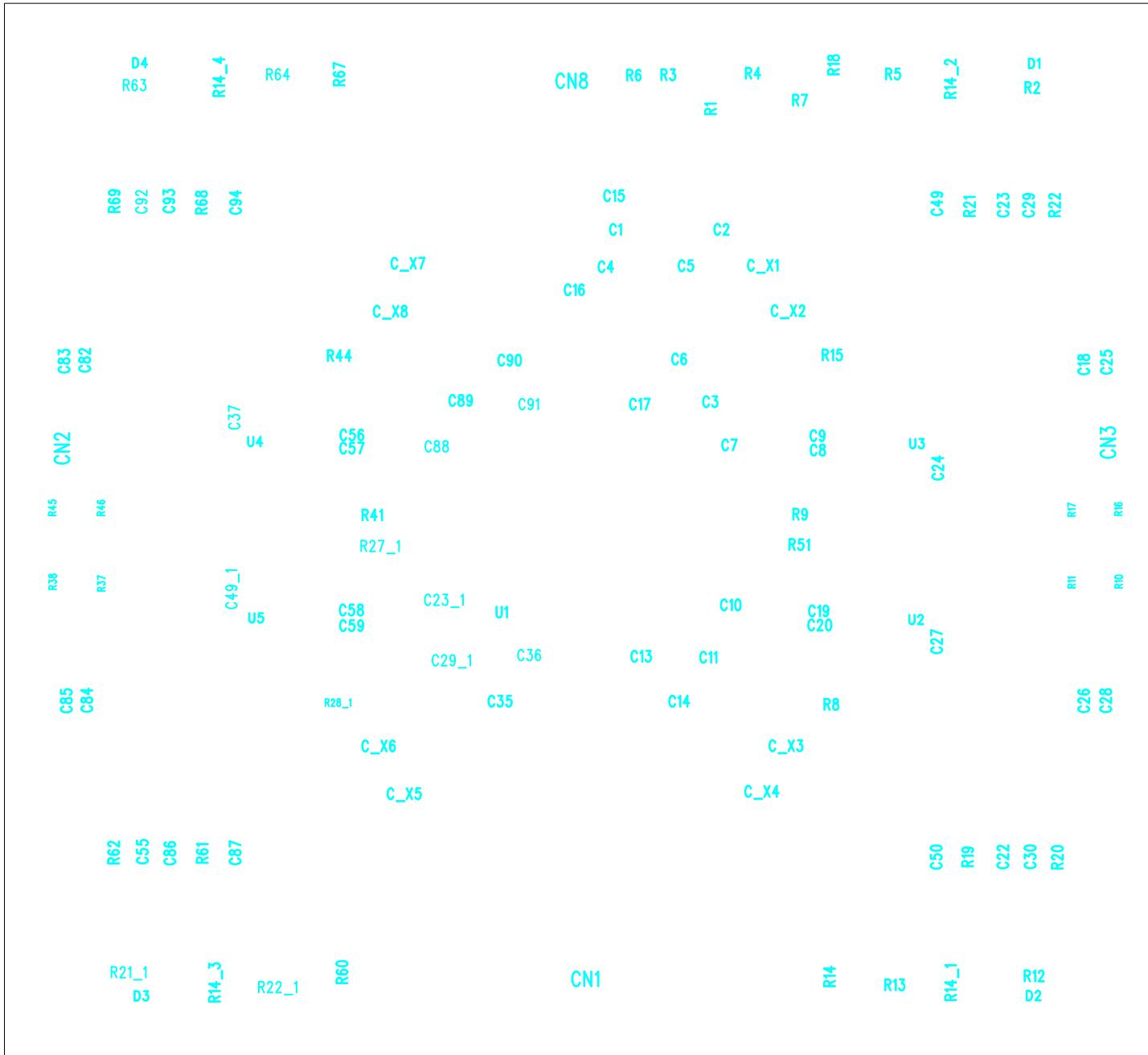
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AK4499

4yo

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AK4499
Lay1

CN1

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AK4499

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CWS

69

630

CM3

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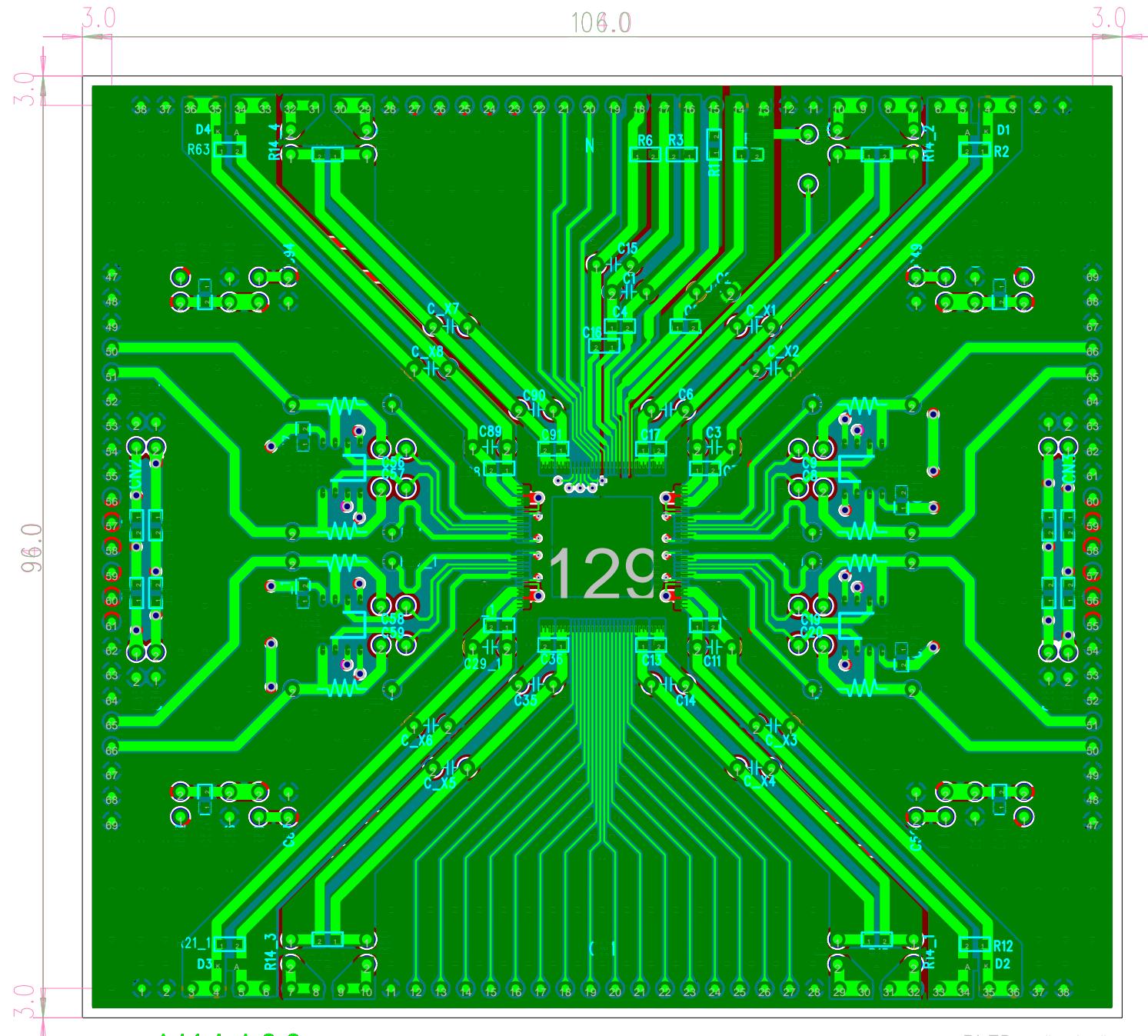
C4e C4f

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C40 C41 C42

CN8

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AK4499

Resist1 Resist2 Resist3

PLTD=スルーホール
NPLTD=キリ穴