

AKD4118A-A

AK4118A Evaluation Board Rev.1

GENERAL DESCRIPTION

AKD4118A-A is the evaluation board for AK4118A, 192 kHz digital audio transceiver. This board has BNC connector to interface with other digital audio equipment.

■ Ordering guide

AKD4118A-A --- Evaluation board for AK4118A (Control software is included in this package.)

FUNCTION

- □ Digital interface
 - -S/PDIF:
 - 8 channel input (BNC)
 - 2 channel output (BNC)
 - Serial audio data I/F:
 - 1 input/output (for DIR data output/DIT data input. 10-pin port)
- ☐ Serial control data I/F
 - 1 input/output port (10-pin port)

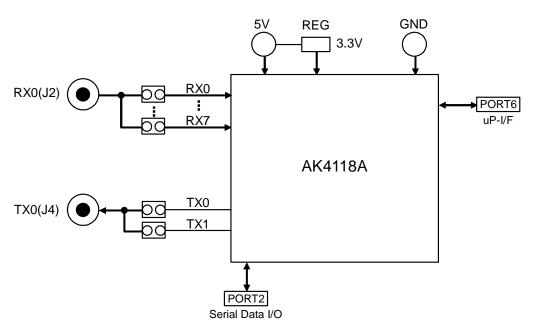


Figure 1. AKD4118A-A Block Diagram

Note 1. Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operating sequence

(1) Set up the power supply lines.

Name	Color	Voltage	Breakdown	Details	Default Setting
+5V	Red	+5V	VDD of AK4118A	Must be connected	+5V
GND	Black	GND	GND	Must be connected	GND

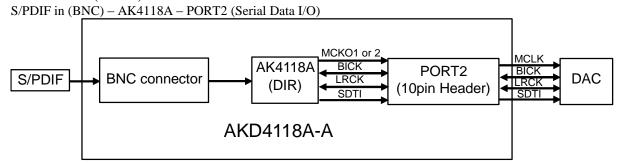
Note 2. Each supply line should be distributed from the power supply unit.

- (2) Set up the evaluation mode and jumper pins. (Refer to the following item.)
- (3) **Connect cables.** (Refer to the following item.)
- (4) Power on.

The AK4118A should be reset once bringing PDN (SW2) "L" upon power-up.

■ Evaluation modes

(1) Evaluation for DIR (Default)



The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector. The AKD4118A-A can be connected with the AKM's DAC evaluation board via 10 pin flat cable.

a. Set-up of Bi-phase Input

Bi-phase signal input is used from BNC (J2) connector.

a-1. Setting for the RX0-7.

Only RX0-3 can be used in parallel mode. The jumper which selects the Rx channel should be short. RX0 and RX0-7 should not select BNC at the same time.

Input Data	JP2	JP4	JP5	JP6	JP7	JP8	JP9	JP10	
RX0	BNC	Open	Open	Open	Open	Open	Open	Open	< Default >
RX1	Open	Short	Open	Open	Open	Open	Open	Open	
RX2	Open	Open	Short	Open	Open	Open	Open	Open	
RX3	Open	Open	Open	Short	Open	Open	Open	Open	
RX4	Open	Open	Open	Open	RX4	Open	Open	Open	
RX5	Open	Open	Open	Open	Open	RX5	Open	Open	
RX6	Open	Open	Open	Open	Open	Open	RX6	Open	
RX7	Open	Open	Open	Open	Open	Open	Open	RX7	

Table 1. Set-up of RX0-7

a-2. Set-up of AK4118A input path

It sets up by SW 1_1 and SW 1_5 in parallel mode. Please set up IPS2-0 bits in serial mode.

-	IPS1 pin (SW1_5)	IPS0 pin (SW1_1)	INPUT Data
IPS2 bit	IPS1 bit	IPS0 bit	
0	0	0	RX0
0	0	1	RX1
0	1	0	RX2
0	1	1	RX3
1	0	0	RX4
1	0	1	RX5
1	1	0	RX6
1	1	1	RX7

< Default >

(In parallel mode, IPS2 is fixed to "0") Table 2. Recovery Data Select

b. Set-up of clock input and output

The signal level outputted/inputted from PORT2 is 3.3V.

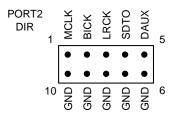


Figure 2. PORT2 pin layout

b-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 is selected by OCKS 1-0.

Output signal	JP12	
MCKO1	MCKO1	< Default >
MCKO2	MCKO2	

Table 3. Set-up of MCKO1/MCKO2

OCKS1 pin (SW3_2)	OCKS0 pin (SW3_3)	(X'tal)	MCKO1	MC	KO2	fs (max)	
OCKS1 bit	OCKS0 bit	, ,		PLL	X'tal	, ,	
0	0	256fs	256fs	"L"	256fs	96 kHz	< Default >
0	1	256fs	256fs	"L"	128fs	96 kHz	
1	0	512fs	512fs	"L"	256fs	48 kHz	
1	1	128fs	128fs	"L"	64fs	192 kHz	

Table 4. Master Clock Frequency Select

b-2. Set-up of input/output of BICK and LRCK

Please select SW 3_7 (DIR_I/O) according to the setup of audio format of AK4118A.

Audio format	SW3_7 (DIR_I/O)	
Slave mode	0	
Master mode	1	< Default >
Table 5. Set-up of D	IR_I/O	<u>-</u> '

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c. Set-up of Audio format

It sets up by SW 1_2, SW 1_3 and SW1_4 in parallel mode. Please set up DIF2-0 bit in serial mode.

Mode	DIF2 pin (SW1_4)	DIF1 pin (SW1_3)	DIF0 pin (SW1_2)	DAUX	SDTO	LR	CK	BIC	CK	
	DIF2 bit	DIF1 bit	DIF0 bit				I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	О	64fs	О	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	О	64fs	О	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	О	64fs	О	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	О	64fs	О	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	О	64fs	О	
5	1	0	1	24bit, I ² S	24bit, I ² S	L/H	О	64fs	О	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64- 128fs	I	< Default >
7	1	1	1	24bit, I ² S	24bit, I ² S	L/H	I	64- 128fs	I	

Table 6. Audio format

d. Set-up of CM1 and CM0

The operation mode of PLL is selected by CM1 and CM0. In parallel mode, it can be selected by SW3_1 and JP18. In serial mode, it can be selected by CM1-0 bits.

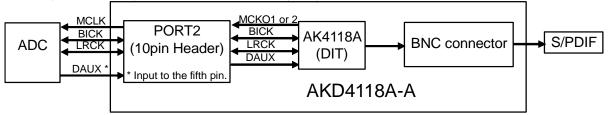
CM1 pin (SW3_1) CM1 bit	CM0 pin (JP18) CM0 bit	(UNLOCK)	PLL	X'tal	Clock source	SDTO source	
0	0 (CM0=L)	-	ON	ON (Note 3)	PLL(RX)	RX	
0	1 (CDTO/CM0=H)	-	OFF	ON	X'tal	DAUX	< Default >
1	0	0	ON	ON	PLL(RX)	RX	
1	(CM0=L)	1	ON	ON	X'tal	DAUX	
1	1 (CDTO/CM0=H)	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note 3. When the X'tal is not used as clock comparison for fs detection (XTL0, 1= "1,1"), the X'tal is OFF. Table 7. Clock Operation Mode Select

(2) Evaluation for DIT

PORT2 (Serial Data I/O) – AK4118A – S/PDIF out (BNC)



MCLK, BICK, LRCK and DAUX are input the via 10pin header (PORT2: DIR).

a. Set-up of a Bi-phase output signal

Bi-phase signal output is used from BNC (J4) connector.

TX0 and TX1 should not select a BNC connector at the same time.

The data outputted from TX1 can be selected by OPS12-10 bit.

As for TX0, only the loop back mode of RX corresponds. This mode is fixed to RX0 in parallel mode. In serial mode, it can be selected by OPS02-00 bits.

Output	JP13	JP19	
Data	(TX0)	(TXP1)	
TX0	BNC	Open	
TX1	Open	BNC	< Default >

Table 8. Set-up of Bi-phase signal

b. Set-up of clock input and output

The used signals are MCLK, LRCK, BICK, and DAUX. The signal level outputted and inputted from PORT2 is 3.3V.

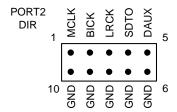


Figure 3. PORT2 pin layout

Clock	PORT	I/O
MCLK	PORT2	OUT
BICK	PORT2	IN / OUT
LRCK	PORT2	IN / OUT
DAUX	PORT2	IN

Table 9. Clock input/output

b-1. MCKO1/MCKO2

Please refer to Table 3 and Table 4.

b-2. Set-up of input/output of BICK and LRCK

Please refer to Table 5.

c. Set-up of audio data format

Please refer to Table 6.

d. Set-up of CM1 and CM0

Please refer to Table 7.

■ Serial control

The AK4118A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT6 (uP-I/F) with PC by 10-line flat cable packed with the AKD4118A-A. Take care of the direction of connector. There is a mark at pin#1. The pin layout of PORT6 is as Figure 4.

Mode	SW1_5	JP18
4 wire Serial	L	[CDTO/CM0=H] is Short.
IIC	Н	[SDA] and [CM0=L] are Short. (Note 4)

Table 10. Set-up of Parallel mode and Serial mode

Note 4. In IIC mode, the chip address is fixed to "01".

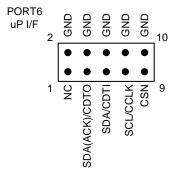


Figure 4. PORT6 pin layout

This evaluation board encloses control software. A software operation procedure is included in an evaluation board manual.

■ Toggle switch set-up

SW2 PDN Reset switch for AK4118A. Set to "H" during normal operation. the power is supplied.
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■ LED indication

LE1	INT0	Bright when INT0 pin goes to "H".	
LE2	INT1	Bright when INT1 pin goes to "H".	

■ DIP switch (SW1) set-up: -off- means "L"

No.	Switch Name	Function	Default	
1	IPS0	Set-up of IPS0 pin. (in parallel mode)	OFF	
2	DIF0	Set-up of DIF0 pin. (in parallel mode)	OFF	
3	DIF1	Set-up of DIF1 pin. (in parallel mode)		
4	DIF2	Set-up of DIF2 pin. (in parallel mode)	OFF	
5	IPS1/IIC	Set-up of IPS1 pin. (in parallel mode) Set-up of IIC pin. (in serial mode) "L": 4 wire Serial, "H": IIC	OFF	
6	P/SN	Set-up of P/SN pin. "L": Serial mode, "H": Parallel mode OF		
7	TEST	Don't care	OFF	
8	ACKS	Don't care	OFF	

■ DIP switch (SW3) set-up: -off- means "L"

No.	Switch Name	Function	Default
1	CM1	Set-up of CM1 pin. (in parallel mode)	OFF
2	OCKS1	Set-up of OCKS1 pin. (in parallel mode)	OFF
3	OCKS0	Set-up of OCKS0 pin. (in parallel mode)	OFF
4	PSEL	Don't care	OFF
5	XTL0	See Table 11.	OFF
6	XTL1		OFF
7	DIR_I/O	Setting the transmission direction of BICK and LRCK of the PORT2. "L": When inputting from PORT2, "H": When outputting from PORT2	ON
8	DIT_I/O	Don't care	OFF

■ Set-up of XTL1 and XTL0

SW3_6 XTL1	SW3_5 XTL0	X'tal Frequency	
0	0	11.2896MHz	< Default >
0	1	12.288MHz	
1	0	24.576MHz	
1	1	(Use channel status)	

■ Jumper set up.

No.	Jumper Name	Function			
	-	Selection the power supply of digital logic circuit.			
1	D3V/VD	D3V: +3.3V input. < Default >			
		VD: +5.0V input.			
		Set-up of RX0 input circuit.			
2	DVD0	OPT: Not to use.			
2	RXP0	XLR: Not to use.			
		BNC: BNC connector (J2) is used. < Default >			
150	DV1 2	Set-up of RX1-3 input circuit.			
4,5,6	RX1-3	Only for the Rx input you want to use, set the jumper pin to "short".			
		RX4-7 set-up depending serial/parallel mode			
7.0.0.10	DX4.7	RX4-7: Serial mode < Default >			
7,8,9,10	RX4-7	Only for the Rx input you want to use, set the jumper pin to "short".			
		DIF2-0,IPS0: Parallel mode			
		MCKO set-up for PORT2 (DIR).			
12	DIR MCLK	MCKO1: MCKO1 of AK4118A < Default >			
		MCKO2: MCKO2 of AK4118A			
	TX0	Set-up of TX0 output circuit.			
13		OPT: Not to use.			
13		BNC: BNC connector (J4) is used.			
		Open: When using TX1 output, JP13 is set to "Open". < Default >			
	SDA/CDTO	Set-up of SDA/CDTO pin.			
		4 wire serial < Default > IIC			
		JP18 JP18 SDA/CDTO SDA/CDTO			
		5 0 1 5 0 1			
18					
		CM0=L CM0=H CM0=H SDA			
		CM0=L CDTO/CM0=H SDA CM0=L SDA SDA			
		5 5			
19	TXP1	Set-up of TXP1 input circuit.			
		OPT: Not to use.			
		XLR: Not to use.			
		BNC: BNC connector (J4) is used. < Default >			
		Open: When using TX0 output, JP19 is set to "Open".			

Control Software Manual

■ Set-up of evaluation board and control software

- 1. Set up the AKD4118A-A according to previous term.
- 2. Connect IBM-AT compatible PC with AKD4118A-A by 10-line type flat cable (packed with AKD4118A-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)
- 3. Insert the CD-ROM labeled "AKD4118A-A Evaluation Kit" into the CD-ROM drive.
- 4. Access the CD-ROM drive and double-click the icon of "akd4118a-a.exe" to set up the control program.
- 5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

- 1. Set up the control program according to explanation above.
- 2. Click "Write default" button.
- 3. Then set up the dialog and input data.

■ Explanation of each buttons

1. [Port Setup]: Set up the printer port.

2. [Write default]: Initialize the register of AK4118A.

3. [All Write]: Write all registers that is currently displayed.
4. [Read All]: All the registers of AK4118A are read.
5. [Function1]: Dialog to write data by keyboard operation.

6. [F3]: Dialog of sequential writing.
7. [SAVE]: Save the current register setting.
8. [OPEN]: Write the saved values to all register.
9. [Write]: Dialog to write data by mouse operation.
10. [Read]: The data corresponding to each register is read.

■ Explanation of each dialog

1. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input register address in 2 figures of hexadecimal.

Data Box: Input register data in 2 figures of hexadecimal.

If you want to write the input data to AK4118A, click "OK" button. If not, click "Cancel" button.

2. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the "Write" button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4118A, click "OK" button. If not, click "Cancel" button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Attention on the operation

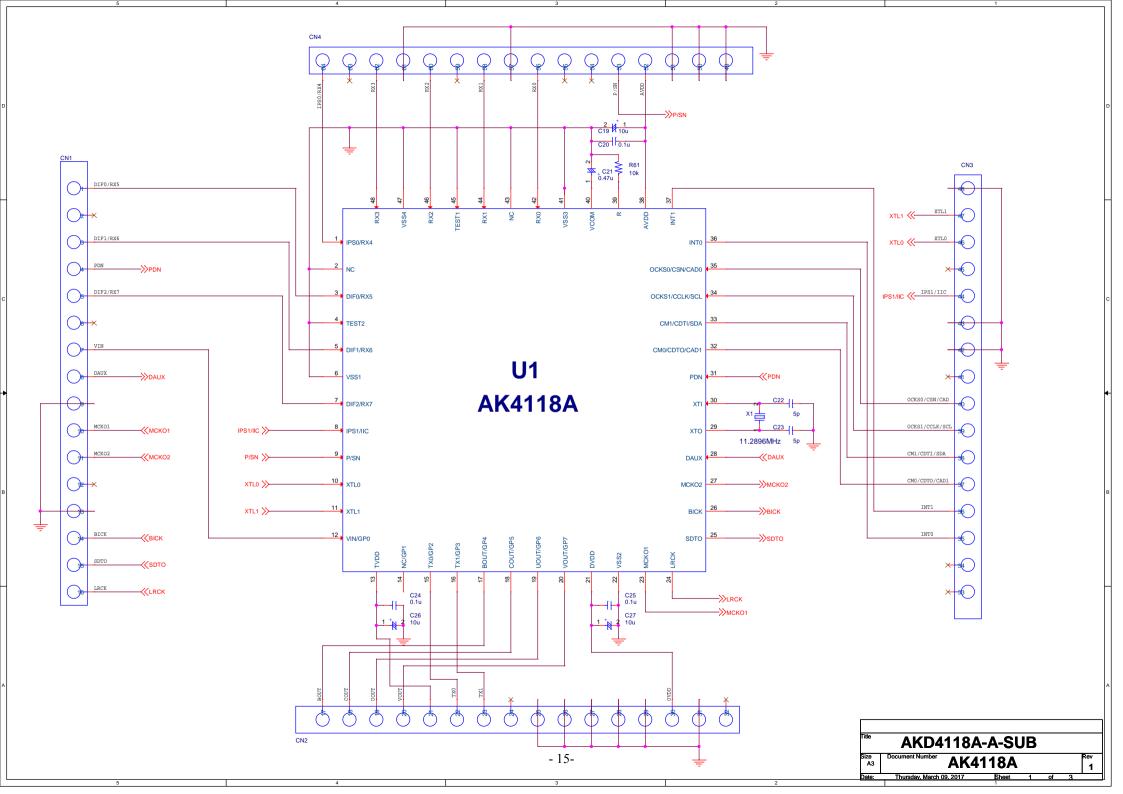
If you set up Function1 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click "OK" button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click "Cancel" button or check the check box.

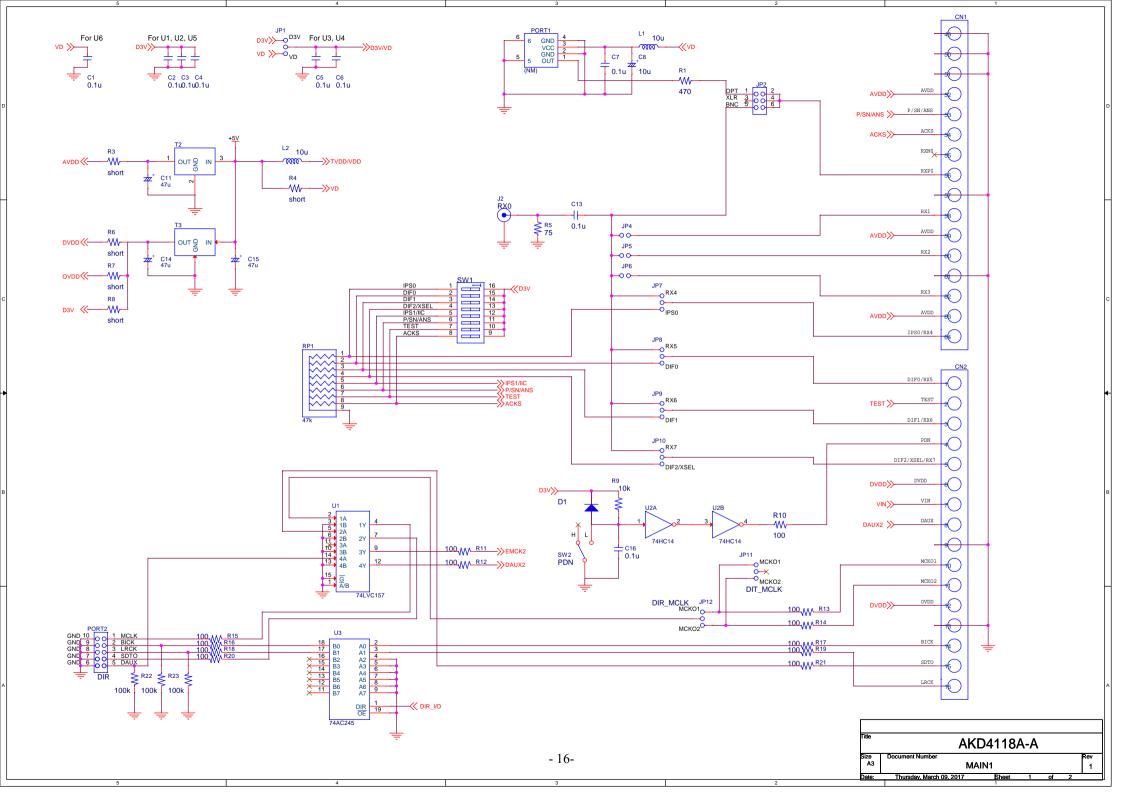
REVISION HISTORY

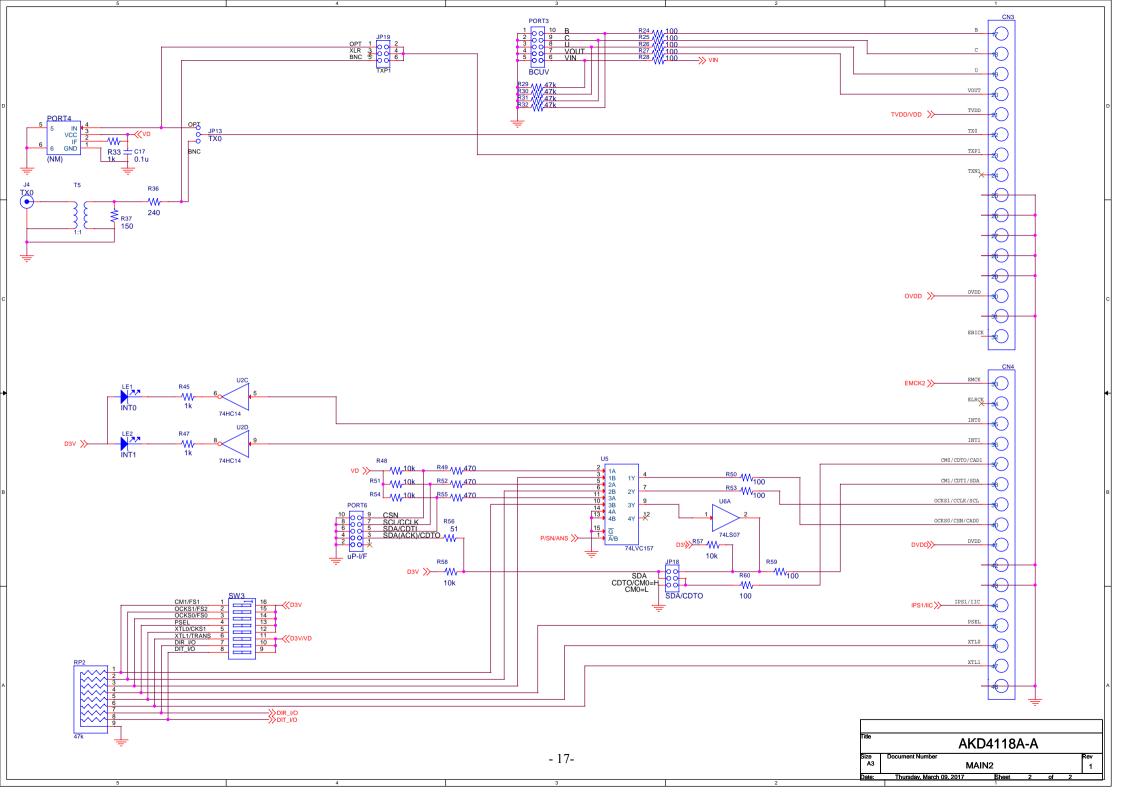
Date	Manual	Board	Reason	Page	Contents
(yy/mm/dd)	Revision	Revision			
09/08/05	KM100300	0	First edition	-	-
17/05/18	KM100301	1	Change	1, 10,	Circuit diagram was changed.
				14	PORT1, PORT4 : "Mount" -> "Unmounts"
					Block diagram was changed.
					Jumper set up was changed.

IMPORTANT NOTICE

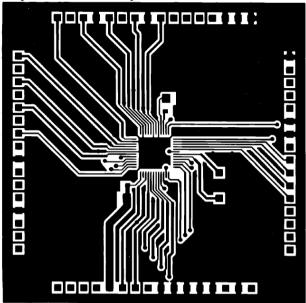
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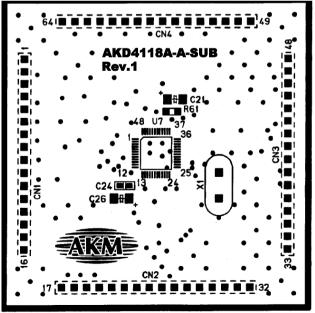




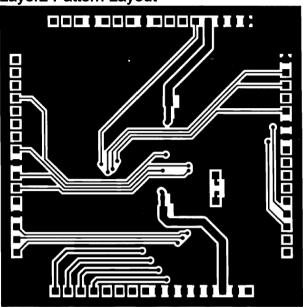
Layer1 Pattern Layout



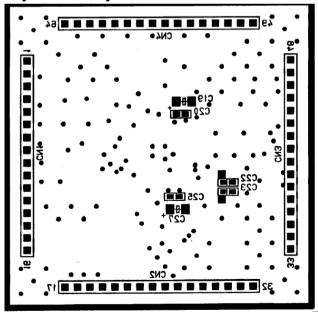
Layer1 Silk Layout

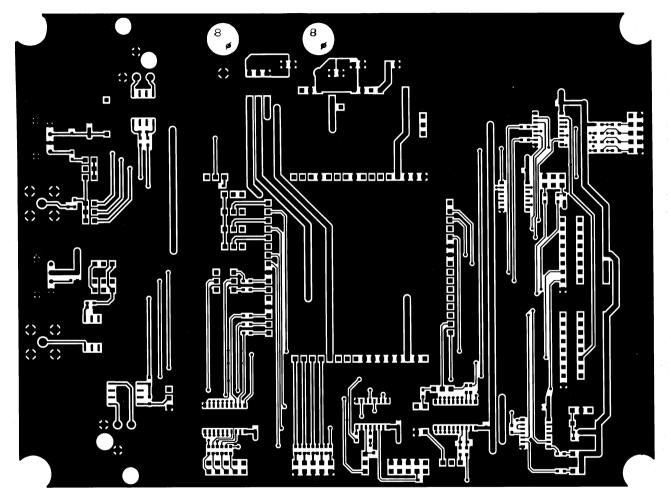


Layer2 Pattern Layout

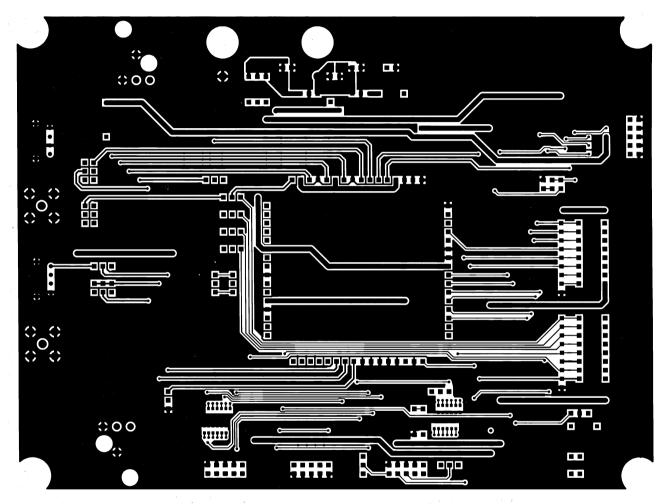


Layer2 Silk Layout

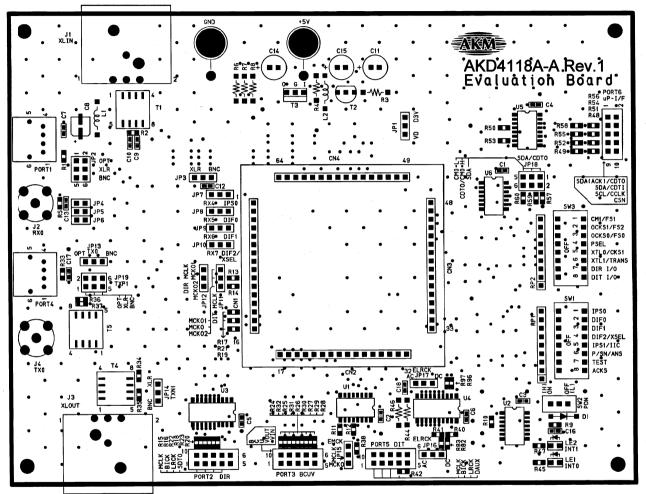




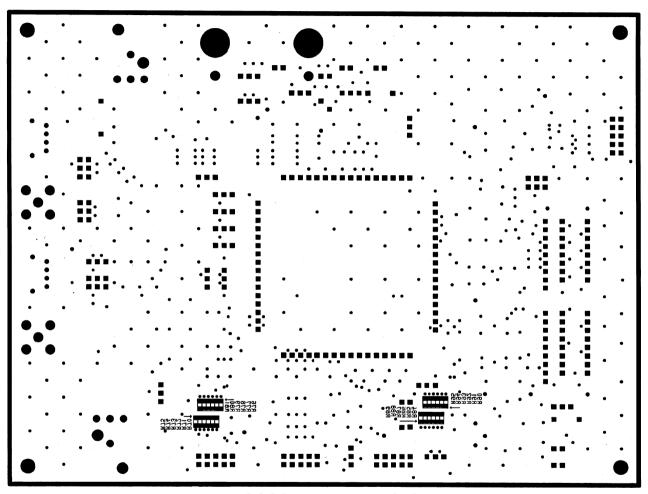
AKD4118A-A Layer1 Pattern Layout



AKD4118A-A Layer2 Pattern Layout



AKD4118A-A Layer1 Silk Layout



AKD4118A-A Layer2 Silk Layout