Design and Implementation of an 8-bit Split-Array Charge Scaling DAC in 45nm CMOS Technology

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***Abstract*—This paper presents the design and implementation of an 8-bit split-array charge-scaling DAC in 45 nm CMOS technology. The proposed topology effectively balances power consumption, linearity, and area constraints, achieving a compact layout of 60 μm^2. The DAC's digital-to-analogue conversion employs a bias-assisted charge-scaling architecture, preceded by a serial-to-parallel converter and followed by a rail-to-rail output buffer. Simulation results confirm compliance with design specifications, including a maximum INL of 1.62 LSB, a maximum DNL of 1.13 LSB, a propagation delay of 4.3 ns, a settling time of 150 ns, and an RMS power consumption of 0.52 mW—all within the specified 0.5 mm^2 area and 5 mW power budget. These results demonstrate that the proposed design is a power-efficient, high-performance DAC suitable for integrated circuit applications.**

I. Introduction

Digital-to-analogue converters (DACs) are essential components in mixed-signal integrated circuits, enabling seamless data conversion between digital and analogue domains. This paper presents the design and implementation of an 8-bit split-array charge-scaling DAC in 45nm CMOS technology. It begins by outlining the system's specifications, design constraints, and the selection process for the most suitable DAC topology. The chosen architecture is then examined in detail, including its preceding and succeeding stages, followed by a discussion of the layout implementation. Finally, the paper presents the DAC's simulated performance, focusing on linearity, dynamic response, and power consumption metrics.

II. System Overview

This section presents the system specifications and outlines the decision-making process for selecting a suitable DAC to meet the design requirements.

A. System Specification

The DAC must feature an 8-bit resolution and perform conversions within 2.5 µs. The relative error, including both integral nonlinearity (INL) and differential nonlinearity (DNL), must remain below 2 least significant bits (LSBs). The output voltage range is specified from 0.1 V to 1 V, while the total power consumption, including both static and dynamic components, cannot exceed 5 mW. Additionally, the layout area is constrained to 0.5 mm^2, and the propagation delay must be less than 1 µs. The load impedance is specified as 10 kΩ in parallel with 10 pF. The assigned specifications are delineated in Table I.

Parameter	Specification
Resolution	8-bit
Conversion Speed	2.5 µs per Conversion
Relative Error	$<$ 2 LSB
Output Range	0.1 V to 1 V
Power Consumption	$<$ 5 mW
Propagation Delay	$<$ 1 µs
Area	$<$ 0.5 mm^2
Load Impedance	10 kΩ / 10 pF

TABLE I: Assigned specifications for the 8-bit DAC.

B. Choosing a Suitable DAC Topology

The following DAC topologies are evaluated for their suitability in meeting the assigned specifications:

- **Resistive String DAC**: This topology is straightforward to implement and inherently monotonic, ensuring reliable linearity. However, its extensive resistor network results in high power consumption and significant area requirements, making it unsuitable for the given specifications.
- **R-2R Ladder DAC**: The R-2R ladder features a compact design with fewer resistors, reducing its area demands. However, it is prone to DNL and non-monotonic behaviour due to resistor mismatches, making it less suitable for the specified performance targets.
- **Current-Steering DAC**: This topology excels in high-speed applications and offers excellent scalability. However, its complex layout, driven by stringent transistor matching requirements, adds design complexity. This complexity is unwarranted for an 8-bit DAC with a relative error specification below 2 LSBs.
- **Charge-Scaling DAC**: This topology is energy-efficient, consuming power only during input transitions. Its main limitation is the exponential growth of the most significant bit (MSB) capacitor size, which dominates the layout area as resolution increases. Additionally, parasitic capacitances degrade performance, especially beyond 10-bit resolution.
- **Split-Array Charge-Scaling DAC**: This topology addresses the traditional charge-scaling DAC's area limitation by dividing the capacitor array into two smaller

arrays connected by an attenuation capacitor. This design significantly reduces area consumption and mitigates parasitic effects. While the split-array approach introduces slightly more design complexity, it provides an optimal trade-off between power efficiency, area usage, and linearity for an 8-bit resolution. As a result, this topology is selected as the most suitable for this design.

III. Circuit Implementation

This section presents the system and details the low-level design of the split-array charge-scaling DAC and its output buffer stage. Finally, the layout implementation is discussed.

A. System Overview

Implementing the split-array charge-scaling DAC requires understanding the signal flow from the digital input to the analogue output across the load. Figure 1 shows the system's block diagram. The serial digital input is clocked at 10 MHz, corresponding to a clock period of 0.1 μs. The input data is stored in an 8-bit shift register, which fills over 8 clock cycles (0.8 μs) within a 2.5 μs sampling cycle, simulating the maximum sampling rate. Once the shift register is fully loaded, its parallel output serves as the DAC input, where the digital code is converted into an analogue voltage ranging from 0.1 V to 1 V using a bias-assisted discharge technique. The analogue output is then buffered to ensure linearity and correct output range when driving the load.

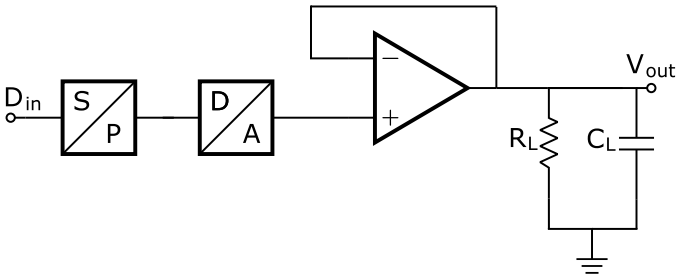

Fig. 1: Signal flow in the DAC system: serial digital input to buffered analogue output.

B. DAC Overview

The schematic for the split-array charge-scaling DAC is shown in Figure 2. The capacitors are numbered from C_0 to C_N, where N represents the number of bits. The attenuation capacitor (C_{atten}) adjusts the impedance of the capacitive array, enabling half the number of scaled unit capacitors to represent an equivalent 8-bit array. This approach significantly reduces the DAC's footprint while preserving its resolution.

The value of the attenuation capacitor is determined by the ratio of the total capacitance of the capacitors to its left to that of the capacitors to its right. This yields C_0 (1 unit) + C_1 (1 unit) + C_2 (2 units) + C_3 (4 units) + C_4 (8 units), divided by C_5 (1 unit) + C_6 (2 units) + C_7 (4 units) + C_8 (8 units), resulting in a capacitance ratio of $^{16}/_{15}$. In practice, this is implemented using 15 unit capacitors connected in parallel with one additional unit capacitor[1].

The bottom plate of each capacitor (except C_0) is connected to two cascading multiplexers (MUXs), which switch between the reference voltage (V_{ref}) and the minimum voltage (V_{min}). Selecting V_{ref} charges the capacitors, while selecting V_{min} discharges them. Unlike conventional textbook examples where capacitors are discharged to ground, V_{min} is used instead to maintain a required 0.1 V offset, achieved through a potential divider tapped from the power rails[2].

The lower MUX is controlled by the digital input code, while the upper MUX is governed by the EN pin, which is part of the system's reset circuitry. This configuration ensures a consistent sampled output by preventing residual charge accumulation. Additionally, the floating (top) plates of the capacitors are connected to transmission gates driven by the EN pin. During the first 800 μs of the sampling cycle, while the 8-bit shift register is being filled, the EN signal is high, discharging the capacitors. Once the shift register is fully loaded, the EN signal goes low, allowing the capacitors to charge according to the digital input code. Sampling occurs within 1 μs after the EN signal goes low, providing sufficient time for the analogue output to stabilise after a non-negligible settling time.

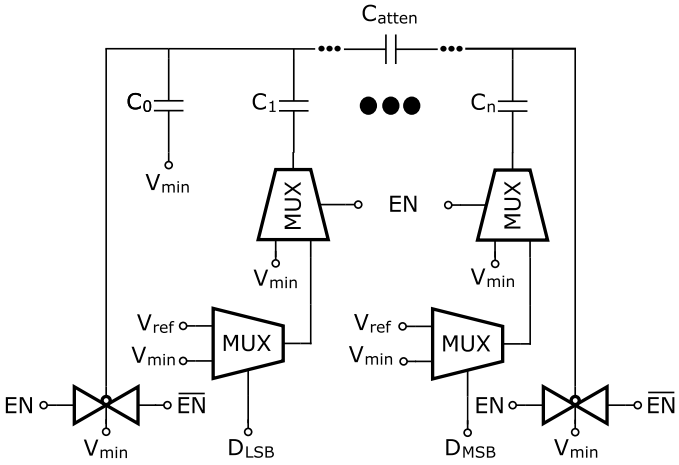

Fig. 2: Split-Array charge scaling DAC topology with bias-assisted discharge.

C. DAC Buffer

To maintain the DAC's specified linearity and output range, a rail-to-rail buffer is required. Figure 3 shows the design of a complementary differential-input op-amp used to achieve rail-to-rail buffering. This is accomplished using two single-stage op-amps operating in tandem: one formed by transistors

[1]The unit capacitance is 37.576 fF, corresponding to the maximum value available for a metal-insulator-metal capacitor (MIMCAP) in the 45nm GPDK library.

[2]Initially, the desired voltage range of 0.1 V to 1 V was set using the theoretical potential divider formula. However, this resulted in an INL exceeding 2 LSBs. To correct this, the resistor values in the potential dividers were fine-tuned iteratively until a satisfactory INL was achieved.

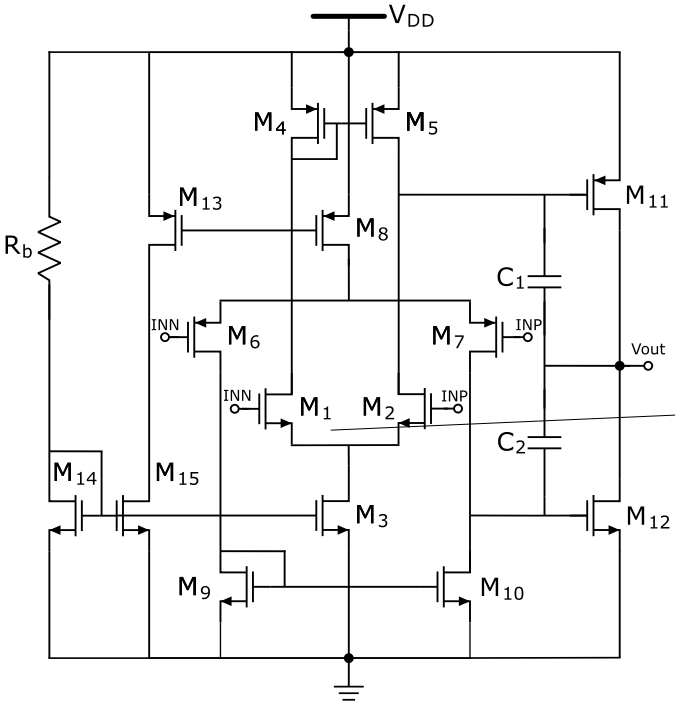

Fig. 3: Complementary differential input op-amp for DAC buffering.

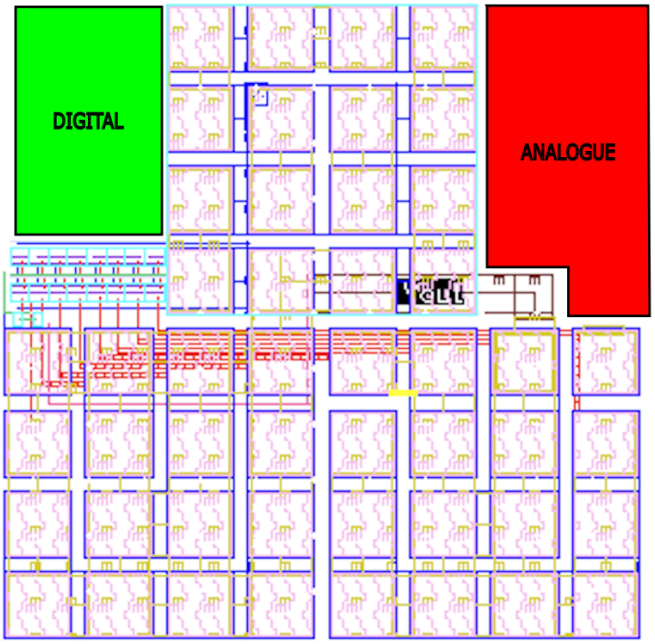

Fig. 4: Layout implementation.

M1, M2, M3, M4, and M5 (the NMOS input stage) and the other by M6, M7, M8, M9, and M10 (the PMOS input stage). Each stage drives its respective output transistor—M11 for the NMOS stage and M12 for the PMOS stage—ensuring a rail-to-rail symmetrical output swing. Additionally, transistors M13, M14, M15, and resistor R_b enable biasing for the tail transistors of the NMOS (M3) and PMOS (M8) differential pairs, while C1 and C2 function as miller compensation capacitors for improved stability.

D. Layout

The layout architecture, shown in Figure 4, features a compact $60\,\mu\text{m}^2$ footprint, with the charge DAC occupying the majority of the area. The digital section, comprising the serial-to-parallel converter, is positioned on one side, while the analogue section, containing the output buffer, is located on the opposite side. This separation minimises power supply coupling between the digital and analogue sections. Additionally, their placement at the two corners simplifies routing to the power rails.

Although the digital and analogue layout sections are still incomplete, the charge DAC layout section has been finalised and successfully verified through both Design Rule Checking (DRC) and Layout Versus Schematic (LVS) checks (see `charge_dac` layout in the submitted Design Files library). Furthermore, it can be deduced from the provisional layout that the DAC's footprint, once complete, is expected to be orders of magnitude smaller than the specified $0.5\,\text{mm}^2$ area constraint.

IV. Simulated Results

This section evaluates the DAC's linearity through DNL, INL, and output characteristic plots. Additionally, it examines the system's dynamic response, including propagation delay and settling time, as well as its static, dynamic, and average power consumption.

A. Linearity

Figure 5 and Figure 6 present the unsigned DNL and INL results, respectively, obtained by sweeping the digital input from the lowest to the highest bit value. The maximum DNL value is 1.1294, and the maximum INL value is 1.6159, indicating that the relative error remains within the specified 2 LSB limit.

Additionally, the output characteristics shown in Figure 7 indicate a minimum output voltage of $0.1046\,\text{V}$ and a maximum output voltage of $0.9943\,\text{V}$, both within the specified output range. The sampled output closely follows the ideal output transfer function, indicating that, in addition to exhibiting an adequate linear response, the overall behaviour is free from significant offset or gain errors.

B. Dynamic Response

Figure 8 illustrates the worst-case propagation delay and settling time obtained from the simulation results. The measured propagation delay is $4.3\,\text{ns}$, which is well below the $1\,\mu\text{s}$ specification. Similarly, the settling time of $150\,\text{ns}$ is shorter than the required propagation delay, indicating compliance with the specification.

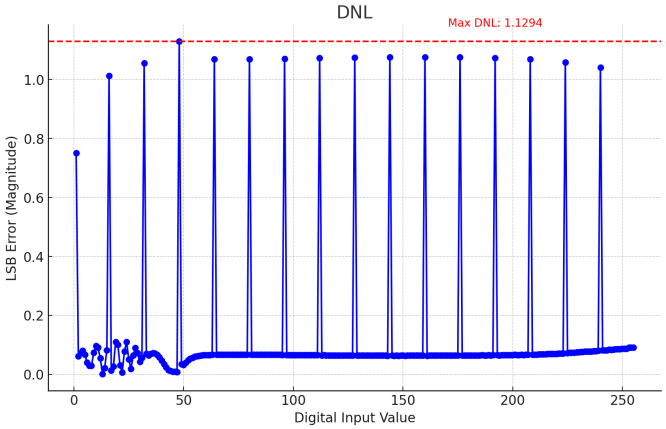

Fig. 5: Unsigned DNL results.

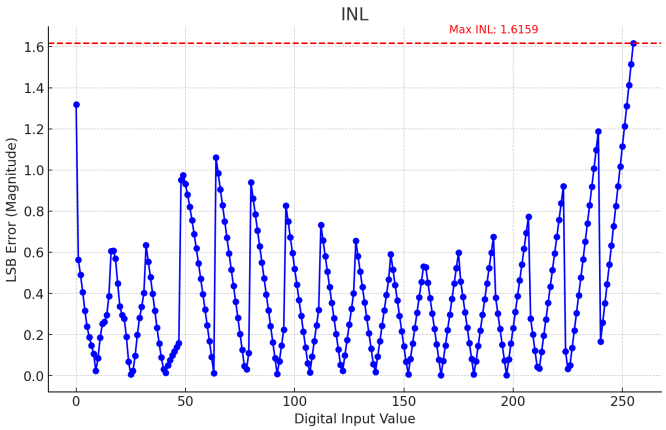

Fig. 6: Unsigned INL results.

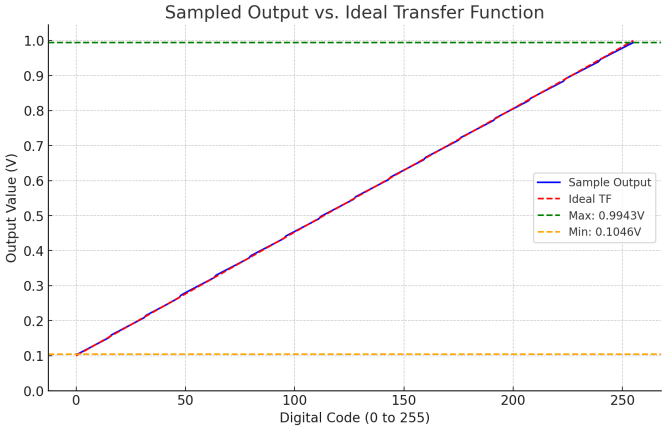

Fig. 7: DAC output vs. ideal transfer function for a given digital code input.

C. Power Consumption

Figure 9 presents the static, dynamic, and RMS power consumption of the DAC. The measured RMS power is $0.52\,\text{mW}$, while the static power is $0.18\,\text{mW}$. These values are within the specified power consumption budget.

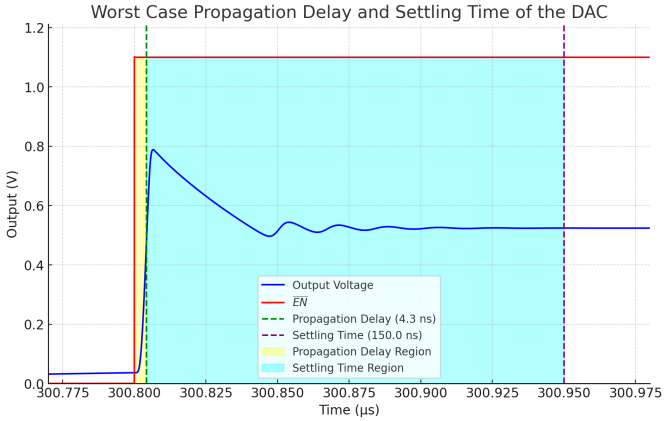

Fig. 8: Propagation delay and settling time of the DAC.

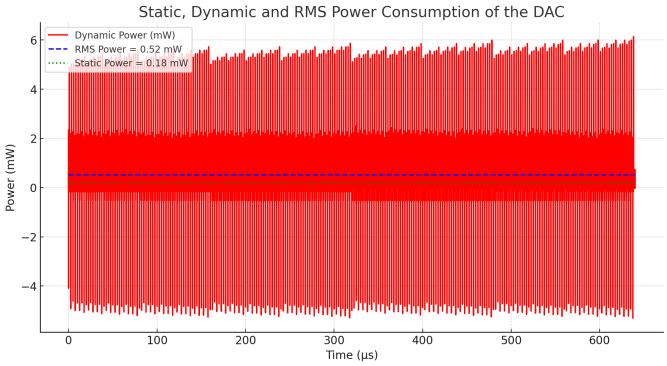

Fig. 9: Static, dynamic and RMS power consumption of the DAC.

V. Conclusion

An 8-bit split-array charge-scaling DAC was designed and implemented in 45nm CMOS technology, meeting specified performance targets. The chosen topology minimised power consumption and area while ensuring linearity. Key results include a maximum INL of 1.62 LSB, a maximum DNL of 1.13 LSB, an RMS power consumption of 0.52 mW, and a compact 60 μm^2 layout. The measured propagation delay of 4.3 ns and settling time of 150 ns met the required timing constraints. DRC and LVS verification confirmed the DAC's correctness and manufacturability.

Incorporating a voltage reference for V_{ref} and V_{min} that is independent of temperature and power supply could further improve the DAC's stability by reducing its sensitivity to environmental variations. The claims presented in this report can be verified by testing the `charge_dac_final` schematic in the submitted Design Files library.

References

[1] T. Constandinou, *Full Custom IC Design Lecture Notes and Panopto Recordings*. Department of Electrical and Electronic Engineering, Imperial College London, London, UK, 2024.