ATLAS ITk Electronics Specification
Component or Facility Name: ABCstar

Version: V 2.0a

Abstract

A brief description of the component being specified and where it will be used.

The ABCStar chip will be the front-end ASIC for the readout of the ITK Silicon Strips detector in the ATLAS experiment for the HL_LHC collider at CERN.

Revision History			
Rev. No.	***Proposed Date*** ***Approved Date***	***Description of Changes*** *(Include section numbers or page numbers if appropriate)*	***Proposed By: author*** ***Approved By: reviewer***
0.0	P: 08/15/2015 A:	Initial draft	P: F. Anghinolfi P: P. Keener P: M. Newcomer A: name
0.9a	P: 16/10/2015	Updated Commands Tables New paragraph 9.8.3 Register Readback Updated ClusterFinder with Cluster_Max insertion paragraph 9.7 Updated packet definition paragraph 9.9 Various syntax and terminology corrections This version is still incomplete as it does not contain a precise description of the L0sync and BCsync signals	P: F. Anghinolfi
1.0	P: 06/09/2016	Many changes, major changes are concerning New FrontEnd Specifications ESD additional information Power options L0_CMD new description L0_tag Trigger capabilities Pad ring Register Readback modes Register settings Intermediate buffer for contiguous L0	P: F. Anghinolfi
1.0a	P: 08/09/2016	Remarks from B. Gallop Addition with LCB mode	P: B. Gallop P: M. Warren P: P. Keener
2.0a	P: 21/01/2017	Major changes to insert the LCB protocol	P: F. Anghinolfi P: P. Keener

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1 Conventions and Glossary

1.1 Conventions

Signal names ending with the letter ‘b’ are active low, all other signals are active high, unless otherwise noted.

Hexadecimal numbers are noted either by prepended a ‘$’ character in front of them or using Verilog notation: <number of bits>’h<hexadecimal value>, eg (32’h0123beef).

1.2 Glossary

BC – Beam Crossing Clock, 40 MHz

BCR – Bunch Counter Reset. A 1-bit BC-synchronous command that resets the BCID counter to zero. Used to ensure front-end synchronization. It is issued through the LCB input.

L0 – Beam crossing synchronous pulse used to transfer the strips data from the fixed latency pipeline to the Random Access Memory (RAM) used as an event buffer (EvtBuffer). L0 does not generate an ABCstar readout.

L0_tag – 7 bits value attached to each L0. It is used to safely identify events with a single identifier number.

LCB – L0A/CMD/BCR protocol

L0ID Preset – An 8-bit short command to load the Local L0ID counter with a preset value from a register. Used only for the internal L0 counter**.**

LP – Low Priority Readout Request. An asynchronous request to read out an event with the given L0ID from the ABCstar Event Buffer with low priority (but still higher priority than Register Read requests).

PR – Priority Readout Request. An asynchronous request to read out an event with the given L0ID from the ABCstar Event Buffer with priority over LP and register read requests.

RCLK – Readout Clock. A 160 MHz clock from the HCCstar used to clock the serial output bit stream from the ABCstar.

lsb – Least Significant Bit. This is the bit in the 2^0 place.

msb – Most Significant Bit. This is the bit with the most value in the word.

2 Related Documents

TBD

3 Description of Component or Facility

The ABCStar ASIC must provide all functions required for processing of signals from 256 strips of a silicon strip detector in the ATLAS experiment employing a binary readout. The architecture chosen for the ABCStar allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, an

asynchronous Regional Readout Request (PR here) and a second level asynchronous data readout intended for a global readout (LP here). The design can be easily adapted to a single level readout (L0 readout mode) simply by not sending priority triggers.
The simplified block diagram of the chip is shown in figure 3.1. The main functional blocks are: front-end including threshold and calibration controls, power regulation, command decoder, Mask and Edge Detection, L0Buffer, EvtBuffer, Cluster Finder and Readout logic. The "Top_Logic" block controls the data path by interpreting the PR and LP trigger signals.

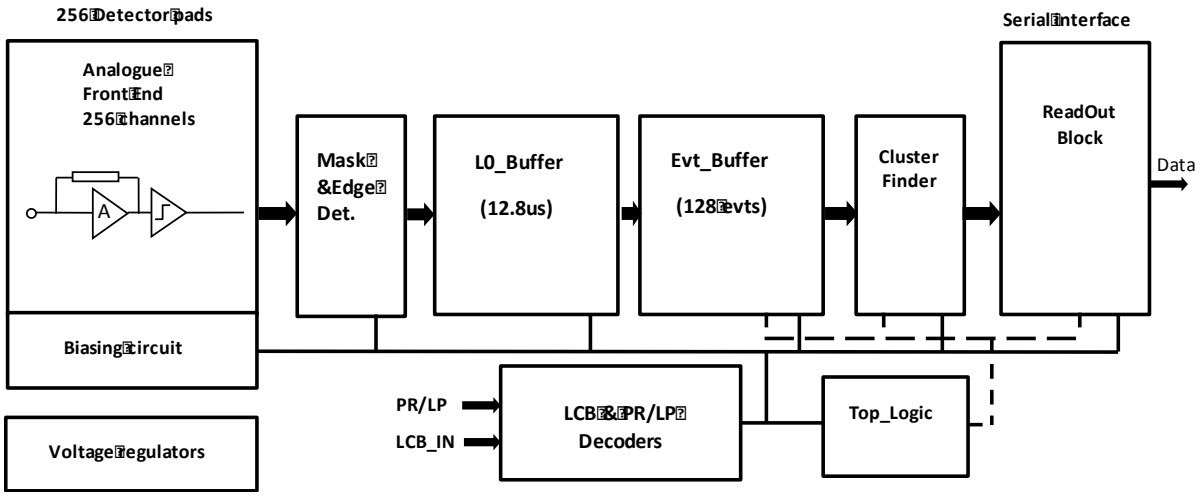


Figure 3-1 Block diagram of the ABCStar chip.

The front-end is optimized for 2.5cm strips [5cm strips] with 25ns shaping time, and a noise level below 1000 electrons after full radiation effects. The discrimination level should be lower than 1fC, possibly reaching 0.5fC. After discrimination, at each bunch crossing the binary outputs of the front-end channels are sampled and stored into the L0Buffer for a duration fixed by the (programmable) latency for receiving the L0 signal.
At each L0 reception the event with the correct latency is transferred to the EvtBuffer. It is maintained for an average duration corresponding to 128 L0 (128 us at 1MHz L0 rate) and tagged with an appropriate identification number (L0ID). If a PR or LP signals are received with the corresponding L0ID number, the event is processed through the Cluster Finder (CF). The CF block acts as a data reduction circuit, creating a "cluster" byte for channels found with hits. The expected average occupancy is of 2 [4 in case of 5cm strips] clusters per event. The Readout block does formatted packets with the event identification and the associated cluster bytes. The data is transmitted serially at 160Mb/s.

The LCB Decoder block receives and distributes internally the L0 trigger signals (L0, L0tag). Through the same LCB_IN input the chip receives the configuration commands (including resets), the analogue bias settings, the mask and test and calibration settings, the register read-back instructions. The signal BCR is also received for real time Bunch Crossing Reset.

The LP/PR input receives the LP and PR trigger signals. The Top Logic block is the autonomous sequencer that controls the data flow path according to the arrival of the L0, PR, LP trigger signals.

4 Interfaces

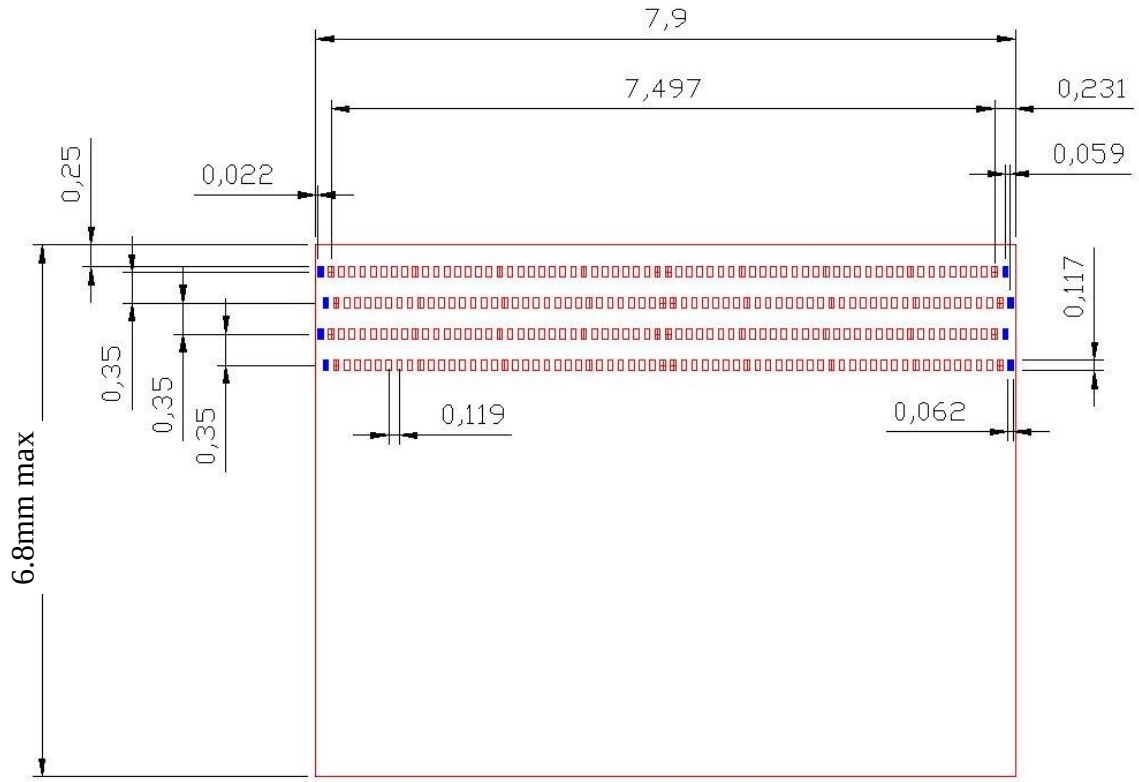
This component interfaces to the other components listed in .

Table 4.1: Components which Interface to This Component

Name of Component	Name of Component Specification
ITk Strip Sensor	TBD
Barrel Hybrid Board	TBD
Endcap Hybrid Board	TBD
HCC ASIC	TBD

5 Physical Description

The ABCSTAR chip will be 7.9 mm wide and to fit at best the input pads to the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors.
The pad size opening are 95um by 190um in the “digital and power” section and 62um by 117um for the pads to the detector.
The front-end pads (to detector) are arranged as shown on Figure 5-1, in 4 rows of 64 pads with a pitch of 119um. For the detector reference GND (HV decoupling and guardring) there are 2x 4 pads on both sides of the staggered input pads.



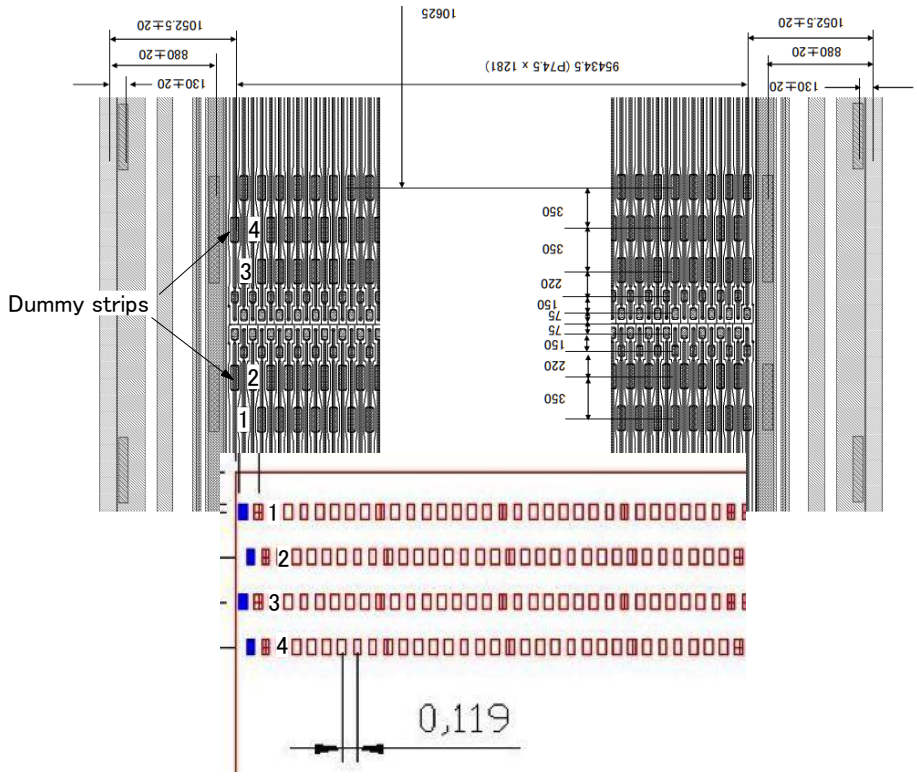


Figure 5-1 ABCStar detector pads arrangement

The other pads will be distributed approximately as shown on Figure 5-2 and Figure 5-3 as a reference. The front-end pads are shown at the right, the left edge has all I/O active signals and power pads, the top side is populated with specific pads that do not need to be bonded on hybrids.

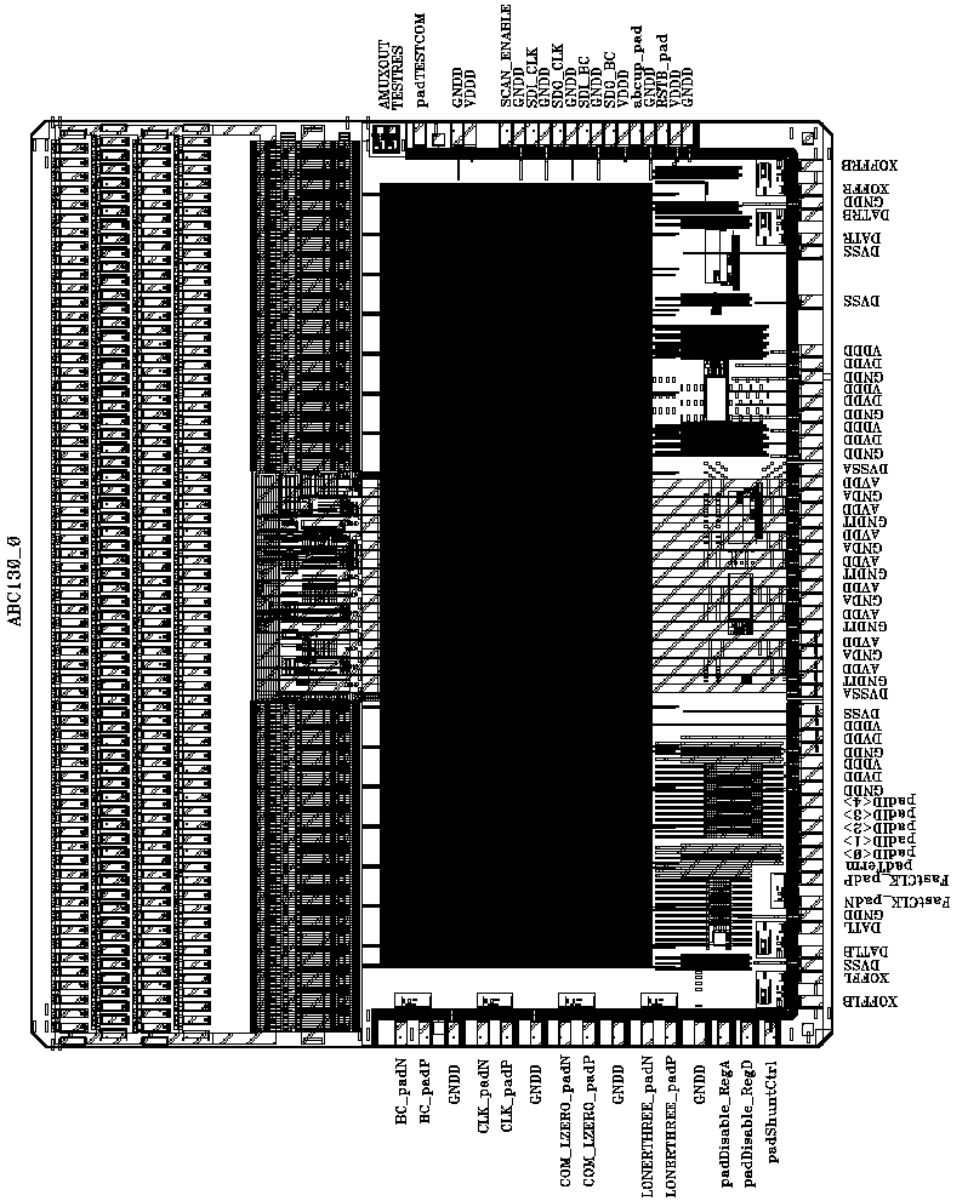


Figure 5-2 ABC130_0 Pads distribution, as a reference for the ABCStar Pads figure

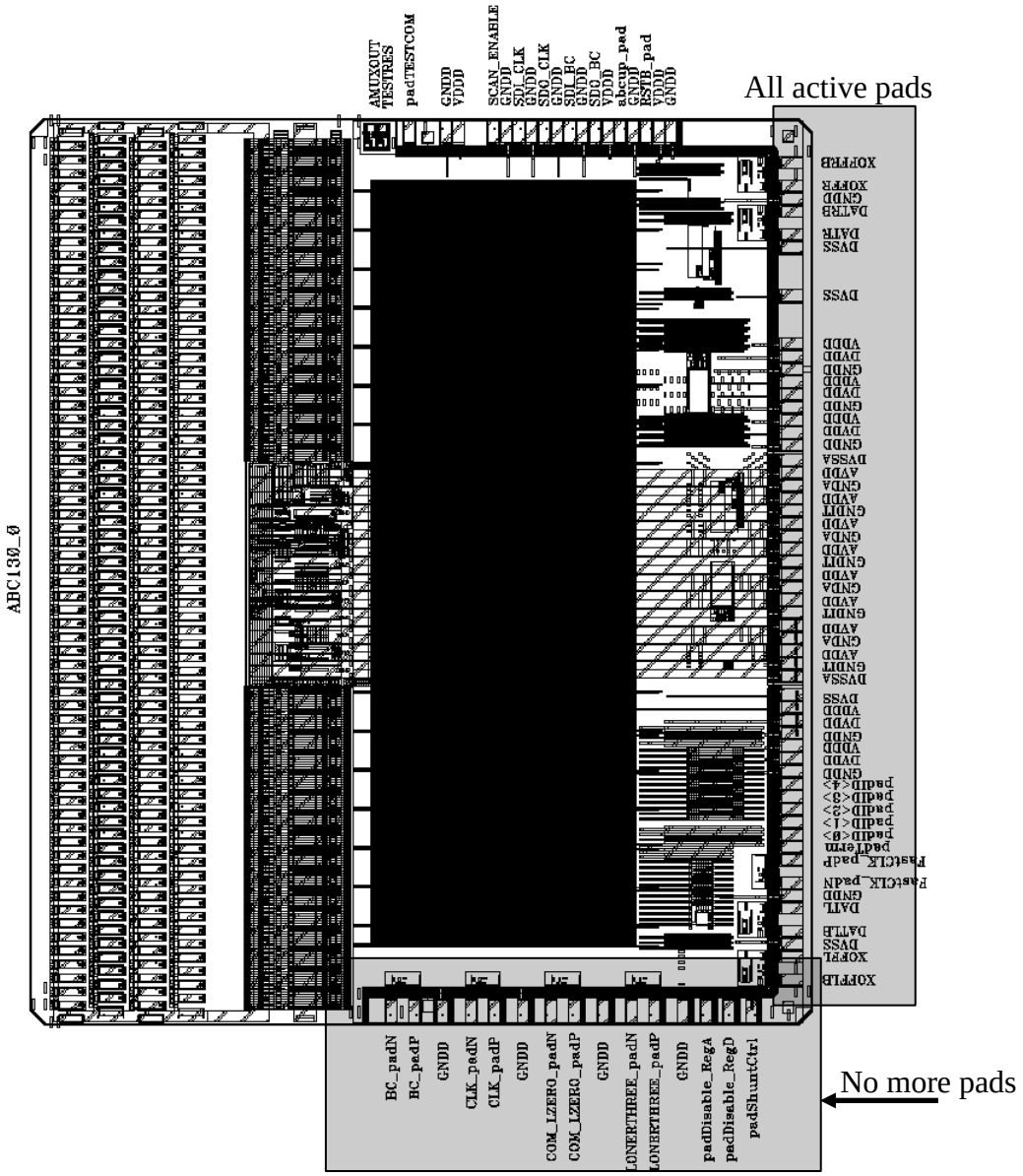


Figure 5-3 Indications for the ABCstar Pads distribution

A precise pin list is provided for the ABCStar design on the following Table 5-1:

	rate (MHz)	direction	Type		PullUp PullDown
module ABCSTAR (					
//right edge signals					
BC_padN	40	I	SLVS	40MHz clock input	
BC_padP	40	I	SLVS	40MHz clock input	
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
PRLP_padN	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)	
PRLP_padP	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
padDisable_RegD1	Static	I	CMOS Pull-Down	Disable Regulator (Digital)	0
padDisable_RegD2	Static	I	CMOS Pull-Down	Disable Regulator (Digital 1/2 pipeline)	0
padDisable_RegA	Static	I	CMOS Pull-Down	Disable Regulator (Analogue)	0
padTerm	Static	I	CMOS Pull-Down	SLVS Termination On/Off	0
GNDD		Power	Digital Ground	0V Digital Ground	0V
padShuntCtrl	Analogue	I	Analogue	Shunt Device Control (analogue signal)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
DVSSA		Power	ESD Return	0V Ground specific to ESD return	0V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
DVSSA		Power	ESD Return	0V Ground specific to ESD return	0V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
padID(0:3)	Static	I	CMOS Pull-up	Chip Address (4 pads)	1
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
LCB_IN_padN	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)	
LCB_IN_padP	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
CLK_padN	160	I	SLVS	Readout rate clock input	
CLK_PadP	160	I	SLVS	Readout rate clock input	
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
DATB	160	O	SLVS	DATA signal	
DAT	160	O	SLVS	DATA signal	
//from the detector (left)					
AIN[255:0]	40	I	Analogue	Inputs to FE channels	
//top edge signals					
RSTB_pad	40	I	CMOS Pull-up	External Hard Reset signal	1
abcup_pad		I	CMOS Pull-Down	Reserved	0
SDO_BC	MHz	I	CMOS 8mA	Output for CLK Scan Path chain	
SDI_BC	MHz	O	CMOS Pull-Down	Input for BC Scan Path chain	0
SDO_CLK	MHz	I	CMOS 8mA	Output for CLK Scan Path chain	
SDI_CLK	MHz	O	CMOS Pull-Down	Input for BC Scan Path chain	0
Scan_Enable	Static	I	CMOS Pull-Down	Enable Scan Path chains	0
padTESTCOM	Analogue	O	Analogue	Discriminator bias "spy" point	
TESTRES	Analogue	I	Analogue	Reference resistance	R
AMUXOUT	Analogue	O	Analogue	Analogue "spy" output	

Table 5-1 : Preliminary ABCStar Pads list

The list of pads on the “top edge” is not complete. In particular pads or eFuses will be added.

6 Manufacturer

The ABCStar will be fabricated in Global Foundry (Ex-IBM foundry) in the CMOS8RF_DM 130nm technology. The wafers are standard 8 inches and will be thinned to 200-320 um.
No packaging is foreseen
The design include the PROMPT circuits.

7 Power

The ABCStar chips can be supplied by a constant current source* or a voltage source. The internal supply voltages for the analogue or digital parts of the circuit are derived from the external voltages separately by two (or three) on-chip linear voltage regulators. Pulling up the Disable_RegA, Disable_RegD1 or Disable_RegD2† inputs to AVDD can disable the linear voltage regulators. Pads are provided to eventually feed the power to the chip directly from outside, not using the regulations circuits.
In case of a current source, the shunt regulator controlled with the ShuntCtrl analogue signal that is part of an external feedback loop circuit regulates the supply voltages for the analogue and digital parts of the circuit. Pulling down the padShuntCtrl signal to GND disables the shunt regulator. The shunt regulators must allow connecting their outputs in parallel on the hybrid even if the output voltages of the individual devices are not perfectly matched. It is required that devices with mismatch of output voltages within a range ±100 mV can be connected in parallel.

7.1 Shunt regulator‡

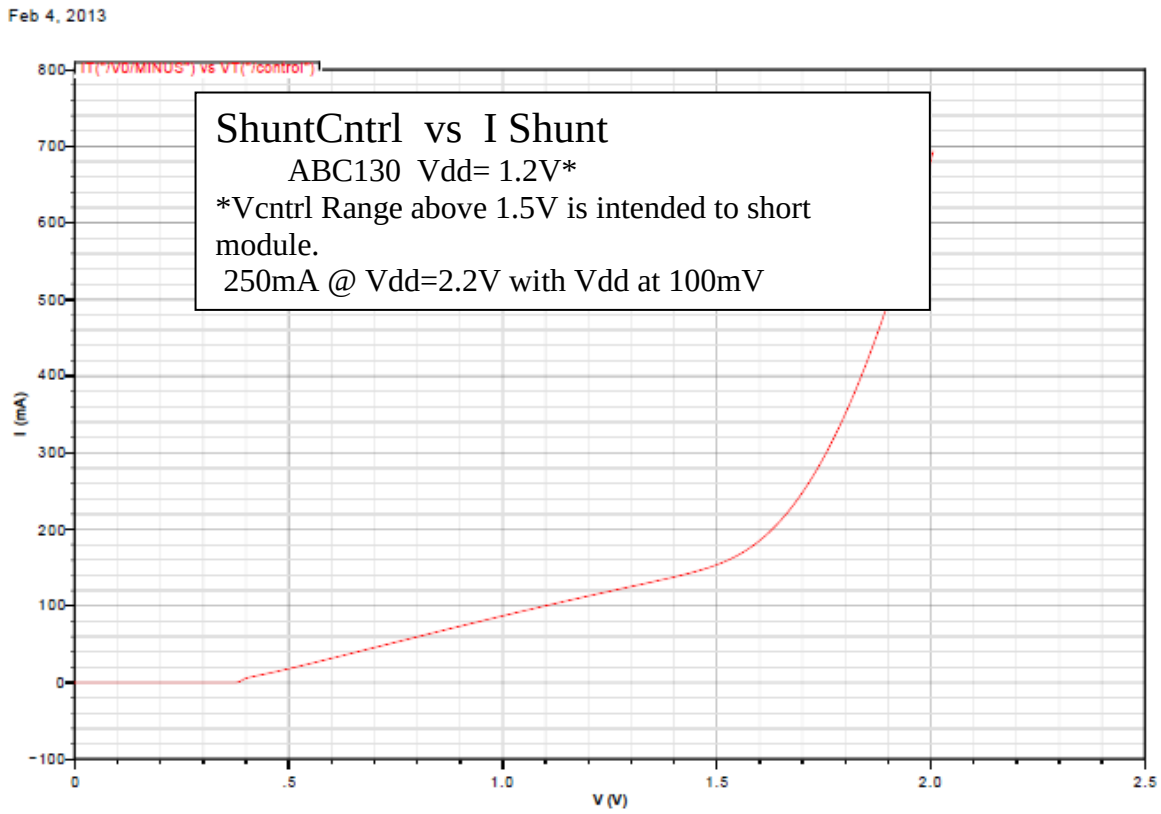
The shunt regulator is consisting of only the shunt power device. The input ShuntCtrl has to be connected to the feedback control circuitry outside of ABCStar to control it. The ABCStar Shunt block is intended to be controlled by the SPP ASIC that has a control range of up to 2.2V. If no control is provided, it is good practice to hard connect ShuntCtrl to GND, so that the shunt device cannot derive any current from the power supply.

		Min	Nominal	Max
Minimum shunt current	Ishuntmin	1uA	30mA@ShuntCtrl= .6V	150mA@ShuntCtrl= 1.5V
Internal shunt current limit	Ishuntlimit0	1uA	250mA@ShuntCTRL=2.2V with Vdd= 0.1V	
Disable inputs	ShuntCtrl		GND	

* In case this feature is maintained
† See 7.2.3 and 9.8.1
‡ In case this feature is maintained

Response Time (0-90%)	ShuntCntrl		75ns	

Table 7-1 : Shunt regulator specifications



7.2 Voltage Regulators

7.2.1 Analogue voltage regulator

		Min	Nominal	Max
Input Voltage	AVDD	1.25	1.5	1.6*
Output voltage	VDDA	1.15	1.2	1.25
Output current	IDDA		70mA	

Table 7-2 : Analogue voltage regulator specifications

The analogue voltage regulator provides the voltage to the front-end circuitry. It can be disabled by pulling up to AVDD the Disable_RegA input. In this case the front-end can be powered from an external voltage source connected to the analogue power pins VDDA and GNDA and GNDIT for the input branch).

* : 1.6V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time).

7.2.2 Main Digital voltage regulator

		Min	Nominal	Max
Input Voltage	DVDD	1.25	1.5	1.6*
Output voltage	VDDD	1.00**	1.2	1.25
Output current	IDDD		140mA	
Output Impedance			0.3 ohm	
Rejection Ratio				
Rejection Ratio with 100nF external capacitor				

Table 7-3 : Digital voltage regulator specification

This digital voltage regulator provides the voltage to all the digital circuitry in general. It can be disabled by pulling up to AVDD the Disable_RegD1 input. In this case the digital part of the chip can be powered from an external voltage source connected to the digital power pins VDDD and GNDD.
* : 1.6V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time).
** : 1.0V is the low range limit of the voltage regulator output : it does not mean that the chip is guaranteed to operate with this low voltage during its lifetime, especially because of the radiation effects.

7.2.3 Secondary Digital voltage regulator (option in the case of a segmented L0Buffer)

		Min	Nominal	Max
Input Voltage	DVDD	1.25	1.5	1.6*
Output voltage	VDDD2	1.00**	1.2	1.25
Output current	IDDD2		140mA	
Output Impedance			0.3 ohm	
Rejection Ratio				
Rejection Ratio with 100nF external capacitor				

Table 7-4 : Digital voltage regulator specification

This digital voltage regulator provides the voltage to the half of the pipeline (L0Buffer) circuitry. It can be disabled by pulling up to AVDD the Disable_RegD2 input. In this case the digital part of the chip can be powered from an external voltage source connected to the digital power pin VDDD2 and GNDD.
* : 1.6V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time).

** : 1.0V is the low range limit of the voltage regulator output : it does not mean that the chip is guaranteed to operate with this low voltage during its lifetime, especially because of the radiation effects.

7.2.4 Core Voltages

The DC supply voltages requirements as defined below apply to the core of the ABCStar chip and will be delivered either from the internal on chip power management circuitry or from the external power sources via bond pads.

	Pad Name	Min	Nominal	Max	Absolute Max
Analogue Supply*	VDDA	1.15	1.2	1.25	1.6
Analogue Ground	GNDA		0		-0.3
Digital Supply#	VDDD/2	1.00**	1.2	1.25	1.6
Digital Ground	GNDD		0		-0.3

Table 7-5 : DC supply voltages

* DC supplies are the one applied to the analogue circuits, from either an output source or from the internal analogue voltage regulator.
# DC supplies are the one applied to the digital circuits, from either an output source or from the internal digital voltage regulator. For the on chip power-up reset to operate correctly the VDD power supply must be ramped up to 90% of its final value in less than 10 ms.
** : 1.0V is the low range limit of the voltage regulator output : it does not mean that the chip is guaranteed to operate with this low voltage during its lifetime, especially because of the radiation effects.

The current draw at each DC input is as follows (values excluding the regulators current).

		Min	Nominal	Max
Analogue Supply	VDDA		66mA	
Analogue Ground	GNDA			
Digital Supply, Main regulator	VDDD		33mA*	
Digital Supply, secondary regulator	VDDD2		2mA*	
Digital Ground	GNDD			

Table 7-6 : DC supply currents for the nominal voltage supplies (VDDA=1.2V, VDDD=1.2V) and nominal operating conditions

* These are the nominal values after configuration. The values may change with configuration, and are increased by a factor 1 to 3 when the TID dose is between 1 and 10Mrad.

		Min	Nominal	Max
Analogue Supply	VDDA			
Digital Supply	VDDD			

Table 7-7 : Absolute Min/Max current draws at power supply inputs which may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips

The expected typical power consumption for nominal bias power supply voltages and bias currents: <1 mW/channel*.

8 Input/Output

Parameter	Conditions	Minimum	Maximum
Input Voltage Range Vi		0	Vdd
InputVoltage Common mode Vicm		0.2V	1.0V
Effective Input Offset	MC result	0V	+/-10mV
Common mode resistance to Vdd/2	Termination On	450 Ω	550 Ω
Receiver input impedance	Termination ON Termination OFF	75Ω >1Meg	82 Ω

Table 8-1 : Input Levels for SLVS Inputs (CLK, BC, CMD-L0, PR-LP)

Parameter		Minimum	Maximum
Output Current	8 programmable steps	1mA	7mA
Output offset Voltage	Symmetric Drive		0
Output Differential Voltage	With 75 Ω Termination	75mV	520mV
Output impedance		k Ω	

Table 8-2 : Output Levels for SLVS Outputs (DAT)

* A design target : this limit should be cross checked against the additional leakage current in the 1-6Mrads range due to the TID effects.

8.1 Input/Output ESD protections

The inputs that are connected to a multidrop line (clocks, L0CMD, LPPR) may use specialized ESD structures based on a SCR protection device[*].

The protection should stand a 2kV HBM (Human Body Model) event and a 100V Machine Model (MM). One of the characteristics[†] of this ESD device is its low capacitance, well below the values of the standard ESD protections of the foundry.

The SLVS outputs (DAT, DATB) may also use SCR devices if it is provided as an option.

9 Detailed Functional Description and Specification

9.1 Detector parameters

The design of the ABCstar will be optimised for performance with short strips. The post-radiation parameters of the different types of sensors, as understood presently, combined with the estimated parameters of the front end, are summarised in Table 9-1.

[*] SOFICS BVBA, Belgium
[†] Exact value to be defined

	Endcap Ring 0 F = 1.61e15	Endcap Ring 1 F = 1.35e15	Endcap Ring 2 F = 1.19e15	Endcap Ring 3 F = 1.10e15	Endcap Ring 4 F = 0.97e15	Endcap Ring 5 F = 0.87e15	Barrel Short Strips F =	Barrel Long Strips F = 0.57e15 neq/cm^2
Coupling type to amplifier	AC						AC	
Readout strip implant	N						N	
Strip pitch	77.2 µm	71.3 µm	76.8 µm	73.6 µm	77.0 µm	77.7 µm	74.5 µm	
Strip Length	1.9 cm	2.4 cm	3.1 cm	2.9 cm	5.4 cm	5.0 cm	2.4 cm	4.8 cm
Coupling capacitance to amp	45.6 pF	76.5 pF	75.0 pF	69.8 pF	130.7 pF	120.3 pF	57.3 pF	114.5 pF
Sensor capacitance of strip to all neighbour strips	1.59 pF	2.15 pF	2.62 pF	2.52 pF	4.56 pF	4.17 pF	1.96 pF	3.91 pF
Sensor capacitance of strip to backplane	0.59 pF	0.75 pF	0.97 pF	0.90 pF	1.69 pF	1.55 pF	0.74 pF	1.48 pF
Possible added capacitance due to gluing hybrid to sensor	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF
Total Load Capacitance ~ENC_{serial} @bias 80/160uA	2.18-2.68 pF	2.90-3.40 pF	3.59-4.09 pF	3.42-3.92 pF	6.25-6.75 pF	5.72-6.22 pF	2.70-3.20 pF	5.39-5.89 pF
Metal strip resistance	57 Ω	72 Ω	94 Ω	87 Ω	163 Ω	150 Ω	72 Ω	143 Ω
Bias Resistor	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ
Max leakage current per strip for shot noise and shot noise estimation	121-134 nA	118-131 nA	145-161 nA	120-133 nA	206-229 nA	171-190 nA	96-106 nA	100-113 nA
Collected charge (at 500 V), estimate from neutrons (conservative), [ke-]	8.6	9.4	9.9	10.3	10.8	11.3	10.4	13.1
Collected charge (at 500 V), estimate from charge/neutral mix, [ke-]	9.5	10.3	10.8	11.1	11.6	12.0	12.3	14.4
Estimates for total noise @bias 80-160uA & max. detector leakage								
Maximum threshold assuming 50% charge division, 10% overdrive and Landau most probable/min) S/T >3.4	2800e-	3030e-	3180e-	3260e-	3410e-	3530e-	3620e-	4230e-
Maximum noise assuming 4 sigma distance to threshold	700e-	750e-	790e-	810e-	850e	880e-	900e	1050e-
Proposed threshold & threshold/noise separation [1]								

Table 9-1 : Assumed detector electrical parameters

9.2 Front-end

9.2.1 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

9.2.2 Input Characteristics:

Input Signal Polarity: The front-end circuit accepts negative signals from n-type strips

Crosstalk: (via detector interstrip capacitance)

The crosstalk should stay below 5% in the nominal biasing conditions with the maximum strip length (5.4cm)

Input Protection:

The front-end input is protected with a specially developed ESD structure* using a SCR protection device. A simplified schematic is reproduced in figure

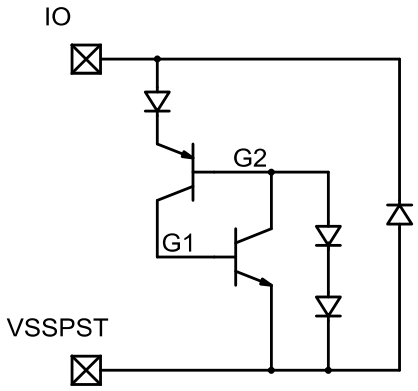


Figure 9-1: Frontend Input ESD protection

The equivalent capacitance loading to the front end input should be around 0.1pF. The protection should stand a 1kV HBM (Human Body Model) event and a 100V Machine Model (MM). The characteristics† of this ESD device are a low trigger voltage and a low holding voltage, well below the values of the standard ESD protections of the foundry. The very low Ron (below 1ohm) should help to sustain charge deposition that occurs in case of detector breakdown.

Open Inputs: Any signal input can be open without affecting performance of other channels.

9.2.3 Preamplifier-Shaper Characteristics

Gain at the discriminator input: 95 mV/fC for the nominal bias currents and the nominal process parameters

Effective gain extracted from the response curve:
90 mV/fC for the nominal bias currents and the nominal process parameters

Linearity: better than 5% in the range 0 – -4 fC
better than 15% in the range 0 – -8 fC

Peaking time: 20 ns
Intrinsic peaking time of 20 ns of the circuit ensures a peaking time below 25 ns including the effect of charge collection time.

Noise: See Table Table 9-1 for maximum RMS noise allowable on fully populated modules after irradiation.

Gain Sensitivity to analogue supply voltage for 1 fC signal: < 1%/100mV

* SOFICS BVBA, Belgium
† Exact values to be defined

Power Supply Rejection Ratio :
(not design targets but simulation results of the circuit)

Strip length [cm]	2.4	4.8
10Hz-10kHz	57dB	57dB
10kHz-1MHz	17dB	16.5dB
1MHz-10MHz	6dB	6dB
10MHz-100MHz	3.5dB	3dB

Table 9-2 : Power Supply Rejection Ratio

Comparator Stage:
A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal 8-bit DAC (bits BVT<0:7>).
Threshold setting range: 0V to -590mV, nominal setting at -90mV (-1fC) before irradiation and as low as -45mV (-0.5 fC) after full dose.
Test MUX output: TEST_THDAC MIN/MAX = 2mV/133mV
Threshold setting step without trimming: 2.3mV (8-bit resolution)
Threshold spread before trimming: < 15 mV RMS

The range of 5 bit trim DACs inside the channel is controllable with 5-bit DAC (bits BTRANGE<0:4>).
TrimDAC threshold setting range MIN/MID/MAX 50mV/150mV/255mV (controllable with 5 bit DAC)
TrimDAC resolution MIN/MID/MAX 5 bit (step 1.55mV/5mV/8mV)
TEST_TRDAC MIN/MID/MAX 36mV /95mV/150mV

9.2.4 Timing Requirements:

Time walk: ≤ 16 ns.
This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer time walk assignment to the rising edge of the shaped signal.
Time walk defined:
For non-irradiated detectors; the maximum time variation in the crossing of the time stamp threshold over a signal range of -0.75 to -10 fC, with the comparator threshold set to -0.5 fC;
For non-irradiated detectors time walk is in the range of 12.5ns
For different cases of irradiated detectors please refer to Table 9-1.
Double Pulse Resolution: ≤ 75 ns for a -3.5 fC signal followed by a -3.5 fC signal at -0.5fC threshold
Max recovery time for a -3.5 fC signal following -80 fC signal: 200ns

9.2.5 Calibration circuit

Calibration signal distributed with one calibration line can be applied to on-chip calibration capacitor (60fF) connected to front end input with CMOS switch controlled with one of the

channel configuration bit. Address and the number of connected channels to the calibration line, as well as the amplitude of the calibration signal and its delay is set via the control logic. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal 8-bit DAC*. The calibration line is also brought through analog test mux to pad where the calibration voltage can be directly measured during the screening of the chip (analog test mux address 12).
A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods is provided. The delay is built in chain of delay cells designed with current starved inverters and it is controlled with 6-bit register (bits STR_DEL<0:5>). The absolute delay magnitude is obtained by the calibration delay scans using known BC period with high input signals and low discriminator threshold. In order to compensate for the process variation a 2 bit register to set the range of the strobe delay is provided (bits STR_DEL_RANGE<0:1>). For nominal corner of the technology process, the following delays of the calibration strobe can be obtained:

STR_DEL_RANGE =00	strobe disabled
STR_DEL_RANGE =01	delay 0 to 50ns
STR_DEL_RANGE =10	delay 0 to 60ns
STR_DEL_RANGE =11	delay 0 to 80ns

Calibration Capacitors: 60 fF ±10% (3 sigma) over full production skew, ±1% (3 sigma) within one chip.
Calibration signal:

amplitude range:	0 – 150 mV	(charge range: 0 – 9 fC)
amplitude step:	0.586 mV	(charge step: 0.035 fC)

Absolute accuracy of amplitude: to be calibrated during chip preselection.
Calibration DAC is controlled through bits BCAL<0:7> of the control registers.

9.2.6 Biasing circuitry and output test multiplexer

The preamplifier input transistor and feedback bias currents are controlled by the internal 5-bit DAC converters referenced to the internal bandgap circuit. The predicted variation of the bandgap reference is of the order of +/- 40mV pk-pk over 592mV nominal value. In order to compensate for the variations of the bandgap reference voltage as well as for the variation of the resistors setting the bias currents, the internal bias reference generators can be calibrated with 5-bit DACs.

The part below is not accurate anymore and will be updated during the biasing block design phase. The main changes are:

IFEED current disabled
IPRE is fixed by design (140uA nominal in the input transistor)

To adjust internal bias for voltages VCS, VCD, VCSP, VBASE and VB one should set bits BVREF<0:4>. For nominal technology parameters BVREF=01101† should give TEST_VR =50mV (nominal).

* A 10-bit DAC is an option that will be envisaged at the frontend design fix
† In all cases bits given in the order <MSB…LSB>

To adjust internal bias for bias current generators (IPRE, IFEED, and many others internal currents) one should set bits BIREF<0:4>. For nominal technology parameters BIREF=01101 should give TEST_IR =50mV (nominal).
To adjust internal bias for 8-bit threshold and calibration DACs one should set bits B8BREF<0:4>. For nominal technology parameters B8BREF=01101 should give TEST_R8B =50mV (nominal).
~~Two bias currents can be set to the desired operating point;~~
~~IPRE (preamplifier input transistor bias), register bits: BIPRE<0:4>~~
~~Nominal value (half DAC range - 10000): 110uA~~
~~MIN/MAX (00000/11111): 80uA/140uA~~
~~Test MUX output: TEST_IPRE MIN/NOM/MAX = 90mV/123mV/155mV~~
~~IFEED (preamplifier feedback transistor bias), register bits: BIFEED<0:4>~~
~~Nominal value (MSB-LSB 01001): 300nA~~
~~MIN/MAX (00000/11111): 160nA/600nA~~
~~Test MUX output: TEST_IFEED MIN/NOM/MAX = 16mV/30mV/65mV~~
ICOM (comparator bias), register bits: BICOM<0:4>
Nominal value (MSB-LSB 10000): 9uA
MIN/MAX (00000/11111): 5uA/13uA
Test output (activated by bit control BTMUXD):
TESTCOM MIN/NOM/MAX = 20mV/36.5mV/52mV

9.2.7 Test multiplexer

For testing purposes the front end block is equipped with analog test multiplexer which is controlled through configuration registers. It connects the test points located in the bias block through switches to common line connected to the output pad.
Analog test MUX:
The list below is not accurate anymore and may be updated during the frontend block design phase.
Address 0 → TEST_TRDAC
Address 1 → TEST_VR (nominal value =50mV → to be adjusted with BVREF<0:4>)
Address 2 → TEST_IR (nominal value =50mV → to be adjusted with BIREF<0:4>)
Address 3 → TEST_R8B (nominal value =50mV → to be adjusted with B8BREF<0:4>)
Address 4 → TEST_IPRE
Address 5 → To be defined
Address 6 → VCS (VCS bias voltage → nominal value 900mV)
Address 7 → VCD (VCD bias voltage → nominal value 600mV)
Address 8 → VCSP (VCSP bias voltage → nominal value 600mV)
Address 9 → VBASE (VBASE bias voltage → nominal value 500mV)
Address 10 → VB (VB bias voltage → nominal value 450mV)
Address 11 → VBG (bandgap voltage → nominal value 592mV)
Address 12 →CALLINE (calibration line)
Address 13 → TEST_THDAC (test point of the threshold DAC)
The access to the analog multiplexer is through the passive analog pad AMUXOUT. The access to the test point of the DAC used for bias of the discriminator (supplied with digital power domain) is at the pad TESTCOM.

9.2.8 Internal Bias, voltage and temperature monitoring

For monitoring purposes the ABCStar chip has an internal 10 bits ADC that connects through an analog multiplexer to the front-end bias block, to the bandgap references, raw and regulated voltages, and to a temperature sensor. The analog multiplexer connection is controlled through 5 bits of the ACDS register $04. When enabled, the ADC is free-running, at a sampling frequency of approx. 1.2KHz. The ADC operation can be enabled/disabled (clock switched off and reduced bias) with the bit 0 of the ADCS Register $04. The default value is disabled with zero value. The 10 bits outputs of the ADC are latched in each conversion cycle into the status register at address $32, together with the 5 bit identifying the analog multiplexer selection.

Monitor	Exp. Range	MUX 5 bits setting, in ADCS Register $04	Index (in Status Register $32)
AGND (Local GND)		$00 (default)	$00
TEST_TRDAC		$01	$01
TEST_VR		$02	$02
TEST_IR		$03	$03
TEST_R8B		$04	$04
TEST_IPRE		$05	$05
VCS		$06	$06
VCSP		$07	$07
VBASE		$08	$08
VB		$09	$09
VBG (analogue)		$0A	$0A
CALLINE		$0B	$0B
TEST_THDAC		$0C	$0C
VBG (digital)		$0D	$0D
AVDD (raw)		$0E	$0E
VDDA (regulated)		$0F	$0F
DVDD (raw)		$10	$10
VDDD (regulated)		$11	$11
DGND (GND in digital)		$12	$12
Temperature		$13	$13

Table 9-3: Internal ADC analogue MUX control (greyed signal names may be modified in relation with 9.2.7)

The ADC range and resolution is fixed by a range adaptor that connects to the bandgap reference voltage of the front-end bias. Three bits Mon_Sw100, Mon_Sw80, Mon_Sw60 (bits 1 to 3 of register $04) can be set to adapt the ADC range and resolution according to the following table:

	Range	Resolution	
Mon_Sw100 = 1 Mon_Sw80 = 0 Mon_Sw60 = 0	0-1.25 V	1.25mV	The ADC range is limited below 1.2v
Mon_Sw100 = 1 Mon_Sw80 = 1 Mon_Sw60 = 0	0-1.0 V	1.00mV	
Mon_Sw100 = 0 Mon_Sw80 = 0 Mon_Sw60 = 1	0-0.75 V	0.75mV	
Mon_Sw100 = 0 Mon_Sw80 = 0 Mon_Sw60 = 0	0-1.5 V Default	1.5mV	The ADC range is limited below 1.2v

Table 9-4: ADC range and resolution at nominal bandgap value VBG=600mV

9.3 Channel Order and Channel Numbering

Channels identification in data packets are using numbers 0 to 127 attributed to “one row” of a strip detector (barrel like geometry) and numbers 128 to 255 to “another row” of the detector.
Therefore 134 and 135 are adjacent strips of the second row, 254 is the last but one strip of the second row while 1 is the second strip of the first row (128 can not be adjacent to 127 …).
The arrangement of the wire bonds from the detector to the input pads of the front-end channels is reported here for the barrel case.
The order in which the front-end channels are physically placed and connected to the detector strips is described in Table 9-5:

ABC channel number (0 to 255) in data packet	FE channel number in calibration, threshold, hit counter and mask setting registers	FE channel physical order from bottom to top of the layout	Detector strips row (2 rows with strips 0 to 127, row 1 and row2)
0	0	0	0 in row1
1	1	1	1 in row1
128	128	2	0 in row2
129	129	3	1 in row2
..	..	..	..
126	126	252	126 in row1
127	127	253	127 in row1
254	254	254	126 in row2
255	255	255	127 in row2

Table 9-5: Channel numbering convention

9.4 Clock and Control Signals

The table below defines the ABCStar control signals.

Name	Type	Description
RCLK	SLVS	160MHz Clock input primarily intended for Data Readout
BC	SLVS	Beam Crossing Clock at 40MHz
LCB_IN	SLVS	160Mb/s, L0 Synchronous Trigger, L0_tag, CMD and BCR bits (framing and encoding mechanism described in paragraph 9.5)
LP_PR	SLVS	80Mb/s, PR with BC falling edge, LP with BC rising edge

Table 9-6: Clock and Control Signals

RCLK - The readout clock is used to clock data out of the chip. It runs at 160 MHz. This clock will be precisely phase shifted, under control of the HCCstar ASIC, with respect to BC to provide optimal operation.

BC - This is the primary clock delivered through the stave that samples the analogue channels outputs. The BC clock will be delayed by an arbitrary amount with respect to the incoming stave clock to accommodate a hybrid wide phase shift to align sensor signals with the BC.

LCB - The four signals L0, L0_tag, BCR and CMD are synchronized to the RCLK 160MHz clock : 16 bits are framed within 4 BC duration, that delivers to the chip: the L0s and the (one to four) BCs to which they belong, the L0_tag for the first L0, then one bit of the CMD frame, or the Bunch-Crossing Reset signal and the BC to which it belongs.

The L0, BCR and command data are encoded using 6b8b and sent at 160 Mbps. A single unit is a frame consisting of two 8-bit symbols covering 4 BC, giving a payload of 12 bits plus four control codes (K0, K1, K2, K3). When there are any L0 with the 4 BC, a L0 frame is sent indicating which of the 4 BC have L0 plus the L0_tag for the first L0. The L0_tags for subsequent L0 in that frame are increments from the sent L0_tag. Frames are required to be aligned with the LHC orbit signal, fixing the position of the BCR signal within the 4 BC covered by the frame. If a BCR is covered by a frame, a bit is set in the payload. The full description of the LCB protocol is given in paragraph 9.5.

LP_PR - This 80Mb/s time is comprised of two time multiplexed 40Mb/s components:
PR - The Priority Request (PR) signal is delivered on one phase of the BC clock and has two fields and a length of 11 bits : 3 bits act as start bit pattern (101), followed by 8 bits containing the L0ID identifier of the event to retrieve in the EvtBuffer. The idle state between consecutive PR commands is zero with at least one zero separating 2 consecutive PR.
LP- The Low Priority Request (LP) signal is delivered on one phase of the BC clock and has two fields and a length of 11 bits : 3 bits act as start bit pattern (110), followed by 8 bits containing the L0ID identifier of the event to retrieve in the EvtBuffer. The idle state between consecutive LP commands is zero with at least one zero separating 2 consecutive LP.

9.5 LCB Protocol at ABC input

The LCB control stream received by the HCCStar chip is transmitted to the ABCStar with minimal added latency. The only modification to the LCB stream operated by the HCCStar is when the HCC ID specified in the K2 frame of a command sequence (see below) do not match the HCCStar ASIC's HCC ID. In this case, the K2 frame payload symbol is replaced with the symbol ('11110') that prevents the ABCstar ASIC's LCB decoder to execute the command.
The basic unit of data transmission is a pair of 6b8b encoded symbols called a frame, providing 12 bits of payload per frame after decoding. Since the LCB signal is transmitted at a data rate of 160 Mbps, a single frame takes 100 ns, or 4 BC, to transmit.

L0 frame: This single frame sequence contains the L0A activity information for the 4 BC of the frame. With an L0A, a 7-bit identifier, called the L0tag, is sent. This identifier is used to request event data from the ABCStar. In addition, the BCR signal may come during a 4 BC space that has L0As. The payload for an L0 frame is shown in Table 9.7. The msb of the L0A mask refers to the earliest BC, while the lsb refers to latest. A '1' in the L0A mask indicates that there is an L0A in the corresponding BC. A '1' in the BCR field indicates that there is to be a BCR in the latest BC covered by the L0A mask. It is important to note that

this implies that frames must have a fixed alignment with respect to the LHC orbit signal in order to guarantee that the BCR is executed at the front-end at the appropriate time.

	MSB		LSB
Field Name	BCR	L0A mask	L0tag
# of bits	1	4	7

Table 9.7: LCB L0 Frame

L0 frames are only sent when at least one of the covered BC has an L0A or a BCR needs to be sent. Therefore, at least one of the first five bits will be '1'.

Fast commands frame: Fast commands and resets are sent in a single frame that contains the 6b8b control symbol K3 plus a symbol whose payload is composed of a 2-bit BC selector indicating in which BC the command or reset is to be generated and a 4-bit action, indicating which command or reset to generate. A value of 0 for the BC selector refers to the earliest BC, while a value of 3 refers to the latest. The payload for the second symbol is shown in Table 9.8. The list of actions (fast commands) for the ABCStar chip is shown in Table 9.9.

	MSB	LSB
Field Name	BC Select	Action
# of bits	2	4

Table 9.8: K3 Frame Payload

Index	Command
0	
1	
2	SYS Reset
3	Soft Reset
4	SEU Register Reset
5	Cal Pulse
6	Digital Pulse
7	Hit Count Reset
8	Hit Count Start
9	Hit Count Stop
10	

Table 9.9: Actions (Fast Commands)

Register command frames: Register reads and writes are composed of a sequence of frames (registers commands). These frames do not need to be consecutive, but must be in order. Frames interleaved in a register command sequence may be of any type. Note, however, that attempting to start a new command sequence while in a middle of such a sequence for any other HCCStar or ABCStar chip under the same LCB stream is not allowed and may produce undefined behavior*. The correct method for aborting a command sequence is described below.

A register command sequence starts with a frame composed of the K2 control symbol followed by a symbol depicted in Table 9.10, containing in first position the ABC/HCC bit. If the ABC/HCC bit is '1' the command is an ABCStar command otherwise it is an

* This should be reworked to define of a proper behavior in case of a wrong sequence

HCCStar command and the instructions for registers are ignored. Next is the Start/End bit: at '1', it identifies the start of a command sequence. If the 4 next bits has the Special HCC ID (1110), the command is discarded and no operation is executed. However, if the HCC ID is any other value, the command decoder proceeds through the next frames.

	MSB		**LSB**
Field	ABC/HCC	Start/End	HCC ID
# of bits	1	1	4

Table 9.10: K2 Frame Payload

The K2 frame is followed by two header frames, depicted in Table 9.11. The 5 msbs of the header frames' payload are '00000' to distinguish these frames from L0 frames. The remainder of the payload is the Read/Write bit, the ABC ID of the target ABCStar ASIC and the address of the target register. If the Read/Write bit is '1', the command is a read command otherwise it is a write command. An ABC ID of '1111' is interpreted to be a broadcast address and all ABCStar ASICs will respond.

Frame		**MSB**			**LSB**
1	**Field**	Marker	R/W	ABC ID	Reg Addr MSB
	Value	00000			
	# of bits	5	1	4	2
2	**Field**	Marker		Reg Addr LSB	SPARE
	Value	00000			
	# of bits	5		6	1

Table 9.11: Register Command Header Frames

For register read commands, the header frames are followed by a K2 frame with the Start/End bit set to 0, indicating the end of the sequence. If the K2 frame has the Special HCC ID (1110), the command is discarded and no operation is executed. However, if the HCC ID is any other value, the command is executed.

For register write commands, the two header frames are followed by 5 frames containing the value to write into the register, as shown in Table 9.12.

Frame		MSB		LSB
1	**Field**	Marker	SPARE	Register contents [31:28]
	Value	00000		
	# of bits	5	3	4
2	**Field**	Marker		Register contents [27:21]
	Value	00000		
	# of bits	5		7
3	**Field**	Marker		Register contents [20:14]
	Value	00000		
	# of bits	5		7
4	**Field**	Marker		Register contents [13:7]
	Value	00000		
	# of bits	5		7
5	**Field**	Marker		Register contents [6:0]
	Value	00000		
	# of bits	5		7

Table 9.12: Register Data Frames

As with the register reads, the sequence ends with a K2 End frame. If the K2 frame has the Special HCC ID (1110), the command is discarded and no operation is executed. However, if the HCC ID is any other value, the command is executed. Register write commands can be issued without any intervening space between commands.

Register access command sequences may be terminated at any time with a valid K2 End frame. A new command sequence may immediately follow.

Idle frame: If there is nothing else to send an IDLE frame composed of the control symbol pair {K0, K1} will be sent. This frame is used to establish initial synchronization on the link and provide for ongoing validation of synchronization.

9.6 Trigger Signals

Latency and other parameters associated with three trigger options being considered

Parameter	
L0 rate	1 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple ROIs to the same region in consecutive BCs.	TBD
Max latency of L0 (at input to LTI and assumptions about arrival at ABCstar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	10 µs
Max latency to deliver data to L1-Track in response to L0+ROI.	

"First bit of requested data to leave HCC after an R3"	4 µs
Assuming ROIs are asynchronous, max delay of ROI after L0.	3 µs
Max latency of L1 (at input to LTI and assumptions about arrival at ABCstar).	Alternate below
Max latency of L1 at output of FELIX (not clear what internal FELIX processing time is included)	60 µs
Max latency to deliver data to FELIX (or some other point) in response to L1.	No Limit

Table 9-13: Original Trigger Scheme: 1 MHz L0s, 10% ROIs, 400 kHz L1s

Parameter	
L0 rate	1 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple ROIs to the same region in consecutive BCs.	NA
Max latency of L0 (at input to LTI and assumptions about arrival at ABCstar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	10 µs
Max latency to deliver data to L1-Track in response to L0+ROI. "Last hit leaving HCC after R3" – Not clear how to define this.	NA
Assuming ROIs are asynchronous, max delay of ROI after L0.	NA
Max latency of L1 (at input to LTI and assumptions about arrival at ABCstar).	NA
Max latency of L1 at output of FELIX (not clear what internal FELIX processing time is included)	NA
Max latency to deliver data to FELIX (or some other point) in response to L1.	NA

Table 9-14: Single Trigger Scheme: 1 MHz L0s – everyone reads everything out at L0

Parameter	
L0 rate	4 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple ROIs to the same region in consecutive BCs.	TBD
Max latency of L0 (at input to LTI and assumptions about arrival at ABCstar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	4.5 µs
Max latency to deliver data to L1-Track in response to L0+ROI. "First bit of requested data to leave HCC after an R3"	4 µs
Assuming ROIs are asynchronous, max delay of ROI after L0.	1.8 µs

Max latency of L1 (at input to LTI and assumptions about arrival at ABCstar).	Alternate below
Max latency of L1 at output of FELIX (not clear what internal FELIX processing time is included)	22.83 µs 22 µs proposed
Max latency to deliver data to FELIX (or some other point) in response to L1.	No Limit

Table 9-15: Low Latency L0 Scheme: 2-4 MHz L0s, < 10% ROIs, 600-800 L1s (with constraint that 10% ROIs + L1s ≤ 1 MHz readout of everything)

9.7 Input Register and Test/Mask Register

The functions of the input register and test/mask register will be implemented in a single functional block.

9.7.1 Input Register

This register latches the incoming data with the rising edge of BC, delivering a clocked pulse to the subsequent circuits.

9.7.2 Channel Mask Register

This register serves a dual purpose. Firstly, the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate due to false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline. In the Mask mode, a channel is masked with '1'. In Test mode, there are two modes of operation, static and pulsed. In the Static Test Mode, the pipeline input gets continuously the Mask bit value. In the Test Pulse mode, there are 2 options controlled by a bit in one of the configuration register (bit 18 of the register at address $20):
Option 1: the pipeline inputs get the Mask bit value for the duration of one clock period, otherwise it is always zero (no hit). The one clock period pulse is generated by the "Digital Test Pulse" Command applied through the LCB fast command protocol.
Option 2: the pipeline inputs get a bit pattern along 4 consecutive BC. Two sets of 4 bit patterns are defined in configuration registers (bits 19 to 26 of the register at address $20). One set is applied to the channels with the Mask bit set and the other set is applied to the channels with the Mask bit unset. The patterns are triggered by the "Digital Test Pulse" Command applied through the LCB fast command protocol.
The bit 4 of the register at address $20 is used to enable (1) or disable (0) the test pulse signal in any mode.
For all Test modes, the front-end channels outputs are disabled (set to zero).

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TM(1:0) bits	Mode of Operation
00	Normal Data Taking (Contents of register used to "Mask Inputs")
01	Static Test Mode (Contents of mask register are used to supply test values to pipeline)
10	Test Pulse Mode (2 options, see the description in the paragraph)

Table 9-16: Masking Register Modes of Operation

9.7.3 Edge Detection Circuitry

The function of this block is to detect the match of the input signal looking on 3 consecutive BC clock periods to a given pattern. For each successful match found the circuit generates a pulse of duration 1 clock cycle. The effect of this block is that only a single '1' is written into the pipeline for every hit detected according to the match criteria, irrespective of the length of the incoming pulse. The various match pattern on 3 consecutive BC as listed on Table-2 :

Det_mode (1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st on the left)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Clear	None	Special Mode

Table-9-17 : Edge Detection Criteria

With Det_mode at 11 the edge detection circuit enforces 0 at its output independently of the input signal (L0Buffer clearing). Det_mode[1:0] are bits 1 and 0 in the configuration register $23.

9.7.4 Input Pattern Register

This register serves as signal pattern monitor at the pipeline input. The 256 bits Pattern Input register is built as 8 registers of 32 bits, each one being addressable in read by Control Commands. (This feature will probably will removed)

9.8 Event Buffers

9.8.1 L0BUFFER (Pipeline)

The binary pipeline L0BUFFER is realized with two single port RAM blocks of 320 bits (wide) by 256 bits (length) (164Kb). The total pipeline length is 512 bits, or 12.8us latency time. Out of the 320 inputs, 256 are for the hit data, 8 are receiving the BC counter value (BCID), and the remaining will be unused (zeroed) or used for Error Recovery Code. When a L0 trigger is received (LCB_IN input), the hit-pattern and BC count from the bits written in the pipeline at a predefined number (LAT) of clock cycles before are readout and transmitted to the EVTBUFFER. LAT is the number of clock cycles representing the L0 latency time. The value of LAT is programmable through the command decoder and stored in the configuration register CFGREG2 at address $22. If a LCB fast command SoftReset or SYSReset is issued, the pointer address generator for the RAM block is reset to address 0 for the write and LAT for the read, while the contents of the pipeline remain unchanged. A description of the L0Buffer arrangement is shown in Figure 9-2.

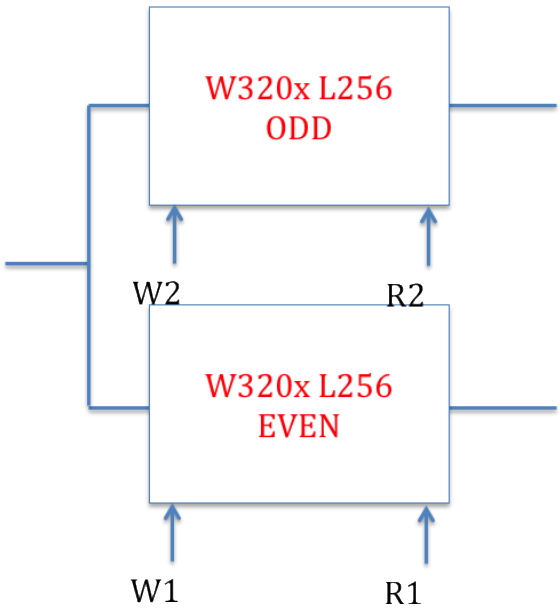


Figure 9-2 L0Buffer (pipeline) arrangement in 2 blocks of 256 320-bits wide words.

One implementation option is to reduce the pipeline length to 128 bits, with the remaining of the pipeline structure being unpowered (local power supply clamped to ground). This feature would save power in case of a L0 latency less than 6.4us. The precise implementation of power down has two options :

- One is to have a power switch control on the power rail of the second part of the L0Buffer
- The other one is to have a voltage regulator dedicated to the second part of the L0Buffer, that can deliver voltage or ground to the power rail.

9.8.2 Hits Accumulators

An 8 bits counter is attached to each channel at the output of the L0Buffer, that count hits moving from the L0Buffer to the EvtBuffer (therefore controlled by the L0 trigger rate). In this way it is possible to accumulate hits counts, a feature that can be useful in some calibration procedures.

The counting capability for all channels is enabled through the control signal Encount (bit 5 of the CFGReg $01. Counters values are caught at the time the counters read commands are issued. A single counter read command is able to get counters values for 4 channels. Counters are stopping when reaching the maximum count($FF).

All counters are controlled through three fast commands of the LCB protocol listed in Table 9.9. The Hit Count Reset command is forcing all counters to zero, the Hit Count Start command indicates the start of count, the Hit Count Stop command interrupts the count and keeps the count values.

9.8.3 EvtBUFFER

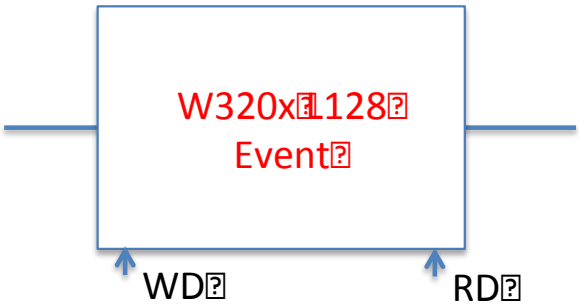


Figure 9-3 EvtBuffer arrangement in 1 block of 128 320-bits wide words.

The readout buffer EvtBUFFER is realized by one single port RAM blocks of 320 bits (wide) by 128 bits (length) (41Kbits in total). The buffer length is able to store 128 L0 tagged “events”. With an average L0 event readout rate of 1MHz, the events are stored in the EvtBUFFER for an average duration of 128 microseconds. Out of the 320 inputs, 256 are for the hit data, 8 are for the BC counter value stored in the L0Buffer (BCID), 8 are for the L0_tag data, 8 are for the BC counter value at the time of arrival of L0 (BCatL0).

BCID and BCatL0 values should be a constant value (modulo 256) that depends on the L0Buffer latency setting. The difference of the two values is compared to a preset “BCoffset” value (bits [31:24] of CFGReg2) that can be programmed during the configuration phase. If the comparison fails, a flag BCIDFlag (bit 8 of StatusReg2, address $32) is set.
The comparison feature can be enabled/disabled by control of the bit 23 of CFGReg2.

EvtBUFFER Readout mechanism

The ABCStar allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, an asynchronous Priority Readout Request (PR) and a second (lower priority) asynchronous Readout Request (LP).
Definitions of terms:
L0: “zero” level trigger signal, broadcast to all chips, encoded in the LCB framing and at fixed latency after the event (BCR_IN signal).
L0_tag: A 7 bits number provided for each L0, that is used internally as the “physical” address of the event in the EventBuffer. The L0_tag is obtained through the decoding circuit of the LCB signal.
PR: signal addressed to a fraction (10%) of the detector, requests the readout of events tagged by a number “PRL0ID”, 8bits streamed with the PR signal. PRL0ID should match the L0_tag value attached to a L0 to retrieve the event associated to this L0.
LP: signal addressed to the full detector, requests the readout of events tagged by a number “LPL0ID”, 8bits streamed with the LP signal. PRL0ID should match the L0_tag value attached to a L0 to retrieve the event associated to this L0.

The EvtBUFFER operation is rather simple to explain: at every occurrence of L0, one event of the L0BUFFER is written in EvtBUFFER (1 BC slot). At any occurrence of PR or LP, one event is read out (1 BC slot) and sent to the Cluster Finder block.
The identification of the event to readout, within the EvtBUFFER memory array, is made with the PRL0ID (or LPL0ID) numbers: these numbers are used as direct pointers (address generators) for reading the EvtBUFFER. If PRL0ID and LPL0ID have the same value, they read the same event.
To correctly address the event to readout, the PRL0ID (LPL0ID) value has to be equal to the L0_tag value that has been written at L0 time.
A typical sequence of signals to operate the data extraction from the L0BUFFER and EvtBUFFER is shown on Figure 9-5.

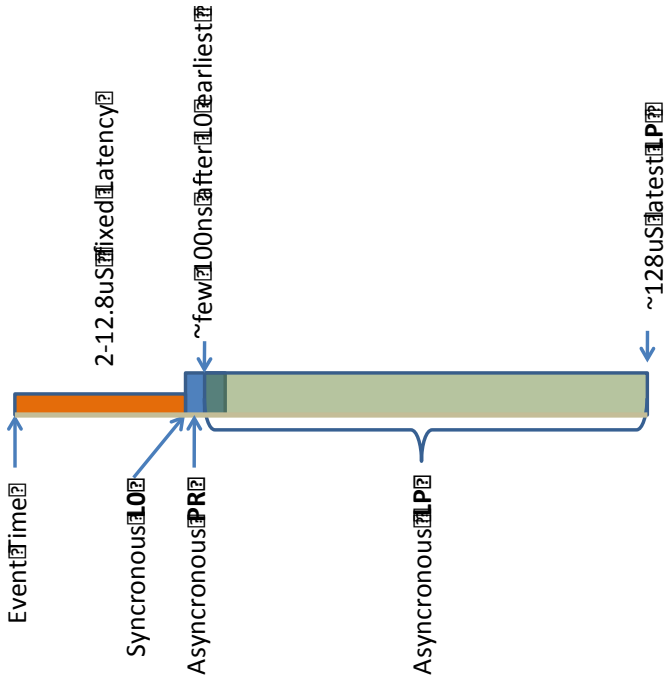


Figure 9-4: L0, PR and LP Latencies

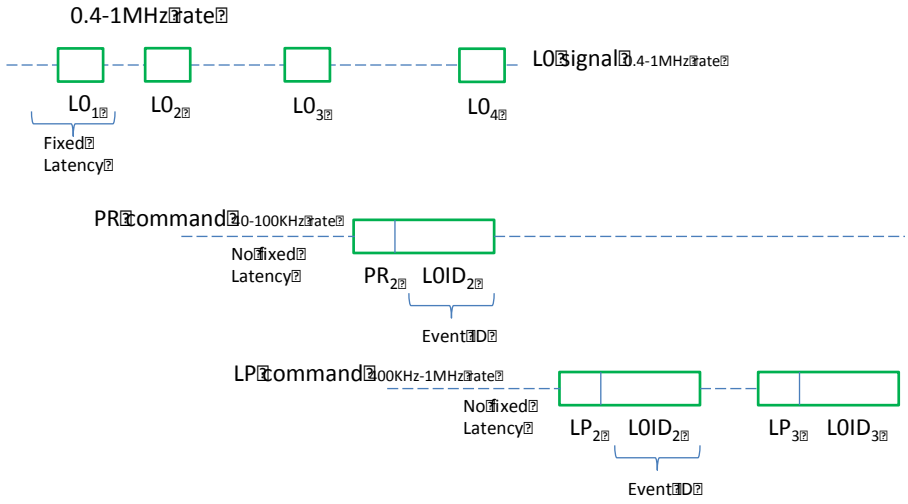


Figure 9-5: Sequence of the internal L0, PR, LP signals used to trigger the physics data readout.

Because the events readout sequences can occur in parallel and independently of the arrival of the PRL0ID or LPL0ID commands, the respective PRL0ID or LPL0ID numbers are stored in 2 separate FIFOs. The size of the FIFO for the LPL0ID numbers is maximum 128 (same size as the EvtBUFFER). The size of the FIFO for the PRL0ID numbers can be reduced to 15 (approx. 1/10th of the size of the EvtBUFFER).

9.8.4 Intermediate FIFO Buffer

The memory blocks of the L0Buffer and EvtBuffer do not support simultaneous write and read in the same clock cycle. In case of writing directly from the L0Buffer to the EvtBuffer, this operation can be continuous for several clock cycles as long as there are contiguous L0 signal. In this case the EvtBuffer Read operation has to be delayed until the write cycles are finished.
There is the requirement to minimize the delay time between receiving a PR trigger and sending the corresponding data out of the chip. To keep this delay independent of the number of L0 and hence keep executing the EvtBuffer Read in case of contiguous L0, a small size intermediate FIFO is inserted between the L0Buffer and the EvtBuffer.
With this structure and the appropriate control logic, the EvtBuffer Read operation is given priority over writing in the EvtBuffer. When a Read (one clock cycle) occurs, after a LP or PR trigger, if a L0 is at the same time, the event is stored into the intermediate FIFO for one clock cycle. It is transferred to the EvtBuffer after the Read cycle.

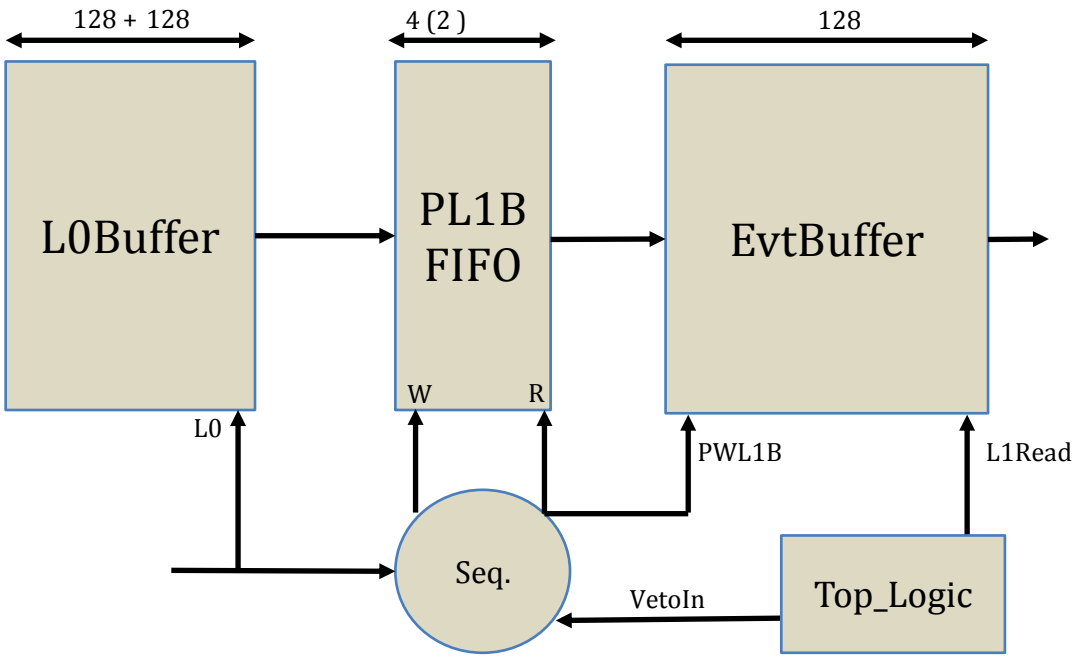
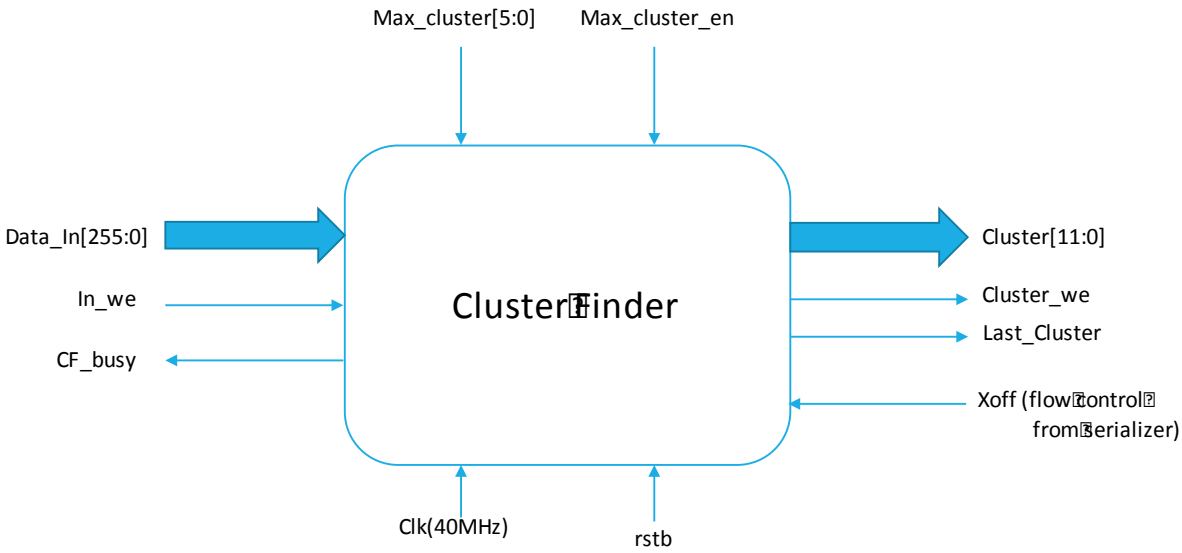


Figure 9-6: PL1B intermediate FIFO insertion between the L0Buffer and the EvtBuffer

9.9 Cluster Finder



9.9.1 Design of the Cluster Finder

The Cluster Finder takes in 256 bits of strip data and reports out 12 bit clusters at 40MHz. A cluster consists of 8 bits of hit address, 3 bits indicating the following 3 strip values and 1 bit denoting whether it is the last cluster or not.

8 bits Address of the Hit	Following 3 strip values	1 bit (Last Cluster)

The input in_we is the input write enable pin which represents valid input data Data_In. The Data_In is latched on the positive clock edge when in_we is high. Once it is latched, the Data_In can be safely changed to the next data from the pipeline. The Cluster Finding algorithm is executed on the input data and it reports out a Cluster of 12 bits. An output pin cluster_we is set high when a valid cluster is sent out. While the Cluster Finder is operating on a 256 data input, it flags out CF_busy as 1 to the preceding pipeline. The last_cluster is enabled high when the Cluster Finder outputs the last cluster detected in the 256 bit strip data. The Xoff is an active high, flow control from the readout which temporarily stops the cluster output transmission. A high Xoff signal halts the Cluster transmission and a low Xoff signal resumes the Cluster transmission.

9.9.2 Interaction of the two 128 strips Cluster Finders to cover 256 strips

Each Cluster Finder sub-block treats 128 strips of the same strip row of the detector. The Cluster Finder deals with strip data as odds and evens. Two identical Cluster Finder sub-blocks (A or C) are required to treat the 256 strips. The rearrange block inside the Cluster Finder takes in 256 bits of input data and separates it into 2 banks of 128 bits called Odd and Even banks, to group together bits of adjacent channels in a strip row. The odd-numbered channels are grouped to the odd data bank and the even-numbered channels are grouped to the even data bank.

$$dataOdd[i] = dataIn[2*i + 1] \qquad i=0,1,2,\ldots 127$$

$$dataEven[i] = dataIn[2*i] \qquad i=0,1,2,\ldots 127$$

The 2 sets of 128 bit data are sent to the CF128_odd and CF128_even blocks which are enabled alternately by a state machine. The 2 banks report out clusters one bank at a time in an alternate fashion to avoid bias to any 1 bank. The Cluster Finder always start reporting clusters from the odd bank first, then the even bank, and continues the process until it has reported out all clusters. When the odd bank is empty, the Cluster Finder starts reporting out clusters from the even bank one clock cycle later. When both the banks are empty, the Cluster Finder reports out a reserved 12 bit No Cluster Output.

The “Max_cluster_enable” and “Max_cluster[5:0] bits can be used to limit the number of clusters produced by the Cluster Finder. The absolute maximum number of clusters per event is 64 (corresponding to 16 packets and approximately 6.8us transmission time)

9.9.3 Pin Configuration for Cluster Finder

Pin Name	Function	Active High/Low	Direction
Clk	40 MHz Clock.		Input
rstb	System Reset	Active Low	Input
Data_in [255:0]	256 bit Strip data	Active High	Input
in_we	Input Data Valid Signal	Active High	Input
Xoff	Output Data Flow Control Signal	Active High	Input

Cluster[11:0]	12 bit cluster (8 bit hit address 3 bit strip values 1 bit last cluster)	Active High	Output
Cluster_we	Output Data Valid Signal	Active High	Output
Last_cluster	Indicates last cluster	Active High	Output
Max_cluster_enable	Enables the maximum number of clusters per event	Active High	Input
Max_cluster[5:0]	Maximum number of clusters per event	Decimal 1 to 63	Input
CF_busy	Input Data Flow Control Signal	Active High	Output

9.9.4 No Cluster Output Case

There are many invalid 12 bit values which cannot be possible cluster values. When the hit addresses are either 125, 126 or 127; all the possible values for next 3 bit strip values don't exist as the next strips are physically absent. There are only 2 next strip values for strip address 125, 1 next strip value for 126 and none for 127. The output cluster value for the no cluster case can be chosen from any one of these invalid 12 bit values.

For the case when no cluster is detected in the 256 bit strip data, a special 12 bit output (3FE) is sent out. This 12 bit is not used otherwise and specially reserved for this case.

9.9.5 Cluster Finder Timing

The Cluster Finder latches in the 256 bit strip data during the positive 40MHz clock edge when the input write signal (in_we) is enabled. The Cluster Finder algorithm is first executed on the odd bank, and the hit address along with the 3 next strip values is obtained in 1 clock cycle. In the next clock cycle, this cluster is checked for the last cluster, and Cluster Finder algorithm is executed in parallel on the even bank.

So, the Cluster Finder reports out the first cluster 2 clock cycles (50ns) after the input data latch, for the case when the odd bank is not empty. When the odd bank is empty, the Cluster Finder reports out the first cluster after 3 clock cycles (75ns) from the even bank. The clusters are reported out every clock after the first cluster unless an Xoff signal is asserted from the Readout Block. For the no cluster case, the special 12 bit output 12'h3FE is sent after 3 clock cycles (75ns).

9.9.6 Interaction with the Readout Block

The transmission of the clusters from the Cluster Finder to the Readout is controlled by the Xoff signal. When the input data is latched and the first cluster is generated (after 2 or 3 cycles), the Cluster Finder checks the Xoff line to determine whether the Readout is ready to accept clusters. An active low Xoff signals that the Readout is ready to accept

clusters. The Cluster Finder then begins the transmission of clusters to the Readout Block. When the Readout is not ready to accept any further clusters, it asserts an active high Xoff signal to the Cluster Finder to halt the transmission of clusters. The Clusters Finder writes any excess clusters generated into an internal FIFO. (In this case it is always 1 or 2 clusters). Once the Readout is available to accept clusters, the Cluster Finder resumes the transmission of the clusters first from this internal FIFO and continues until another high Xoff signal is asserted or it reaches the end of Cluster Finding.

9.10 Readout Circuitry

The readout circuitry is responsible for building data packets with the hit patterns coming from the Cluster Finder blocks or from the registers to be read. Each packet is transmitted to the fast 160Mb/s serializer. For physics data, the header is presented to the output, and then the consecutive bits forming the clusters bytes are following until one data packet is completed. For Register read-back, a different header is presented to the output, and then the register bit values are following until the full register content is sent out.
A controller defines the order in which packets are formatted and then sent out serially. All packets belonging to the same event are sent out consecutively.

9.10.1 Detailed Description: Interaction with the Cluster Finder

The description of the readout system follows the elements of Figure 9-7.

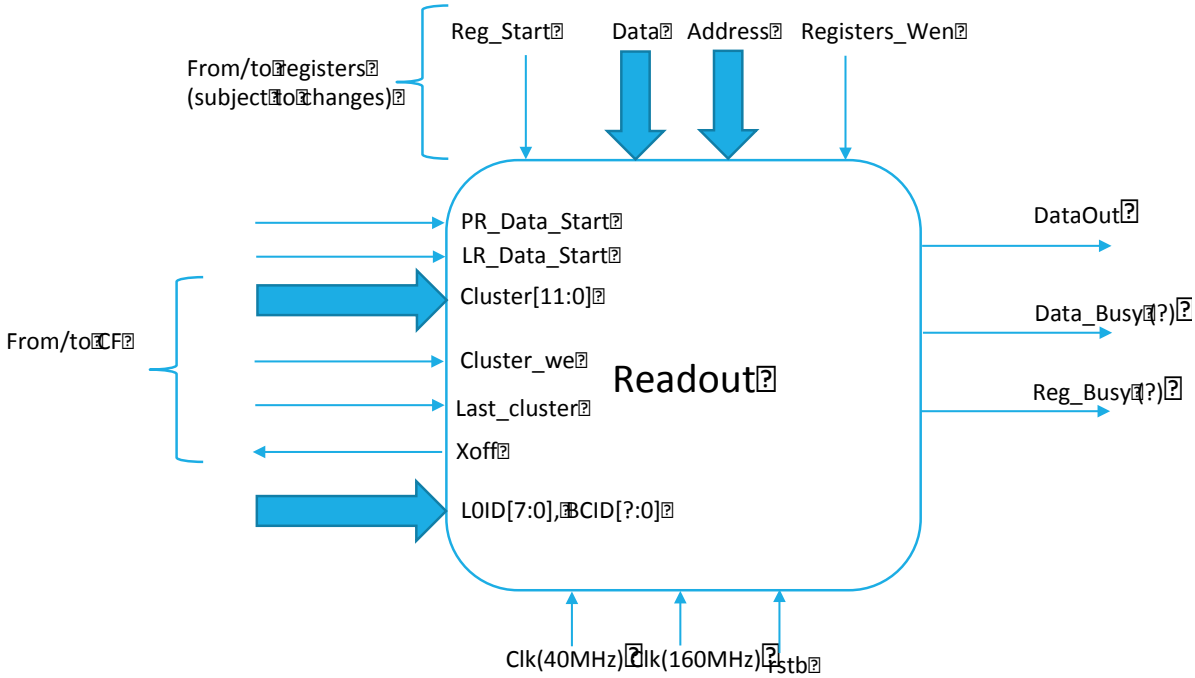


Figure 9-7 Readout logic blocks showing the core packet builder

The following description is done for the case of LP trigger signal. It applies equally well for the operation with a PR trigger signal. The interaction between LP trigger and PR trigger in the Readout is discussed in a subsequent paragraph.
As soon as an LP readout is authorized, the Readout obtains from the higher control level logic the LP_Data_Start signal, and from the EvtBuffer the L0ID value and the BCID value.

(The Data_Busy signal is set to one.) The 16 bits header for physics data is assembled and the transmission at 160 Mhz starts as soon as possible.
During the time of the header transmission, the Cluster Finder has performed the first cluster finder action. When the first cluster data is valid (12 bits, made of 8 bits of address, 3 bits of bitmap and the Last_cluster bit) the Cluster data is sent to the Readout with the Write_en signal. At the end of the header transmission, the Readout sends the first cluster data.
During the transmission of the any cluster data, if the Last_cluster bit of the current cluster is 0, the next cluster data is presented to the Readout with the Cluster_we signal. The Readout sets the Xoff output bit high to freeze the cluster search in Cluster Finder, until the Readout is able to process it. If the LastCluster bit of the current cluster is 1, the serialisation process stops after the current cluster last bit is transmitted.

9.10.2 Detailed Description: Interaction between PR and LP in the Readout

PR and LP triggers are using the same Cluster Finder block.
The difference is in the priority given to the PR triggered events.
If a PR (or LP) trigger is received, in the absence of LP (resp. PR) trigger, the Cluster Finder and Readout mechanisms are identical to what is described above (except TYP values are different in the long header).
If a PR trigger signal is received when the Readout is already processing a LP triggered event, the process of sending packets of the PR event is appended at the end of the existing LP event transmission Only when the PR trigger event buffer is empty, and the last cluster of the last PR event has been found, can packets of pending LP events be processed.

9.10.3 Registers Read-back

All internal 32 bits registers contents can be read out through a 68 bits packet format.

Sending a command to read a given register, as described in **Error! Reference source not found.**, will result in the transmission of one “Register packet” that contains the register identification and the 32 bits of data, as described in paragraph 9.11.

However, the physics packets transmissions have some level of priority, in particular the PR packets. Because of this, at reception of the read register command, the register data are internally stored into a 32 positions Register Data FIFO, and the transmission occurs only when some conditions are met. We define 2 cases for the transmission of register packets, independent of when the read register command has been received:

First case (default): the register packet(s) are transmitted as soon as there is no pending LP or PR events in the Event Buffer of the chip.

Second case: because it is possible that events are queued for a long time in the chip, and because some of the registers may contain critical data (like status bits), a command called “RRforce” (writing bit 3 in register $00) can be send : in such a case the oldest register data pending inside the Register Data FIFO is transmitted after the current LP or PR event packet transmission is finished, and if there is no pending PR events[*].

[*] The compatibility of this option with the HCCstar has to be assessed

9.11 Readout Packet Format

In ABCStar the output format has a 68 bits fixed length readout packet format. A packet in case of physics data is made of a 3-bits preamble (start bits), a 16-bit "Physics Header" part containing data type and event identification, 4 cluster bytes of 12 bits, followed by a 1-bit trailer ('0').
The initial 3 preamble bits and the last bit (trailer) define the packet framing, in the subsequent text.
The cluster byte is made with 12 bits as defined in Table 9-18 :

Last Cluster Flag	Cluster Address	Next Strips Pattern
1	8	3

Table 9-18 : Cluster Byte definition

In case of events with less than 4 clusters, the 'empty cluster byte' is used.
In case of events with more than 4 clusters, a first packet is formed with the framing and the Physics Header (16 bits) followed by the 4 cluster bytes. Then other packets are formed with the framing and the same Physics Header (16 bits) followed by 4 cluster bytes or empty cluster bytes, until all clusters for one event are transmitted. A "LAST_CLUSTER" bit value set at one marks the last cluster for a given event.
For a register readback packet, which contains the register identification and register contents (status, flags, SEU detection, configuration, input patterns, analogue bias setting, etc.), a packet is formed with the 4 bits framing (3 bits preamble and 1 bit trailer), the 16-bit "Register Header" part containing the data type and register identification, followed by the payload made of the the 32-bit register contents, and 16 bits left for TBD purpose.

Register Contents	Monitor Data
32	16

Table 9-19 : Register Packet Payload

The 16 last bits of the 48 bits payload can be used for general monitor purpose (TBD)

9.11.1 Packet framing

Start Bits	Header	Payload	Trailer
3	16	48	1

Start Bits = 111 (Could be 11 followed by an “Error” bit like :
111: 2 Start bits and no error reported
110: 2 Start bits and error reported (TBD)
Trailer = 0 (1 bit)

9.11.2 PHYSICS HEADER:

TYP	L0ID	BCID
4	8	4

Table 9-20 : Physics Packet Header

The Physics Data Header is made of 16 bits arranged as shown in Table 9-20.
The TYP field identifies the packet type:

TYP code	Meaning
0001	PR packet
0010	LP packet
0100	ABC register read packet
0111	Reserved to HCC
1000	Reserved to HCC
1011	Reserved to HCC
1101	Reserved to HCC
1110	Reserved

Table 9-21 : TYP descriptor

L0ID and BCID fields are the event identifiers.
The BCID field contains the 3 least significant bits of the BCID associated to the event followed by a 1-bit parity field calculated over the entire 8-bit width of the BCID.

9.11.3 REGISTER HEADER:

TYP	Register Address	TBD
4	8	4

Table 9-22 : Packet Header (Register Data)

The Header is made of 16 bits arranged as shown in Table 9-22:
TYP is defined as in Table 9-21.
The next 8 bits field is reserved for containing the register address.
The last 4 bits of the Register Header may contain status bits (TBD).

9.12 Beam Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either hardware reset, a software reset, or the BCR signal issued from the LCB input protocol and its decoding circuit. The BC counter value is entered in the pipeline at each clock cycle and transferred to the readout buffer at the time of a L0. It is also directly entered in the EvtBuffer at the time of the L0. It is expected that the difference of BCID values between entering the pipeline and entering the EvtBuffer is constant once the pipeline latency has been fixed. A detection circuit produces a flag if a deviation from the expected value is observed.

9.13 L0ID Counter

This a 8-bit binary counter which is incremented every time the chip receives a L0 trigger. The counter is set to $FF by either a hardware reset or software reset. The L0ID counter is actually provided as a spare to crosscheck with the L0_tag values issued from the LCB input protocol and its decoding circuit.

9.14 LCB Command Decoder

In ABCStar there are two classes of commands (CMD bit of the LCB protocol): fast commands (6-bit command format) and register commands (55-bit or 20-bit command format). Fast commands are global and have a direct effect on the chips operation: they are used to resynchronize the BC and Trigger counters, and eventually they return the chip in predefined default states (SoftReset or SYSReset).
Register commands are global or addressable commands to execute Write or Read operations into the internal registers. The read register commands should not interfere with the data taking operation, however there may be limitations if such commands are received when the chip is in data taking mode (see the HCCStar operation).

9.14.1 Fast commands:

The 6 bits commands are received on the 4BC frame format of the LCB protocol. The description for the 6 bits is given in paragraph 9.5 and Table 9.9. In the case of the ABCstar chip, different reset commands have been defined, i.e. the Soft Reset, BC Reset commands, L0ID counter Preset command, SEU registers reset. It is expected that these commands will be sent to the chip at regular intervals during periods of time when no triggers signals will be sent to the chip. The purpose of these commands is to perform controlled resets of the chip. (See Section 9.18 for details). The digital test and the analogue calibration pulse signals are also generated by fast commands to control precisely the synchronization to the BC number:
CalPulse : Generate the analogue calibration pulse, 200ns wide (8BC). The polarity is controlled by the bit 5 in register $21. The analogue calibration pulse is enabled only if bit 4 of the register $21 is set.
DigitalPulse : Generate a test signal at the input of the pipeline (through the Channel Mask Register, see 9.7.2). The digital test signal is enabled only if bit 4 of the register $20 is set.

9.14.2 Register commands

These are long packets that enable the operation of the chip to be controlled by setting bits in registers. Only the addressed chips will act on the packet, unless the address sent equals '1111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed chips erroneously decoding parts of the data field as the start of packets. Write and Read register commands can be sent to the chip during normal data taking (ie. at the same time as L0, PR or LP inputs), however this should be done with precaution as it may affect the chip settings or produce additional data added to the data flow toward the HCCStar. The transmission of registers data packets produced by read commands are taking the lowest priority as compared to the PR or LP packets transmissions: the register content addressed by the Read command are sent out only if no PR or LP packets are pending. A mode is set through the RRenforce bit (bit 0 on the configuration register $00) to enforce one read register transmission in front of pending LP packets. Write commands executions can be switched-off by setting bit 1 in the configuration register $00, to prevent a chip to be accidentally reconfigured.

The register commands are received through the LCB protocol. Significant bits of the commands are presented in the form of the continuous significant bit streams in the tables below.

Field 1 1 bit HCC/ABC	Field 2 '1'+4 bits HCC ChipID	Field 3 1 bit (R/W)	Field 4 4 bits ABC ChipID	Field 5 8 bits Register address	Field 6 Spare 4/1 bits	Field 7 (32 bits) Data	Description
1	1cccc	0 = W	aaaa	$00	nnnn	32'hddddddddd	Special Register
1	1cccc	0 = W	aaaa	$0F-$01	nnnn	32'hddddddddd	Analogue and DCS registers
1	1cccc	0 = W	aaaa	$17-$10	nnnn	32'hddddddddd	Mask Registers
1	1cccc	0 = W	aaaa	$1F-$18	nnnn	32'hddddddddd	Pattern input registers
1	1cccc	0 = W	aaaa	$2F-$20	nnnn	32'hddddddddd	Configuration registers
1	1cccc	0 = W	aaaa	$3F-$30	nnnn	32'hddddddddd	Status registers
1	1cccc	0 = W	aaaa	$5F-$40	nnnn	32'hddddddddd	LSB Trim DAC registers
1	1cccc	0 = W	aaaa	$5F-$40	nnnn	32'hddddddddd	LSB Trim DAC registers
1	1cccc	0 = W	aaaa	$67-$60	nnnn	32'hddddddddd	MSB Trim DAC registers
1	1cccc	0 = W	aaaa	$6F-$68	nnnn	32'hddddddddd	Calibration Enable registers

Table 9-23 : Register Commands (Write). Greyed rows are not executable.

Field 1 1 bit HCC/ABC	Field 2 '1'+4 bits HCC ChipID	Field 3 1 bit (R/W)	Field 4 4 bits ABC ChipID	Field 5 8 bits Register address	Field 6 Spare 4/1 bits	Field 7 (32 bits) Data	Description
1	1cccc	1=R	aaaa	$00	n	-	Special Register
1	1cccc	1=R	aaaa	$0F-$01	n	-	Analogue and DCS registers
1	1cccc	1=R	aaaa	$17-$10	n	-	Mask Registers
1	1cccc	1=R	aaaa	$1F-$18	n	-	Pattern input registers
1	1cccc	1=R	aaaa	$2F-$20	n	-	Configuration registers
1	1cccc	1=R	aaaa	$3F-$30	n	-	Status registers
1	1cccc	1=R	aaaa	$5F-$40	n	-	LSB Trim DAC registers
1	1cccc	1=R	aaaa	$5F-$40	n	-	LSB Trim DAC registers
1	1cccc	1=R	aaaa	$67-$60	n	-	MSB Trim DAC registers
1	1cccc	1=R	aaaa	$6F-$68	n	-	Calibration Enable registers
1	1cccc	1=R	aaaa	$AF-$70	n	-	Hit Counters registers

Table 9-24 : Register Commands (Read)

Legends:

n = don't care value**.**
aaaa = 4 bits chip address(MSB bit first)
1cccc = ‘1’ + HCCID code
32’hdddddddd = 32 bits values for registers (MSB bit first)

Field 2
This is the 5 bit reserved for the HCC ChipID. If it has the special code ‘1110’ the command is aborted. Otherwise this field is ignored by ABCStar chips.
Field 3
This bit is zero if command is to Write in register, 1 if command is to Read register.
Field 4
This is the 4 bit of the ABCStar ChipID. ‘1111’ is used as the broadcast address.
Field 5
The register addresses are distributed in ranges of 16 consecutive addresses per part of the chip. There can be unused bits per register and unused addresses in the range. Precise definition of the register content per address will be part of each block functional description.
Field 6
This field holds 1 to 4 unused bits : they are here to adapt the command length to the segmentation into fixed length frames occurring in the LCB encoding mechanism.
Field 7
This field holds the 32 bits data that is to be written into the selected register.

Registers banks are separated in groups :
ANALOG and DCS : Write and Read registers, default setting at reset. Write protected by a bit set in Register $00.
INPUT : Mask bits (also test pattern injection), Write and Read, masked by default at reset ? (to avoid noisy signals propagation at startup?). Write protected by a bit set in Register $00.
CONFIGURATION : Configuration bits, Write and Read, Preset value at reset. Write protected by a bit set in Register $00.
STATUS and SEU : Read only registers. The STATUS register at address $37 is defined as the high priority Status Register. SEU registers are reset by the OR of SoftResetb and the specific SEU Reset command.
TrimDAC and Calibration : Write and Read registers, default setting at reset. Write protected by a bit set in Register $00.

9.14.3 SEU Protection:

The logic for decoding the RESET commands should be triplicated

REG type	TRIPLICATION	
ANALOG & DCS	YES	
MASK	YES	
CONFIG	YES	
STATUS & SEU	NO	
CHANNELS	YES	

Table 9-25: registers subject to triplication

The signals issued by the command decoder to operate write or read access to the protected registers do not need triplication: the probability to get false write is low (needs simultaneous corruption of two different signals). False read has no impact.

9.15 Registers

Table 9-26: SPECIAL REGISTER

Addresses : $00 (1 register of 32 bits)

	SCREg
	$00
31	0
30	0
29	0
28	0
27	0
26	0
25	0
24	0
23	0
22	0
21	0
20	0
19	0
18	0
17	0
16	0
15	0
14	0
13	0
12	0
11	0
10	0
9	0
8	0
7	0
6	0
5	0
4	0
3	0
2	0
1	WriteDisable
0	RRforce
SEUbit	scREGSEU(serSC)
model	SCREg
ResetValue	00000000

Bit Functions :
RRforce : When set, the oldest pending “Read Register” packet is transmitted after the current LP or PR event packet transmission is finished, and if there is no pending PR events. The RRforce bit is internally reset after the Read Register packet transmission.
WriteDisable : if set this bit prevents write commands on registers other than $00 to be active (protection against spurious commands).

Table 9-27: ANALOG AND DCS REGISTERS

Addresses : $01 to $0F (15 registers of 32 bits)

	ADCS1	ADCS2	ADCS3	ADCS4	ADCS5	ADCS6	ADCS7
	$01	$02	$03	$04	$05	$06	$07
31	0	0	0				A_EN_CTRL
30	0	0	0				A_S15
29	0	0	0				A_S14
28	BTRANGE(4)	BIPRE(4)	0				A_S13
27	BTRANGE(3)	BIPRE(3)	0				A_S12
26	BTRANGE(2)	BIPRE(2)	0				A_S11
25	BTRANGE(1)	BIPRE(1)	BCAL(9)				A_S10
24	BTRANGE(0)	BIPRE(0)	BCAL(8)				A_S9
23	0	0	BCAL(7)				A_S8
22	0	0	BCAL(6)				A_S7
21	0	0	BCAL(5)				A_S7
20	B8BREF(4)	BIFEED(4)	BCAL(4)				A_S6
19	B8BREF(3)	BIFEED(3)	BCAL(3)				A_S5
18	B8BREF(2)	BIFEED(2)	BCAL(2)				A_S4
17	B8BREF(1)	BIFEED(1)	BCAL(1)				A_S3
16	B8BREF(0)	BIFEED(0)	BCAL(0)			D_EN_CTRL	A_S2
15	0	0	0			D_S16	A_S1
14	0	0	0			D_S15	BTMUXD
13	0	0	STR_DEL(5)			D_S14	BTMUX(13)
12	BIREF(4)	COMBIAS(4)	STR_DEL(4)			D_S13	BTMUX(12)
11	BIREF(3)	COMBIAS(3)	STR_DEL(3)			D_S12	BTMUX(11)
10	BIREF(2)	COMBIAS(2)	STR_DEL(2)			D_S11	BTMUX(10)
9	BIREF(1)	COMBIAS1)	STR_DEL(1)			D_S10	BTMUX(9)
8	BIREF(0)	COMBIAS(0)	STR_DEL(0)			D_S9	BTMUX(8)
7	0	BVT(7)				D_S8	BTMUX(7)
6	0	BVT(6)				D_S7	BTMUX(6)
5	0	BVT(5)				D_S6	BTMUX(5)
4	BVREF(4)	BVT(4)				D_S5	BTMUX(4)
3	BVREF(3)	BVT(3)		Mon_Sw60		D_S4	BTMUX(3)
2	BVREF(2)	BVT(2)		Mon_Sw80		D_S3	BTMUX(2)
1	BVREF(1)	BVT(1)	STR_DEL_R(1)	Mon_Sw100		D_S2	BTMUX(1)
0	BVREF(0)	BVT(0)	STR_DEL_R(0)	ADC Enable		D_S1	BTMUX(0)
SEUbit	ADCS1SEU (serNC1)	ADCS2SEU (serNC2)	ADCS3SEU (serNC3)	ADCS4SEU (serNC3)		ADCS6SEU (serNC6)	ADCS7SEU (serNC7)
model	reg32tr	reg32tr	reg32tr	reg32tr		reg32tr	reg32tr
Reset Value	00000000	000000FF	00000000	00000000		00000000	00000000

Bit Functions :
See the Front-end section for the bias under control by each bits group. The default sets all bias currents to the minimum, the discriminator voltage (BVT) to the maximum, the calibration pulse delay and amplitude to zero or minimum, the MUX output is not enabled, and the regulators output value tuning are non active. The regulator outputs are set to the maximum.
A_EN_CTRL : at one activates the output voltage tuning with bits A_S1 to A_S7. At zero the regulator output is at maximum voltage.
D_EN_CTRL : at one activates the output voltage tuning with bits D_S1 to D_S7. At zero the regulator output is at maximum voltage.

Table 9-28: INPUT (MASK) REGISTERS

Addresses : $10 to $17 (8 registers of 32 bits)

	MaskInput0	MaksInput1	MaksInput2	MaksInput3	MaksInput4	MaskInput5	MaskInput6	MaskInput7
	$10	$11	$12	$13	$14	$15	$16	$17
31	ch31	ch63	ch95	ch127	ch159	ch191	ch223	ch255
30								
29								
28								
27								
26								
25								
24								
23								
22								
21								
20								
19								
18								
17								
16								
15								
14								
13								
12								
11								
10								
9								
8								
7								
6								
5								
4								
3								
2								
1								
0	ch0	ch32	ch64	ch96	ch128	ch160	ch192	ch223
SEUbit	MT0SEU	MT1SEU	MT2SEU	MT3SEU	MT4SEU	MT5SEU	MT6SEU	MT7SEU
model	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr
Reset state	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

The Input (Mask) Registers bits are used to mask the channel when bit TM[0] is clear (bit 16 of register $20). Channels are numbered from 0 to 255 in the same order as for the readout (column 2 in Table 9-5).
The Input (Mask) Registers bits inject a fixed pattern or a test pulse sequence in the L0 pipeline if bit TM[0] is set (bit 16 of register $20)

Table 9-29: INPUT Pattern REGISTERS

Addresses : $18 to $1F (8 registers of 32 bits)

	RegInput0	RegInput1	RegInput2	RegInput3	RegInput4	RegInput5	RegInput6	RegInput7
	$18	$19	$1A	$1B	$1C	$1D	$1E	$1F
31	ch31	ch63	ch95	ch127	ch159	ch191	ch223	ch255
30								
29								
28								
27								
26								
25								
24								
23								
22								
21								
20								
19								
18								
17								
16								
15								
14								
13								
12								
11								
10								
9								
8								
7								
6								
5								
4								
3								
2								
1								
0	ch0	ch32	ch64	ch96	ch128	ch160	ch192	ch223
SEUbit	no	no	no	no	no	no	no	no
model	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro
Reset State	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

The Input Pattern Registers bits are read-only registers loaded at each bunch crossing with the hit pattern at the L0 pipeline input.
The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as the front-end inputs (column 2 in Table 9-5).

Table 9-30: CONFIGURATION REGISTER

Address Range $20 to $2F is reserved for configuration registers (16 registers of 32 bits). Actually 4 registers are defined from $20 to $23.

	CREG0	CREG1	CREG2	CREG3
	$20	$21	$22	$23
31		0	BCoffset(7)	0
30	0	0	BCoffset(6)	0
29	0	0	BCoffset(5)	0
28	0	0	BCoffset(4)	0
27	TestPatt2(3)	0	BCoffset(3)	0
26	TestPatt2(2)	0	BCoffset(2)	0
25	TestPatt2(1)	0	BCoffset(1)	0
24	TestPatt2(0)	0	BCoffset(0)	SEUCNT_E
23	TestPatt1(3)	0	BCFlagEnable	0
22	TestPatt1(2)	0	0	0
21	TestPatt1(1)	0	0	0
20	TestPatt1(0)	0	0	0
19	0	0	0	0
18	TestPattEnable	0	L0IDPreset.	Max_Cluster_Enable
17	TM(1)	0	PreL0ID(8).	Max_Cluster(5)
16	TM(0)	0	PreL0ID(7).	Max_Cluster(4)
15	0	0	PreL0ID(6).	Max_Cluster(3)
14	0	0	PreL0ID(5).	Max_Cluster(2)
13	0		PreL0ID(4).	Max_Cluster(1)
12	0		PreL0ID(3).	Max_Cluster(0)
11	RRmode(1)	0	PreL0ID(2).	0
10	RRmode(0)	0	PreL0ID(1).	0
9	LP_Enable	0	PreL0ID(0).	0
8	PR_enable	0	Latency(8).	0
7	0	0	Latency(7).	0
6	0	0	Latency(6).	0
5	EnCount	CalPulsePolarity	Latency(5).	0
4	TestPulseEnable	CalPulseEnable	Latency(4).	0
3			Latency(3).	0
2	0	CurrDriv(2).	Latency(2).	0
1	0	CurrDriv(1).	Latency(1).	Det□mode(1).
0	0	CurrDriv(0).	Latency(0).	Det□mode(0).
SEUbit	CFG0SEU(serI)	CFG1SEU(serJ)	CFG2SEU(serK)	SFG3SEU(serL)
model	reg32tr	reg32tr	reg32tr	reg32tr
Reset□Value	00000000	00000004	0000000F	00000000

Bit Functions :

Register $20 :
TestPulseEnable : When set enables the digital test pulse functions at the input of the pipeline
EnCount : when set enables the counters at the end of the L0Buffer (pipeline). When reset the counters are disabled (counting stopped).
CF_enable is the bit to enable (1) or disable (0) the transmission of data originating from the Cluster Finder.
RRmode[1:0] controls the Read Register function as shown on Table 9-31.
Disabling the read register transmission does not prevent the internal FIFO to fill up, and may result in the FIFO full/overflow flags going high.
TM(1:0) : these bits control the functions of the Input (Mask) Registers bits.

TestPattEnable : if zero the digital test pulse command generate 1 BC long pulse per unmasked channels. If one, the 8 bits TestPatt1(3:0) and TestPatt2(3:0) are used to create the test pulse patterns applied to Unmask channels or Mask channels.
TestPatt1(3:0) are used to create the test pulse patterns applied to Unmask channels.
TestPatt2(3:0) are used to create the test pulse patterns applied to Mask channels.
TestPulse Disable : if set it prevents any spurious activation of a digital test pulse at the Pipeline inputs (SEU mitigation).

RRmode[1:0]	Meaning
00	Read Register disabled
01	Read Register if no pending LP/PR
10	One Read Register if no PR pending, when RRforce is set to one in register $00.
11	Unused

Table 9-31: RRmode settings

Register $21 :
CurrDrive(3:0) : set current drive of DAT outputs
CalPulseEnable : When set enables the analogue pulse functions at the input of channels
CalPulsePolarity swaps the 8BC wide analog calibration pulse polarity

Register $22 :
Latency(8:0) sets the latency in the L0 pipeline in number of BC clocks (default at reset is 16)
PreL0ID(8:0) is the preset value of the internal L0ID counter (default is $00)
L0IDPreset : with this bit at zero the L0ID number starts from $1FF (hence has the value 0 at reception of the first L0 after a SoftReset or L0IDReset command). With this bit at one the start value is given by the PreL0ID(8:0) bits.
BCFlagEnable : when set enables flag generator if a BCID count mismatch is found between the BCID counter value at event time and the BCID counter value at L0 time.
BCoffset(7:0) : Preset value for the delta between the BCID counter value at event time and the BCID counter value at L0 time.

Register $23 :
Det_mode(1:0) are bits controlling the Input Register detection criteria according to Table-9-17
Max_Cluster(5:0) : if the bit Max_Cluster_Enable is set, these bits value fixes the maximum number of clusters sent per event.
Max_Cluster_Enable : at one limits the number of clusters to the value represented by Max_Cluster(5:0). At zero the number of packets can reach the maximum possible number of clusters per LP or PR event ie. 64.

Table 9-32: STATUS REGISTER $30 (-$3E)

Addresses range $30 to $3E is reserved for Status Registers (15 registers of 32 bits)

	STAT0	STAT1	STAT2	
	$30	$31	$32	$33
31	CR47SEU			
30	CR43SEU			
29	CR39SEU			
28	CR35SEU			
27	CR31SEU			
26	CR27SEU			
25	CR23SEU			
24	CR19SEU			
23	CR15SEU			
22	CR11SEU			
21	CR7SEU			
20	CR3SEU			
19	MT7SEU			
18	MT6SEU			
17	MT5SEU			
16	MT4SEU			
15	MT3SEU			
14	MT2SEU			
13	MT1SEU			
12	MT0SEU			
11	TopLSEU			
10	SCRegSEU			
9	ADCS7SEU			
8	ADCS6SEU		BCIDFlag	
7	ADCS4SEU		LocalL0ID(7)	
6	ADCS3SEU	LPFIFOOVFL	LocalL0ID(6)	
5	ADCS2SEU	PRFIFOOVFL	LocalL0ID(5)	
4	ADCS1SEU	ReadRegOVFL	LocalL0ID(4)	
3	CFG3SEU		LocalL0ID(3)	
2	CFG2SEU	LPFIFOFull	LocalL0ID(2)	
1	CFG1SEU	PRFIFOFull	LocalL0ID(1)	
0	CFG0SEU	ReadRegFull	LocalL0ID(0)	
SEUbit	no	no	no	no
model	reg32ro	reg32ro	reg32ro	reg32ro
ResetValue	00000000	00000000	00000000	00000000

Register $30 :
This register contains the SEU flags generated in the triplicated various registers (if one SEU occurs, the protected register value may not change because of the triplication but the SEU bit flag is set)
Register $31 :
This register contains the Overflow and Full flags of the internal FIFOs (LP FIFO, PR FIFO, ReadRegister FIFO). “Full” indicates that the next write in the FIFO will overwrite data but data has currently not been overwritten. “Overflow” indicates that one overwrite at least as occurred, hence the oldest data is lost.
Register $32 :
LocalL0ID value (incremented according to L0, picked up at the time the Status Read command is executed). The LocalL0ID value is given for information only, as the L0ID values are distributed together with the L0 signal through the LCB protocol

Register $33 :
eFuse Register Data (Unique Chip Identification). The number of bits has to be fixed.

Table 9-33: TRIMDAC REGISTERS ($40 to $67, 40 registers)

Each 32 bits register in the range $40 to $5F contains the 4 LSB bits of the TrimDAC for 8 channels. In such a way the 32-bit register contains the value for 8 channels.
Each 32 bits register in the range $60 to $6F contains the MSB bit of the TrimDAC for 32 channels.
The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as for the readout (column 2 in Table 9-5).

	TrimDAC0-31	TrimDAC32-40
	$40 to $5F	$60 to $67
31	TRIMDAC<3> CH7:mod8	TRIMDAC<4> CH31:mod32
30	TRIMDAC<2> CH7:mod8	TRIMDAC<4> CH30:mod32
29	TRIMDAC<1> CH7:mod8	TRIMDAC<4> CH29:mod32
28	TRIMDAC<0> CH7:mod8	TRIMDAC<4> CH28:mod32
27	TRIMDAC<3> CH6:mod8	TRIMDAC<4> CH27:mod32
26	TRIMDAC<2> CH6:mod8	TRIMDAC<4> CH26:mod32
25	TRIMDAC<1> CH6:mod8	TRIMDAC<4> CH25:mod32
24	TRIMDAC<0> CH6:mod8	TRIMDAC<4> CH24:mod32
23	TRIMDAC<3> CH5:mod8	TRIMDAC<4> CH23:mod32
22	TRIMDAC<2> CH5:mod8	TRIMDAC<4> CH22:mod32
21	TRIMDAC<1> CH5:mod8	TRIMDAC<4> CH21:mod32
20	TRIMDAC<0> CH5:mod8	TRIMDAC<4> CH20:mod32
19	TRIMDAC<3> CH4:mod8	TRIMDAC<4> CH19:mod32
18	TRIMDAC<2> CH4:mod8	TRIMDAC<4> CH18:mod32
17	TRIMDAC<1> CH4:mod8	TRIMDAC<4> CH17:mod32
16	TRIMDAC<0> CH4:mod8	TRIMDAC<4> CH16:mod32
15	TRIMDAC<3> CH3:mod8	TRIMDAC<4> CH15:mod32
14	TRIMDAC<2> CH3:mod8	TRIMDAC<4> CH14:mod32
13	TRIMDAC<1> CH3:mod8	TRIMDAC<4> CH13:mod32
12	TRIMDAC<0> CH3:mod8	TRIMDAC<4> CH12:mod32
11	TRIMDAC<3> CH2:mod8	TRIMDAC<4> CH11:mod32
10	TRIMDAC<2> CH2:mod8	TRIMDAC<4> CH10:mod32
9	TRIMDAC<1> CH2:mod8	TRIMDAC<4> CH9:mod32
8	TRIMDAC<0> CH2:mod8	TRIMDAC<4> CH8:mod32
7	TRIMDAC<3> CH1:mod8	TRIMDAC<4> CH7:mod32
6	TRIMDAC<2> CH1:mod8	TRIMDAC<4> CH6:mod32
5	TRIMDAC<1> CH1:mod8	TRIMDAC<4> CH5:mod32
4	TRIMDAC<0> CH1:mod8	TRIMDAC<4> CH4:mod32
3	TRIMDAC<3> CH0:mod8	TRIMDAC<4> CH3:mod32
2	TRIMDAC<2> CH0:mod8	TRIMDAC<4> CH2:mod32
1	TRIMDAC<1> CH0:mod8	TRIMDAC<4> CH1:mod32
0	TRIMDAC<0> CH0:mod8	TRIMDAC<4> CH0:mod32
SEUbit	CR3SEU-CR31SEU	CR35SEU-39SEU
model	reg32tr	reg32tr
Reset state	00000000	00000000

Note : one SEU flag bit is generated for a group of 4 registers. For the 40 TrimDAC registers there are 10 SEU bit names : CR3SEU CR7SEU CR11SEU CR15SEU CR19SEU CR23SEU CR27SEU CR31SEU CR35SEU CR39SEU.

Table 9-34: Calibration Enable REGISTERS ($68 to $6F, 8 registers)

Each 32 bits register contains 1 bit per channel enabling the calibration pulse.
The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as for the raedout (column 2 in Table 9-5).

	CalREG0-7
	$68 to $6F
31	CAL_EN CH31:mod32
30	CAL_EN CH30:mod32
29	CAL_EN CH29:mod32
28	CAL_EN CH28:mod32
27	CAL_EN CH27:mod32
26	CAL_EN CH26:mod32
25	CAL_EN CH25:mod32
24	CAL_EN CH24:mod32
23	CAL_EN CH23:mod32
22	CAL_EN CH22:mod32
21	CAL_EN CH21:mod32
20	CAL_EN CH20:mod32
19	CAL_EN CH19:mod32
18	CAL_EN CH18:mod32
17	CAL_EN CH17:mod32
16	CAL_EN CH16:mod32
15	CAL_EN CH15:mod32
14	CAL_EN CH14:mod32
13	CAL_EN CH13:mod32
12	CAL_EN CH12:mod32
11	CAL_EN CH11:mod32
10	CAL_EN CH10:mod32
9	CAL_EN CH9:mod32
8	CAL_EN CH8:mod32
7	CAL_EN CH7:mod32
6	CAL_EN CH6:mod32
5	CAL_EN CH5:mod32
4	CAL_EN CH4:mod32
3	CAL_EN CH3:mod32
2	CAL_EN CH2:mod32
1	CAL_EN CH1:mod32
0	CAL_EN CH0:mod32
SEUbit	CR43SEU-CR47SEU
model	reg32tr
Reset State	00000000

Note : one SEU flag bit is generated for a group of 4 registers. For the 8 TrimDAC registers there are 2 SEU bit names : CR43SEU CR47SEU.

Table 9-35: Hit Counters REGISTERS ($70 to $AF, 64 registers)

Each 32 bits register contains the 8 bit counts of the Hit Counters for 4 channels.
The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as for the readout (column 2 in Table 9-5).

	HitCountREG0-63
	$70 to $AF
31	HitCount<7> CH3:mod4
30	HitCount<6> CH3:mod4
29	HitCount<5> CH3:mod4
28	HitCount<4> CH3:mod4
27	HitCount<3> CH3:mod4
26	HitCount<2> CH3:mod4
25	HitCount<1> CH3:mod4
24	HitCount<0> CH3:mod4
23	HitCount<7> CH2:mod4
22	HitCount<6> CH2:mod4
21	HitCount<5> CH2:mod4
20	HitCount<4> CH2:mod4
19	HitCount<3> CH2:mod4
18	HitCount<2> CH2:mod4
17	HitCount<1> CH2:mod4
16	HitCount<0> CH2:mod4
15	HitCount<7> CH1:mod4
14	HitCount<6> CH1:mod4
13	HitCount<5> CH1:mod4
12	HitCount<4> CH1:mod4
11	HitCount<3> CH1:mod4
10	HitCount<2> CH1:mod4
9	HitCount<1> CH1:mod4
8	HitCount<0> CH1:mod4
7	HitCount<7> CH0:mod4
6	HitCount<6> CH0:mod4
5	HitCount<5> CH0:mod4
4	HitCount<4> CH0:mod4
3	HitCount<3> CH0:mod4
2	HitCount<2> CH0:mod4
1	HitCount<1> CH0:mod4
0	HitCount<0> CH0:mod4
SEUbit	-
model	reg32
Reset state	00000000

Note : No SEU flag is provided, the registers are not protected against SEU, as these registers are used outside of physics. When used inside physics, they may be used as pipeline SEU counters if there are no physics hits entering the L0buffer (by masking all channels).

9.16 Chip ID

The ABCstar chip address field is 4 bits, different from the ABCD case, where it was 6 bits (and only 4 bits transmitted).
To enable a chip to be individually addressed five inputs ID(3:0) will be used to implement a geographical addressing scheme. This is because there may be up to 16 chips to be addressed on each hybrid. These inputs will be wire bonded to a unique set of logic levels for each chip. This set of logic levels will form a geographical address that will enable individual chips on the hybrid to be addressed. Each address input has an internal pull-up. The address "1111" (15) is reserved for global addressing (all chips respond).

9.17 Chip Initialisation and Configuration

The following sequence of instructions should normally be sent to the chip after power-up
1) Send command to load the configuration registers with the appropriate settings.
2) Send a command to load the mask registers
3) Send a series of commands to load the DAC register/s and Delay registers
The chip will now be in a state to receive L0 and PR or LP trigger commands and send data.

9.18 Resets

There are several kinds of reset in the system.

9.18.1 RST_b pin

The external reset pin acts as a general reset (identical to Power up Reset or SoftReset), but is provided only as a safe hardware reset access. Acting on it is not expected in detector operation.

9.18.2 Power up Reset

The power-up reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips registers to their default value, and clears all the buffers in the chip, thus placing the chip into a well defined state. This type of reset is issued automatically when power is applied to the chip. Provision will be made to enable this signal to be supplied externally to the chip, through the input RSTB_pad.

9.18.3 Reset by Long LP_PR input state (discarded ?)

An alternative method for resetting the circuit is to provide more than 32 consecutive BC wide "one" state on the LP_PR input. The reset action is similar to the one provided by the power up reset or external Reset through RSTB_pad. It requires that the BC clock is present.

9.18.4 Soft Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to reset all the registers to their default value, and clears the pointers and readout mechanism, hence losing the chip configuration and the physics data. It should result in a chip being in the same status as after a power-up reset.

9.18.5 SYS Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset can be issued to the chip periodically during data taking to eliminate synchronization errors.
1) Upon receipt of the SYSReset command, the ABC-130 chip resets all internal counters and clears pending operations. If it was transmitting data, it terminates this immediately.

9.18.6 SEU Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to reset the bits tagging SEU events in the register $30.

9.18.7 BC Reset (BCR)

This type of reset is sent to the chip via a fast command. Its purpose is to zero the Beam Crossing counter. It has no effect on the operation of any other part of the chip.

9.18.8 Local L0ID Preset

This type of reset is sent to the chip via a command instruction. Its purpose is to preset the Local L0ID counter. It has no effect on the operation of any other part of the chip. If the bit 16 in the configuration register $22 is at zero the L0ID preset value is $FF (hence first L0 is identified with number $00). If the bit 16 in the configuration register $22 is at one the L0ID preset value is given by the bits 8 to 15 in the configuration register $22.

9.19 Default Register Values

On power up or SoftReset command, the contents of the configuration registers will be set to default. This results in the following configuration (summary) :
Minimum Bias currents for the analogue channels
Maximum channel threshold value
TrimDACS setting at 0
All calibration enable at 0
SLVS drivers current at mid-range
L0 counter at $FF and BC counter at $00
Register Readout is enabled
Input register in Mask mode
L0 buffer latency at $0F
L0ID preset at $FF, preset function disabled
Detection mode 00
CF packet disabled
No packet number limit
After proper synchronization of the BCR_IN inputs to the BC and CLK clocks, a repetitive signature pattern should be emitted at the output (TBD), until valid commands are executed to stop the transmission and/or configure the chip (TBD).

9.20 Other items to be described

9.20.1 E-FUSE option

9.20.2 Analogue Monitor option

9.20.3 Initialisations signatures

Like : After powerup, application of clocks, there is the requirement that the ABCstar detects correctly the frame on the LCB_IN inputs, a preliminary step necessary to get the capability to act on the chip with the CMD bits and commands. A repetitive “good-condition” signature (like a significant data pattern) should be delivered spontaneously at the output of the chip when the correct framing conditions are met. The signature pattern emission should be stopped by an appropriate command (TBD).

9.21 Programming Model

The various registers of the ABCStar ASIC should be programmed after powerup according to the register description in the functional description. The default state at power up is described in 9.19.

10 Radiation Tolerance and Other Special Requirements

The requirements for the accumulated ionizing dose are around 350KGy for the inner barrel layer. The radiation tolerance will be measured up to 700KGy.

Various mitigation techniques are implemented in the design, to lower the occurrence of SEU bit flips, that may result in single or multiple bit errors (that can be accepted up to a certain point) or into functional interrupts (SEFI).

Below are given some expected values for bit error rates, that are projected from the current SEU error rates measurements done with the ABC130 ASIC.

The ABCStar chip should not experience any latchup in the LHC radiation environment.

10.1 Error rate in the L0BUFFER

Calculations to estimate the probability of bit flip in the L0BUFFER.
Bit flip cross section : 5E-14/cm2 (CHARM measurements, June 2015)
Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.
One run year time (6 months run) 15E6 seconds
Hit rate per second : 4.0E6/cm2.s
Bit flip 2E-7 per second per bit
In 12.8us : probability of bit flip per bit : 2.56E-12
For 164Kbits memory : probability of one bit flip per 30.5 seconds per memory
In 12.8us : probability of one bit flip within 164K : 42E-6

From these numbers it appears that the physics data bit error rate will be 1 bit error per 1525 seconds (1/40 reduction rate and 256 physics data bit over 320), ie per ~1.5E9 packets transmitted (a bit error translates in a false cluster position or false hit bit)

Considering only the 8 BCID bits for event identification the rate is reduced to one bit flip per 4.88E4 seconds per chip, ie per 48.8E9 packets transmitted (a BCID bit error translates into a false packet-to-event identification).

10.2 Error rate in the EvtBUFFER

Calculations to estimate the probability of bit flip in the EvtBUFFER
Bit flip cross section : 5E-14/cm2 (CHARM measurements, June 2015)

Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.
One run year time (6 months run) 15E6 seconds
Hit rate per second : 4.0E6/cm2.s
Bit flip 2E-7 per second per bit
In 128us : probability of bit flip per bit : 2.56E-11
For 41Kbits memory : probability of one bit flip per 122 seconds per memory
In 128us : probability of one bit flip within 41K : 1.05E-6
From these numbers it appears that the physics data bit error rate will be 1 bit error per 152 seconds, (256 physics data bit over 320) ie per 152M packets transmitted (a bit error translates in a false cluster position or false hit bit).
Considering only the 16 bits for event identification (L0ID and BCID) the rate is reduced to one bit flip per 2440 seconds, ie per 2.44E9 packets transmitted (a ID bit error translates into a false packet-to-event identification).

11 Testing, Validation and Commissioning

Describe testing procedures that will be used to demonstrate that the fabricated component meets the specifications. This should include radiation testing if radiation tolerance is one of the requirements.

It is not required to complete this section prior to the first specification review but it should be completed prior to the PDR. Prior to the FDR, the production testing must be described, and prior to the PRR, commissioning plans must be included.

12 Reliability Matters

12.1 Consequences of Failures

Describe the consequences to the detector of a failure of one unit of this component, e.g. x% of the sub-detector channels will be lost, or one stave or petal could overheat causing delamination of its component parts. The severity of the consequences will determine the level of reliability required and the level to be validated by QA and QC procedures defined in sections 12.4 and 12.5.

12.2 Prior Knowledge of Expected Reliability

Based upon industry experience, collaboration experience or personal experience, give an estimate of the reliability of this component.

12.3 Measures Proposed to Insure Reliability of Component and/or System

Include such measures as conservative design techniques (give specific examples), redundancy and possibilities to replace failed part. . If failed part could be replaced, estimate the difficulty and time involved for installing replacements,

12.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

Describe what stress tests will be applied during the development period to validate the reliability of this component. Give a brief outline of any appropriate reliability theory being used. These tests could involve destructive tests.

It is not required to complete this section prior to the first specification review but it must be completed prior to the PDR. It is strongly recommended that these plans be reviewed and approved prior to the actual PDR to avoid the possibility of failing the PDR and thus delaying the fabrication or construction of the prototype parts,

12.5 Quality Control to Validate Reliability Specifications during Production

Describe what stress tests will be applied during production, possibly on a sampling basis, to validate the reliability of production units. These could likely be destructive tests. Specify the required sampling percentage of production units.

It is not required to complete this section prior to the first specification review but it must be completed prior to the FDR. It is strongly recommended that these plans be reviewed and approved prior to the actual FDR to avoid the possibility of failing the FDR and thus delaying the fabrication or construction of the pre-production parts,

13 References

If there are any references pertaining to the development of this component, list them here.