ATLAS ITk Electronics Specification
Component or Facility Name: HCCStar

Version: V 0.2

Abstract

The HCCStar chip will be the digital front-end ASIC for the readout of the ITK Silicon Strips detector in the ATLAS experiment for the HL_LHC collider at CERN.

Revision History			
Rev. No.	***Proposed Date*** / ***Approved Date***	***Description of Changes*** *(Include section numbers or page numbers if appropriate)*	***Proposed By: author*** / ***Approved By: reviewer***
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1 Conventions and Glossary

1.1 Conventions

Signal names ending with the letter ‘b’ are active low, all other signals are active high, unless otherwise noted.

Hexadecimal numbers are noted either by prepended a ‘$’ character in front of them or using Verilog notation: <number of bits>’h<hexadecimal value>, eg (32’h0123beef).

1.2 Glossary

BC – Beam Crossing Clock, 40 MHz

BCID – Bunch Counter ID. An 8-bit clock counter used to detect front-end desynchronization.

BCR – Bunch Counter Reset. A 1-bit BC-synchronous command that resets the BCID counter to zero. Used to ensure front-end synchronization. It is issued through the LCB input.

CMD – Command signal. Used for asynchronous setup of the ABCstar or certain resets.

Command Sequence – A set of command frames starting with a Start of Sequence frame and ending with an End of Sequence frame that together make up a single command. The frames in a Command Sequence must be in order, but need not be consequtive.

L0 – Beam crossing synchronous pulse used to transfer the strips data from the fixed latency pipeline to the Random Access Memory (RAM) used as an event buffer (EvtBuffer). L0 does not generate an ABCstar readout.

L0tag – 7 bits value attached to each L0. It is used to safely identify events with a single identifier number.

LCB – L0A/CMD/BCR signal

LP – Low Priority Readout Request. An asynchronous request to read out an event with the given L0ID from the ABCstar Event Buffer with low priority (but still higher priority than Register Read requests).

lsb – Least Significant Bit. This is the bit in the 2^0 place.

msb – Most Significant Bit. This is the bit with the most value in the word.

PR – Priority Readout Request. An asynchronous request to read out an event with the given L0ID from the ABCstar Event Buffer with priority over LP and register read requests.

RCLK – Readout Clock. A 160 MHz clock from the HCCStar used to clock the serial output bit stream from the ABCStar.

2 Related Documents

TBD

3 Description of Component or Facility

The HCCStar ASIC is the digital interface for the ITk Strips hybrids, both in the endcap and in the barrel. It receives the 40 MHz bunch crossing clock and 160 Mbps control lines on multidrop line originating from the End-of-Structure (EOS) card. The HCCStar interprets the control data and forwards the clock and relevant control data to between 5 and 11 ABCStar ASICs on the hybrid on shared, multidrop lines. This control data includes triggers, event data readout requests, register read and write commands, test pulse generation, and resets. ABCStar event data, as well as register read data, are sent on point to point lines back to the HCCStar. The HCCStar combines data for the same event from all input and sends out this combined data at either 320 or 640 Mbps on a point to point link on the bus tape to the EOS.

The HCCStar is provided as bare die and is electrically connected to the hybrid with bond wires.

4 Interfaces

This component interfaces to other components listed in Table 4.1.

Table 4.1: Components which Interface to This Component

Name of Component	Name of Component Specification
ABCStar ASIC	TBD
AMAC ASIC	TBD
Barrel Hybrid Board	TBD
Endcap Hybrid Board	TBD
Barrel Bus Tape	TBD
Endcap Bus Tape	TBD

5 Physical Description

The HCCStar ASIC will be provided as unpackaged die. It is expected that the die size will be 3.5mm x 5.2 mm, as measured between the outside pad edges. The physical die will be slightly larger due to manufacturing constructs such as the seal ring.

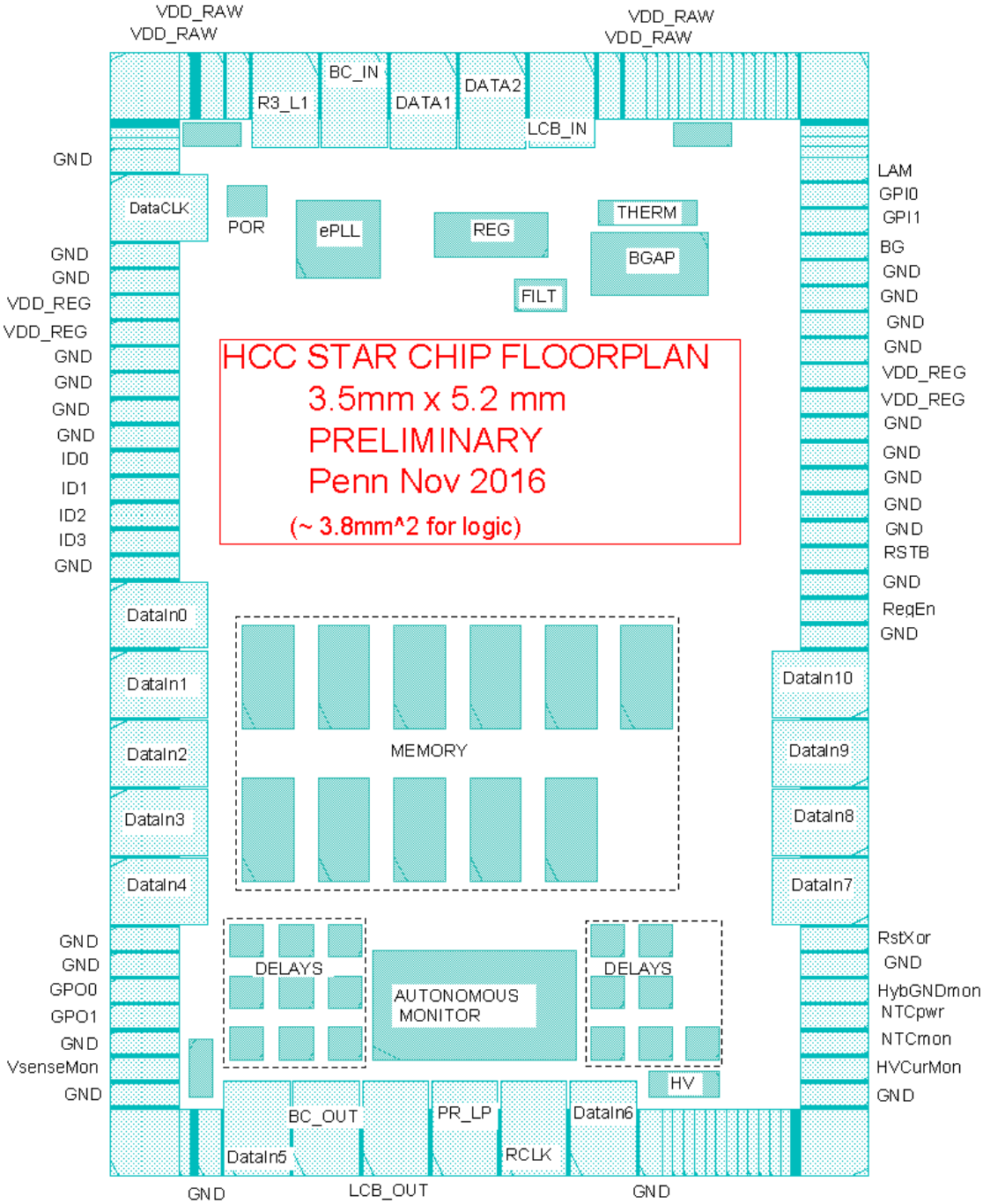

Figure 5.1: HCCStar Floorplan

Table 5.1: Pad list

Class	Type	Dir	Name	#	Default	Description
Supply		In	VDD_RAW	4	1.3 – 1.6V	Power In
		In/Out	VDD_REG	4	1.2V	Core Power
		In	GND	24+	0V	Voltage Return
Diagnostic		Out	BG	1	0.5 – 0.8V	Band Gap
Address	SE	In	ID0-3	4	Pull up	Address Bits: Bonding to GND sets bit to '1'
Bond Options		In	RstXor	1	Pull Up	HI = Invert sense of RSTB
		In	OutEncode	1	Pull Up	HI = Output 8b10b encoded
DATA	LVDS	In	DataIn	11	0	ABC Data Inputs **100Ω**
	LVDS	Out	Data	2	0	Output Data
	LVDS	Out	DataCLK	1	0	Clock in phase with Output Data
Logic	SE	In	GPI	2	Pull Up	General Purpose In
	SE	In	RegEn	1	Pull Up	High = Enable Regulator
	SE	In	RSTB	1	Pull Up	Low = Hard Reset
	SE	In	LAM	1	Pull Up	Rising Edge = LAM
	SE	Out	GPO	2	Low	General Purpose Out
Stave Control	LVDS	In	BC_IN	1		40 MHz System Clock
	LVDS	In	LCB_IN	1	Idle	L0A/CMD/BCR
	LVDS	In	R3_L1	1	Idle	R3 & L1 Readout Req
Hybrid Control	LVDS	Out	BC_OUT	1	Low	40 MHz Clock
	LVDS	Out	LCB_OUT	1	Idle	L0A/CMD/BCR
	LVDS	Out	PR_LP	1	Low	Readout Request
	LVDS	Out	RCLK	1	Low	160 MHz Clock
Analog Monitor	Analog	In	Vsense	1	DC	Generic Voltage Measurement
	Analog	In	NTC	1	DC	Temperature Measurement
	Analog	In	AMRef	1	DC	GND Reference for AM

6 Manufacturer

The HCCStar will be fabricated in Global Foundry (Ex-IBM foundry) in the CMOS8RF_DM 130nm technology. The wafers are standard 8 inches. No packaging is foreseen.

7 Power

The nominal power requirements are listed in Table 7.1. There is significant uncertainty in the current values. It is expected that the power-on nominal current will be approximately 15 mA lower. In addition, at 1 MRad TID, the nominal current is expected to be around 225 mA, again with significant uncertainty.

Table 7.1: Power Requirements

Name	Max/Nom/Min V Supplied	Nom/Max I	Other Requirements
VDD_RAW	1.6/1.5/1.15	200 mA? / TBD	TBD

8 Input/Output

Table 8.1: Input and Output Signals

Name	In, Out or I/O	Signal Type	Description
DataIn	Input	LVDS point to point	Data inputs with internal termination
Data	Output	LVDS point to point	HCC Data outputs
Data Clock	Output	LVDS point to pint	HCC Data clock – diagnostic use
Control / Clock	Input	LVDS multi-drop	Input from Stave Side. High Z
Control / Clock	Output	LVDS multi-drop	Output to hybrid. High Z
Digital I/O	Input or Output	CMOS point to point	Regulator Control. Look At Me. Etc.

8.1 LVDS

The LVDS driver and receiver designs have been slightly evolved from what was used in the first version of HCC. We maintain the programmable current capability between about 0.5 to 6mA on drivers, add a resistor defined common mode output voltage at Vdd/2 (~600mV) and a disable function that drops the driver current to near zero. The receivers are bandwidth limited to about 160MHz in a similar way to the bandwidth limitation implementation that was tested on the Repeater Chip [cite Repeater Chip].

8.2 Receiver Control Signals – GBT Side

GBT data receivers are bandwidth limited to about 160MHz – twice the possible data frequency for the input signals. It may be necessary to AC couple due to the GBTX SLVDS-compatible 200mV common mode output, which is not compatible with the predicted return-voltage increase from End-of-Structure (EOS) card to the end of the

stave. Thus the HCCStar keeps the hysteresis circuits that have been successfully employed on previous ASICS, eg HCC130. AC coupling will require the use of 120pF capacitors on each HCCStar. This value may be changed when the lpGBT design is finalized. Wirebond-selectable terminations are not included due to the risk that unpowered HCCstar chips may pull down the multi-drop lines making communication impossible if DC coupling is used.

8.3 Receiver Data Signals – Hybrid Side

Each LVDS input channel utilized bandwidth limited (160MHz) receivers with 100 ohm terminations on the hybrid side input to the HCCStar.

8.4 Driver Control Signals – Hybrid Side

The HCCStar uses programmable current (0.5 to 6mA) LVDS outputs capable of multi-drop signaling to 10 ABCStar control inputs. The LVDS common mode will be maintained at Vdd/2 (~ 600mV) by a resistive divider on each LVDS driver output.

8.5 Driver Data Signal – GBT Side

The HCCStar has two programmable-current drivers capable of up to 800Mbps data rate. A resistive divider will maintain a Vdd/2 common mode although the common mode operational range will be within about 300mV from the upper and lower rails.

9 Detailed Functional Description and Specification

The top level block diagram for HCCStar is show in Figure 9.1. System clock and control signals flow from the stave through the Control Path in the HCC. The Control Path interprets the signals for its own purposes and modifies them for use in the ABCStar ASICs on the hybrid where the HCCStar is located. Data coming back from the hybrid's ABCStar ASICs goes into the HCCStar's Input Channels, one per ABCStar. The Packet Builder collects the data from various Input channels and sends out packets to the stave. Each of these three components is described below.

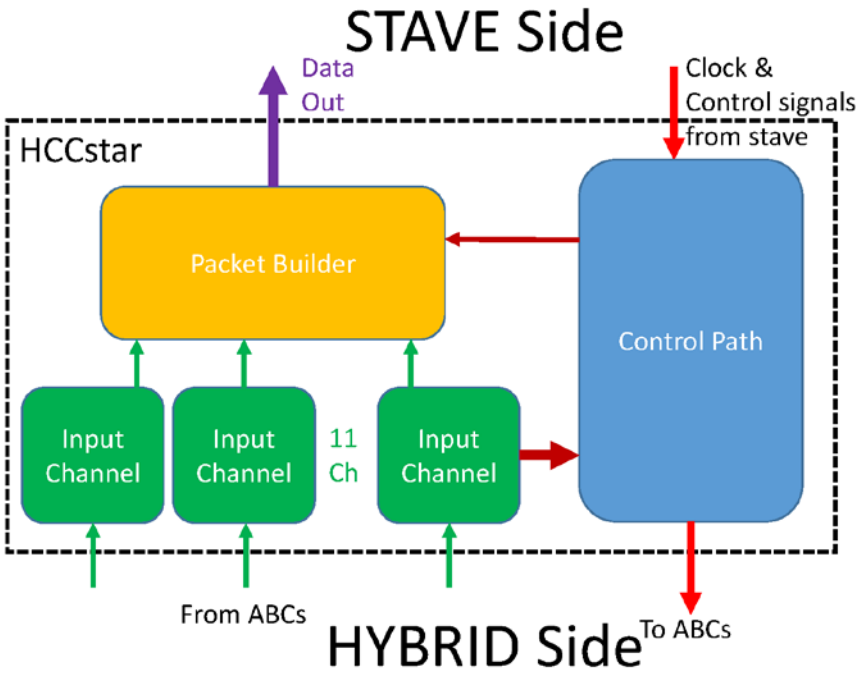

Figure 9.1: HCCStar Top Level Block Diagram

9.1 Control Path

The block diagram for the Control Path is shown in Figure 9.2. The control protocols are described below, followed by a description of its behavior.

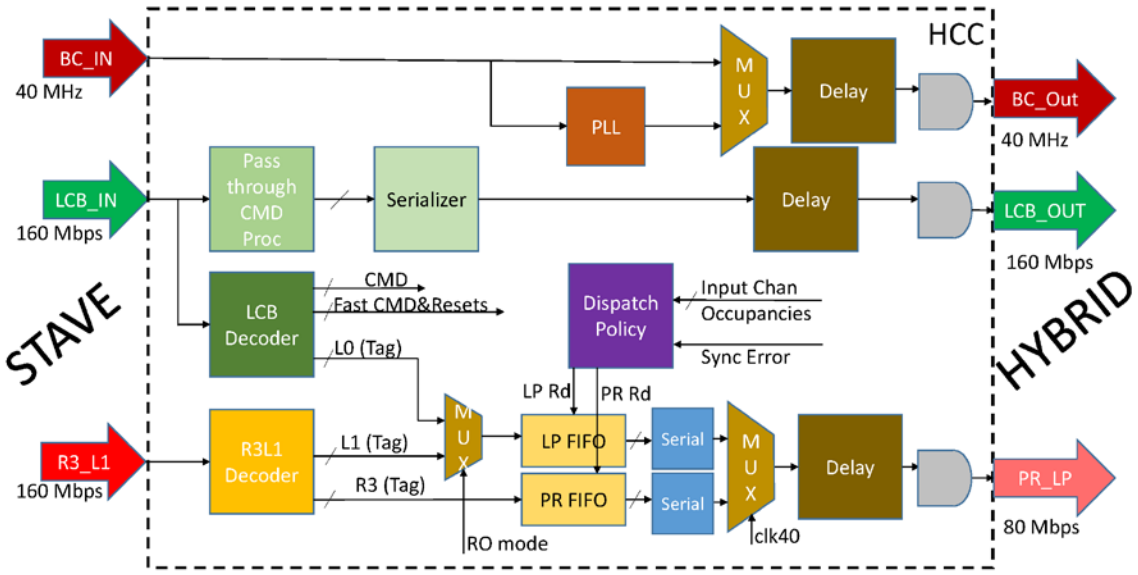

Figure 9.2: Control Path Block Diagram

9.1.1 Clock

The HCCStar receives its 40 MHz system clock on the LVDS BC_IN line. This is used as a reference for a PLL that provides the ASIC with three independent, adjustable phase 160 MHz clocks, three independent, adjustable phase 320 MHz clock, a recovered 40

MHz clock and a 640 MHz clock that is produced from two internal phases of the 320 MHz clock.

The BC_OUT LVDS clock can be selected to be either the received BC_IN clock or the PLL recovered 40 MHz clock. In either case, it can be delayed with a coarse/fine delay block. This block provides for coarse delay adjustment in four 6.25 ns steps and fine delay adjustment in 16, ~1.9 ns steps. At power-up or hard reset, the BC_OUT signal is configured to be the BC_IN clock.

The BC_OUT can be turned on and off through a setting in a register. The default state of BC_OUT at power-up and hard reset is OFF.

9.1.2 LCB Protocol

The LCB signal is 6b8b[1] encoded and sent over an LVDS bus that is shared by between two and ten HCCStar ASICs. The basic unit of data transmission is a pair of 8-bit symbols called a frame, providing 12 bits of payload per frame.

9.1.2.1 L0A

Since the LCB signal is transmitted at a data rate of 160 Mbps, a single frame takes 100 ns, or 4 BC, to transmit. Thus, a frame containing L0A data must cover 4 BC worth of L0A activity information. With an L0A, a 7-bit identifier, called the L0tag, is sent. This identifier is used to request event data from the ABCStar. In addition, the BCR signal may come during a 4 BC space that has L0As. The payload for an L0 frame is shown in Table 9.1. The msb of the L0A mask refers to the earliest BC, while the lsb refers to latest. A '1' in the L0A mask indicates that there is an L0A in the corresponding BC. A '1' in the BCR field indicates that there is to be a BCR in the latest BC covered by the L0A mask. It is important to note that this implies that frames must have a fixed alignment with respect to the LHC orbit signal in order to guarantee that the BCR is executed at the front-end at the appropriate time.

	MSB		**LSB**
Field Name	BCR	L0A mask	L0tag
# of bits	1	4	7

Table 9.1: LCB L0 Frame

L0 frames are only sent when at least one of the covered BC has an L0A or a BCR needs to be sent. Therefore, at least one of the first five bits will be '1'.

9.1.2.2 Fast Commands and Resets

Fast commands and resets are sent with a frame that contains the 6b8b control symbol K3 plus a symbol whose payload is composed of a 2-bit BC selector indicating in which BC the command or reset is to be generated and a 4-bit action, indicating which command or reset to generate. A value of 0 for the BC selector refers to the earliest BC, while a value of 3 refers to the latest. The payload for the second symbol is shown in Table 9.2. The list of fast commands is show in Table 9.3. Note that fast commands are broadcast commands and are interpreted on all ASICs that share the LCB control line.

[1] 6b8b is an encoding scheme that produces 8-bit symbols from 6-bit input words. It guarantees a minimum signal transition density and provides 4 8-bit out of band control codes, which have no 6-bit representation, designated K0, K1, K2 and K3.

	MSB	LSB
Field Name	BC Select	Command
# of bits	2	4

Table 9.2: K3 Frame Payload

Index	Command
0	
1	
2	SYS Reset
3	Soft Reset
4	SEU Register Reset
5	Cal Pulse
6	Digital Pulse
7	
8	RR force
9	
10	Count Reset

Table 9.3: Fast Commands

9.1.2.3 Register Reads and Writes

Register reads and writes are composed of a sequence of frames. These frames do not need to be consecutive, but must be in order. Frames interleaved in a register command sequence may be of any type.

A register command sequence starts with a frame composed of the K2 control symbol followed by a symbol containing an ABC/HCC bit and the HCC ID for the HCCStar on the target hybrid. If the ABC/HCC bit is '1' the comand is an ABCStar command otherwise it is an HCCStar command. If the Stop/End bit is '1', it indicate the start of a command sequence, while '0' indicates it is the end of a command sequence. An HCC ID of '1111' is interpreted to be a broadcast address and all HCCStar ASICs will respond. A Special HCC ID of 1110 is used to indicate that the command sequence should be ignored. The payload for the second symbol in this K2 frame is shown in Table 9.4.

	MSB		LSB
Field	ABC/HCC	Stop/End	HCC ID
# of bits	1	1	4

Table 9.4: K2 Frame Payload

The K2 frame is followed by two header frames. The 5 msbs of the header frames' payload are '00000' to distinguish these frames from L0 frames. The remainder of the payload is a Read/Write bit, the ABC ID of the target ABCStar ASIC (these bits are ignored if it is an HCC command) and the address of the target register. If the Read/Write bit is '1', the command is a read command otherwise it is a write command. The mapping of these fields to the frame payloads is shown in Table 9.5.

Frame		MSB			LSB
1	**Field**	Marker	R/W	ABC ID	Reg Addr MSB
	Value	00000			
	# of bits	5	1	4	2
2	**Field**	Marker		Reg Addr LSB	SPARE
	Value	00000			
	# of bits	5		6	1

Table 9.5: Register Command Header Frames

For register read commands, the header frames are followed by a K2 frame with the Start/End bit set to 0, indicating the end of the sequence. If the K2 frame has the Special HCC ID (1110), the command is discarded and no operation is executed. However, if the HCC ID is any other value, the command is executed.

For register write commands, the two header frames are followed by 5 frames containing the value to write into the register, as shown in Table 9.6.

Frame		MSB		LSB
1	**Field**	Marker	SPARE	Register contents [31:28]
	Value	00000		
	# of bits	5	3	4
2	**Field**	Marker		Register contents [27:21]
	Value	00000		
	# of bits	5		7
3	**Field**	Marker		Register contents [20:14]
	Value	00000		
	# of bits	5		7
4	**Field**	Marker		Register contents [13:7]
	Value	00000		
	# of bits	5		7
5	**Field**	Marker		Register contents [6:0]
	Value	00000		
	# of bits	5		7

Table 9.6: Register Data Frames

As with the register reads, the sequence ends with a K2 End frame. Register write commands can be issued without any intervening space between commands.

Register access command sequences may be terminated at any time with a K2 End frame. While not encouraged, a K2 Start frame will terminate and pending command and start a new one. A new command sequence may immediately follow the K2 End frame.

9.1.2.4 Idle

The IDLE frame, composed of the control symbol pair {K0, K1}, will be sent if there is nothing else to send. This frame is used to establish initial synchronization on the link and provide for ongoing validation of synchronization.

9.1.3 R3_L1 Protocol

As with LCB, the R3_L1 signal is 6b8b encoded and sent over an LVDS bus that is shared by between two and ten HCCStar ASICs. The basic unit of data transmission is a pair of 8-bit symbols called a frame. Since the R3_L1 signal is transmitted at a data rate of 160 Mbps, a single frame takes 100 ns, or 4 BC, to transmit.

The R3_L1 protocol contains three types of frames: R3, L1 and IDLE. IDLE frames are as in LCB: the symbol pair {K0, K1}, and is sent when there is nothing else to send.

An R3 frame is composed of a module mask indicating which modules should respond to the request, plus the L0tag of the event to read out. The payload for the R3 frame is as shown in Table 9.7.

	MSB	**LSB**
Field	Module Mask	L0tag
# of bits	5	7

Table 9.7: R3 Frame

The module an HCCStar is associated with is its HCC ID divided by 2. Thus HCC IDs 2 and 3 are module 1, 4 and 5 are module 2, etc. Note that HCC IDs 0, 1 and larger than 11 are invalid for the purposes of R3 and do not correspond to any module. The msb of the module mask corresponds to module 5 and the lsb corresponds to module 1.

An L1 frame is composed of a marker of '00000' to distinguish it from R3 frames and the L0tag of the event to read out. The payload for the L1 frame is as shown in Table 9.8.

	MSB	**LSB**
Field	Marker	L0tag
Value	00000	
# of bits	5	7

Table 9.8: L1 Frame

9.1.4 Control Path Behavior

9.1.4.1 LCB Path

The control path passes the entire LCB control stream through to the LCB_OUT pads, with minimal added latency. The only modification to the LCB stream is the modification of command sequences where the HCC ID specified in the K2 frame does not match the HCCStar ASIC's HCC ID or the broadcast HCC ID (1111). In this case, the command sequence is modified by replacing the HCC ID with a special ID (1110) that is ignored on the ABCStar so that it will not execute on any ABCStar ASIC on the same hybrid. This is done by replacing the K2 frame payload symbol with a symbol that decodes to something that will be ignored by the ABCstar ASIC's LCB decoder.

The outgoing LCB_OUT data stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ~420 and ~830 ps, with a full range of 16 steps.

The LCB_OUT can be turned on and off through a setting in a register. The default state of LCB_OUT at power-up and hard reset is OFF.

The HCC also decodes the LCB control stream for its own purposes. The relevant fast commands and resets are honored by the HCCStar and register command sequences with the ABC/HCC bit set to 0 in K2 frame are decoded for use in the HCCStar. The L0A and L0tag information is also decoded for use in the L0-only single level trigger mode.

9.1.4.2 R3_L1 Path

The FIFO for L1 requests, and the subsequent control path, is named "LP" (Low Priority), as its source may either be L1 from the ATLAS trigger system or directly from L0A triggers decoded in the LCB decoder. The FIFO for R3 requests, and the subsequent control path, is named "PR" (Priority).

In multilevel (L0/R3/L1) readout mode, the L0tags associated with R3 and L1 frames are inserted in separate FIFOs that hold these requests. The L1/LP FIFO will be 64 positions deep. The R3/PR FIFO will be 8 positions deep. Both of these FIFOs will implement the policy that the oldest entry will be discarded if the FIFO overflows. In single level trigger (L0-only) mode, the R3_L1 decoder can be disabled so as not to require signal on that control line. The L0tag from the LCB decoder will be inserted into the L1/LP FIFO.

The data, upon leaving either FIFO, get a 3-bit preamble prepended, are serialized and then time multiplexed based on the 40 MHz BC_OUT clock. The PR bits are sent when BC_OUT is low and the LP bits are sent when BC_OUT is high. This is summarized in Table 9.9.

	Sent left to right, MSB first		
Request	**Preamble**	**Data**	**BC_OUT phase**
PR	101	7-bit L0tag	LOW
LP	110	7-bit L0tag	HIGH

Table 9.9: PR_LP Control Line

The outgoing PR_LP data stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ~420 and ~830 ps, with a full range of 16 steps.

The PR_LP can be turned on and off through a setting in a register. The default state of PR_LP at power-up and hard reset is OFF.

The release of read requests from the PR and LP FIFOs is controlled by a policy block. This block guarantees that a FIFO read does not occur until the previous one has been serialized. It also enforces at least one '0' bit between requests. Furthermore, it will not issue a PR or LP unless all of the enabled Input Channels have space in their respective buffers to handle another event of maximal size. In addition, an Input Channel can request that read requests be held in order to guarantee the link from the ABCStar goes into its quiescent state. This can be done in order to re-establish synchronization.

9.2 Input Channel

The block diagram for the Input Channel is shown in Figure 9.3. There are 11 Input Channels in the HCCStar. The Input Channel receives fixed length packets as a 160 Mbps serial stream from the ABCStar. It separates the data packets based on type and organizes the data for the output Packet Builder. Each Input Channel can be individually enabled or disabled. At Power-On, all Input Channels are disabled.

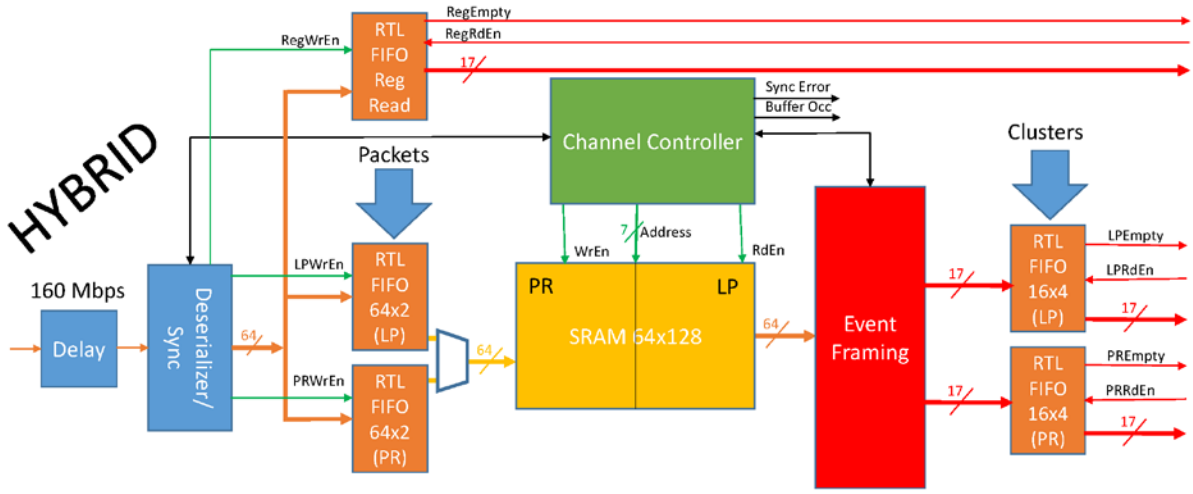

Figure 9.3: Simplified Input Channel Block Diagram

The serial stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ~420 and ~830 ps. The quiescent state of the ABCStar input line is expected to be '0'. Data from the ABCStar are expect to come in fixed-length 64-bit packets, with a 3-bit framing header prepended and one '0' appended as a framing trailer. The expected data format is as defined in the ABCStar Specification[2].

Repeated failure to identify valid packets will be noted in a status register and optionally can cause the Control Path Policy Block to temporarily stop sending readout requests to the ABCStar ASICs. The details of this mechanism are TBD.

The type of data packet is determined by the TYP field. Valid TYP field values are shown in Table 9.10. The ABCStar will only generate packets of the first three types; the rest are used by the HCCStar.

[2] EDMS Document ATU-SYS-ES-0030

TYP code		Meaning
Binary	**Decimal**	
0001	1	PR packet
0010	2	LP packet
0100	4	ABC register read
0111	7	ABC packet “transparent” packet
1000	8	HCC register read
1011	11	ABC full “transparent” packet
1101	13	Reserved
1110	14	Reserved

Table 9.10: TYP codes

The input channel has four operating modes which determine how it handles ABCStar packets: Physics Mode, Register Read Special Mode, Packet Transparent Mode, and Full Transparent Mode. The HCCStar defaults to Physics Mode.

9.2.1 Physics Mode

In physics mode, the framing bits are removed and just 64-bit packet is considered. The SRAM memory is divided into two halves; one half for PR packets and one half for LP packets and the packets are stored in their entirety. The number of packets in each event is counted and compared to a programmed maximum value. The HCCStar can be programmed via a register setting to stop storing packets for any event whose packet count exceeds the maximum. The maximum number of packets allowed will configurable to 1, 2, 4, 8, or 16. The Input Channel will detect the boundary between events to keep an accurate count of the number of pending readout requests in the ABCStar.

The event data packets will be read from the SRAM memory, split into pieces and inserted into a 12-bit wide by 8-position deep FIFO. One of the bit positions will be used exclusively to make the end of events. The first data word pushed into the FIFO will be 8-bit L0tag and 4-bit BCID. Following this will be the 12-bit clusters from the ABCStar, including the Last Cluster bit.

Register read packets will be transfered into a small, 17-bit wide, compiled-logic FIFO. One of the bit positions will be used exclusively to make the end of the register read packet. The entirety of the packet will be saved, but the TYP field will be overwritten with HCCStar hardware Input Channel number to indicate where the packet came from. The 64-bit packet will be split into 4 16-bit pieces and inserted into the FIFO. The size of this FIFO will be 16 (four packets) deep. The policy on this FIFO is that the oldest packet will be discarded on FIFO overflow.

9.2.2 Register Read Special Mode

In Register Read Special Mode, the framing bits are removed and just the 64-bit packet is considered. Any LP or PR packets are discarded and register read packets are stored in the SRAM memory. This mode is useful when trying to read registers quickly, for example, the ABCStar counter registers in calibration mode. All input channels can operate in this mode simultaneously.

9.2.3 Packet Transparent Mode

In Packet Transparent Mode, the framing bits are removed and just the 64-bit packet is considered. All input packets are directed to the SRAM memory. Only a small number (2 or 3) input channels can operating in this mode simultaneously. This mode is potentially useful in understanding the packets coming from the ABCStar.

9.2.4 Full Transparent Mode

In Full Transparent Mode, the deserializer is continuously capturing 64-bit chunks of the input bit stream. These 64-bit chunks are placing in the SRAM and made available to the packet builder. Only one input channel can be in this mode at a time. This is useful in understanding the bit stream coming from the ABCStar and the input side of the input channel.

9.3 Packet Builder

The Packet Builder retrieves event and register read data from the enabled Input Channels. It also retrieves register read data from the HCCStar's command decoder.

9.3.1 Output Packet Format

The HCCStar has a bond pad option for selecting the default encoding mode. Without a bond from OutEncode to GND, the HCCStar will default to 8b10b encoding its output. If OutEncode is bonded to GND, the HCCStar will default to no output encoding. In either case, the encoding can be changed by a register setting.

The 8b10b encoding used is the one described in [cite IBM paper][cite IBM patent], using the "out of band" control codes K28.7[3] for Start-of-Packet, K28.1 for End-of-Packet and K28.5 for IDLE[4]. The packet will be divided up into 8-bit chunks to be encoded, ignoring any internal packet fields. Any bits required to make a full 8-bit chunk before the End-of-Packet control code will be set to 0.

If 8b10b encoding is not used, packets will be framed with a 3'b110 preamble and a 45'b0 postample. This makes the pre+post-ample a multiple of 8 and makes the inter-event gap longer than any possible string of zeros within an event.

9.3.1.1 Generic Packet Format

All packets start with a 4-bit TYP code. These TYP codes are the same as used in the ABCStar. The codes have been generated so that they all differ by at least two bits from each other. The codes are listed in Table 9.10.

[3] The encoding explicitly disallows back-to-back K28.7 symbols. Thus the HCCStar will never generate two Start-of-Packet symbols without at least one intervening symbol.
[4] These are different from what is specified in the "FELIX Phase-1 Technical Specificaiton and Implementation" document [cite]. The HCCStar arrangement is considered more robust.

9.3.1.2 Event Packets

For PR and LP events, the full header consists of the 4-bit TYP code, the 8-bit L0tag, and a 4-bit BCID. The BCID field contains the 3 least significant bits of the full 8-bit BCID counter associated with the event followed by a 1-bit parity, calculated over the entire 8-bit width of the counter.

After the 16-bit header, ABCStar clusters will be sent. These 15-bit clusters are composed of the 4-bit Input Channel number the cluster was received on, and the 11-bit Cluster as received from the ABCStar.

These clusters will be sent, one after another without separator, from all input channels. The packet will end with a fixed 15-bit cluster pattern that does not represent any valid cluster: 15b'110_1111_1110_1101.

An error block, if needed for this event, will appear at the end of the packet before the end of packet cluster pattern. It will be marked with a different invalid cluster pattern (15b'1110 11111110 100). Following the start of error block marker will be information about which Input Channel the error occurred on and what the error was. Details TBD.

9.3.1.3 Register Read Packets

The header for Register Read Packets is simply the 4-bit TYP code. Note that the TYP is different for ABCStar and HCCStar register reads and the data from the two will never be combined.

In the case of ABCStar Register Read data, the HCCStar will output the incoming ABCStar Register Read packets, replacing the ABCStar 4-bit TYP code with the 4-bit HCCStar Input Channel number. Multiple ABCStar Register Read packets may be packed into one HCCStar packet.

In the case of HCCStar Register Read data, the packet will consist of 41-bit records containing the 8-bit register address, the 32-bit register contents and a "last" bit. Multiple records can be packed into one packet, with the "last" bit set to '0' for all but the last record where it will be set to '1'.

9.3.1.4 Packet Transparent Mode

In Packet Transparent Mode, the header will be the 4-bit TYP code plus the 4-bit Input Channel number. Following this header will be the full, unmodified 64-bit ABCStar packet, with the framing bits removed. The HCCStar will generate one packet for each incoming packet. The HCCStar supports a small number of channels (~3) simultaneously in this mode.

9.3.1.5 Full Transparent Mode

In Full Transparent Mode, the header will be the 4-bit TYP code plus the 4-bit Input Channel number. This header will be followed by a 512-bit chunk of data. The HCCStar supports only one Input Channel at a time in this mode.

9.3.1.6 Startup Data Mode

On power-up or hard reset, the HCCStar will turn off all hybrid out outputs and will disable all Input Channels. In addition, it will start outputting register read packets for the Special Status Register at low rate (1ms? TBD). This register will contain at least the LCB_IN and R3_L1 link status and the HCC ID.

9.4 Serializer

In the case of 8b10 encoded data, the serializer will output the 10-bit symbols lsb first, otherwise it will send the data msb first.

The output data rate will be selectable between 320 Mbps and 640 Mbps, with 320 Mbps as the default. The clock used to send the data will be available on the DataCLK output pad for diagnostic and test use. By default, the driver for this pad is turned off.

9.5 Command Decoder and Registers

The Command Decoder interfaces with the LCB decoder and provides access to read and write control registers and read status registers. The control registers contain auto-correcting triplicated logic. The register read values are made available to the Packet Builder in the same format as the register read values from the ABCStar in the Input Channel.

9.6 Autonomous Analog Monitor

The HCCStar includes an autonomous monitor block, similar to the blocks implemented in the HCC130 and AMAC. This block contains a Wilkinson type ADC based on an autonomous ten bit counter that drives a switched capacitor integrator voltage ramp, whose range is 0 to 1V. Each channel of the Autonomous monitor is instrumented with a low power comparator, looking at the monitored quantity (scaled as necessary) and the integrator ramp voltage. When the value of the ramp exceeds the monitored voltage the comparator output is used to latch the current value of the counter in a 10-bit channel-specific latch. The ramp scale can be adjusted for values between 0.8 and 1.2mV per count. At the end of the ramp, the latched value is transferred to the associated HCCStar register and compared with programmable upper and lower limits set in the register. If either limit is exceeded an appropriate bit is set in the register. The layout of the Autonomous Monitor's control/status registers is show in Table 9.11.

AM Channel	High Limit	Low Limit	High Limit Flag	Low Limit Flag	Channel Data
Bit positions	31:22	21:12	11	10	9:0

Table 9.11: Autonomous Monitor Control/Status Register Layout

More details about the operation of the Autonomous Monitor block described in the AMAC (Autonomous Monitor And Control) chip specification document [cite AMAC Spec]

Table 9.12 lists the autonomous monitor channels and their input attenuation scale factor.

Channel	Monitor	Scale factor
1	Vdd Raw	1/2:1
2	Vdd	2/3:1
3	BandGap HCC	1:1
4	BandGap AM	1:1
5	Internal Temp Diode	1:1
6	NTC	Programmable Range TBD
7	Ext. Gnd	1:1
8	Ext. Vsense	1:1

Table 9.12: Autonomous Monitor Channels

9.7 Addressing

Each HCCStar die will have a 20-bit serial number set by eFuse bits when the wafers are probed. This serial number will allow for tracking throughout the life of the project. Note that the serial number can be read without knowing or using the HCC ID of the ASIC by issuing a Global Read command.

The HCCStar also has a 4-bit command address, referred to as "HCC ID". This is used to identify a target HCCStar when issuing register read and write commands. This address can be set in two ways. One is through the use of the ID bond pads. Bonding a pad to ground sets the corresponding bit to '1'. If none of the bond pads are connected, a dynamic addressing mode is enabled.

The serial number will be accessible (read only) as the least significant bits of a 32-bit register. The most significant 4 bits of this register will be read-write bits and used as the HCC ID in dynamic addressing mode. These bits can be written by issuing a Write (even a Global Write) command with the least significant bits being the serial number of the ASIC for which the write command is intended and the most significant bits being the value to set the HCC ID to. The HCCStar will only write the most significant bits if the least significant bits match its serial number.

The register holding the dynamic HCC ID will be protected with five-fold redundancy.

Note, as a special case, if the ID pads are not bonded, and the dynamic address has not been programmed, the HCCStar will respond to address 0. Be aware, that this does not correspond to a valid module for R3 commands.

9.8 Resets

9.8.1 Hard Reset

Hard Reset is activated by grounding the RSTB bond pad. It will hold the entire ASIC in reset (except for the Power-On Reset logic) until the logic level on the RSTB is brought back high. The pad has an internal pull-up so that it need not be connected. This signal brings the HCCStar back to its power-on state.

9.8.2 Power-On Reset

Powering up HCCStar requires the external BC clock and the supply voltage at or above 1 Volt. Two blocks are used to ensure that the HCCStar powers up into a known state. The ASIC level reset is held true until both the Power Good Block (PGB) and the Power-up Clock Counter Block (PCCB) have completed their sequential power-up sequences.

The PGB holds the PowerGood signal false, which locks out the clock supplying the PCCB until the supply voltage exceeds the bandgap voltage by approximately 200mV. Once PowerGood is asserted true, it is held true by a triplicated latch until power down occurs to avoid the possibility that a power glitch executes the reset sequence.

When true, PowerGood releases the reset on the PLL and enables the PCCB counter to count 65535 40 MHz (BC_in) clocks before enabling a second counter on the PLL 40 MHz clock. This counter counts to 63 then sets PowerUpReset false. The first counters corresponds to a 1.6mS settling time to allow the HCCStar voltage supply and regulators to settle before enabling the PLL. The second counter corresponds to 1.6us to allow the derived clocks to settle before all clocked registers to be set to their default values.

PowerUpReset releases the ASIC level reset, allowing the reset of the ASIC to bring it into its default state.

9.8.3 Triggered Reset

An ASIC level reset will be generated if the LCB input is held high continuously for more than 400 ns, provided the BC clock is being received properly.

9.8.4 Soft Reset

Soft Reset is a fast command send through the LCB protocol (see Section 9.1.2). It resets the entire ASIC (except for the Power-On Reset logic) and brings the HCCStar back to its power-on state.

9.8.5 Logic Reset

Soft Reset is a fast command send through the LCB protocol (see Section 9.1.2). It resets all of the sequential logic back to its power-on state. It does not reset the memory blocks.

9.8.6 PLL Reset

PLL Reset is a fast command send through the LCB protocol (see Section 9.1.2). It resets the PLL block.

9.9 Power-On State

The full reset state for the HCCState is

- Hybrid side drivers: OFF
- Input Channels: DISABLED
- Input Channel & Packet Builder mode: PHYSICS
- Trigger Mode: SINGLE LEVEL
- Output Data Rate: 320 Mbps

9.10 Trigger Rate Limitations

The HCCStar does not have any inherent rate limitations. There is no limit to the L0A rate in multilevel trigger mode. In single level trigger mode, the only limitation is from the LP readout request path.

The rate limit for L1 (LP) and R3 (PR) readout requests ultimately comes from the data output bandwidth from the HCC, with buffering available in the SRAM memories of the Input Channels, the ABCStar ASICS and the LP and PR FIFOs in the Control Channel. It is hard to estimate what the real limit is, particular as it is dependent on the occupancy and occupancy distribution across the hybrid

9.11 Programming Model

The register access mechanism is as described in the LCB protocol and Command Decoder sections above. The list of programmable values includes

- PLL output clock phases
- PLL control parameters
- Pad Driver enables
- Pad Driver current drive
- Stave side driver pre-emphasis amplitude

- Receiver enable
- Delay values for hybrid side control signals
- Delay value for Readout Clock
- Delay values for Input Channel DataIn
- Input Channel enables
- Input Channel / Packet Builder Mode
- Trigger Mode
- Autonomous Monitor limit values
- Maximum clusters per event
- Output data encoding
- Startup data mode enable
- Bandgap control

10 Radiation Tolerance and Other Special Requirements

If some level of radiation tolerance is required, state the minimum total ionizing dose (TID) and non-ionizing fluence after which the component must remain functional and meet all other specifications. Also, describe the allowable single event upset (SEU) rate, possibly by sections of the component if the allowable rate is not the same across the whole component. If there are other special requirements beyond those covered in other sections describe them here.

If there are no radiation tolerance or other special requirements, then state "Not Applicable" for this section.

The HCCStar will have SEU mitigations in the form of automatically correcting triplicated registers and, where appropriate, triple modular redundancy (TMR) techniques.

11 Testing, Validation and Commissioning

Describe testing procedures that will be used to demonstrate that the fabricated component meets the specifications. This should include radiation testing if radiation tolerance is one of the requirements.

It is not required to complete this section prior to the first specification review but it should be completed prior to the PDR. Prior to the FDR, the production testing must be described, and prior to the PRR, commissioning plans must be included.

12 Reliability Matters

12.1 Consequences of Failures

Describe the consequences to the detector of a failure of one unit of this component, e.g. x% of the sub-detector channels will be lost, or one stave or petal could overheat causing delamination of its component parts. The severity of the consequences will determine the level of reliability required and the level to be validated by QA and QC procedures defined in sections 12.4 and 12.5.

12.2 Prior Knowledge of Expected Reliability

Based upon industry experience, collaboration experience or personal experience, give an estimate of the reliability of this component.

12.3 Measures Proposed to Insure Reliability of Component and/or System

Include such measures as conservative design techniques (give specific examples), redundancy and possibilities to replace failed part. . If failed part could be replaced, estimate the difficulty and time involved for installing replacements,

12.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

Describe what stress tests will be applied during the development period to validate the reliability of this component. Give a brief outline of any appropriate reliability theory being used. These tests could involve destructive tests.

It is not required to complete this section prior to the first specification review but it must be completed prior to the PDR. It is strongly recommended that these plans be reviewed and approved prior to the actual PDR to avoid the possibility of failing the PDR and thus delaying the fabrication or construction of the prototype parts,

12.5 Quality Control to Validate Reliability Specifications during Production

Describe what stress tests will be applied during production, possibly on a sampling basis, to validate the reliability of production units. These could likely be destructive tests. Specify the required sampling percentage of production units.

It is not required to complete this section prior to the first specification review but it must be completed prior to the FDR. It is strongly recommended that these plans be reviewed and approved prior to the actual FDR to avoid the possibility of failing the FDR and thus delaying the fabrication or construction of the pre-production parts,

13 References

If there are any references pertaining to the development of this component, list them here.