ATLAS ITk Electronics Specification: HCCStar

Version: V1.0
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Abstract

The HCCStar chip is the digital front-end ASIC for the readout of the ITK Silicon Strips detector in the ATLAS experiment for the HL_LHC collider at CERN.

Revision History

Revision	Date	Author(s)	Description
0.1	15 Nov 2016	Keener, Anghinolfi, Newcomer, Warren	Initial draft
0.2	30 Jan 2017	Keener, Anghinolfi, Newcomer, Warren	Extension/Revision
0.3	28 Mar 2017	Keener, Anghinolfi, Newcomer, Warren	Extension/Revision
1.0	15 Jan 2018	Keener, Anghinolfi, Newcomer, Warren	Version for sign-off/PDR

Contents

List of Figures

List of Tables

1 Conventions and Glossary

1.1 Conventions

Signal names ending with the letter 'b' are active low, all other signals are active high, unless otherwise noted.

Hexadecimal numbers are noted either by prepended with "0x" or using Verilog notation: <number of bits>'h<hexadecimal value>, eg (32'h0123beef).

1.2 Glossary

BC — Beam Crossing Clock, 40 MHz

BCID — Bunch Counter ID. An 8-bit clock counter used to detect front-end desynchronization.

BCR — Bunch Counter Reset. A 1-bit BC-synchronous command that resets the BCID to zero. It is used to ensure front-end synchronization. It is issued through the LCB input.

BTC — Bus Tape Clock, 160 MHz. Clock that is sent on the bus tape from the EOS to the HCCStar.

CMD — Command signal. Used for asynchronous setup of the HCCStar and ABCStar or for performing certain resets.

Command Sequence — A set of LCB command frames starting with a Start of Sequence frame and ending with an End of Sequence frame that together make up a signle command. The frames in a Command Sequence must be in order, but need not be consequtive.

Control Segment — The portion of the bus tape and attached modules and HCCStars that share TCC buses. Global commands on a Control Segment affect all of the hybrids on that segment.

EOS — End-Of-Substructure card. Cad card that sits at the end of the stave or petal that contains, among other things, an lpGBT ASIC that provides the clock and control signals to the HCCStar and receives the data send by the HCCStar.

HPR — High Priority Register. A special register (number 15) that contains HCCStar status information that can be send automatically at ASIC started, reset, or when LCB link lock is lost.

L0A — Level 0 Accept. A beam crossing synchronous pulse that transfers strips data from the fixed latency pipeline on the ABCStar to its Random Access Memory (RAM) that is used as a an event buffer.

L0tag — A 7-bit value attached to each L0A. It is used to safely identify events for readout.

LCB — L0A/CMD/BCR signal.

LP — Low Priority readout request. An asynchronous request from the HCCStar to the ABCStar to read out an event with the given L0tag from the ABCStar event buffer with low priority. Generated on the HCCStar by either an L1 request or an L0A, depending on the trigger mode.

lsb — Least Significant Bit. This is the bit in the 2^0 place.

msb — Most Significant Bit. This is the bit with the most value in the word.

PR — Priority readout request. An asynchronous request from the HCCStar to the ABCStar to read out an event with the given L0tag from the ABCStar event buffer with high priority. Generated on the HCCStar by an R3 request.

RCLK — Readout Clock. A 160 MHz clock from the HCCStar used to decode the LCB signal on the ABCStar and to clock the serial output bit stream from the ABCStar back to the HCCStar.

SEE — Single Event Effect. Any of a number of effects induced by radiation, electromagnetic interference, or other causes that may make change the stored stated or behavior of a circuit. Single Event Upset (SEU) and Single Event Transients (SET) are two types of SEE.

2 Related Documents

"ATLAS ITk Strip System Architecture", EDMS AT2-IS-ER-0001,
https://edms.cern.ch/document/AT2-IS-ER-0001

3 Description of Component or Facility

The HCCStar ASIC is the digital interface for the ITk Strips hybrids, both in the endcap and in the barrel. It receives 160 MHz clock and 160 Mbps control lines on multidrop line originating from the End-of-Substructure (EOS) card. The HCCStar interprets the control data, generates the 40 MHz bunch crossing clock from the control data framing, and forwards this clock and relevant control data to between 5 and 11 ABCStar ASICs on the hybrid on shared, multidrop lines. This control data includes triggers, event data readout requests, register read and write commands, test pulse generation, and resets. ABCStar event data, as well as register read data, are sent on point to point lines back to the HCCStar. The HCCStar combines data for the same event from all input and sends out this combined data at either 320 or 640 Mbps, selectable, on a point to point link on the bus tape to the EOS.

The HCCStar is provided as bare die and is electrically connected to the hybrid with bond wires.

4 Interfaces

This component uses and interfaces with other components listed in Table 4.1.

5 Physical Description

The HCCStar ASIC will be provided as unpackaged die. The die size will be 3.5 mm $\times$ 5.2 mm, as measured between the outside pad edges. The physical die will be slightly larger due to manufac-

Name of Component	Name of Component Specification
ABCStar ASIC	ABCStar Specification [1]
AMAC ASIC	AMAC Specification [2]
Barrel and Endcap Hybrid Boards	Hybrid Board Specification [5]
Barrel and Endcap Power Boards	Power Board Specification [7]
Barrel and Endcap Modules	Module Specification [6]
Barrel and Endcap Bus Tapes	Bus Tape Specification [3]
End of Substructure Card	EOS Specification [4]

Table 4.1: Components which interface to this component.

turing constructs such as the seal ring. The wafers containing the HCCStar die will be thinned to $300 \pm 20\,\mu$m before dicing.

The floorplan for HCCStar is shown in Figure 5.1 and the pad list is shown in Table 5.1

6 Manufacturer

The HCCStar will be fabricated in Global Foundry (Ex-IBM foundry) in the CMOS8RF_DM 130 nm technology. The wafers are standard 8 inches and will be thinned to $300 \pm 20\,\mu$m. No packaging is foreseen.

7 Power

The nominal power requirements are listed in Table 7.1. There is significant uncertainty in the current values. It is expected that the power-on nominal current will be approximately 15 mA lower. In addition, at 1 MRad TID, the nominal current is expected to be around 225 mA, again with significant uncertainty.

8 Input/Output

8.1 LVDS

The LVDS driver and receiver designs have been slightly evolved from what was used in the first version of HCC. We maintain the programmable current capability between about 0.5 to 6 mA on drivers, with the addition of a resistor defined common mode output voltage at Vdd/2 (~ 600 mV) and a disable function that drops the driver current to near zero. The receivers are bandwidth limited to about 160 MHz in a similar way to the bandwidth limitation implementation that was tested on the Repeater Chip [cite Repeater Chip].

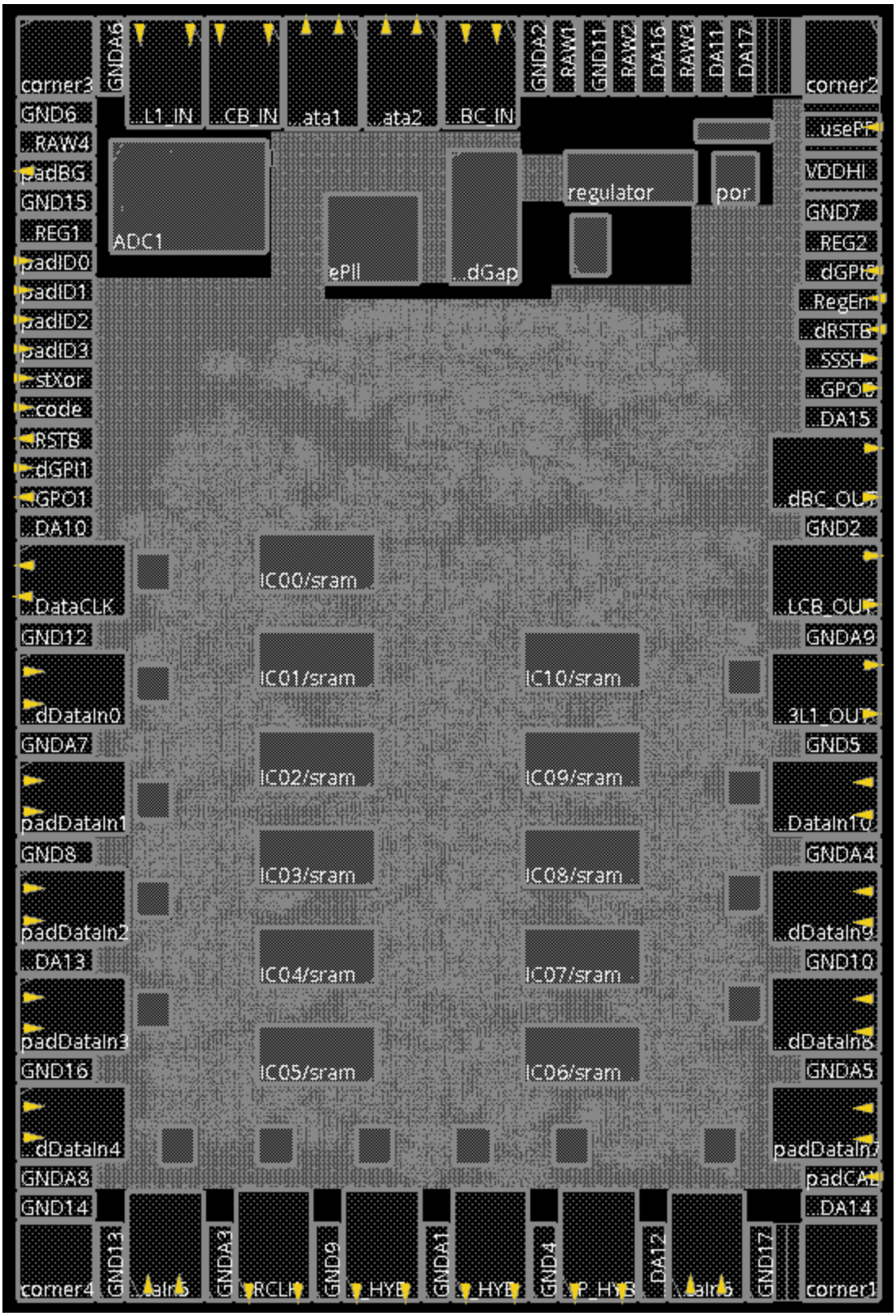

Figure 5.1: HCCStar Floorplan

Class	Type	Dir	Name	#	Default	Description
Supply		In	VDD_RAW	4	1.3 – 1.6 V	Power In
		In/Out	VDD_REG	4	1.2 V	Core Power
		In	GND	24	0 V	Voltage Return
Diagnostic	Analog	Out	BG	1	0.5 – 0.8 V	BandGap
Address	SE	In	ID0–3	4	Pull up	Address Bits: Bond to GND sets bit to '0'
		In	FusePP	1	Pull down	Pulse to program eFuse bits
Bond Options		In	RstXor	1	Pull up	Invert sense of RSTB
		In	OutEncode	1	Pull up	Default output encoding (GND=8b10b)
Data	LVDS600	In	DataIn	11	0	ABCStar data inputs, 75Ω
		Out	Data	2	0	Output data
		Out	DataCLK	1	0	Diagnostic clock in phase with output data
Logic	SE	In	GPI	2	Pull up	General purpose input
		In	RegEn	1	Pull up	High = Enable Regulator
		In	RSTB	1	Pull up	Low = Hard Reset
		In	LAM	1	Pull up	Rising Edge = Look At Me
		Out	GPO	1	Low	General purpose output
		Out	SSSH	1	Low	Reset AMAC communications
		Out	ABC_RSTB	1	Pull up	ABCStar Hard Reset
Stave Cntl	LVDS600	In	BTC_IN	1		Bus Tape 160 MHz system clock
		In	LCB_IN	1	Idle	L0A/CMD/BCR
		In	R3L1_IN	1	Idle	R3 & L1 Readout Req
Stave Cntl Repeater	LVDS600	Out	BTC_OUT	1	OFF	Bus Tape 160 MHz system clock
		Out	LCB_OUT	1	OFF	L0A/CMD/BCR
		Out	R3L1_OUT	1	OFF	R3 & L1 Readout Req
Hybrid Control	LVDS600	Out	BC_HYB	1	OFF	40 MHz clock
		Out	LCBa_HYB	1	OFF	L0A/CMD/BCR
		Out	PR_LP	1	OFF	Readout Request
		Out	RCLK	1	OFF	160 MHz clock

Table 5.1: HCCStar Pad List

8.2 Receiver Clock Signal — GBT Side

This GBT receiver is the same as the receive for the control signals (detailed below), except it does not have the hysteresis implemented.

Name	Min	Nominal	Max	Nominal	Max
	Voltage Supplied			Current Required	
VDD_RAW	1.15 V	1.5 V	1.6 V	200 mA	225 mA

Table 7.1: HCCStar Power Requirements

Name	In, Out or I/O	Signal Type	Description
DataIn	Input	LVDS point to point	Data inputs with internal termination
Data	Output	LVDS point to point	HCCStar data output
Data clock	Output	LVDS point to point	HCCStar data clock diagnostic output
Control/Clock	Input	LVDS multi-drop	Input from stave side. High-Z
Control/Clock Repeater	Output	LVDS point to point	Repeater for stave side control & clock to 2nd HCCStar on hybrid
Control/Clock	Output	LVDS multi-drop	Output to ABCstar ASICs on hybrd. High-Z
Digital I/O	Input or Output	CMOS point to point	Regulator Control, Resets, etc.

Table 8.1: HCCStar Input and Output Signals

8.3 Receiver Control Signals — GBT Side

GBT data receivers have a bandwidth in excess of 250 MHz — more than twice the bit rate for the input signals. It may be necessary to AC couple due to the GBTX SLVDS-compatible 200 mV common mode output, which is not compatible with the predicted return-voltage increase from End-of-Structure (EOS) card to the end of the stave. Thus the HCCStar keeps the hysteresis circuits that have been successfully employed on previous ASICS, eg HCC130. AC coupling will require the use of 120 pF capacitors on each HCCStar. This value may be changed when the lpGBT design, which is expected to have a 600 mV common mode, is finalized. Wirebond-selectable terminations are not included due to the risk that unpowered HCCstar chips may pull down the multi-drop lines making communication impossible if DC coupling is used.

8.4 Repeater Control Signals — Hybrid Side

The HCCStar will be able to optionally repeat the GBT Side Control Signals on the hybrid side of the ASIC for use of a second HCCStar. These drivers are the same as the drivers described in Section 8.6.

8.5 Receiver Data Signals — Hybrid Side

Each LVDS input channel utilized bandwidth limited (160 MHz) receivers with 75 Ω terminations on the hybrid side input to the HCCStar.

8.6 Driver Clock and Control Signals — Hybrid Side

The HCCStar uses programmable current (0.375 to 1.5 mA) LVDS outputs capable of multi-drop signaling to up to 11 ABCStar control inputs. The LVDS common mode will be maintained at Vdd/2 ($\sim$ 600 mV) by a resistive divider on each LVDS driver output. When the drivers are disabled, the differential lines are held apart to keep any attached receiver in a well-defined state.

8.7 Driver Data Signal — GBT Side

The HCCStar has two programmable-current drivers with a maximum bandwidth of 640 MHz. This is more than twice the minimum required bandwidth for 640 Mbps bit rate. A resistive divider will maintain a Vdd/2 common mode although the common mode operational range will be within about 300 mV from the upper and lower rails. The current drive is selectable in 8 steps from 0 to 3 mA.

9 Detailed Description and Specification

The top level block diagram for HCCStar is shown in Figure 9.1. System clock and control signals flow from the stave through the Control Path in the HCC. The Control Path interprets the signals for its own purposes and modifies them for use in the ABCStar ASICs on the hybrid where the HCCStar is located. Data coming back from the hybrid's ABCStar ASICs goes into the HCCStar's Input Channels, one per ABCStar. The Packet Builder collects the data from various Input Channels and combines them into event fragments. It then serializes the data and sends out packets across the bus tape to the EOS. Each of these three HCCStar components is described below.

9.1 Control Path

The block diagram for the Control Path is shown in Figure 9.2. The control protocols are described below, followed by a description of their behavior.

9.1.1 Clocks

The HCCStar receives a 160 MHz clock on the LVDS BTC_IN line. This clock is used to decode the LCB and R3_L1 control signals. The LCB decoder produces a 40 MHz clock from the LCB framing that is at constant phase with respect the framing. This 40 MHz clock is the system 40 MHz clock on the HCCStar and is used as the reference for a PLL that provides the ASIC with three independent, adjustable phase 160 MHz clocks, three independent, adjustable phase 320 MHz clocks, a recovered 40 MHz clock, and a 640 MHz clock that is produced from two internal phases of the 320 MHz clock.

The 40 MHz clock is primarily used in the HCCStar for the R3_L1 Path, the registers and the Controller and SRAM blocks in the Input Channels. One of the 160 MHz phases is used at the sytem 160 MHz clock, running the rest of the Input Channel, the Packet Builder, and the Output Path logic. Another 160 MHz phase is sent to the ABCStar ASICs on the hybrid as RCLK, and the

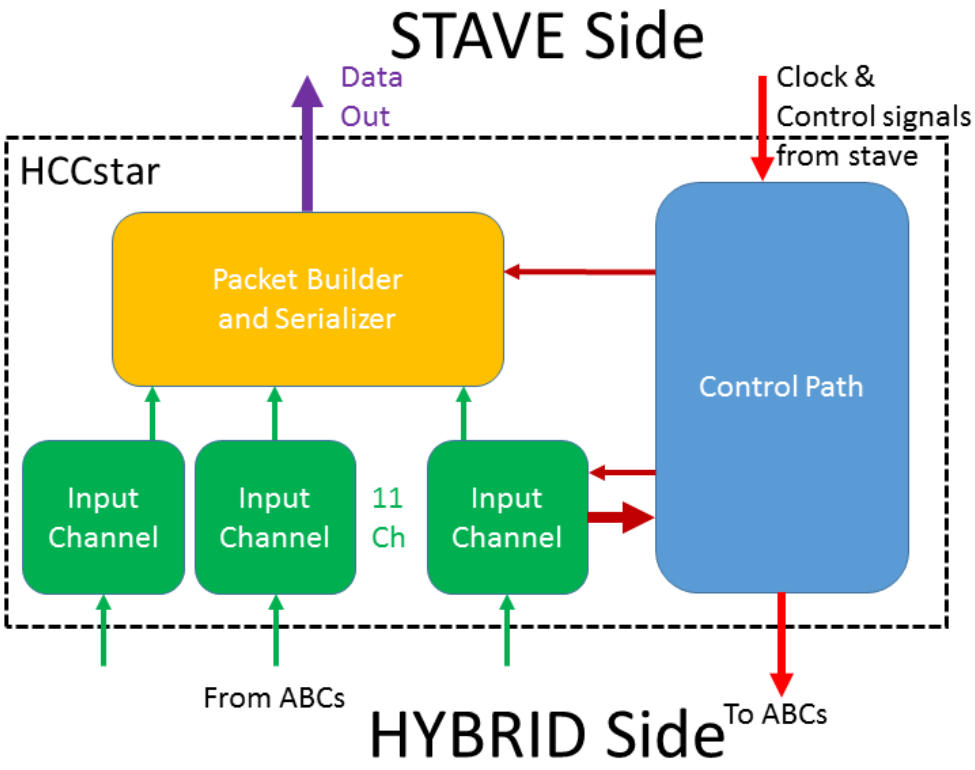

Figure 9.1: HCCStar Top Level Block Diagram

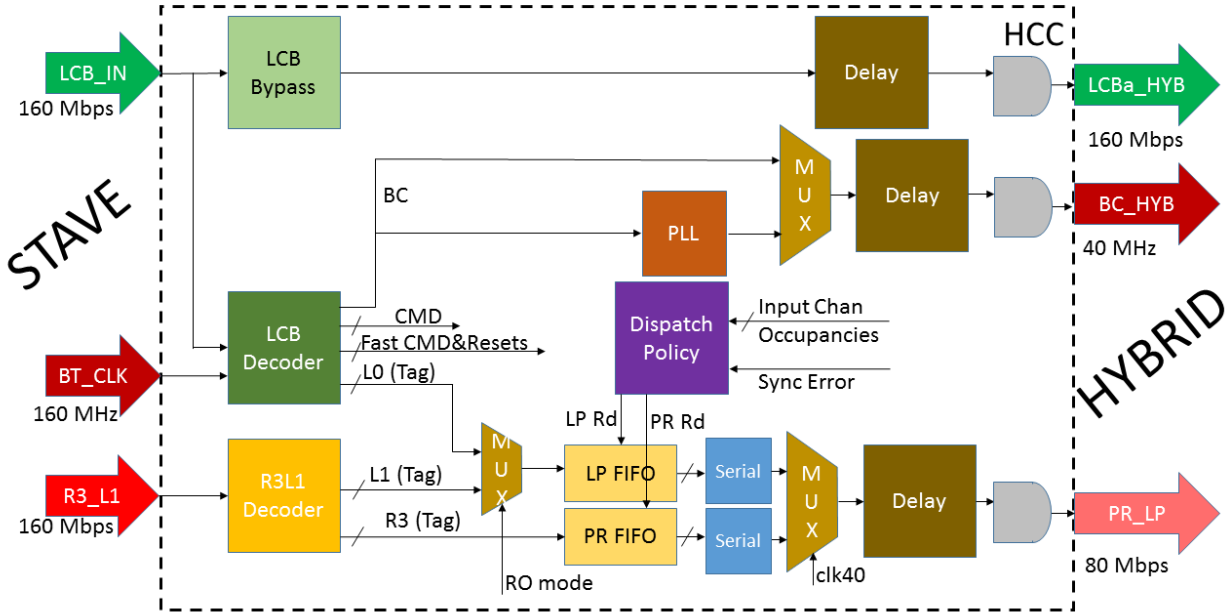

Figure 9.2: HCCStar Control Path Block Diagram

third 160 MHz phase is used in the delay blocks for the hybrid BC and PRLP signals. A 320 MHz phase is used in the Output Path as the serializer clock, for 320 Mbps data output, or as the clock used to feed the serializer, for 640 Mbps output. The 640 MHz clock is used in the serialize, for 640 Mbps output.

The BC_HYB LVDS clock can be selected to be either the HCCStar system 40 MHz clock or the PLL recovered 40 MHz clock. In either case, it can be delayed with a coarse/fine delay block. This block provides for coarse delay adjustment in four 6.25 ns steps and fine delay adjustment in 16, ∼1.9 ns steps. At power-up or hard reset, the BC_HYB signal is configured to be the HCCStar system 40 MHz clock.

The BC_HYB can be turned on and off through a setting in a register. The default state of BC_HYB at power-up reset, hard reset, and register reset is OFF. All of the clocks used internally on the HCCStar will be enabled by default after these resets.

9.1.2 LCB Signaling Protocol

The L0A/CMD/BCR — LCB — signal transfers triggers (L0A), fast-commands, register read-writes (CMD) and bunch-counter-reset (BCR) to the HCCStar (and ABCStar) ASICs. The signal is 6b8b[1] encoded and sent at 160Mbps over an LVDS bus that is shared by between two and ten HCCStar ASICs. The serial stream is synchronous with the BCO, although not necessarily in-phase. The HCCStar must "lock" onto the LCB stream at initialisation (see 9.1.2.1 below). The basic unit of data transmission is a pair of 8-bit symbols called a frame, providing 12 bits of payload per frame. Frames have four distinct frame-types: Idle, L0A, Fast Command (including resets) and K2 (for start and end of command sequences).

9.1.2.1 LCB Locking Mechanism

The 160 Mbps LCB signal is sampled (and pipelined) by the 160 MHz BT_CLK clock (that travels with it on the stave or petal) upon entering the HCCStar. The BT_CLK to LCB phase is controlled by the LpGBT. The LCB stream is sampled 4 bits at a time by the 40 MHz BCO clock edge, with the off-detector system being responsible for setting the correct phase of the 160 Mbps stream with respect to the BCO to allow for correct framing. When a sufficient number of correct "IDLE" frames have been counted the link is considered "locked", and decoding can proceed. When locked, the this count will be decremented by 6b8b decoder errors.

When unlocked, the HPR (Section 9.6) will be sent at regular intervals. The HPR will provide information to assist off-detector firmware or software to modify settings to achieve lock.

9.1.2.2 L0A

Transferred at 160 Mbps, a 16 bit LCB frame takes 100 ns, or 4 BC, to transmit. Thus, a frame containing L0A data must cover 4 BC worth of L0A activity information. Along with the 4 L0As, a 7-bit identifier, called the L0tag, is sent. This identifier is used to request event data from the ABCStars. In addition, a BCR signal may come during a 4 BC period that also has L0As. The

[1] 6b8b is an encoding scheme that produces 8-bit symbols from 6-bit input words. It guarantees a minimum signal transition density and provides 4 8-bit out-of-band control codes which have no 6-bit representation.

payload for an L0 frame is shown in Table 9.1. The msb of the L0A mask refers to the earliest BC, while the lsb refers to latest. A '1' in the L0A mask indicates that there is an L0A in the corresponding BC. A '1' in the BCR field indicates that there is to be a BCR in the latest BC covered by the L0A mask. It is important to note that this implies that frames must have a fixed alignment with respect to the LHC orbit signal in order to guarantee that the BCR is executed at the front-end at the appropriate time.

	MSB		**LSB**
Field Name	BCR	L0A mask	L0tag
# of bits	1	4	7

Table 9.1: LCB L0 Frame

L0 frames are only sent when at least one of the covered BC has an L0A or a BCR needs to be sent. Therefore, at least one of the first five bits will be '1'. Note: when no triggers or BCRs are present, this frame-type is used to transfer command data, as detailed below in Section 9.1.2.4.

9.1.2.3 Fast Commands and Resets

Fast commands and resets are sent with a frame that contains the 6b8b control symbol K3 plus a symbol whose payload is composed of a 2-bit BC selector indicating in which BC the command or reset is to be generated, and a 4-bit action, indicating which command or reset to generate. A value of '0' for the BC selector refers to the earliest BC, while a value of '3' refers to the latest. The payload for the second symbol is shown in Table 9.2. The list of fast commands is show in Table 9.3. Note that fast commands are broadcast commands and are interpreted on all ASICs that share the LCB control line.

	MSB	**LSB**
Field Name	BC Select	Command
# of bits	2	4

Table 9.2: LCB K3 Frame Payload

9.1.2.4 Register Reads and Writes

Register reads and writes are composed of a sequence of frames. These frames do not need to be consecutive, but must be in order. Frames interleaved in a register command sequence may be of any type. A register command sequence starts and ends with a "K2 frame" — composed of the K2 control symbol followed by a symbol containing an ABC/HCC select bit, a Start/End bit, and the HCC ID for the HCCStar on the target hybrid. If the ABC/HCC bit is '1' the command is an ABCStar command otherwise it is an HCCStar command. If the Start/End bit is '1', it indicates the start of a command sequence ("K2 Start"), while '0' indicates it is the end of a command sequence ("K2 End"). An HCC ID of "1111" is interpreted to be a broadcast address and all HCCStar ASICs will respond. A special HCC ID of "1110" is used to indicate that the command sequence should be ignored. The payload for the second symbol in this K2 frame is shown in Table 9.4.

Index	Command
0	Reserved
1	Reserved
2	Logic Reset
3	ABC Register Reset
4	ABC SEU Reset
5	ABC Calibration Pulse
6	ABC Digital Pulse
7	ABC Hit Counter Reset
8	ABC Hit Counter Start
9	ABC Hit Counter Stop
10	ABC Slow Command Reset
11	Stop PR & LP to ABCStar ASICs
12	HCC Register Reset
13	HCC SEU Reset
14	HCC PLL Reset
15	Start PR & LP to ABCStar ASICs

Table 9.3: Fast Commands

	MSB		LSB
Field Name	ABC/HCC	Start/End	HCC ID
# of bits	1	1	4

Table 9.4: LCB K2 Payload

The K2 frame is followed by two header frames. The 5 msbs of the header frames' payload are "00000" to distinguish these frames from L0 frames. The remainder of the payload is a Read/Write bit, the ABC ID of the target ABCStar ASIC (these bits are ignored if it is an HCC command) and the address of the target register. If the Read/Write bit is '1', the command is a read command otherwise it is a write command. The mapping of these fields to the frame payloads is shown in Table 9.5.

Frame		MSB			LSB
1	**Field**	Marker	R/W	ABC ID	Reg Addr MSB
	Value	00000			
	# of bits	5	1	4	2
2	**Field**	Marker		Reg Addr LSB	SPARE
	Value	00000			
	# of bits	5		6	1

Table 9.5: LCB Register Command Header Frames

For register read commands, the header frames are followed by a K2 End frame (with the Start/End bit set to '0') indicating the end of the sequence. The K2 End resets the CMD decoder. The HCC ID field is ignored.

For register write commands, the two header frames are followed by 5 frames containing the value to write into the register, as shown in Table 9.6.

Frame		MSB		LSB
1	**Field**	Marker	SPARE	Register Contents [31:28]
	Value	00000		
	# of bits	5	3	4
2	**Field**	Marker		Register Contents [27:21]
	Value	00000		
	# of bits	5		7
3	**Field**	Marker		Register Contents [20:14]
	Value	00000		
	# of bits	5		7
4	**Field**	Marker		Register Contents [13:7]
	Value	00000		
	# of bits	5		7
5	**Field**	Marker		Register Contents [6:0]
	Value	00000		
	# of bits	5		7

Table 9.6: LCB Register Command Data Frames

As with the register reads, the sequence ends with a K2 End frame. Register write commands can be issued without any intervening space between commands.

Register access command sequences may be terminated at any time with a K2 End frame. While not encouraged, a K2 Start frame will terminate and pending commands and start a new one. A new command sequence may immediately follow the K2 End frame.

To guard against spurious register writes, the number of words in a command sequence is counted, and no action will be taken if the K2 End frame occurs at the wrong stage in the process.

9.1.2.5 Idle

The IDLE frame, composed of the control symbol pair {K0, K1}, will be sent if there is nothing else to send. This frame is used to establish initial synchronization on the link and provide for ongoing validation of synchronization.

9.1.2.6 Error Monitoring

The LCB system will provide information that off-detector firmware or software (or human operators) can use to diagnose link problems. In particular, information is needed about an un-locked LCB, such that the situation can be remedied. This will be achieved via the HPR mechanism, where information is automatically sent by the HCCStar (or ABCStar) when not locked.

The following flags are available, and can be used by the HPR system, for example.

- Lock
- Decoder error (invalid symbol, parity and stuck high or low checks)
- Decoder error-count too high (transgression of a threshold)

- Command sequence error (end-before-start, start-before-end and correct frame count checks)
- Error counter - number of decoder-errors, user resetable)

9.1.3 R3_L1 Protocol

As with LCB, the R3_L1 signal is 6b8b encoded and sent over an LVDS bus that is shared by between two and ten HCCStar ASICs. The basic unit of data transmission is a pair of 8-bit symbols called a frame. Since the R3_L1 signal is transmitted at a data rate of 160 Mbps, a single frame takes 100 ns, or 4 BC, to transmit.

The R3_L1 protocol contains three types of frames: R3, L1 and IDLE. IDLE frames are as in LCB: the symbol pair {K0, K1}, and is sent when there is nothing else to send.

An R3 frame is composed of a module mask indicating which R3 readout regions should respond to the request, plus the L0tag of the event to read out. The payload for the R3 frame is as shown in Table 9.7.

	MSB	**LSB**
Field Name	Module Mask	L0tag
# of bits	5	7

Table 9.7: R3_L1 K3 Frame Payload

The module an HCCStar is associated with is its HCC ID divided by 2. Thus HCC IDs 2 and 3 are module 1, 4 and 5 are module 2, etc. Note that HCC IDs 0, 1 and larger than 11 are invalid for the purposes of R3 and do not correspond to any module. The msb of the module mask corresponds to module 5 and the lsb corresponds to module 1.

An L1 frame is composed of a marker of “00000” to distinguish it from R3 frames and the L0tag of the event to read out. The payload for the L1 frame is as shown in Table 9.8.

	MSB	**LSB**
Field	Marker	L0tag
Value	00000	
# of bits	5	7

Table 9.8: R3_L1 L1 Frame

9.1.4 Control Path Behavior

9.1.4.1 LCB Path

The control path passes the entire LCB control stream through to the LCBa_HYB pads, with minimal added latency. The only modification to the LCB stream is the modification of the K2 Start frame when the HCC ID specified does not match the HCCStar ASIC’s HCC ID or the broadcast HCC ID (4’b1111). In this case, the command sequence is modified by replacing the HCC ID with a special ID (4’b1110) that directs the ABCStar to ignore subsequent CMD frames until a K2 End frame is seen. As such it will not execute on any ABCStar ASIC on the same hybrid.

The outgoing LCBa_HYB data stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ∼ 420 and ∼ 830 ps, with a full range of 16 steps.

The LCBa_HYB can be turned on and off through a setting in a register. The default state of LCBa_HYB at power-up and hard reset is OFF.

The HCC also decodes the LCB control stream for its own purposes. The relevant fast commands and resets are honored by the HCCStar and register command sequences with the ABC/HCC bit set to '0' in K2 frame are decoded for use in the HCCStar. The L0A and L0tag information is also decoded for use in the L0-only single level trigger mode.

9.1.4.2 R3_L1 Path

The FIFO for L1 requests, and the subsequent control path, is named "LP" (Low Priority), as its source may either be L1 from the ATLAS trigger system or directly from L0A triggers decoded in the LCB decoder. The FIFO for R3 requests, and the subsequent control path, is named "PR" (Priority).

In multilevel (L0/R3/L1) readout mode, the L0tags associated with R3 and L1 frames are inserted in separate FIFOs that hold these requests. The L1/LP FIFO will be 64 positions deep. The R3/PR FIFO will be 8 positions deep. Both of these FIFOs implement the policy that new entries will be discarded if the FIFO fills. In single level trigger (L0-only) mode, the R3_L1 decoder can be disabled so as not to require signal on that control line. The L0tag from the LCB decoder will be inserted into the L1/LP FIFO.

The data, upon leaving either FIFO, get a 3-bit preamble prepended, are serialized and then time multiplexed based on the 40 MHz BC_HYB clock. The PR bits are sent when BC_HYB is low and the LP bits are sent when BC_HYB is high. This is summarized in Table 9.9.

	Sent left to right, MSB first			
Request	**Preamble**	**Data**	**Trailer**	**BC_HYB Phase**
PR	3'b101	7-bit L0tag	1'b0	LOW
LP	3'b110	7-bit L0tag	1'b0	HIGH

Table 9.9: PR_LP Control Line

The outgoing PR_LP data stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ∼ 420 and ∼ 830 ps, with a full range of 16 steps.

The PR_LP can be turned on and off through a setting in a register. The default state of PR_LP at power-up and hard reset is OFF.

The release of read requests from the PR and LP FIFOs is controlled by a policy block. This block guarantees that a FIFO read does not occur until the previous one has been serialized. It also enforces at least one '0' bit between requests. Furthermore, it will not issue a PR or LP unless all of the enabled Input Channels have space in their respective buffers to handle another event of maximal size. In addition, an Input Channel can request that read requests be held in order to guarantee the link from the ABCStar goes into its quiescent state. This can be done in order to re-establish synchronization.

9.2 Input Channel

The block diagram for the Input Channel is shown in Figure 9.3. There are 11 Input Channels in the HCCStar. The Input Channel receives fixed length packets as a 160 Mbps serial stream from the ABCStar. It separates the data packets based on type and organizes the data for the output Packet Builder. Each Input Channel can be individually enabled or disabled. At Power-On, all Input Channels are disabled.

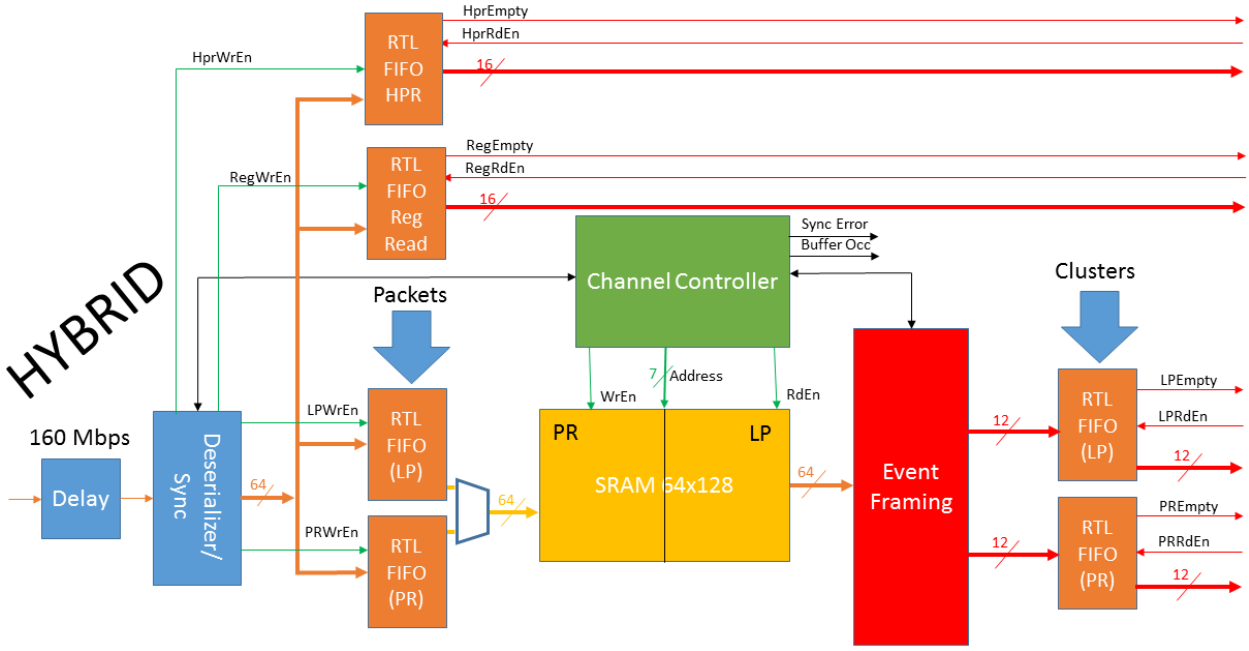

Figure 9.3: HCCStar Simplified Input Channel Block Diagram

The serial stream can be delayed with the use of a fine delay block that has a process/temperature/voltage dependent step size of between ~ 420 and ~ 830 ps. The quiescent state of the ABCStar input line is expected to be '0'. Data from the ABCStar are expect to come in fixed-length 64-bit packets, with a 3-bit framing header prepended and one '0' appended as a framing trailer. The expected data format is as defined in the ABCStar Specification[1].

Repeated failure to identify valid packets will show up as synchronization errors in the Packet Builder. It is the responsibility of the external system to pause the sending of Readout Requests to the ABCStar ASICs so that their inputs to the HCCStar will go idle and allow the deserializer to reset. The pausing and restarting of the dispatch of Readout Requests is done through Fast Commands (Section 9.1.2.3).

The type of data packet is determined by the TYP field. Valid TYP field values are shown in Table 9.10. The ABCStar will only generate LP, PR, Register Read and High Priority packet types; the rest are used by the HCCStar.

The input channel has four operating modes which determine how it handles ABCStar packets: Physics Mode, Register Read Special Mode, Packet Transparent Mode, and Full Transparent Mode. The HCCStar defaults to Physics Mode.

TYP code		Meaning
Binary	**Decimal**	
0001	1	PR Packet
0010	2	LP Packet
0100	4	ABC Register Read
0111	7	ABC “Packet Transparent” Packet
1000	8	HCC Register Read
1011	11	ABC “Full Transparent” Packet
1101	13	ABC High Priority Packet
1110	14	HCC High Priority Packet

Table 9.10: Packet TYP codes

9.2.1 Physics Mode

In physics mode, the framing bits are removed and just 64-bit packet is considered. The SRAM memory is divided into two halves; one half for PR packets and one half for LP packets and the packets are stored in their entirety. The number of packets in each event is counted and compared to the value set by bits [14:12] in the Operating Mode Registers (41 & 42). Any packets for the same event received past the maximum number set will not be stored. The maximum number of packets per event configurable to 1, 2, 4, 8, or 16 packets. The Input Channel will detect the boundary between events to keep an accurate count of the number of pending readout requests in the ABCStar.

The event data packets will be read from the SRAM memory, split into pieces and inserted into a 12-bit wide by 8-position deep FIFO. One of the bit positions will be used for the ABC Error bit from the packet header and the cluster byte last cluster bit.

The first data word pushed into the FIFO will be the 1-bit ABCStar Error bit, the 7-bit L0tag and the 4-bit BCID from the ABCStar header. Following this will be the 12-bit clusters from the ABCStar, including the Last Cluster bit. If the number of clusters is not a multiple of 4, the Last Cluster bit will be attached to the last physics cluster and the unused cluster positions in the packet will not be put into the FIFO.

Register read packets will be transferred into a small, 16-bit wide, compiled-logic FIFO. The 64-bit packet will be split into 4 16-bit pieces and inserted into the FIFO. The size of this FIFO will be 16 (four packets) deep. The policy on this FIFO is that the new packets will be discarded on FIFO overflow.

9.2.2 Register Read Special Mode

In Register Read Special Mode, the framing bits are removed and just the 64-bit packet is considered. Any LP or PR packets are discarded and register read packets are stored in the SRAM memory. This mode is useful when trying to read registers quickly, for example, the ABCStar counter registers in calibration mode. All input channels can operate in this mode simultaneously.

9.2.3 Packet Transparent Mode

In Packet Transparent Mode, the framing bits are removed and just the 64-bit packet is considered. All input packets are directed to the SRAM memory. This mode is potentially useful in understanding the packets coming from the ABCStar.

9.2.4 Full Transparent Mode

In Full Transparent Mode, the deserializer is continuously capturing 64-bit chunks of the input bit stream. These 64-bit chunks are placing in the SRAM and made available to the packet builder. This is useful in understanding the bit stream coming from the ABCStar and the input side of the input channel. This mode has been turned on for a programmable number of 25 ns clock cycles, up to 2^{32} ($\sim$ 107 seconds).

9.3 Packet Builder

The Packet Builder retrieves event, register read, and high priority data from the enabled Input Channels. It also retrieves register read and high priority data from the HCCStar's command decoder and HPR logic.

9.3.1 Output Packet Format

The HCCStar has a bond pad option for selecting the default encoding mode. With a bond from the OutEncode pad to GND, the HCCStar will default to 8b10b encoding its output. If OutEncode is not bonded to GND, the HCCStar will default to no output encoding. In either case, the encoding can be changed by a register setting.

The 8b10b encoding used is the one described in [cite IBM paper][cite IBM patent], using the "out of band" control codes K28.1 for Start-of-Packet, K28.6 for End-of-Packet and K28.5 for IDLE. The packet will be divided up into 8-bit chunks to be encoded, ignoring any internal packet fields. Any bits required to make a full 8-bit chunk before the End-of-Packet control code will be set to 0.

If 8b10b encoding is not used, packets will be framed with a 3'b110 preamble and a 45'b0 postample. This makes the pre+post-ample a multiple of 8 and makes the inter-event gap longer than any possible string of zeros within an event.

9.3.1.1 Generic Packet Format

All packets start with a 4-bit TYP code. These TYP codes are the same as used in the ABCStar. The codes have been generated so that they all differ by at least two bits from each other. The codes are listed in Table 9.10.

9.3.1.2 Physics Event Packets

For PR and LP events, the full header consists of the 4-bit TYP code, a 1-bit Error Flag, the 7-bit L0tag, and a 4-bit BCID. The conditions that go into the 1-bit Error Flag will be programmable, but are TBD. The BCID field contains the 3 least significant bits of the full 8-bit BCID counter associated with the event followed by a 1-bit parity, calculated over the entire 8-bit width of the counter. While the L0tag will be check for coherence amongst the ABCStar packets and the list of L0tags in Readout Requests, the BCID will only be checked for coherence and taken from the ABCstar packets, ie the BCID will not be computed on the HCCStar.

Field	**TYP**	**Flag**	**L0ID**	**BCID**
# of bits	4	1	7	4

Table 9.11: Physics Event Packet Header

After the 16-bit header, ABCStar clusters will be sent. These 15-bit clusters are composed of the 4-bit Input Channel number the cluster was received on, and the 11-bit Cluster as received from the ABCStar, dropping the Last Cluster bit.

These clusters will be sent, one after another without separator, from all enabled input channels, taking all of the cluster for the current event before going to the next input channel. The packet will end with a fixed 15-bit cluster pattern that does not represent any valid cluster: 15'b110_1111_1110_1101 (15'h6FED).

An error block, if needed for this event, will appear at the end of the packet before the end of packet cluster pattern. It will be marked with a different invalid cluster pattern (15'b1110_11111110_100 (15'h77F4)). Following the start of error block marker will be information about which Input Channel the error occurred on and what the error was. Details TBD, but will include any set Error Flags from the ABCStar ASICs.

9.3.1.3 Register Read Packets

The header for Register Read Packets is simply the 4-bit TYP code. Note that the TYP is different for ABCStar and HCCStar register reads and the data from the two will never be combined in the same HCCStar packet.

In the case of ABCStar Register Read data, the HCCStar will output the incoming ABCStar Register Read packets, replacing the ABCStar 4-bit TYP code with the 4-bit HCCStar Input Channel number. Multiple ABCStar Register Read packets may be packed into one HCCStar packet.

The Register Read Special Mode will produce standard Register Read Packets.

[First Packet]	ABC Reg TYP (4b)	HCC Input Ch # (4b)	Register Addr (8b)	TBD (4b)	Register Data (32b)	Status Bits (16b)
[Second Packet]	—	HCC Input Ch # (4b)	Register Addr (8b)	TBD (4b)	Register Data (32b)	Status Bits (16b)

Table 9.12: ABC Register Read Packet(s)

In the case of HCCStar Register Read data, the packet will consist of the TYP code followed by 40-bit records containing the 8-bit register address, the 32-bit register contents. Multiple records can be packed into one packet.

9.3.1.4 High Priority Register Packets

High Priority Packets (HPR Packets) are exactly like Register Read Packets, except they have a dedicated TYP and contain only the High Priority Register (0x1f for ABCStar and 0xf for HCCStar). There are distinct TYPs for ABCStar and HCCStar HPR packets. These packets are sent at power-up, or full chip reset, at low rate and whenever the LCB lock status changes. See Section 9.6 for details on the HCCStar HPR.

9.3.1.5 Packet Transparent Mode Packets

In Packet Transparent Mode, the header will be the 4-bit TYP code plus the 4-bit Input Channel number. Following this header will be the full, unmodified 64-bit ABCStar packet, with the framing bits removed. The HCCStar will generate one packet for each incoming packet.

9.3.1.6 Full Transparent Mode Packets

In Full Transparent Mode, the header will be the 4-bit TYP code plus the 4-bit Input Channel number. This header will be followed by a 512-bit chunk of data.

9.4 Serializer

In the case of 8b10 encoded data, the serializer will output the 10-bit symbols lsb first, otherwise it will send the data msb first.

The output data rate will be selectable between 320 Mbps and 640 Mbps, with 320 Mbps as the default. The clock used to send the data will be available on the DataCLK output pad for diagnostic and test use. By default, the driver for this pad is turned off.

9.5 Command Decoder and Registers

The Command Decoder interfaces with the LCB decoder and provides access to read and write control registers, read status registers, and generate single pulses for various purposes with HCCStar. The control registers contain auto-correcting triplicated logic. The register read values are made available to the Packet Builder in a FIFO containing the 40-bit words, composed of the 8-bit register address and the 32-bit register value. Details of the registers and their contents can be found in Section 9.15.

9.6 High Priority Register and Logic

One Read Only register (address 0xF) is designated as the High Priority Register (HPR) and while it can be read out with a normal register read command, it can be automaticaly sent, with high priority, if any of a number of conditions are true. It is intended to provide a snapshot of the state of the HCCStar, especially the status of the LCB link, as a debugging aid.

9.6.1 HPR Packet Format

HPR packets have the same format as Register Read packets, except they have their own TYP code (Table 9.10) and they are sent in preference to any other packet type.

9.6.2 Sending of HPR Packets and Timing

An initial HPR packet is sent 500 μs after a reset, once clock signals are established. This includes: power-on reset, external hard reset (RSTB pin), Register Reset and Logic Reset.

After that, HPR packets are sent every 1 ms (subject to small timing variations).

HPR packets are also sent if the LCB_Locked bit changes state, indicating the LCB circuit has lost or regained its synchronization with the LCB signal frame.

9.6.3 Priority of HPR packets and interactions with Physics data

In the HCCStar readout, the highest priority is given to HPR packets, followed by PR, then LP packets, then other register read packets. As HPR packet transmission occurs periodically ($\sim$ 1 KHz rate), there are enough time intervals left to transmit other packets.

9.6.4 Configuration of HPR Logic Behavior

How HPR packets are sent can be controlled using 3 bits, TestHPR, StopHPR and MaskHPR, as follows:

- **To send an HPR packet immediately:** Set the TestHPR bit (bit 1) in configuration register 16 to '1'. Assuming the MaskHPR bit in configuration register 43 is '0', this actis as a one time pulse, as if the LCB_Locked bit had changed. If StopHPR had been set to '1' previously, TestHPR resumes the periodic sending of HPR packets.
- **To not receive periodic HPR packets:** Set the StopHPR bit (bit 0) in configuration register 16 to '1'. Note that a subsequent change of LCB link synchronization status will restart the periodic sending of HPR packets.
- **To not receive HPR packets when LCB_Locked changes:** Set the MaskHPR bit (bit 8) in configuration register 43 to '1'. Note that if StopHPR has not been set to one, the periodic sending of HPR packets will continue. Also, note that when MaskHPR is one, TestHPR will also be ignored.

- **To not receive *any* HPR packets:** Set the MaskHPR bit to '1'' then set the StopHPR bit to '1'. No further HPR packets will be sent.

9.6.5 Initial HPR Packet After a Reset

In all cases, at least one initial HPR packet will be sent 500 μs after the release of power-on reset or external hard reset (RSTB pin), or a Register Reset or Logical Reset (see Section 9.12).

If TestHPR is set to '1' before the 500 μs elapses, an HPR packet will be sent immediately, followed by the usual sending of HPR packets as described above.

If StopHPR is set to '1' before the 500 μs elapses, a single HPR packet will be sent immediately, and periodic HPR packets will not be sent, as described above.

9.7 Special Control Mechanism

For particularly sensitive control signals, a mechanism has been installed in HCCStar to mitigate SEU errors. The control bits in the registers have been duplicated and the requirement set that both of the control bits need to be set or cleared in order to change the state of the output. This is implemented as a 3-state state machine. The Operating Mode Register and External Reset Control registers (41/42 and 44/45) are protected by this mechanism.

9.8 Analog Monitor

A single channel Analog Monitor (AM) is implemented on the HCCStar. The AM uses a 10-bit Wilkinson ADC to measure one of five voltages, selectable via an analog MUX. The ADC is a variant the ADC used in the AMAC ASIC[2]. The quantities that can be measured are

- Bandgap voltage (for diagnostic use)
- VDD_RAW — Incoming supply voltage
- VDD_REG — Regulated voltage
- Hybrid ground
- Die temperature

The measured value is made available in a status register. In addition, it is compared with lower and upper limit values, set in a configuration register. If the measured value is outside of these limits a flag is set in the HPR register (Section 9.6) and, optionally, the HPR logic can be trigger to start sending HPR packets until the value is back within the set limits.

9.9 Voltage Regulator

The HCCStar will contain the CERN Microelectronics designed LDO voltage regulator, modified to provide an extended output range.

9.10 Addressing

Each HCCStar die will have a 24-bit serial number set by eFuse bits when the wafers are probed. This serial number will allow for tracking throughout the life of the project. Note that the serial number can be read without knowing or using the HCC ID of the ASIC by issuing a Global Read command.

The HCCStar also has a 4-bit command address, referred to as "HCC ID". This is used to identify a target HCCStar when issuing register read and write commands. This address can be set in two ways. One is through the use of the ID bond pads. Bonding a pad to ground sets the corresponding bit to '0'. If none of the bond pads are connected, a dynamic addressing mode is enabled.

The serial number will be accessible (read only) as the least significant bits of a 32-bit register, the "Addressing" register (Register 17). The most significant 4 bits of this register will be read-write bits and used as the HCC ID in dynamic addressing mode. These bits can be written by first writting a '1' into bit 2 of Register 16 to load the serial number bits into Register 17. Then issuing a Write (even a Global Write) command with the least significant 24-bits being the serial number of the ASIC for which the write command is intended and the most significant 4-bits being the value to set the HCC ID. The HCCStar will only write the most significant bits if the least significant bits match its serial number.

The register holding the dynamic HCC ID will be protected with five-fold redundancy. It will only be reset on power-up and Hard Reset.

Note, as a special case, if the ID pads are not bonded, and the dynamic address has not been programmed, the HCCStar address will be set to 0xF. Be aware, that this does not correspond to a valid module for R3 commands and corresponds to the Global Address.

9.11 eFuse Programming

Twenty-four (24) eFuse bits are available for individual chip marking. The fuse programming in done using two specific pads.

The recommended sequence for programming the eFuse bits is

1. Pull Vfuse pad from 1.5 V to 3.3 V.
2. Write the bit position to set to '1' into bits [15:12] of the CFG1 configuration register (43) using regular register write commands.
3. Pull the FusePP pad from 0 V to 1.5 V for $\sim 200\,\mu$s.
4. Pull the FusePP pad back to 0 V.
5. Repeat steps 2 through 4 until all bits to be set to '1' have been programmed.
6. Pull Vfuse pad to 1.5 V.

Once programmed the fuse bits are read only with the Fuse Register at address 17. To read the fuse bits a '1' must be first written to bit 2 of Register 16. However, this only need to be done once after Power-On, or external RSTB.

Except when programming, **the Vfuse pad power input should *always* be connected to the external VDD (1.5 V). The FusePP pad should be at 0 V. It has an internal pulldown that forces this input to zero if unconnected, satisfying this requirement.**

9.12 Resets

9.12.1 Hard Reset

Hard Reset is activated by grounding the RSTB bond pad. It will hold the entire ASIC in reset (except for the Power-On Reset logic) until the logic level on the RSTB is brought back high. The pad has an internal pull-up so that it need not be connected. This signal brings the HCCStar back to its power-on state. Hard Reset, along with Power-On Reset, are the only resets that will reset the Address Mapping register (Section 9.10).

9.12.2 Power-On Reset

Powering up HCCStar requires the external BC clock and the supply voltage at or above 1 Volt. Two blocks are used to ensure that the HCCStar powers up into a known state. The ASIC level reset is held true until both the Power Good Block (PGB) and the Power-up Clock Counter Block (PCCB) have completed their sequential power-up sequences.

The PGB holds the PowerGood signal false, which locks out the clock supplying the PCCB until the supply voltage exceeds the bandgap voltage by approximately 200 mV. Once PowerGood is asserted true, it is held true by a four-fold redundant custom latch, to avoid the possibility that a power glitch executes the reset sequence

When true, PowerGood releases the reset on the PLL and enables the PCCB counter to count 65535 40 MHz (BTC divided by 4) clocks before enabling a second counter on the PLL 40 MHz clock. This counter counts to 63 then sets PowerUpReset false. The first counter corresponds to a 1.6 ms settling time to allow the HCCStar voltage supply and regulators to settle before enabling the LCB decoder and PLL. The second counter corresponds to 1.6 μs to allow the derived clocks to settle before all clocked registers to be set to their default values.

PowerUpReset releases the ASIC level reset, allowing the reset of the ASIC to bring it into its default state.

9.12.3 Register_Reset

Register_Reset is a fast command send through the LCB protocol (see Section 9.1.2.3). It resets the entire ASIC (except for the PLL, Power-On Reset logic, and Address Mapping register, cf Section 9.10) and brings the HCCStar back to its power-on state except the programmed chip address is retained. This reset command will only affect HCCStar ASICs and will affect all HCCStar ASICs on the control segment.

9.12.4 Logic_Reset

Logic Reset is a fast command send through the LCB protocol (see Section 9.1.2.3). It resets all of the sequential logic back to its power-on state. It does not reset the memory blocks or FIFOs. This reset command will reset all ABCStar and HCCStar ASICs on the control segment.

9.12.5 PLL Reset

PLL Reset is a fast command send through the LCB protocol (see Section 9.1.2.3). It resets the PLL block.

9.12.6 SEU Reset

SEU Reset is a fast command used to reset the bits tagging SEU events in the configuration registers noted in Register 0.

9.13 Power-On State

The full reset state for the HCCState is

- Hybrid side drivers: OFF
- Input Channels: DISABLED
- Input Channel & Packet Builder mode: PHYSICS
- Trigger Mode: SINGLE LEVEL
- Output Data Rate: 320 Mbps

9.14 Trigger Rate Limitations

The HCCStar does not have any inherent rate limitations. There is no limit to the L0A rate in multilevel trigger mode. In single level trigger mode, the only limitation is from the LP readout request path.

The rate limit for L1 (LP) and R3 (PR) readout requests ultimately comes from the data output bandwidth from the HCC, with buffering available in the SRAM memories of the Input Channels, the ABCStar ASICS and the LP and PR FIFOs in the Control Channel. It is hard to estimate what the real limit is, particular as it is dependent on the occupancy and occupancy distribution across the hybrid

9.15 Programming Model

The register access mechanism is as described in the LCB protocol and Command Decoder sections above. The list of programmable values includes

- PLL output clock phases
- PLL control parameters
- Pad Driver enables

- Pad Driver current drive
- Stave side driver pre-emphasis amplitude
- Receiver enable
- Delay values for hybrid side control signals
- Delay value for Readout Clock
- Delay values for Input Channel DataIn
- Input Channel enables
- Input Channel / Packet Builder Mode
- Trigger Mode
- Autonomous Monitor limit values
- Maximum clusters per event
- Output data encoding
- Startup data mode enable
- Bandgap control

9.15.1 Register List

RO Register 0: SEU		
Signal Name	**Bits**	**Description**
HPR_SEU	[31]	SEU in HPR Logic State Machine
Reg 45 SEU	[14]	SEU in Register 45
Reg 44 SEU	[13]	SEU in Register 44
Reg 43 SEU	[12]	SEU in Register 43
Reg 42 SEU	[11]	SEU in Register 42
Reg 41 SEU	[10]	SEU in Register 41
Reg 40 SEU	[9]	SEU in Register 40
Reg 39 SEU	[8]	SEU in Register 39
Reg 38 SEU	[7]	SEU in Register 38
Reg 37 SEU	[6]	SEU in Register 37
Reg 36 SEU	[5]	SEU in Register 36
Reg 35 SEU	[4]	SEU in Register 35
Reg 34 SEU	[3]	SEU in Register 34
Reg 33 SEU	[2]	SEU in Register 33
Reg 32 SEU	[1]	SEU in Register 32
Reg 17 SEU	[0]	SEU in Register 17

RO Register 2: FrameRaw		
Signal Name	**Bits**	**Description**
lcb_frame_raw	[31:16]	LCB Raw Frame
R3L1_frame_raw	[15:0]	R3L1 Raw Frame

RO Register 15: HPR		
Signal Name	**Bits**	**Description**
lcb_frame_raw	[31:16]	LCB Raw Frame
R3L1_frame_raw	[15:2]	R3L1 Raw Frame [15:2]
lcb_locked	[1]	LCB Locked Flag
R3L1_locked	[0]	R3L1 Locked Flag

WO Register 16: Pulse		
Signal Name	**Bits**	**Description**
eFuseL	[2]	Load the eFuse register from the Fuses
TestHPR	[1]	Send a Single HPR Packet
StopHPR	[0]	Stop Sending HPR Packets

Fuse Register 17: Addressing			
Signal Name	**Bits**	**Default**	**Description**
Comm_id	[31:28] – 4	1111	Communications ID
Fuse_ID	[23:0] – 24	24'h00_0000	eFuse Serial Number
Reg 17	**[31:0]**	**32'hF000_0000**	

W/R Register 32: Delay1			
Signal Name	**Bits**	**Default**	**Description**
lcba_delay160	[25:24] – 2	00	Internal LCB processor delay for LCBa
FD_RCLK_fineDelay	[23:20] – 4	0000	Hybrid RCLK Fine Delay
hFD_LCBa_fineDelay	[19:16] – 4	0000	Hybrid LCBa Fine Delay
CFD_PRLP_coarseDelay	[13:12] – 2	00	Hybrid PRLP Coarse Delay
CFD_PRLP_fineDelay	[11:8] – 4	0000	Hybrid PRLP Fine Delay
CFD_BC_coarseDelay	[5:4] – 2	00	Hybrid BC Coarse Delay
CFD_BC_fineDelay	[3:0] – 4	0000	Hybrid BC Fine Delay
Reg 32	**[31:0]**	**32'h0000_0000**	

W/R Register 33: Delay2			
Signal Name	**Bits**	**Default**	**Description**
FD_DataIn7_fineDelay	[31:28] – 4	0000	ABC Data In 7 Fine Delay
FD_DataIn6_fineDelay	[27:24] – 4	0000	ABC Data In 6 Fine Delay
FD_DataIn5_fineDelay	[23:20] – 4	0000	ABC Data In 5 Fine Delay
FD_DataIn4_fineDelay	[19:16] – 4	0000	ABC Data In 4 Fine Delay
FD_DataIn3_fineDelay	[15:12] – 4	0000	ABC Data In 3 Fine Delay
FD_DataIn2_fineDelay	[11:8] – 4	0000	ABC Data In 2 Fine Delay
FD_DataIn1_fineDelay	[7:4] – 4	0000	ABC Data In 1 Fine Delay
FD_DataIn0_fineDelay	[3:0] – 4	0000	ABC Data In 0 Fine Delay
Reg 33	**[31:0]**	**32'h0000_0000**	

W/R Register 34: Delay3			
Signal Name	**Bits**	**Default**	**Description**
FD_DataIn10_fineDelay	[11:8] – 4	0000	ABC Data In 10 Fine Delay
FD_DataIn9_fineDelay	[7:4] – 4	0000	ABC Data In 9 Fine Delay
FD_DataIn8_fineDelay	[3:0] – 4	0000	ABC Data In 8 Fine Delay
Reg 34	**[31:0]**	**32'h0000_0000**	

W/R Register 35: PLL1			
Signal Name	**Bits**	**Default**	**Description**
ePllEnablePhase	[23:16] – 8	1111_1111	Enable specific phasesPhase
ePllReferenceFrequency	[13:12] – 2	01	01 = 40 MHZ, 10 = 80 MHz, 11 = 160 MHz
ePllRes	[11:8] – 4	1011	ePLL Resistor value (6 KΩ)
ePllCap	[5:4] – 2	00	ePLL Loop Filter Capacitance value (0 = 30 pF)
ePllIcp	[3:0] – 4	0101	ePLL Charge Pump Current (5 = 42.5 μA)
Reg 35	**[31:0]**	**32'h00FF_1B05**	

W/R Register 36: PLL2			
Signal Name	**Bits**	**Default**	**Description**
ePllPhase320MHzC	[11:8] – 4	0000	Phase of clk320C (22.5 degree steps)
ePllPhase320MHzB	[7:4] – 4	0000	Phase of clk320B (22.5 degree steps)
ePllPhase320MHzA	[3:0] – 4	0000	Phase of clk320A (22.5 degree steps)
Reg 36	**[31:0]**	**32'h0000_0000**	

W/R Register 37: PLL3			
Signal Name	**Bits**	**Default**	**Description**
ePllPhase160MHzC	[20:16] – 4	0_0000	Phase of clk160C (11.25 degree steps)
ePllPhase160MHzB	[12:8] – 4	0_0000	Phase of clk160B (11.25 degree steps)
ePllPhase160MHzA	[4:0] – 4	0_0001	Phase of clk160A (11.25 degree steps)
Reg 37	**[31:0]**	**32'h0000_0001**	

W/R Register 38: DRV1			
Signal Name	**Bits**	**Default**	**Description**
RCLK_HYB_en	[27] – 1	0	Enable Hybrid RCLK driver
RCLK_HYB_cur	[26:24] – 3	000	Hybrid PRLP driver current
PRLP_HYB_en	[23] – 1	0	Enable Hybrid RCLK driver
PRLP_HYB_cur	[22:20] – 3	000	Hybrid RCLK driver current
LCBa_HYB_en	[19] – 1	0	Enable Hybrid RCLK driver
LCBa_HYB_cur	[18:16] – 3	000	Hybrid RCLK driver current
BC_HYB_en	[15] – 1	0	Enable Hybrid RCLK driver
BC_out_cur	[14:12] – 3	000	Hybrid RCLK driver current
R3L1_out_en	[11] – 1	0	Enable Hybrid RCLK driver
R3L1_out_cur	[10:8] – 3	000	Hybrid RCLK driver current
LCB_out_en	[7] – 1	0	Enable Hybrid RCLK driver
LCB_out_cur	[6:4] – 3	000	Hybrid RCLK driver current
STVclk_out_en	[3] – 1	0	Enable Hybrid RCLK driver
STVclk_out_cur	[2:0] – 3	000	Hybrid RCLK driver current
Reg 38	**[31:0]**	**32'h0000_0000**	

W/R Register 39: DRV2			
Signal Name	**Bits**	**Default**	**Description**
DataCLK_enable	[4] – 1	0	Enable DataCLK driver
DataCLK_enpre	[3] – 1	0	Enable DataCLK driver pre-emphasis
DataCLK_cur	[2:0] – 3	000	DataCLK driver current
Data2_enable	[4] – 1	0	Enable Data2 driver
Data2_enpre	[3] – 1	0	Enable Data2 driver pre-emphasis
Data2_cur	[2:0] – 3	000	Data2 driver current
Data1_enable	[4] – 1	1	Enable Data1 driver
Data1_enpre	[3] – 1	0	Enable Data1 driver pre-emphasis
Data1_cur	[2:0] – 3	100	Data1 driver current
Reg 39	**[31:0]**	**32'h0000_0014**	

W/R Register 40: ICenable			
Signal Name	**Bits**	**Default**	**Description**
IC_enable	[10:0] – 11	000_0000_0000	Input Channel Enables
Reg 40	**[31:0]**	**32'h0000_0000**	

W/R Register 41/42: OPmode/OPmodeC			
Signal Name	**Bits**	**Default**	**Description**
encode_8b10b	[17] – 1	1	0 = no encoding, 1 = 8b10b encoding
encode_cntl	[16] – 1	0	0 = Use pad, 1 = Use register to control output encoding
max_Npacket	[14:12] – 3	000	Maximum number of ABC packets: 0 = 16,1 = 1,2 = 2,3 = 4,4 = 8
operating_mode	[9:8] – 2	00	'00 = Physics
readout_speed	[4] – 1	0	'0 = 320MHz,1 = 640MHz
trigger_mode	[0] – 1	0	'0 = Multilevel trigger, 1 = Single level trigger
Reg 41/42	**[31:0]**	**32'h0002_0000**	

W/R Register 43: Cfg1			
Signal Name	**Bits**	**Default**	**Description**
efuse_prog_bit	[16:12] – 5	0	Bit of eFuse to set to '1' when programming
MaskHPR	[8] – 1	0	Prevent HPR packets from being sent
BG_setting	[4:0] – 5	0_0000	Bandgap setting
Reg 43	**[31:0]**	**32'h0000_0000**	

W/R Register 44/45: ExtRst/ExtRstC			
Signal Name	**Bits**	**Default**	**Description**
AMAC_SSSH	[4] – 1	0	AMAC Communications Reset
ABC_ResetB	[0] – 1	1	ABCStars External Reset
Reg 44/45	**[31:0]**	**32'h0000_0000**	

10 Radiation Tolerance and Other Special Requirements

HCCStar must be radiation tolerant to a Total Ionizing Dose (TID) of 50 MRad and non-ionizing fluence of $12.2\times10^{14}\,n_{\mathrm{eq}}\mathrm{cm}^2$[8]. The effects of SEU must be mitigated throught the use of triplication and hamming codes. See Section 12.3.

11 Testing, Validation and Commissioning

The initial testing of HCCStar will use single chip cards to verify basic funcationality. ABCStar ASICs, interfaced to the HCCStar, will be emulated in an FPGA. It is expected that test vectors generated from pre-submission verification simulations can be used for ASIC verfication. More realistic data flows and timings from emulated ABCStar ASICs will also be used.

Further functional tests will occur on hybrids with multiple real ABCStar ASICs and an HCCStar. Either these boards, or specially built multi-chip boards will be irradiated to look at radiation tolerance and SEU effects within the chipset.

Production testing will be done as wafer probing. The experience with the single chip card funcational testing will drive the decision making for what needs to be tested during wafer probing.

12 Reliability Matters

12.1 Consequences of Failure

A failure of the HCCStar will cause the lost of the ability to read out an entire hybrid of 5 – 11 ABCStar ASICs.

12.2 Prior Knowledge of Expected Reliability

The reliability of the GF130 process has been validated over many designs for various LHC experiments. The previous version of the HCCStar, the HCC130, has been used in many of modules and has been irradiated without significant problems. The HCCStar differs in several important ways from the HCC130, but several of the underlying blocks are the same and the standard cell library is the same.

12.3 Measures Proposed to Insure Reliability of Component and/or System

All of the control registers in HCCStar have been triplicated to mitigate the effects of SEU. This triplication includes an auto-correction feature. In addition, certain particularly sensitive control functions have been protected by two separate bits in the control registers to further mitigate the effects of SEU (cf: 9.7).

Also, all state registers in Finite State Machines (FSMs) in HCCStar have been protected with a hamming code so that any single bit error will bring the FSM back to the correct state.

For the LCB and R3_L1 decoders, logic influencing the locked status of the link is protected. Flags and counts of errors are provided.

12.4 Quality Control to Validate Reliability Specifications during Production

A statistically significant sample of HCCStar ASICs will be tested under adverse environmental conditions, including irradiation, to demonstrate their reliability. Tests well beyond the expected temperature and radiation ranges are foreseen.

12.5 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

References

[1] "ATLAS ITk Electronics Specification: ABCStar", EDMS AT2-IS-CD-0002, https://edms.cern.ch/document/AT2-IS-CD-0002

[2] "ATLAS ITk Electronics Specification: AMAC", EDMS AT2-IS-CD-0004, https://edms.cern.ch/document/AT2-IS-CD-0004

[3] "ATLAS ITk Electronics Specification: Bus TApe", EDMS AT2-IS-ES-0006, https://edms.cern.ch/document/AT2-IS-ES-0006

[4] "ATLAS ITk Electronics Specification: EOS", EDMS AT2-IS-ES-0003, https://edms.cern.ch/document/AT2-IS-ES-0003

[5] "ATLAS ITk Electronics Specification: Hybrid", EDMS AT2-IS-CD-0005, https://edms.cern.ch/document/AT2-IS-CD-0005

[6] "ATLAS ITk Electronics Specification: Module", EDMS AT2-IS-CD-0006, https://edms.cern.ch/document/AT2-IS-CD-0006

[7] "ATLAS ITk Electronics Specification: Power Board", EDMS AT2-IS-CD-0007, https://edms.cern.ch/document/AT2-IS-CD-0007

[8] ATLAS ITk Strips TDR