ITk Strip Module Powerboard Specification

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4 Abstract

The powerboard is a circuit board located on each Strip module. It serves three functions: local low-voltage regulation, low-voltage and high-voltage switching, and monitoring. It uses four custom ASICs to fulfil these functions: the bPOL12V for low-voltage regulation, the HVmux for high-voltage switching, the AMAC for control and monitoring, and linPOL12V to provide both voltages for AMAC.

10 Revision History

Revision	Date	Author(s)	Description			
1.2	23.01.2018	Heim	Updating fluence, TID numbers, and max			
			& nom. currents, implementing some com-			
			ments from EDMS (Sperlich, Weidberg)			
1.1	05.11.2017	Sperlich, Heim	Implementing commends from EDMS			
			(Phllips, Greenall, Weidberg, Sperlich,			
			Mahboubi, Goettlicher), update of geometry			
			constrains of EC PB, linPOL12V potentially			
			untested on PB, 1.5kV is 2xnominal			
1.0	10.10.2017	Heim	Major revision of barrel powerboard sections			
0.3	21.3.2017	Sperlich, Heim	Adding comments from Affolder, Fadeyev,			
			Stanitzki, Sawyer, Teuscher			
0.2	21.3.2017	Sperlich, Heim	Add Endcap specification, add updated sys-			
			tem info			
0.1	06.01.2017	Heim	Initial version			

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1 Conventions and Glossary

The acronyms used are listed in Table 2.

Table 2: List of Acronyms

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Acronym	Description				
bPOL12V	Rad-hard DC-DC buck converter ASIC				
linPOL12V	Rad-hard dual voltage linear regulator ASIC				
AMAC	Autonomous monitor and control ASIC				
HVmux	Rad-hard high-voltage (transistor) switch				
EoS	End of Substructure				
PCB	Printed circuit board				

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2 Related Documents

- 41 The powerboard is loaded with the following custom ICs or special devices:
- bPOL12V [ref]
- linPOL12V [ref]
- AMAC [5]
- HVmux ¹
- 46 The powerboard interfaces with two components: the Strip hybrid and the bus tape. The
- powerboard is a component of the Strip Module.

⁴⁸ 3 Description of Component or Facility

- 49 The powerboard fulfils four functions: local low-voltage regulation, monitoring and control
- 50 of low-voltage and high-voltage, enable signals and shunt current on the hybrids as well
- 51 as monitoring of temperatures on the hybrids and powerboard. The power architecture is
- shown in Figure 1 for the barrel modules and some of the end-cap modules and in Figure 2
- 53 for dual converter end-cap R3 module. Each module is connected in parallel to LV power,
- 54 HV bias and two multi-drop, AC coupled LVDS communication buses.

¹Equivalent to device PGA26E19BA https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/FLY000075_EN.pdf

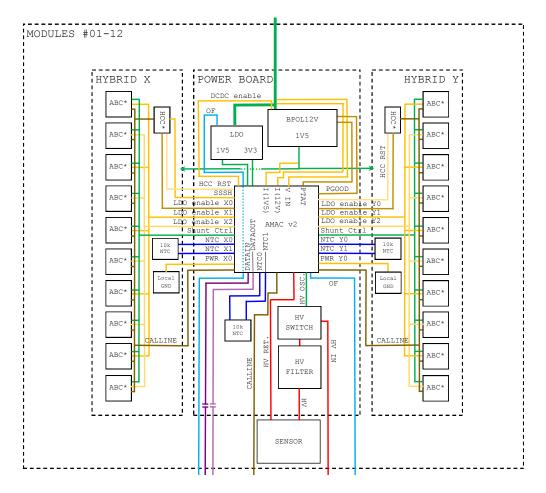


Figure 1: Diagram interconnection of the powerboard to the hybrids and bustape in case of a barrel or end-cap R0 or R1 module.

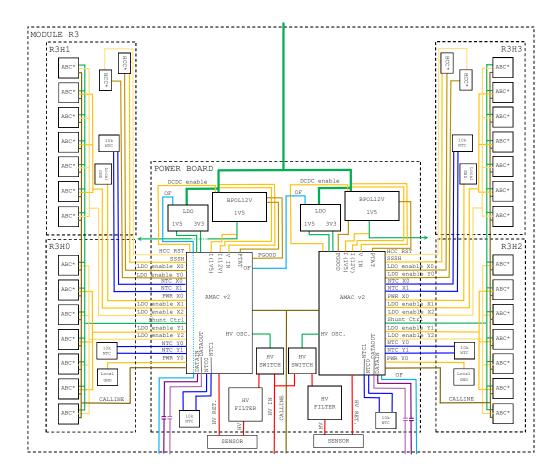


Figure 2: Diagram interconnection of the powerboard to the hybrids and bustape in case of an end-cap R3 module.

To reduce currents through the LV bus the voltage will be nominally 10-11 V and regulated locally on the powerboard to the required 1.5V for the hybrid. Regulation is performed by the bPOL12V ASIC which contains a switching DC-DC buck-converter circuit. The buck-converter circuit requires an external inductor, which needs to be an air-core coil due to the 2 T magnetic field the strip detector is submerged in. Conducted noise is reduced by implementing appropriate filtering. To prevent the radiated switching noise from coupling into the sensor or front-end electronics, the circuitry relevant for the DC-DC conversion is encased in an EM shield box.

The HV bias is supplied to up to four modules in parallel. This could be an issue in the case of one sensor suffering from an early breakdown, preventing the other sensors from being biased at their operational voltage. For this reason the HVmux is located on the powerboard, it is a rad-hard high voltage transistor which can switch on/off the HV bias for the module it is located on.

Each powerboard has an RC filter on the HV output towards the sensor to reduce conducted noise.

The bPOL12V and HVmux are controlled by the AMAC, which has two control outputs specifically for this purpose. As the HVmux requires a higher voltage than the AMAC can supply for switching, the AMAC generates a clock signal with programmable frequency of 25 kHz, 50 kHz or 100 kHz at an I/O voltage of 3 V, which is fed into an AC coupled quad voltage multiplier circuit to create the gate voltage with reference to the HVin. The AMAC is powered by a 1.4V linear regulator in the linPOL12V, by default this regulator is enabled such that the default power-on state of the AMAC is on, but it can be disabled by the OF line from a neighbouring module. The linPOL12V is also used to generate the 3 V reference voltage for the HV enable signal of the AMAC.

To allow for a controlled turn on of the Hybrids, the AMAC has 6 additional digital control outputs to enable the LDO in each HCCStar [4] and half of each hybrids ABCStars [3] separately. The AMAC also accommodates four DACs. Two are used to provide a voltage reference to all ABCStar on each hybrid. The other two are used to control the gate of a shunt transistor in all ABCStar on each hybrid. This provision adds the possibility to artificially increase the power consumption, which might be used to keep constant power consumptions and thus constant temperatures even during changing current draws due to radiation damage.

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The AMAC can also control the bPOL12V output voltage via two digital lines.

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The full list of AMAC functionalities is shown in its specification document [?]. For convenience we provide an abbreviated description below.

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- The AMAC contains an ADC which enables the monitoring of various quantities:
 - Input voltage: the input voltage can be monitored by attenuating it on the power-board such that it is in the acceptable range of the AMAC ADC (x1/10).
 - Input current: to measure the input current the filter inductor can be used as a shunt with (50 m Ω -100 m Ω) and the voltage differential has to be amplified inside the AMAC by an operational amplifier.
 - bPOL12V Pgood: bPOL12V power good signal (digital), which should signal good voltage output conditions of the bPOL12V.
 - Output voltage: the output voltage can be monitored by attenuating it within AMAC such that it is in the acceptable range of the ADC (x2/3).
 - Output current: to measure the output current the filter inductor can be used as a shunt with ($\approx 7 \text{ m}\Omega$) and the voltage differential has to be amplified inside the AMAC by an operational amplifier.
 - bPOL12V internal temperature: the internal temperature of the bPOL12V is converted by a diode circuit to a voltage which can be monitored (no absolute measurement).
 - bPOL12V external temperature: the resistance of a thermistor placed inside the shield volume can monitored.
 - AMAC internal temperature: the internal temperature of the AMAC is converted by a diode circuit to a voltage which can be monitored (no absolute measurement).
 - 2x Hybrid temperature: the resistance of thermistors placed on each hybrid can be monitored.
 - Hybrid ground rise: the voltage drop along the wirebonds to the hybrid and the groundplane in the hybrids
 - Sensor leakage current: the sensor leakage current is sinked into the AMAC and converted into a voltage which can be monitored, over the lifetime of the detector the leakage current will increase from the nA range to mA.
 - Calibration line: a voltage to calibrate the AMAC ADC supplied by the EoS in parallel to all powerboards

$_{\scriptscriptstyle 11}$ 4 Interfaces

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This component uses and interfaces with other components listed in Table 3.

Table 6. Components	which interface to this component.
Name of Component	Name of Component Specification
Bustape	Bus Tape Specification [7]
Hybrid	Hybrid Specification Document [6]
AMAC	AMAC specification document [5]
bPOL12V	bPOL12V Datasheet [ref]
linPOL12V	linPOL12V Datasheet [ref]

Table 3: Components which interface to this component.

5 Physical Description

The powerboard is a PCB made of a 4-layer Polyimide and Copper stack-up, see Figure 3 with blind or buried vias, such that bottom GND plane is not perforated with other, potentially noise inducing, signals. The bottom GND is fully covered with stop mask to avoid direct electrical contact to the sensor.

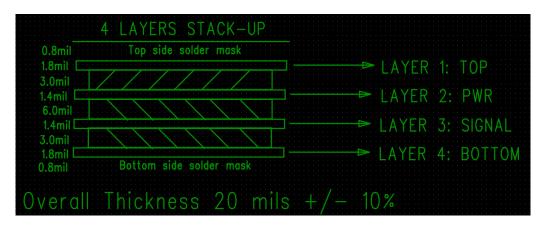


Figure 3: Cross section picture of the flex PCB stack-up. PRELIMINARY rigid!

The powerboard is 11 mm wide, 74 mm long, and 5 mm high (at the highest point, excluding PCB stackup height) for the barrel modules. For the 6 endcap modules, there will 4 different powerboards. For the modules R0, R1 there will be a powerboard with similar connectivity as the barrel powerboard with a maximal width of 17 mm and 60 mm length, following a curve of 530 mm radius. The R2 powerboard needs to be more narrow with 14 mm but can be longer with up to 80 mm with a curvature of 630 mm. The current needs in R3 requires a powerboard to contain two bPOL12V and thus due to the 4 HCCStar and 4 hybrids, two AMACs will be used here as well. The size of this powerboard should be 30 mm wide and 62 mm long with a curvature of 700 mm radius. R4 and R5 get the same powerboard geometry. In both cases the two hybrids are only on

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one side of the powerboard and the outer constrains of the powerboard are 35 mm width and 75 mm length with a curvature of 940 mm radius. For all endcap powerboards the height from the bottom surface of the powerboard should not be higher than 5.3 mm and the bPOL12V containing DCDC block will be located near the center of the sensor. A top-down schematic of the barrel powerboard is shown in Figure 4, also shown are the pad locations of the connections made to the bus tape and hybrid. It has connections to the bus tape on one short side and connection on both long sides to the left and right hybrid. All pads are listed in Table 6-9.

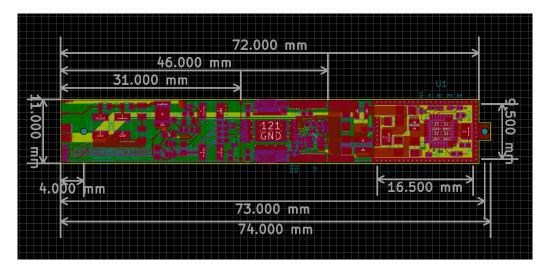


Figure 4: Powerboard x/y dimensions. PRELIMINARY!

146 6 Thermal characteristics

The bPOL12V DCDC converter will dissipate around 1.8 W of power and the linear regulator will dissipate around 0.5 W due to the large drop from 11 V to 1.4V at 50 mA, hence good thermal conductivity also needs to be ensured underneath the linear regulator. The backside of the powerboard will be cooled. It is therefore important that there is a good thermal contact from the bPOL12V thermal pad and the linear regulator thermal pad underneath the chip packages.

7 Identification

154 TBD, either AMAC unique ID or some visual marking

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TBD 157

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9 Power

Table 4 contains the estimates for nominal current draw. The powerboard is designed to 159 be able to supply a maximum of 4 A per bPOL12V at a nominal input voltage of 11 V and an efficiency of at least 60% (at max current), summarised on Table 5. The R3 powerboard 161 has two bPOL12V, and is specified to supply up to 6 A $(2 \times 3 \text{ A})$. This maximum current 162 draw is sufficient to cope with the expected temporary increase in current draw due to radiation damage in the readout chips. The HV ratings given are operational conditions at end-of-life of the detector.

Table 4: Expected nominal input and output power requirements (nominal scenario, not including safety factors). The HV input is increased with respect to the sensor input to accommodate the voltage drop created by HV filter.

Board	HV		LV in		LV out		
	voltage	current	voltage	current	voltage	current	
Barrel	520 V	1.3 mA	11 V	0.6 A	1.5 V	2.66 A	
R0/R1/R2	520 V	1.2 mA	11 V	0.58 A	1.5 V	2.7.6 A	
R3	530 V	2.1 mA	11 V	0.85 A	1.5 V	$2 \times 1.98 \text{ A}$	
R4/R5	520 V	1.3 mA	11 V	0.52 A	1.5 V	2.42 A	

Table 5: Maximum HV and LV input and output power ratings (pessimistic scenario, including safety factors). The HV input is increased with respect to the sensor input to accommodate the voltage drop created by HV filter.

Board	HV		LV in		LV out		
	voltage	current	voltage	current	voltage	current	
Barrel	750 V	4.1 mA	11 V	0.86 A	1.5 V	3.38 A	
R0/R1/R2	730 V	2.8 mA	11 V	0.81 A	1.5 V	3.54 A	
R3	770 V	6.9 mA	11 V	1.09 A	1.5 V	$2 \times 2.43 \text{ A}$	
R4/R5	730 V	$2.6 \mathrm{mA}$	11 V	0.68 A	1.5 V	3.04 A	

6 10 Input/Output

The inputs and outputs of the powerboard are listed in Tables 6-9. All enable and disable signals are chosen in a way that the default (unbonded and unpowered) state results in an operating module, except for the enable of the bPOL12V DCDC converter, which needs to be actively enabled with AMAC. A single failed AMAC should not pull the OF line to a state where the linPOL12V powering the AMAC of the neighbouring powerboard is switched off. This is summarised in Table 10.

Table 6: Pad/Pin or Connector Assignment for barrel powerboards. X hybrid is located on one side of the powerboard, Y on the other.

	owerboard, I on the other.
Name or Number	Description
Bus tape:	
$\mathrm{HV}_{-}\mathrm{IN}$	High voltage bias input
$\mathrm{HV}_{ ext{-}}\mathrm{OUT}$	High voltage bias output to sensor
$\mathrm{LV}_{-}\mathrm{IN}$	Low voltage input positive
LV_IN_RTN	Low voltage input return
DATAIN_P	differential data in
DATAIN_N	differential data in
DATAOUT_P	differential data out
DATAOUT_N	differential data out
OF_IN	control line from neighboring module, to bPOL12V
OF_OUT	control line to neighboring module, from AMAC
CALLINE	analog calibration voltage from EoS to AMAC ADC
To hybrids:	
HV_OUT_RTN_X	High voltage bias output return
HV_OUT_RTN_Y	High voltage bias output return
LV_OUT_X	Regulated low voltage output to X hybrid
LV_OUT_X_RTN	Regulated low voltage output return from X hybrid
LV_OUT_Y	Regulated low voltage output to Y hybrid
LV_OUT_Y_RTN	Regulated low voltage output return from Y hybrid
NTC_X0	Thermistor temp. measurement on X hybrid
$NTC_{-}X1$	Thermistor temp. measurement return on X hybrid
$NTC_{-}Y0$	Thermistor temp. measurement on Y hybrid
NTCY1	Thermistor temp. measurement return on Y hybrid
CALLINE_X	analog voltage, from AMAC DAC for all ASICs on the hybrids
$CALLINE_Y$	analog voltage, from AMAC DAC for all ASICs on the hybrids
$Shunt_Ctrl_X$	Shunt control from AMAC to ABCStar on hybrids
$Shunt_Ctrl_Y$	Shunt control from AMAC to ABCStar on hybrids
$SSSH_X$	Communication reset of AMAC from HCCStar of X hybrid
$\mathrm{SSSH}_{-}\mathrm{Y}$	Communication reset of AMAC from HCCStar of X hybrid
HCC_RST_X	Reset of HCCStar on hybrid X from AMAC
HCC_RST_Y	Reset of HCCStar on hybrid Y from AMAC
LDO_EN_X0	Regulator enable from AMAC to HCCStar on X hybrid
LDO_EN_X1	Regulator enable from AMAC to half of the ABCStar on X hybrid
LDO_EN_X2	Regulator enable from AMAC to half of the ABCStar on X hybrid
LDO_EN_Y0	Regulator enable from AMAC to HCCStar on Y hybrid
LDO_EN_Y1	Regulator enable from AMAC to half of the ABCStar on Y hybrid
LDO_EN_Y2	Regulator enable from AMAC to half of the ABCStar on Y hybrid
PWR_X0	local ground on X hybrid measured by AMAC
$PWR_{-}Y0$	local ground on Y hybrid measured by AMAC 12

Table 7: Pad/Pin or Connector Assignment for the end-cap R0,R1 and R2 module powerboard. H0 hybrid is located on one side of the powerboard, H1 on the other.

	ocated on one side of the powerboard, fit on the other.
Name or Number	Description
Bus tape:	
HV_IN	High voltage bias input
$\mathrm{HV}_{-}\mathrm{OUT}$	High voltage bias output to sensor
LV_IN	Low voltage input positive
LV_IN_RTN	Low voltage input return
DATAIN_P	differential data in
DATAIN_N	differential data in
DATAOUT_P	differential data out
DATAOUT_N	differential data out
$OF_{-}IN$	control line from neighboring module, to bPOL12V
$\mathrm{OF}_{ ext{-}}\mathrm{OUT}$	control line to neighboring module, from AMAC
CALLINE	analog calibration voltage from EoS to AMAC ADC
Left/Right hybrid:	
HV_OUT_RTN	High voltage bias output return
LV_OUT_0	Regulated low voltage output to H0 hybrid
LV_OUT_0_RTN	Regulated low voltage output return from H0 hybrid
LV_OUT_1	Regulated low voltage output to H1 hybrid
LV_OUT_1_RTN	Regulated low voltage output return from H1 hybrid
NTC_H0_0	Thermistor temp. measurement on H0 hybrid
NTC_H0_1	Thermistor temp. measurement on H0 hybrid
NTC_H1_0	Thermistor temp. measurement on H1 hybrid
NTCH11	Thermistor temp. measurement on H1 hybrid
CALLINE	analog voltage, from AMAC DAC for all ASICs on the hybrids
$Shunt_Ctrl$	Shunt control from AMAC to ABCStar on hybrids
$SSSH_0$	Communication reset of AMAC from HCCStar of H0 hybrid
HCC_RST_H0	Reset of HCCStar on hybrid H0 from AMAC
$HCC_RST_H0_1$	Reset of second HCCStar on hybrid H0 from AMAC
HCC_RST_H1	Reset of HCCStar on hybrid H1 from AMAC
LDO_EN_H0_0	Regulator enable from AMAC to HCCStar on H0 hybrid
LDO_EN_H0_1	Regulator enable from AMAC to half of the ABCStar on H0 hybrid
LDO_EN_H0_2	Regulator enable from AMAC to half of the ABCStar on H0 hybrid
LDO_EN_H0_3	Regulator enable from AMAC to second HCCStar on H0 hybrid, same as LDO_EN_H1_0
LDO_EN_H1_0	Regulator enable from AMAC to HCCStar on H1 hybrid
LDO_EN_H1_1	Regulator enable from AMAC to half of the ABCStar on H1 hybrid
LDO_EN_H1_2	Regulator enable from AMAC to half of the ABCStar on H1 hybrid
PWR_H0	local ground on H0 hybrid measured by AMAC
PWR_H1	local ground on H1 hybrid measured by AMAC

 PWR_H3

Table 8: Pad/Pin or Connector Assignment for the end-cap R3 module powerboard. H0 and H1 hybrid is located on one side of the powerboard, H2 and H3 on the other.

	ed on one side of the powerboard, H2 and H3 on the other.	_
Name or Number	Description	_
Bus tape:		-
HV_IN	High voltage bias input	
HV_OUT_S0	High voltage bias output to sensor S0	
HV_OUT_S1	High voltage bias output to sensor S1	
$LV_{-}IN$	Low voltage input positive	
LV_IN_RTN	Low voltage input return	
$DATAIN_{-}P$	differential data in	
DATAIN_N	differential data in	
DATAOUT_P	differential data out	
DATAOUT_N	differential data out	
OF_IN	control line from neighboring module, to bPOL12V	
OF_OUT	control line to neighboring module, from AMAC	
CALLINE	analog calibration voltage from EoS to AMAC ADC	_
Left/Right hybrid:		=
HV_OUT_S0_RTN	High voltage bias output return from sensor S0	
HV_OUT_S1_RTN	High voltage bias output return from sensor S1	
LV_OUT_01	Regulated low voltage output for hybrids H0 and H1	
LV_OUT_01_RTN	Regulated low voltage output return from hybrids H0 and H1	
LV_OUT_23	Regulated low voltage output for hybrids H2 and H3	
LV_OUT_23_RTN	Regulated low voltage output return from hybrids H2 and H3	
NTC_H0_0	Thermistor temp. measurement on H0 hybrid	
NTC_H0_1	Thermistor temp. measurement on H0 hybrid	
NTC_H1_0	Thermistor temp. measurement on H1 hybrid	
NTC_H1_1	Thermistor temp. measurement on H1 hybrid	
${ m NTC_H2_0}$	Thermistor temp. measurement on H2 hybrid	
$NTC_{-}H2_{-}1$	Thermistor temp. measurement on H2 hybrid	
NTC_H3_0	Thermistor temp. measurement on H3 hybrid	
NTC_H3_1	Thermistor temp. measurement on H3 hybrid	
CALLINE	analog voltage, from AMAC DAC for all ASICs on the hybrids	
$Shunt_Ctrl$	Shunt control from AMAC to ABCStar on hybrids	
SSSH_0	Communication reset of AMAC from HCCStar of H0 hybrid	
HCC_RST_H0	Reset of HCCStar on hybrid H2 serving H0 from AMAC	
HCC_RST_H2	Reset of HCCStar on hybrid H2 serving H2 from AMAC	
SSSH_1	Communication reset of AMAC from HCCStar of H3 hybrid	
HCC_RST_H1	Reset of HCCStar on hybrid H3 serving H1 from AMAC	
HCC_RST_H3	Reset of HCCStar on hybrid H3 serving H3 from AMAC	
LDO_EN_H0_0	Regulator enable from AMAC to HCCStar on H0 hybrid	
LDO_EN_H0_1	Regulator enable from AMAC to half of the ABCStar on H0 hybrid	
LDO_EN_H0_2	Regulator enable from AMAC to half of the ABCStar on H0 hybrid	
LDO_EN_H1_0	Regulator enable from AMAC to HCCStar on H1 hybrid	
LDO_EN_H1_1	Regulator enable from AMAC to half of the ABCStar on H1 hybrid	
LDO_EN_H1_2	Regulator enable from AMAC to half of the ABCStar on H1 hybrid	
LDO_EN_H2_0	Regulator enable from AMAC to HCCStar on H2 hybrid	
LDO_EN_H2_1	Regulator enable from AMAC to half of the ABCStar on H2 hybrid	14
LDO_EN_H2_2	Regulator enable from AMAC to half of the ABCStar on H2 hybrid	
LDO_EN_H3_0	Regulator enable from AMAC to HCCStar on H3 hybrid	
LDO_EN_H3_1	Regulator enable from AMAC to half of the ABCStar on H3 hybrid	
LDO_EN_H3_2 PWR_H0	Regulator enable from AMAC to half of the ABCStar on H3 hybrid local ground on H0 hybrid measured by AMAC	
PWR_H1	local ground on H0 hybrid measured by AMAC	
PWR_H2	local ground on H1 hybrid measured by AMAC local ground on H2 hybrid measured by AMAC	
1 1111111111111111111111111111111111111	local ground on 112 hybrid measured by AMAC	

local ground on H3 hybrid measured by AMAC

Table 9: Pad/Pin or Connector Assignment for the end-cap R4 and R5 module powerboard.

H0 and H1 hybrid are located on one side of the powerboard.

	e located on one side of the powerboard.
Name or Number	Description
Bus tape:	
$\mathrm{HV}_{-}\mathrm{IN}$	High voltage bias input
HV_OUT_S0	High voltage bias output to sensor S0
HV_OUT_S1	High voltage bias output to sensor S1
$LV_{-}IN$	Low voltage input positive
LV_IN_RTN	Low voltage input return
DATAIN_P	differential data in
DATAIN_N	differential data in
DATAOUT_P	differential data out
DATAOUT_N	differential data out
OF_IN	control line from neighboring module, to bPOL12V
$\mathrm{OF}_{ ext{-}}\mathrm{OUT}$	control line to neighboring module, from AMAC
CALLINE	analog calibration voltage from EoS to AMAC ADC
Left/Right hybrid:	
HV_OUT_S0_RTN	High voltage bias output return from sensor S0
HV_OUT_S1_RTN	High voltage bias output return from sensor S1
LV_OUT	Regulated low voltage output
LV_OUT_RTN	Regulated low voltage output return
NTC_H0_0	Thermistor temp. measurement on H0 hybrid
NTC_H0_1	Thermistor temp. measurement on H0 hybrid
NTC_H1_0	Thermistor temp. measurement on H1 hybrid
NTC_H1_1	Thermistor temp. measurement on H1 hybrid
CALLINE	analog voltage, from AMAC DAC for all ASICs on the hybrids
$Shunt_Ctrl$	Shunt control from AMAC to ABCStar on hybrids
$SSSH_0$	Communication reset of AMAC from HCCStar of H0 hybrid
HCC_RST_H0	Reset of HCCStar on hybrid H1 serving H0 from AMAC
HCC_RST_H1	Reset of HCCStar on hybrid H1 serving H1 from AMAC
$LDO_EN_H0_0$	Regulator enable from AMAC to HCCStar on H0 hybrid
$LDO_EN_H0_1$	Regulator enable from AMAC to half of the ABCStar on H0 hybrid
$LDO_EN_H0_2$	Regulator enable from AMAC to half of the ABCStar on H0 hybrid
LDO_EN_H1_0	Regulator enable from AMAC to HCCStar on H1 hybrid
LDO_EN_H1_1	Regulator enable from AMAC to half of the ABCStar on H1 hybrid
LDO_EN_H1_2	Regulator enable from AMAC to half of the ABCStar on H1 hybrid
PWR_H0	local ground on H0 hybrid measured by AMAC
PWR_H1	local ground on H1 hybrid measured by AMAC

Table 10: Logic Level definitions for signals interfacing with the powerboard

C: 1	G	D+:+:	D-1	After	Normal	Pull-Up
Signal	Source	Destination	Polarity	power-up	operation	/Down
DCDC enable	AMAC	bPOL12V	Enable High	Low	High	Down
OF	AMAC	linPOL12V	Enable Low	Low	Low	Down
HCC RST	AMAC	HCCstar	Reset Low	High	High	Up
SSSH	HCCstar	AMAC	Reset Low	High	High	Up
LDO enable	AMAC	HCCstar	Enable High	Low	High	Up
LDO enable	AMAC	ABCstar	Enable High	Low	High	Up
PGood	bPOL12V	AMAC	Enable High	Low	High	Down
HV enable	AMAC	HVmux	Enable On	Off	On	N/A

173 11 Detailed Description and Specification

The powerboard fulfils four functions on the ITk Strip module: it generates 1.5 V to power the hybrids, control LV and HV supply to the module, it contains autonomous interlock functionality, as well as enabling groups of ASICs on the hybrid, and monitors various voltages, currents, and temperature on the module.

178 11.1 Power

The powerboard is connected to the 11 V LV bus. It uses the bPOL12V buck converter to step down the input voltage to 1.5 V for the hybrids. Also it contains a dual-voltage linear regulator, the linPOL12V, to power the AMAC (1.4 V), and supply the voltage to drive the enable signal for the HVmux (3.3 V).

184 11.2 Control

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The powerboard controls the LDO enable of the HCCStars and the ABCStars. The ABC-185 Star LDO control is segmented in two segments per hybrid. Additionally the LV to the 186 hybrid can be switched off and the HV to the sensors as well. Four analogue signals gen-187 erated by DACs. Two are used to calibrate the analog sections of the ABCStars with 188 one calibration line per hybrid. The other two are used to control the shunt in the ABC-189 Star to artificially increase the current draw of the ABCStars for each hybrid individually. 190 Each powerboard has a digital output used to disable the linPOL12V of the neighbouring 191 powerboard to be able to switch off or restart individual powerboards completely. The 192 powerboard has for each HCCStar a dedicated reset line, to assert a HCCStar reset with-193 out cycling the LDO enable for the HCCStar. The communications block within AMAC 194 can be also reset using SSSH provided by one or both of the HCCStars connected to an AMAC. Two digital control from from the AMAC can change the output of the bPOL12V 196 to 1.3, 1.4, 1.5 and 1.6V. 197

198 11.3 Monitoring

The AMAC on the powerboard has several ADC inputs to monitor several parameters of the hybrids and the powerboard itself. The quantities measured are:

• Temperature of the powerboard in the shield box volume using one NTC (type $10 k\Omega$ e.g. 103 KT 1005 T - 1P)

- bPOL12V internal temperature
- the hybrid temperatures using NTCs on all hybrids (type $10k\Omega$ e.g. 103KT1005T-1P)
- die temperature of AMAC
- bPOL12V output voltage and current
- bPOL12V input voltage and current
- Ground rise on the hybrids
 - HV return current

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- External calibration line
- AMAC internal bandgap
- outputs of the DACs

213 11.4 Programming Model

See AMAC specification.

215 12 Radiation Tolerance and Other Special Requirements

- The powerboard needs to be functional in an electrical and structural sense up to 66 Mrad ionising dose and $1.6 \cdot 10^{15}$ 1 MeV neq fluence. ASICs have been proven to work within specification under this dose. Polyimide based flex circuit boards and passive components have been tested to be maintain structural integrity and electrical functionality for this dosage on a batch basis.
- Component will be used in 2 T B-Field, need to test prototypes in magnet fields for correct functionality.

13 Testing, Validation and Commissioning

Produced PCBs are electrically tested by the PCB vendor, only qualified PCBs will be loaded with components. Only tested AMAC, bPOL12V, and HVmux will used for loading. linPOL12V might be loaded untested due to the expected high yield and comparitivly high testing cost. The assembly vendor will be supplied with a testing and burn-in setup and perform all testing and the full burn-in. Only fully tested barrel powerboards will be

delivered to LBNL, where quality assurance can be performed on a random subset. Powerboards can then be shipped to the module production sites. The end-cap powerboards will be assembled in industry and either tested and burned-in in industry or at one end-cap module production site. A subset of end-cap powerboards will also be used for quality assurence tests at a module production site. A set of powerboards from each production batch shall be put into an accelerated life-time test, to ensure quality and find possible production faults.

236 13.1 Testing metrics

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The metrics to access the structural quality of the powerboard are the following:

- Visual inspection of bare PCB
- E-test bare PCB, including high voltage test of HV lines up to 1.5 kV (2 times nominal)
- Visual inspection of stuffed PCB
- Blind Via test coupon resistance measurement (After thermal stressing)
 - Wirebond pull test coupon
- The metrics to access the electrical quality of the powerboard are the following:
- DCDC conversion efficiency, see example in Figure 5, should not drop below 65% at 2.0 A.
 - Measure thermal contact to pad below DCDC converter
- Output voltage of bPOL12V should not be below 1.45 V and not above 1.55 V.
 - Output voltages of linPOL12V should not be below 1.35 V and not above 1.45 V (nominal 1.4 V), and not be below 3.2 V and not above 3.4 V (nominal 3.3 V)
- Radiated EMI should be below XX at YY distance from shield box.
- No performance degradation after 144 hours of burn-in at max. settings.
- Test digital outputs for correct voltage and response
 - Test ADC response for linearity, slope and offset
 - Test DAC response for linearity, slope and offset
- Cycle HVmux 100 times under max voltage/current.
- All metrics have to be satisfied in a temperature range from -40° C to $+40^{\circ}$ C of the cooling fixture the powerboard is mounted on during testing.

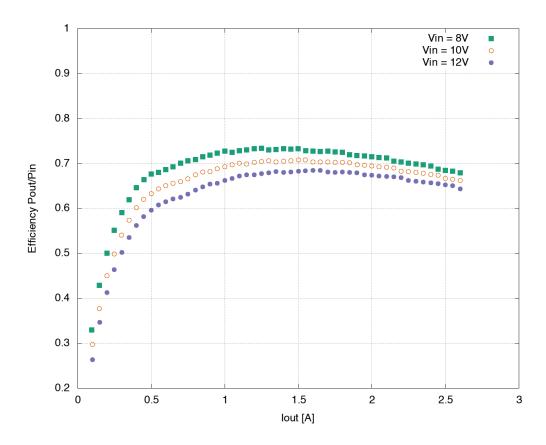


Figure 5: Example of the DCDC conversion efficiency.

59 14 Reliability Matters

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14.1 Consequences of Failure

²⁶¹ Two types of failures have to be considered.

Single module failure This type of failure only influences the capability to power, control, or monitor a single module. This failure can be produced by a multitude of modes:

- ASIC failure: Failure of the bPOL12V, HVmux, linPOL12V or AMAC would lead to single module failure.
- PCB failure: Traces of signals which are necessary for operation will be at least 120 μ m wide to avoid micro-cracks and multiple vias will be used for these type of signals.
- Wire bond failure: Multiple wire bonds will be used wherever possible, therefor single module failure should not occur because of that.

Multi module failure This type of failure impedes the ability to power, control or monitor a whole stave due to the failure of a single powerboard. As multiple modules share LV, HV, and communication a failure which influences this bus somehow might lead to a subsequent whole stave failure. For the LV and HV a low ohmic connection would prevent from powering or biasing the stave or HV group of four sensors, respectively. The communication bus is AC-coupled and a steady state failure of the AMAC output should not lead to any problems. If an AMAC is blocking the bus due to random switching activity, the HCCStar on the same module can mute it via the SSSH line or the entire single module can be disabled via OF.

281 14.2 Prior Knowledge of Expected Reliability

The active components on the powerboard (bPOL12V, Linear regulator, AMAC, and HV-mux) should be tested for reliability irrespectively of the powerboard. There is extensive experience on the useage of Polyimide based PCBs, passive components, and wire bonds in high energy physics experiments and their environments.

REFERENCES v1.2

14.3 Measures Proposed to Ensure Reliability of Component and/or System

Fully assembled powerboards shall be tested in custom reliability measurements, as well as going through highly accelerated lifetime and highly accelerated stress tests by external specialised vendors. Results from these reliability measurements shall be feed back into the powerboard design, production, and QC to if possible increase its reliability.

292 14.4 Quality Control to Validate Reliability Specifications during Production

Full power and control test, 6 days of burn-in at maximum settings.

Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

Additionally to the QC, a random sub sample from each production batch shall undergo a detailed set of tests at the institute supervising the production. These tests include accelerated lifetime and stress testing to monitor the production quality of each batch.

$_{\scriptscriptstyle{300}}$ 15 References

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