NUFRONT ®

NS115 Datasheet

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Revision History

Rev	Description of Changes	Date
V 1.0	Initial Release	2012.06.26

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Chapter 1 Introduction

The NS115 high-performance and low power multimedia application device is based on Cortex-A9 dual core processor, and manufacture at 40LP process, offered in a 481-ball, 19mm x 19mm, 0.8-mm ball pitch FCBGA package.

1.1 Features Overview

The architecture is designed to provide best-in-class video, image, and graphics processing for SmartPhone and Tablet.

- The device supports the following functions:
  - Supporting up to 1080p video decoder and 720p video encoder
  - High performance multi-core2D/3D graphic processor
  - Supporting true dual-view display

- The device supports high-level operating systems(OSs) such as:
  - Android, Ubuntu, Linux

- The device is composed of the following subsystem:
  - Cortex-A9 microprocessor unit(MPU) subsystem, including two ARM Cortex-A9 cores.
  - 2D/3D graphic accelerator subsystem
  - Display subsystem
  - Video subsystem
  - Camera subsystem
  - Memory subsystem

- The device also integrates:
  - On-chip memory
  - External memory interfaces
  - Memory management
  - High performance interconnects
  - System and connecting peripherals

1.2 Block diagram

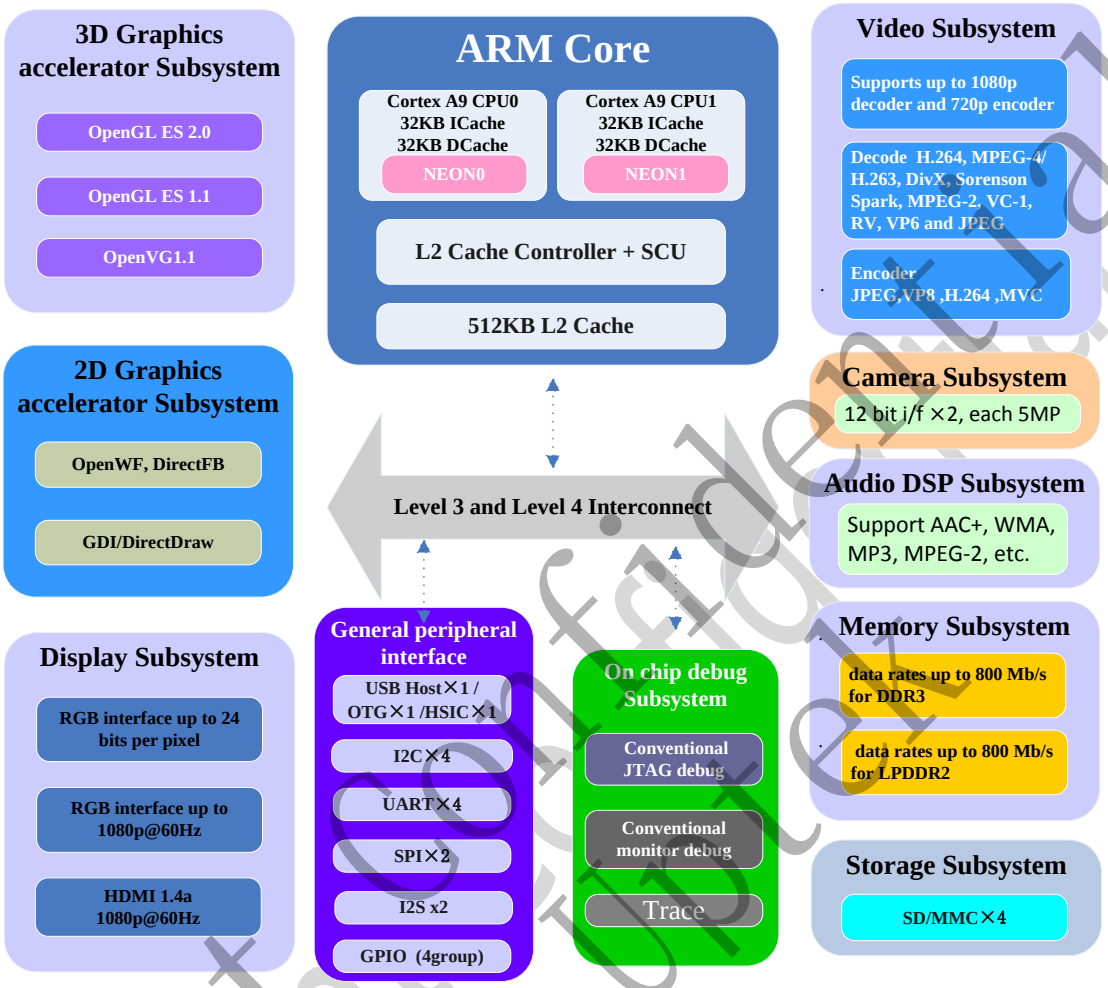

Figure 1 Block Diagram

1.3 Conventions and Notations

The following conventions are used throughout this manual.

Pin Names

Pins are identified by their pin names or ball references. All active-low signals are identified by the suffix '_N' in their names (e.g., DDR_CK2_N).

Pin Types

The pins are assigned different codes according to their operational characteristics. These codes are listed in the following table:

Table 1 Conventions and Notations

Code	Pin Type
I	Digital Input

O	Digital Output
I/O	Bi-Directional Digital Input or Output
A-I	Analog Input
A-O	Analog Output
A-I/O	Bi-Directional Analog Input or Output
GND	Digital Ground
AGND	Analog Ground
other	Pin types not included in any of the categories above

Chapter 2 Functional Description

2.1 Dual Cortex-A9 MPU Subsystem Description

The Cortex-A9 MPU subsystem integrates the following sub modules:

- ARM Cortex A9 MPCore
  - Two Cortex-A9 processor,CPU0 and CPU1.Each contains a private timer and watchdog unit
  - Each CPU has 32KB of L1 instruction cache, 32KB of L1 data cache
  - Two media processing engines,NEON0 and NEON1,that support NEON technology and floating-point operations
  - A Snoop Control Unit(SCU)
  - A global timer
  - An integrated interrupt controller that is an implementation of the generic interrupt controller architecture
  - Coresight Program Trace Microcells(PTMs) and a Cross Trigger Matrix(CTM)
- An integrated level 2 cache controller, with 512KB cache size
- A Coresight ATB Bridge
- A debug APB Bridge
- A peripheral clock divider that creates a fixed 2:1 clock ratio
- Coresight timestamp synchronizers

2.2 3D Graphics Accelerator Description

The pixel processor features are:

- each pixel processor used processes a different tile, enabling a faster turnaround
- programmable fragment shader
- alpha blending
- complete non-power-of-2 texture support
- cube mapping
- fast dynamic branchin
- fast trigonometric functions, including arctangent
- full floating-point arithmetic
- framebuffer blend with destination Alpha
- indexable texture samplers
- line, quad, triangle and point sprites
- no limit on program length
- perspective correct texturing
- point sampling, bilinear, and trilinear filtering
- programmable mipmap level-of-detail biasing and replacement

- stencil buffering, 8-bit
- two-sided stencil
- unlimited dependent texture reads
- 4-level hierarchical Z and stencil operations
- Up to 512 times Full Scene Anti-Aliasing (FSAA). 4x multisampling times 128x
- supersampling
- 4-bit per texel compressed texture format.

The geometry processor features are:

- programmable vertex shader
- flexible input and output formats
- autonomous operation tile list generation
- indexed and non-indexed geometry input
- primitive constructions with points, lines, triangles and quads.

The L2 cache controller features are:

- configurable sizes of 8KB, 16KB, 32KB, 64KB, 128KB and 256KB
- 4-way set-associative
- supports up to 32 outstanding AXI transactions
- implements a standard pseudo-LRU algorithm
- cache line and line fill burst size is 64 bytes
- supports eight to 64bytes uncached read bursts and write bursts
- 64-bit or 128-bit interface to memory sub-system
- support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.

The MMU features are:

- accesses control registers through the bus infrastructure to configure the memory system.
- each processor has its own MMU to control and translate memory accesses that the GPU initiates.

The PMU features are:

- programmable power management
- powers up and down each GP, PP and Level 2 cache controller separately
- controls the clock, isolation and power of each device
- provides an interrupt when all requested devices are powered up.

2.3 2D Graphics Accelerator Description

Hardware Acceleration for DirectFB

- High-speed video scaler
- ROP2/3/4 (render operation code)
- Rectangle filling / drawing
- Line drawing
- Simple blitting

- Stretch blitting
- Blending with alpha channel (per-pixel alpha)
- Blending with alpha factor (alpha modulation)
- Nine source and destination blending functions
- Porter-Duff rules support
- Premultiplied alpha support
- Colorized blitting (color modulation)
- Source color keying
- Destination color keying

API support
- OpenWF, DirectFB
- GDI/DirectDraw
- Flash

Featured 2D GPU
- BitBlt and StretchBlt
- DirectFB hardware acceleration
- ROP2, ROP3, ROP4 full alpha blending and transparency
- Clipping rectangle support
- Alpha blending includes Java 2 Porter-Duff compositing rules
- 90o, 180o, 270o rotation on every primitive
- YUV-to-RGB color space conversion
- Programmable display format conversion with 14 source and 7 destination formats
- High quality 9-tap, 32-phase filter for image and video scaling at 1080p
- Monochrome expansion for text rendering
- 32K x 32K coordinate system

2.4 Video Decoder Subsystem Description

The supported standards, profiles and levels are presented in Table as follows:

Table 2 Video Decoder supported standards, profiles and levels

Standard	Decoder support
H.264 profile and level	Baseline Profile, levels 1 - 4.2 Main Profile, levels 1 - 4.2 High Profile, levels 1 - 4.2 Image size up to 1080p at level 4.2
SVC profile and level	Scalable Baseline Profile, base layer only Scalable High Profile, base layer only
MVC profile and level	Stereo High
MPEG-4 visual profile and level	Simple Profile, levels 0 - 6 Advanced Simple Profile, levels 0 - 5

MPEG-2 profile and level	Main Profile, low, medium and high levels
MPEG-1 profile and level	Main Profile, low, medium and high levels
H.263 profile and level	Profile 0, levels 10-70. Image size up to 720x576
Sorenson Spark profile and level	Bitstream version 0 and 1
VC-1 profile and level	Simple Profile, low, medium and high levels Main Profile, low, medium and high levels Advanced Profile, levels 0-3
JPEG profile and level	Baseline interleaved
RV profile and level	RV8 RV9 RV10
VP6 profile and level	VP6.0 (Simple Profile) VP6.1 VP6.2 (Advanced Profile)
VP7 profile and level	VP7 versions 0-3
VP8 profile and level	VP8 version 2 (WebM)
WebP profile and level	WebP
AVS profile and level	P2 Jizhun Proflie, level 6.0 and 6.2
DivX ® profile and level	DivX Home Theater Profile Qualified TM DivX3 DivX4 DivX5 DivX6

Table 3 H.264 / MVC / SVC BASE LAYER FEATURES

Feature	Decoder support
Input data format	H.264 byte or NAL unit stream / SVC stream / MVC stream
Decoding scheme	Frame by frame (or field by field) Slice by slice
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled YCbCr 4:0:0 (monochrome)
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by H.264 HP level 4.2
Error detection and concealment	Supported

Table 4 MPEG-4 / H.263 / SORENSON SPARK FEATURES

Feature	Decoder support
Input data format	MPEG-4 / H.263 / Sorenson Spark elementary video stream

Decoding scheme	Frame by frame (or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088(MPEG-4, Sorenson Spark) 48 x 48 to 720 x 576 (H.263) Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by MPEG-4 ASP level 5
Error detection and concealment	Supported

Table 5 MPEG-2 / MPEG-1 FEATURES

Feature	Decoder support
Input data format	MPEG-2 / MPEG-1 elementary video stream
Decoding scheme	Frame by frame (or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by MPEG-2 MP high level
Error detection and concealment	Supported

Table 6 JPEG FEATURES

Feature	Decoder support
Input data format	JFIF file format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
Decoding scheme	Input: buffer by buffer, from 5kB to 8MB at a time Output: from 1 MB row to 16 Mpixels at a time
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar raster-scan
Supported image size	48 x 48 to 8176 x 8176 (66.8 Mpixels) Step size 8 pixels
Maximum data rate	Up to 76 million pixels per second
Thumbnail decoding	JPEG compressed thumbnails supported
Error detection	Supported

Table 7 VC-1 FEATURES

Feature	Decoder support
Input data format	VC-1 stream
Decoding scheme	Frame by frame (or field by field)

	Slice by slice
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by VC-1 AP level 3
Error detection and concealment	Supported

Table 8 RV FEATURES

Feature	Decoder support
Input data format	RV8, RV9 or RV10 stream
Decoding scheme	Frame by frame Slice by slice
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by RV specification
Error detection and concealment	Supported

Table 9 VP6 FEATURES

Feature	Decoder support
Input data format	VP6.0 / VP6.1 / VP6.2 stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by VP6 specification
Error detection and concealment	Supported

Table 10 VP7 FEATURES

Feature	Decoder support
Input data format	VP7 stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088

Maximum bit rate	As specified by VP7 specification
Error detection and concealment	Supported

Table 11 VP8, WEBP FEATURES

Feature	Decoder support
Input data format	VP8 tream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by VP8specification
Error detection and concealment	Supported

Table 12 AVS FEATURES

Feature	Decoder support
Input data format	AVS stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by AVS specification
Error detection and concealment	Supported

Table 13 DIVX FEATURES

Feature	Decoder support
Input data format	Divx3, 4, 5 or 6 stream
Decoding scheme	Frame by frame Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:0 semi-planar 8x4 tiled
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30fps at1920 x 1088
Maximum bit rate	As specified by the DivX specification
Error detection and concealment	Supported

2.5 Video Encoder Subsystem Description

The features of the encoder for each supported standard are shown in as follows:

Table 14 VP8/H.264/MVC FEATURES

Standard	Decoder support
Input data format	YCbCr formats: o YCbCr 4:2:0 planar o YCbCr 4:2:0 semi-planar o YCbYCr 4:2:2 raster-scan o CbYCrY 4:2:2 raster-scan RGB formats:1) o RGB444 and BGR444 o RGB555 and BGR555 o RGB565 and BGR565 o RGB888 and BRG888 o RGB101010 and BRG101010
Output data format	VP8: o VP8 bitstream H.264/MVC: o Byte unit stream o NAL unit stream
Supported image size	144 x 96 to 1280 x 720 Step size 4 pixels
Maximum frame rate	Unlimited by the hardware 30 fps at 1280 x 720
Bit rate	Minimum: 10kbps Maximum: 40 Mbps at 720p 30 fps
Motion detection	Encoder outputs a motion vector and motion estimation quality information (a SAD value) for each macroblock
Region-of-interest	Two user definable rectangular areas with separate quantizer setting
Region-of-intra	One user definable rectangular area coded as intra
Cyclic Intra Refresh	Supported

Table 15 JPEG FEATURES

Feature	Decoder support
Input data format	YCbCr formats: o YCbCr 4:2:0 planar o YCbCr 4:2:0 semi-planar o YCbYCr 4:2:2 raster-scan o CbYCrY 4:2:2 raster-scan

	RGB formats:1) o RGB444 and BGR444 o RGB555 and BGR555 o RGB565 and BGR565 o RGB888 and BRG888 o RGB101010 and BRG101010
Output data format	JFIF file format 1.02 Non-progressive JPEG
Supported image size	96 x 32 to 8192 x 8192 (64 million pixels) Step size 4 pixels
Maximum data rate	Up to 90 million pixels per second
Thumbnail insertion	RGB 8-bits, RGB 24-bits and JPEG compressed thumbnails supported

2.6 Camera Subsystem Description

- Maximum input resolution of 2600x2048 pixels (5 Mega Pixel)
- About 100 MHz system clock
- Up to 100 MHz sensor clock (parallel sensor)
- Generic Sensor Interface with programmable polarity for synchronization signals
- 2nd ITU-R BT 601/656 compliant video interface supporting YCbCr or raw data
- 12 bit camera interface
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start,v_start) interrupts
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Main- and Self scaler with pixel-accurate up- and down-scaling to any resolution between 2600x2048 (depending on SRAM Buffer Size) and 32x16 pixel in processing mode
- Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
- Rotation unit in self-picture path (90 °, 180 °, 270 °and h/v flipping) for RGB output
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Rotation in 90 °Steps for Display-Ready RGB Output
- Two Independent Data Paths to Memory for Self and Main Picture

2.7 Audio DSP Subsystem Description

Table 16 Audio DSP support format and sample rate

FORMAT	CHANNELS	SAMPLERATE(khz)	BITRATE
AAC+	2channels	up to 48	up to 320kbps

AAC-LC	1/2channels	up to 48	up to 320kbps
EAAC+	2 channels	up to 48	up to 320kbps
AMR-NB	1 channels	Up to 8	up to 12.2kbps
AMR_WB	1 channels	Up to 16	up to 23.8kbps
WMA	2 channels	up to 8	up to 384kbps
MP3	2channels	up to 48	up to 320kbps
MPEG-2	2channels	up to 48	up to 384kbps
Ogg Vorbis	2channels	up to 48	up to 256kbps

2.8 Display Subsystem Description

Input data formats:
- Support big-endian/ little-endian RGB8-8-8
- Support big-endian/ little-endian RGB5-5-5
- Support big-endian/ little-endian RGB5-6-5

Example of supported resolutions (and aspect ratios):
- QVGA –320 x 240 85Hz (4:3)
- VGA–640 x 480 85Hz (4:3)
- SVGA–800 x 600 85Hz (4:3)
- XGA–1024 x 768 85Hz (4:3)
- HD 720–1280 x 720 60Hz (16:9)
- SXGA–1280 x 1024 85Hz (5:4)
- UXGA–1600 x 1200 60Hz (4:3)
- WSXGA –1680 x 1050 60Hz (16:10)
- HD 1080–1920 x 1080 60Hz (16:9)
- WUXGA–1920 x 1200 60Hz (16:10)

Output parallel RGB interface:
- RGB8-8-8 (8:8:8)
- RGB6-6-6 (6:6:6)
- HSYNC and VSYNC signals or one composite synchronization signal
- Blanking (Data Enable) signal
- Pixel Clock
- Polarity of HSYNC, VSYNC, BLANK can be programmed

Progressive scanning mode support
Fully display timing parameters and aspect ratios
Dedicated unidirectional DMA controller with burst transaction support
Configurable and programmable internal FIFO (Depth/almost-full/almost-empty)
Internal, event stimulated, interrupt request generation with masking capability
Integrated test mode – generates color bar without any DMA-AXI bus transactions
Little-endian and Big-endian can be programmable

Integrated with AMBA bus:
AXI3.0-128-Master Port
AHB 32-bit Slave Interface
Support Atom-Operation (lock operation)
Support Outstanding (Issue read capability is configurable)
AFIFO: 512 x 192-bit (12KB)

- HDMI 1.4a and DVI 1.0 compliant transmitter
- Flexible video interface supports video decoder of HD set-top boxes, HD DVD and Blu-ray Disc players
  - 24-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2
  - 16/20/24-bit YCbCr 4:2:2 (ITU.601 and 656)
  - dual-edge clocking input modes
  - YCbCr-to-RGB color space conversion
  - xvYCC-to-RGB color space conversion
  - BTA-T1004 video input format
  - 4:2:2 to 4:4:4 up sampling
  - 4:4:4 to 4:2:2 down sampling
  - RGB-to-YCbCr color space conversion
  - RGB-to-xvYCC color space conversion
  - Clip full range video to limit range video (16-235)
- High-end digital audio interface for lossless multi-channel audio transmission (7.1-surround at 192 kHz sampling rate and 24-bit words), mandatory for HD DVD & Blu-ray Disc

  Note: the HDMI 1.4a Tx Advanced IP integrates the 4xI2S
  - Dolby® TrueHD and DTS-HD Master Audio™ high bit rate support up to 24Mb/s through 4xI2S inputs
  - DVD-Audio support through 4xI2S inputs
  - Support of audio up to 8 channels at 192kHz
  - Flexible, programmable I2S channel mapping
  - 2:1 and 4:1 Down-sampling to handle 96 kHz and 192 kHz audio streams
- Master I2C interface for DDC connection simplifies board layout and lowers cost
- HDMI compliant Consumer Electronics Control (CEC) support (configuration option)
- parallel data and address interface
- Monitor Detection supported through Hot Plug and Receiver Detection
- Programmable Data Enable Generator
- Programmable Sync Extraction
- Flexible power management

2.9 Memory Subsystem Description

Memory Controller Features:

- Fully pipelined command, read and write data interfaces to the memory controller.
- Advanced bank look-ahead features for high memory throughput.
- Front-end interface to 1 standard AXI port.
- A programmable register interface to control memory device parameters and protocols including auto pre-charge.
- Full initialization of memory on memory controller reset.
- Built-in Self Test (BIST) for external DRAM devices.
- Programmable memory data path size of full memory data width or half memory data width.
- Clock frequencies from 100 MHz to 400 MHz supported.
- Back-end interface to a DFI 2.1-Compliant PHY.

PHY Features

- Contains all data registers used to launch data, address and control signals to the
- DDR memory and the memory controller.
- Controls the off-chip data capture and synchronization logic for the read data.
- Includes a Digital DLL for timing.
- At-speed manufacturing testability circuitry for the data path elements which allows it to be easily self-checked at commercially available Automatic Test.
- Supported DDR3/3L, LPDDR2

2.10 Storage Subsystem Description

2.10.1 SD/MMC

- Compatibility
  - SD Host Specification version 3.00
  - SD Memory (SDSC, SDHC and SDXC) version 3.00 (and lower)
  - SDIO version 3.00 (and lower)
  - MMC/eMMC Card version 4.4
  - SD1/SD4/MMC-8 modes of operation
  - Suspend/Resume mechanism for SDIO cards
  - Read Wait mechanism for SDIO cards
  - Sample Clock Tuning mechanism
  - Signaling voltage level support
- Multislot operation
  - There are 4 slots
  - Independent clock/configuration for each slot

  - Independent register set for each slot
  - Datapath (including DMA and FIFO) shared among all slots to reduce the silicon area
- Standard Register Set
  - Compatible with SD Host Specification version 3.00
  - Independent Interrupt and Wakeup outputs
- Integrated DMA (SDMA/ADMA) controllers
  - SDMA Controller is compatible with SDIO Host Specification version 1.00
  - ADMA Controller is compatible with SDIO Host Specification version 2.00
  - Burst length 2 for DMA transfers
- Data buffering
  - 1024x32-bit FIFO buffers
  - Dual-Buffer mode for optimized throughput
  - Dual-Port RAM support
- Low power features
  - Master SD card side clock can be switched off
  - Each card clock can be switched off independently

2.11 General Peripheral Interface Description

2.11.1 USB

- Design methodology supports full scan for testability
- All clock synchronization is handled within the controller
- No bidirectional or three-state buses
- No level-sensitive latches
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- AHB interface to the application Complies with the AMBA Specification, Revision 2.0
- Bus Interface Unit (BIU) handles retry, error and split transactions on the AHB
- EHCI controller, as an AHB Master, 32-bit addressing; OHCI controller, as an AHB Master, supports 32-bit addressing
- EHCI and OHCI controllers, as AHB Masters, support 8- or 32-bit data transfers
- Complies with the USB 2.0 Specification
- Supports ping and split transactions
- UTMI+ HSIC interface to the PHY
- UTMI/UTMI+ PHY interface clock supports 60-MHz operation for an 8-bit interface
- Heterogeneous selection of UTMI+, or HSIC interfaces per port using strap pins. In Heterogeneous mode, only the 8-bit interface (60 MHz) is supported.

2.11.2 I2C

- Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds:
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
  - High-speed mode (3.4 Mb/s)
- Clock synchronization
- Master I2C operation
- 7bit addressing
- 7bit combined format transfers
- Bulk transmit mode
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handles Bit and Byte waiting at all bus speeds
- Simple software interface consistent with DesignWare APB peripherals
- Component parameters for configurable software driver support
- DMA handshaking interface compatible with the DW_ahb_dmac handshaking interface

2.11.3 I2S

- The I2S-APB Bus Controller provides a three wire serial interface
- receiver/transmitter modes are supported
- external or internal transmit/receive
- integrated APB slave wrapper to interface with the host APB controller
- several I2S modes implemented - the transmission unit and receive unit may separately operate in one of the Left Justified, Right Justified, I2S – Philips, DSP compatible modes
- I2S bus interface modes activated separately for transmission and reception unit
- master DMA handshake interfacing
- two configurable internal FIFOs - one for data to be transmitted and one for received data
- Special Function Register block common for all channels
- internal event stimulated interrupt request generation with masking capability
- 8 stereo I2S I/O channels
- two sets of SCK and WS I/Os - one common for all transmitters and one common for all receivers

2.11.4 UART

- AMBA APB interface allows easy integration into AMBA SoC implementations
- Configurable parameters for the following:
  - APB data bus widths of 32
  - Additional DMA interface signals for compatibility with DesignWare DMA interface
  - DMA interface signal polarity
  - Transmit and receive FIFO depths of 16, 64
  - Internal FIFO (RAM) selection
  - Use of two clocks (pclk and sclk) instead of one (pclk)
  - IrDA 1.0 SIR mode support with up to 115.2 Kbaud data rate and a pulse duration (width) as follows: width = 3/16 ×bit period as specified in the IrDA physical layer specification
  - Clock gate enable output(s) used to indicate that the TX and RX pipeline is clear (no data) and no activity has occurred for more than one character time, so clocks may be gated
  - Auto Flow Control mode as specified in the 16750 standard
  - Loopback mode that enables greater testing of Modem Control and Auto Flow Control features (Loopback support in IrDA SIR mode is available)
  - Transmitter Holding Register Empty (THRE) interrupt mode
- Functionality based on the 16550 industry standard, as follows:
  - Programmable character properties, such as number of data bits per character (5-8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)
  - Line break generation and detection
  - Prioritized interrupt identification
- Programmable FIFO enable/disable
- Programmable serial data baud rate as calculated by the following: baud rate = (serial clock frequency)/(16 × divisor)
- Modem and status lines are independently controlled
- Complete RTL version
- Separate system resets for each clock domain to prevent metastability

2.11.5 SPI

- APB interface
- Serial-master or serial-slave operation – Enables serial communication with serial-master or serial-slave peripheral devices.
- DMA Controller Interface – Enables the DW_apb_ssi to interface to a DMA controller over the bus using a handshaking interface for transfer requests.
- Independent masking of interrupts – Master collision, transmit FIFO overflow,

transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.

- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Bypass of meta-stability flip-flops for synchronous clocks – When the APB clock (pclk) and the DW_apb_ssi serial clock (ssi_clk) are synchronous, meta-stable flip-flops are not used when transferring control signals across these clock domains.
- Programmable features:
  - Serial interface operation – default work as motorola SPI, can be programmed as TI SSP or NatSemi MicroWire
  - Clock bit-rate – Dynamic control of the serial bit rate of the data transfer; used in only serial-master mode of operation.
  - Data Item size (4 to 16 bits) – Item size of each data transfer under the control of the programmer.
- Configurable features:
  - FIFO depth – depth of the transmit and receive FIFO buffers is 20. The FIFO width is fixed at 16 bits.
  - Number of slave select outputs – When operating as a serial master, 1 serial slave-select output signals.
  - Software slave-select – software control can be used to target the serial-slave device.
  - Combined interrupt lines – one combined interrupt line from the DW_apb_ssi to the interrupt controller.
  - Interrupt polarity – high active.

2.11.6 General-Purpose I/O

- core gpio support 128 and wakeup gpio support 8 independently configurable signals
- core gpio support four ports, A to D, and wakeup gpio support one port, which are separately configurable
- Separate data registers and data direction registers for each signal
- Configurable hardware and software control for each signal, or for each bit of each signal
- Separate auxiliary data input, data output, and data control for each I/O in Hardware Control mode
- Independently controllable signal bits
- Configurable interrupt mode for Port A
- debounce logic with an external slow clock to debounce interrupts
- multiple interrupts
- GPIO Component Type register
- GPIO Component Version register

- Configurable reset values on output signals
- include synchronization of interrupt signals

2.12 On-Chip Debug Subsystem Description

CoreSight™, the ARM debug and trace technology, is the most complete on-chip debug and real-time trace solution for the entire System-On-Chip (SoC), making ARM processor-based SoCs the easiest to debug and optimize.

CoreSight systems provide all the infrastructure you require to debug, monitor, and optimize the performance of a complete System on Chip (SoC) design.

There are historically three main ways of debugging an ARM processor based SoC:

- Conventional JTAG debug. This is invasive debug with the core halted using:
  - Breakpoints and watch points to halt the core on specific activity
  - A debug connection to examine and modify registers and memory and provide single-step execution.
- Conventional monitor debug. This is invasive debug with the core running using a debug monitor that resides in memory.
- Trace. This is non-invasive debug with the core running at full speed using:
  - Collection of information on instruction execution and data transfers
  - Delivery off-chip in real-time
  - Tools to merge data with source code on a development workstation for later analysis.

The CoreSight Design Kit addresses the requirement for a multi-core debug and trace solution with high bandwidth for whole systems beyond the core, including trace and monitor of the system bus.

The CoreSight Design Kit provides:

- Debug and trace visibility of whole systems
- Cross triggering support between SoC subsystems
- Higher data compression than previous solutions
- Multi-source trace in a single stream
- Standard Programmer's Models for standard tool support
- Open interfaces for third party cores
- Low pin count
- Low silicon overhead.

Chapter 3 Signal Descriptions

3.1Pin Mux Descriptions

Table 17 Pin Mux Descriptions

Ball Num	Pin name	Alternate functions									Resistor type	IO Ring	Voltage
		Function0(default)			Function1			Function2					
		Signal name	I/O	Functional description	Signal name	I/O	Functional description	Signal name	I/O	Functional description			
DDR													
G2	ddr_ba0	ddr_ba[0]	O	ddr bank address	-	-	-	-	-	-	-		1.5/1.2v
G1	ddr_ba1	ddr_ba[1]	O	ddr bank address	-	-	-	-	-	-	-		1.5/1.2v
H5	ddr_ba2	ddr_ba[2]	O	ddr bank address	-	-	-	-	-	-	-		1.5/1.2v
M4	ddr_ca0	ddr_ca[0]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
L3	ddr_ca1	ddr_ca[1]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
J3	ddr_ca10	ddr_ca[10]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
J1	ddr_ca11	ddr_ca[11]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
J2	ddr_ca12	ddr_ca[12]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
J4	ddr_ca13	ddr_ca[13]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
H4	ddr_ca14	ddr_ca[14]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
H3	ddr_ca15	ddr_ca[15]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v

M2	ddr_ca2	ddr_ca[2]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
M1	ddr_ca3	ddr_ca[3]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
L4	ddr_ca4	ddr_ca[4]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
K5	ddr_ca5	ddr_ca[5]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
K2	ddr_ca6	ddr_ca[6]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
L5	ddr_ca7	ddr_ca[7]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
K1	ddr_ca8	ddr_ca[8]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
J5	ddr_ca9	ddr_ca[9]	O	ddr address	-	-	-	-	-	-	-		1.5/1.2v
P3	ddr_cas_n	ddr_cas_n	O	ddr column address strobe signal, active low	-	-	-	-	-	-	-		1.5/1.2v
N1	ddr_ck_c	ddr_cas_n	O	ddr nagative clock	-	-	-	-	-	-	-		1.5/1.2v
N2	ddr_ck_t	ddr_ck	O	ddr positive clock	-	-	-	-	-	-	-		1.5/1.2v
R1	ddr_cke	ddr_cke	O	clock enable, high active	-	-	-	-	-	-	-		1.5/1.2v
T1	ddr_cs0_n	ddr_cs_n[0]	O	chip select, low active	-	-	-	-	-	-	-		1.5/1.2v
M3	ddr_cs1_n	ddr_cs_n[1]	O	chip select, low active	-	-	-	-	-	-	-		1.5/1.2v
AA3	ddr_dm0	ddr_dm[0]	I/O	ddr data mask, high active	-	-	-	-	-	-	-		1.5/1.2v
U3	ddr_dm1	ddr_dm[1]	I/O	ddr data mask, high active	-	-	-	-	-	-	-		1.5/1.2v
E4	ddr_dm2	ddr_dm[2]	I/O	ddr data mask, high active	-	-	-	-	-	-	-		1.5/1.2v
A5	ddr_dm3	ddr_dm[3]	I/O	ddr data mask, high active	-	-	-	-	-	-	-		1.5/1.2v
AB5	ddr_dq0	ddr_dq[0]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
AA4	ddr_dq1	ddr_dq[1]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
V4	ddr_dq10	ddr_dq[10]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
V5	ddr_dq11	ddr_dq[11]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
U5	ddr_dq12	ddr_dq[12]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
U4	ddr_dq13	ddr_dq[13]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v

T5	ddr_dq14	ddr_dq[14]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
R5	ddr_dq15	ddr_dq[15]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
G5	ddr_dq16	ddr_dq[16]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
F3	ddr_dq17	ddr_dq[17]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
F1	ddr_dq18	ddr_dq[18]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
F2	ddr_dq19	ddr_dq[19]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
AA5	ddr_dq2	ddr_dq[2]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
F4	ddr_dq20	ddr_dq[20]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
E3	ddr_dq21	ddr_dq[21]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
F5	ddr_dq22	ddr_dq[22]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
E5	ddr_dq23	ddr_dq[23]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
D5	ddr_dq24	ddr_dq[24]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
C5	ddr_dq25	ddr_dq[25]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
C1	ddr_dq26	ddr_dq[26]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
C2	ddr_dq27	ddr_dq[27]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
C4	ddr_dq28	ddr_dq[28]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
B5	ddr_dq29	ddr_dq[29]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
Y4	ddr_dq3	ddr_dq[3]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
C3	ddr_dq30	ddr_dq[30]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
B3	ddr_dq31	ddr_dq[31]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
Y5	ddr_dq4	ddr_dq[4]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
W5	ddr_dq5	ddr_dq[5]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
Y3	ddr_dq6	ddr_dq[6]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
W2	ddr_dq7	ddr_dq[7]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
V2	ddr_dq8	ddr_dq[8]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v

V3	ddr_dq9	ddr_dq[9]	I/O	ddr data	-	-	-	-	-	-	-		1.5/1.2v
AA1	ddr_ds0n	ddr_dqs_m[0]	I/O	ddr negative data strobe	-	-	-	-	-	-	-		1.5/1.2v
AA2	ddr_ds0p	ddr_dqs_p[0]	I/O	ddr positive data strobe	-	-	-	-	-	-	-		1.5/1.2v
W1	ddr_ds1n	ddr_dqs_m[1]	I/O	ddr negative data strobe	-	-	-	-	-	-	-		1.5/1.2v
V1	ddr_ds1p	ddr_dqs_p[1]	I/O	ddr positive data strobe	-	-	-	-	-	-	-		1.5/1.2v
D2	ddr_ds2n	ddr_dqs_m[2]	I/O	ddr negative data strobe	-	-	-	-	-	-	-		1.5/1.2v
D1	ddr_ds2p	ddr_dqs_p[2]	I/O	ddr positive data strobe	-	-	-	-	-	-	-		1.5/1.2v
A4	ddr_ds3n	ddr_dqs_m[3]	I/O	ddr negative data strobe	-	-	-	-	-	-	-		1.5/1.2v
B4	ddr_ds3p	ddr_dqs_p[3]	I/O	ddr positive data strobe	-	-	-	-	-	-	-		1.5/1.2v
P5	ddr_odt0	ddr_odt[0]	O	ODT control signal	-	-	-	-	-	-	-		1.5/1.2v
R2	ddr_odt1	ddr_odt[1]	O	ODT control signal	-	-	-	-	-	-	-		1.5/1.2v
P4	ddr_ras_n	ddr_ras_n	O	row address strobe, active low	-	-	-	-	-	-	-		1.5/1.2v
R3	ddr_retention	ddr_retention	I	data retention enable in S3 state, active high	-	-	-	-	-	-	-		1.5/1.2v
R4	ddr_rst_n	ddr_reset_n	O	reset signal, active low	-	-	-	-	-	-	-		1.5/1.2v
T2	ddr_we_n	ddr_we_n	O	write enable signal, active low	-	-	-	-	-	-	-		1.5/1.2v
N3	ddr_zq	ddr_zq	-	controller calibration pin, connect to 60ohm resistor	-	-	-	-	-	-	-		-
LCD													
H23	lcd_data0	disp0_data[0]	o	Parallel blue data signal 0	debug_signal[0]	o	debug signal	trace_data[0]	o	trace data	-	1	1.8/3.3V
H22	lcd_data1	disp0_data[1]	o	Parallel blue data signal 1	debug_signal[1]	o	debug signal	trace_data[1]	o	trace data	-	1	1.8/3.3V
H21	lcd_data2	disp0_data[2]	o	Parallel blue data signal 2	debug_signal[2]	o	debug signal	trace_data[2]	o	trace data	-	1	1.8/3.3V
H20	lcd_data3	disp0_data[3]	o	Parallel blue data signal 3	debug_signal[3]	o	debug signal	trace_data[3]	o	trace data	-	1	1.8/3.3V
H19	lcd_data4	disp0_data[4]	o	Parallel blue data signal 4	debug_signal[4]	o	debug signal	trace_data[4]	o	trace data	-	1	1.8/3.3V
J21	lcd_data5	disp0_data[5]	o	Parallel blue data signal 5	debug_signal[5]	o	debug signal	trace_data[5]	o	trace data	-	1	1.8/3.3V

J20	lcd_data6	disp0_data[6]	o	Parallel blue data signal 6	debug_signal[6]	o	debug signal	trace_data[6]	o	trace data	-	1	1.8/3.3V
J19	lcd_data7	disp0_data[7]	o	Parallel blue data signal 7	debug_signal[7]	o	debug signal	trace_data[7]	o	trace data	-	1	1.8/3.3V
K23	lcd_data8	disp0_data[8]	o	Parallel green data signal 0	debug_signal[8]	o	debug signal	trace_data[8]	o	trace data	-	1	1.8/3.3V
K22	lcd_data9	disp0_data[9]	o	Parallel green data signal 1	debug_signal[9]	o	debug signal	trace_data[9]	o	trace data	-	1	1.8/3.3V
K21	lcd_data10	disp0_data[10]	o	Parallel green data signal 2	debug_signal[10]	o	debug signal	trace_data[10]	o	trace data	-	1	1.8/3.3V
K20	lcd_data11	disp0_data[11]	o	Parallel green data signal 3	debug_signal[11]	o	debug signal	trace_data[11]	o	trace data	-	1	1.8/3.3V
K19	lcd_data12	disp0_data[12]	o	Parallel green data signal 4	debug_signal[12]	o	debug signal	trace_data[12]	o	trace data	-	1	1.8/3.3V
L23	lcd_data13	disp0_data[13]	o	Parallel green data signal 5	debug_signal[13]	o	debug signal	trace_data[13]	o	trace data	-	1	1.8/3.3V
L22	lcd_data14	disp0_data[14]	o	Parallel green data signal 6	debug_signal[14]	o	debug signal	trace_data[14]	o	trace data	-	1	1.8/3.3V
L21	lcd_data15	disp0_data[15]	o	Parallel green data signal 7	debug_signal[15]	o	debug signal	trace_data[15]	o	trace data	-	1	1.8/3.3V
L20	lcd_data16	disp0_data[16]	o	Parallel red data signal 0	debug_signal[16]	o	debug signal	-	-	-	-	1	1.8/3.3V
L19	lcd_data17	disp0_data[17]	o	Parallel red data signal 1	debug_signal[17]	o	debug signal	-	-	-	-	1	1.8/3.3V
M23	lcd_data18	disp0_data[18]	o	Parallel red data signal 2	debug_signal[18]	o	debug signal	-	-	-	-	1	1.8/3.3V
M22	lcd_data19	disp0_data[19]	o	Parallel red data signal 3	debug_signal[19]	o	debug signal	-	-	-	-	1	1.8/3.3V
M21	lcd_data20	disp0_data[20]	o	Parallel red data signal 4	debug_signal[20]	o	debug signal	-	-	-	-	1	1.8/3.3V
N23	lcd_data21	disp0_data[21]	o	Parallel red data signal 5	debug_signal[21]	o	debug signal	-	-	-	-	1	1.8/3.3V
N22	lcd_data22	disp0_data[22]	o	Parallel red data signal 6	debug_signal[22]	o	debug signal	-	-	-	-	1	1.8/3.3V
N21	lcd_data23	disp0_data[23]	o	Parallel red data signal 7	debug_signal[23]	o	debug signal	-	-	-	-	1	1.8/3.3V
G20	lcd_de	disp0_de	o	Parallel RGB data enable signal	-	-	-	-	-	-	-	1	1.8/3.3V
G21	lcd_hsync	disp0_hsync	o	Parallel RGB horizontal sync signals	-	-	-	-	-	-	-	1	1.8/3.3V
G23	lcd_pclk	disp0_pclk	o	Parallel RGB pixel clock	-	-	-	trace_clk	o	trace clock	-	1	1.8/3.3V
G19	lcd_sync	disp0_sync	o	Parallel RGB composite sync signal	gpio_ext_portc[30]	io	gpio	trace_ctrl	o	trace control signal	-	1	1.8/3.3V
G22	lcd_vsync	disp0_vsync	o	Parallel RGB vertical sync signals	-	-	-	-	-	-	-	1	1.8/3.3V
HDMI													
AA11	hdmi_cec	io_cec_a_i	I/O	HDMI CEC signal	-	-	-	-	-	-	-		1.8V

AC15	hdmi_clock_p	hdmi_clockx	I/O	HDMI analog phy output differential clock	-	-	-	-	-	-	-		-
AB15	hdmi_clock_n	hdmi_clocky	I/O	HDMI analog phy output differential clock	-	-	-	-	-	-	-		-
AB14	hdmi_data0_p	hdmi_data0x	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AC14	hdmi_data0_n	hdmi_data0y	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AB12	hdmi_data1_p	hdmi_data1x	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AC12	hdmi_data1_n	hdmi_data1y	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AB11	hdmi_data2_p	hdmi_data2x	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AC11	hdmi_data2_n	hdmi_data2y	I/O	HDMI analog phy output differential data	-	-	-	-	-	-	-		-
AA13	hdmi_ddc_scl	io_dscl_i	I/O	DDC clock signal	-	-	-	-	-	-	PU w/o en		1.8V
AA12	hdmi_ddc_sda	io_dsda_i	I/O	DDC data signal	-	-	-	-	-	-	PU w/o en		1.8V
W13	hdmi_ext_swing	hdmi_ext_swing	I/O	HDMI analog pht reference resistor	-	-	-	-	-	-	-		-
Y13	hdmi_hpd	io_hpd	i	HDMI hot plug detect signal	-	-	-	-	-	-	-		1.8V
USB													
AB19	usb0_padm	Usb_host_padm	I/O	USB host data pin Data-	-	-	-	-	-	-	-		3.3v
AC19	usb0_padp	Usb_host_padp	I/O	USB host data pin Data+	-	-	-	-	-	-	-		3.3v
AB18	usb0_vbus	Usb_host_vbus	O	Connect to the VBUS pin on the connector	-	-	-	-	-	-	-		5v

Y14	usb0_vres	Usb_host_vres	I/O	Connect to an external 8.2K(±1%) Ohm resistor for band-gap reference circuit	-	-	-	-	-	-	-		3.3v
AB17	usb1_padm	Usb_otg_padp	I/O	USB device data pin Data-	-	-	-	-	-	-	-		3.3v
AC17	usb1_padp	Usb_otg_padm	I/O	USB device data pin Data+	-	-	-	-	-	-	-		3.3v
AB16	usb1_vbus	Usb_otg_vbus	I/O	Connect to the VBUS pin on the connector	-	-	-	-	-	-	-		5v
AA14	usb1_vres	Usb_otg_vres	I/O	Connect to an external 8.2K(±1%) Ohm resistor for band-gap reference circuit	-	-	-	-	-	-	-		3.3v
AA16	hsic_data	hsic_data	I/O	This bidirectional pin carries HSIC USB data to and from the HSIC PHY.	-	-	-	-	-	-	-		1.2v
Y16	hsic_strobe	hsic_strobe	I/O	This bidirectional pin carries the HSIC USB strobe signal to and from the HSIC PHY	-	-	-	-	-	-	-		1.2v
Camera													
AC21	cam_data0	cameric0_data[0]	i	camera0 data input	cameric1_data[0]	i	camera1 data input	gpio_ext_portd[2]	io	gpio	PD w/ en	6	1.8/3.3V
AB21	cam_data1	cameric0_data[1]	i	camera0 data input	cameric1_data[1]	i	camera1 data input	gpio_ext_portd[3]	io	gpio	PD w/ en	6	1.8/3.3V
Y17	cam_data2	cameric0_data[2]	i	camera0 data input	cameric1_data[2]	i	camera1 data input	gpio_ext_portd[4]	io	gpio	PD w/ en	6	1.8/3.3V
Y19	cam_data3	cameric0_data[3]	i	camera0 data input	cameric1_data[3]	i	camera1 data input	gpio_ext_portd[5]	io	gpio	PD w/ en	6	1.8/3.3V
Y20	cam_data4	cameric0_data[4]	i	camera0 data input	cameric1_data[4]	i	camera1 data input	gpio_ext_portd[6]	io	gpio	PD w/ en	6	1.8/3.3V
AA20	cam_data5	cameric0_data[5]	i	camera0 data input	cameric1_data[5]	i	camera1 data input	gpio_ext_portd[7]	io	gpio	PD w/ en	6	1.8/3.3V
AA21	cam_data6	cameric0_data[6]	i	camera0 data input	cameric1_data[6]	i	camera1 data input	gpio_ext_portd[8]	io	gpio	PD w/ en	6	1.8/3.3V
W16	cam_data7	cameric0_data[7]	i	camera0 data input	cameric1_data[7]	i	camera1 data input	gpio_ext_portd[9]	io	gpio	PD w/ en	6	1.8/3.3V
W17	cam_data8	cameric0_data[8]	i	camera0 data input	cameric1_data[8]	i	camera1 data input	gpio_ext_portd[10]	io	gpio	PD w/ en	6	1.8/3.3V

W19	cam_data9	cameric0_data[9]	i	camera0 data input	cameric1_data[9]	i	camera1 data input	gpio_ext_portd[11]	io	gpio	PD w/ en	6	1.8/3.3V
Y21	cam_data10	cameric0_data[10]	i	camera0 data input	cameric1_data[10]	i	camera1 data input	gpio_ext_portd[12]	io	gpio	PD w/ en	6	1.8/3.3V
AA23	cam_data11	cameric0_data[11]	i	camera0 data input	cameric1_data[11]	i	camera1 data input	gpio_ext_portd[13]	io	gpio	PD w/ en	6	1.8/3.3V
AA19	cam_hsync	cameric0_hsync	i	camera0 hsync input	cameric1_hsync	i	camera1 hsync input	gpio_ext_portd[1]	io	gpio	PD w/ en	6	1.8/3.3V
AA17	cam_pclk	cameric0_pclk	i	camera0 clock input	cameric1_pclk	i	camera1 clock input	gpio_ext_portc[31]	io	gpio	PD w/ en	6	1.8/3.3V
AA18	cam_vsync	cameric0_vsync	i	camera0 vsync input	cameric1_vsync	i	camera1 vsync input	gpio_ext_portd[0]	io	gpio	PD w/ en	6	1.8/3.3V
W20	alt_clk0	alt_clk[0]	o	Alternative output clock0, for system usage.	-	-	-	-	-	-	-		1.8V
W21	alt_clk1	alt_clk[1]	o	Alternative output clock1, for system usage.	-	-	-	-	-	-	-		1.8V
MMC													
R21	mmc0_cd_n	sdcd_s0_n	i	SDMMC slot0 card detect siganl	gpio_ext_portc[23]	io	gpio	-	-	-	PU w/o en		1.8V
N20	mmc0_clk	sdclk_s0	o	SDMMC slot0 interface clock	gpio_ext_portc[29]	io	gpio	-	-	-	-	2	1.8/3.3V
P20	mmc0_cmd	cmd_s0_i	io	SDMMC slot0 command signal	gpio_ext_portc[28]	io	gpio	-	-	-	-	2	1.8/3.3V
P21	mmc0_dat0	dat_s0_i[0]	io	SDMMC slot0 data signal	gpio_ext_portc[24]	io	gpio	-	-	-	-	2	1.8/3.3V
P22	mmc0_dat1	dat_s0_i[1]	io	SDMMC slot0 data signal	gpio_ext_portc[25]	io	gpio	-	-	-	-	2	1.8/3.3V
N19	mmc0_dat2	dat_s0_i[2]	io	SDMMC slot0 data signal	gpio_ext_portc[26]	io	gpio	-	-	-	-	2	1.8/3.3V
P19	mmc0_dat3	dat_s0_i[3]	io	SDMMC slot0 data signal	gpio_ext_portc[27]	io	gpio	-	-	-	-	2	1.8/3.3V
R20	mmc0_psw	bus_lvs0	o	SDMMC slot0 IO power 3.3v/1.8v switch control signal	gpio_ext_portc[21]	io	gpio	-	-	-	-		1.8V
P23	mmc0_wp	sdwp_s0_n	i	SDMMC slot0 write protection signal	gpio_ext_portc[22]	io	gpio	-	-	-	-		1.8V
T23	mmc1_clk	sdclk_s1	o	SDMMC slot1 interface clock	gpio_ext_portc[20]	io	gpio	-	-	-	-		1.8V
U23	mmc1_cmd	cmd_s1_i	io	SDMMC slot1 command signal	gpio_ext_portc[19]	io	gpio	-	-	-	-		1.8V
T20	mmc1_dat0	dat_s1_i[0]	io	SDMMC slot1 data signal	gpio_ext_portc[11]	io	gpio	-	-	-	-		1.8V
U21	mmc1_dat1	dat_s1_i[1]	io	SDMMC slot1 data signal	gpio_ext_portc[12]	io	gpio	-	-	-	-		1.8V

V22	mmc1_dat2	dat_s1_i[2]	io	SDMMC slot1 data signal	gpio_ext_portc[13]	io	gpio	-	-	-	-		1.8V
W23	mmc1_dat3	dat_s1_i[3]	io	SDMMC slot1 data signal	gpio_ext_portc[14]	io	gpio	-	-	-	-		1.8V
T22	mmc1_dat4	dat_s1_i[4]	io	SDMMC slot1 data signal	gpio_ext_portc[15]	io	gpio	-	-	-	-		1.8V
T21	mmc1_dat5	dat_s1_i[5]	io	SDMMC slot1 data signal	gpio_ext_portc[16]	io	gpio	-	-	-	-		1.8V
U22	mmc1_dat6	dat_s1_i[6]	io	SDMMC slot1 data signal	gpio_ext_portc[17]	io	gpio	-	-	-	-		1.8V
V23	mmc1_dat7	dat_s1_i[7]	io	SDMMC slot1 data signal	gpio_ext_portc[18]	io	gpio	-	-	-	-		1.8V
Y23	mmc2_clk	sdclk_s2	o	SDMMC slot2 interface clock	gpio_ext_portc[10]	io	gpio	-	-	-	-		1.8V
Y22	mmc2_cmd	cmd_s2_i	io	SDMMC slot2 command signal	gpio_ext_portc[9]	io	gpio	-	-	-	-		1.8V
U19	mmc2_dat0	dat_s2_i[0]	io	SDMMC slot2 data signal	gpio_ext_portc[5]	io	gpio	-	-	-	-		1.8V
U20	mmc2_dat1	dat_s2_i[1]	io	SDMMC slot2 data signal	gpio_ext_portc[6]	io	gpio	-	-	-	-		1.8V
V21	mmc2_dat2	dat_s2_i[2]	io	SDMMC slot2 data signal	gpio_ext_portc[7]	io	gpio	-	-	-	-		1.8V
W22	mmc2_dat3	dat_s2_i[3]	io	SDMMC slot2 data signal	gpio_ext_portc[8]	io	gpio	-	-	-	-		1.8V
I2C													
E16	scl0	i_i2c_0_ic_clk_in_a	io	I2C0 interface clock	gpio_ext_portc[4]	io	gpio	-	-	-	PU w/o en		1.8V
C16	scl1	i_i2c_1_ic_clk_in_a	io	I2C1 interface clock	gpio_ext_portc[2]	io	gpio	-	-	-	PU w/o en		1.8V
A7	scl2	i_i2c_2_ic_clk_in_a	io	I2C2 interface clock	gpio_ext_portc[0]	io	gpio	-	-	-	PU w/o en	3	1.8/3.3V
B9	scl3	i_i2c_3_ic_clk_in_a	io	I2C3 interface clock	gpio_ext_portb[30]	io	gpio	-	-	-	PU w/o en	3	1.8/3.3V
D16	sda0	i_i2c_0_ic_data_in_a	io	I2C0 interface data	gpio_ext_portc[3]	io	gpio	-	-	-	PU w/o en		1.8V
B16	sda1	i_i2c_1_ic_data_in_a	io	I2C1 interface data	gpio_ext_portc[1]	io	gpio	-	-	-	PU w/o en		1.8V
A6	sda2	i_i2c_2_ic_data_in_a	io	I2C2 interface data	gpio_ext_portb[31]	io	gpio	-	-	-	PU w/o en	3	1.8/3.3V
A9	sda3	i_i2c_3_ic_data_in_a	io	I2C3 interface data	gpio_ext_portb[29]	io	gpio	-	-	-	PU w/o en	3	1.8/3.3V
I2S													
C15	i2s0_sck0	i2s_0_rsck_i	io	I2s0 bit clock for rx.	gpio_ext_portb[23]	io	gpio	-	-	-	-		1.8V
A17	i2s0_sck1	i2s_0_tsck_i	io	I2s0 bit clock for tx.	gpio_ext_portb[24]	io	gpio	-	-	-	-		1.8V
B15	i2s0_sdi	i2s_0_sd_i[0]	i	I2s0 serial data for rx.	gpio_ext_portb[27]	io	gpio	-	-	-	-		1.8V

A15	i2s0_sdo	i2s_0_sd_o[1]	o	I2s0 serial data for tx.	gpio_ext_portb[28]	io	gpio	-	-	-	-		1.8V
D15	i2s0_ws0	i2s_0_rws_i	io	I2s0 channel select for rx.	gpio_ext_portb[25]	io	gpio	-	-	-	-		1.8V
A16	i2s0_ws1	i2s_0_tws_i	io	I2s0 channel select for tx.	gpio_ext_portb[26]	io	gpio	-	-	-	-		1.8V
SPI													
B18	spi0_clk	i_ssi_0_sclk_out	o	spi0 interface clock	i_ssi_3_sclk_in	i	spi3 interface clock	gpio_ext_portb[21]	io	gpio	-		1.8V
A19	spi0_cs_n	i_ssi_0_ss_0_n	o	spi0 chip select signal	i_ssi_3_ss_in_n	i	spi3 chip select signal	gpio_ext_portb[20]	io	gpio	PU w/o en		1.8V
B17	spi0_miso	i_ssi_0_rxd	i	spi0 input data signal	i_ssi_3_rxd	i	spi3 input data signal	gpio_ext_portb[22]	io	gpio	PU w/o en		1.8V
A18	spi0_mosi	i_ssi_0_txd	o	spi0 output data signal	i_ssi_3_txd	o	spi3 output data signal	gpio_ext_portb[19]	io	gpio	-		1.8V
C18	spi1_clk	i_ssi_1_sclk_out	o	spi1 interface clock	i_ssi_2_sclk_in	i	spi2 interface clock	gpio_ext_portb[17]	io	gpio	-		1.8V
D18	spi1_cs_n	i_ssi_1_ss_0_n	o	spi1 chip select signal	i_ssi_2_ss_in_n	i	spi2 chip select signal	gpio_ext_portb[16]	io	gpio	PU w/o en		1.8V
C17	spi1_miso	i_ssi_1_rxd	i	spi1 input data signal	i_ssi_2_rxd	i	spi2 input data signal	gpio_ext_portb[18]	io	gpio	PU w/o en		1.8V
E18	spi1_mosi	i_ssi_1_txd	o	spi1 output data signal	i_ssi_2_txd	o	spi2 output data signal	gpio_ext_portb[15]	io	gpio	-		1.8V
UART													
C11	uart0_cts	i_uart_0_SIO_cts_n	i	uart0 clear to send modem status	gpio_ext_portb[14]	io	gpio	-	-	-	-		1.8V
B11	uart0_rts	i_uart_0_SIO_rts_n	o	uart0 modem control request to send output	gpio_ext_portb[13]	io	gpio	-	-	-	-		1.8V
A10	uart0_rxd	i_uart_0_SIO_sin	i	uart0 received data	gpio_ext_portb[12]	io	gpio	-	-	-	-		1.8V
A11	uart0_txd	i_uart_0_SIO_sout	o	uart0 transmitted data	gpio_ext_portb[11]	io	gpio	-	-	-	-		1.8V
B12	uart1_cts	i_uart_1_SIO_cts_n	i	uart1 clear to send modem status	gpio_ext_portb[10]	io	gpio	zsp_tdo	o	zsp jtag tdo	-		1.8V
E12	uart1_rts	i_uart_1_SIO_rts_n	o	uart1 modem control request to send output	gpio_ext_portb[9]	io	gpio	zsp_tms	i	zsp jtag tms	-		1.8V
C12	uart1_rxd	i_uart_1_SIO_sin	i	uart1 received data	gpio_ext_portb[8]	io	gpio	zsp_tdi	i	zsp jtag tdi	-		1.8V
D12	uart1_txd	i_uart_1_SIO_sout	o	uart1 transmitted data	gpio_ext_portb[7]	io	gpio	zsp_ntrst	i	zsp jtag ntrst	-		1.8V
C13	hs_uart2_cts	i_uart_2_SIO_cts_n	i	uart2 clear to send modem status	gpio_ext_portb[4]	io	gpio	-	-	-	-		1.8V
B13	hs_uart2_rts	i_uart_2_SIO_rts_n	o	uart2 modem control request to send	gpio_ext_portb[3]	io	gpio	-	-	-	-		1.8V

				output									
E13	hs_uart2_rxd	i_uart_2_SIO_sin	i	uart2 received data	gpio_ext_portb[2]	io	gpio	-	-	-	-		1.8V
D13	hs_uart2_txd	i_uart_2_SIO_sout	o	uart2 transmitted data	gpio_ext_portb[1]	io	gpio	-	-	-	-		1.8V
D14	hs_uart3_cts	i_uart_3_SIO_cts_n	i	uart3 clear to send modem status	gpio_ext_portb[0]	io	gpio	-	-	-	-		1.8V
C14	hs_uart3_rts	i_uart_3_SIO_rts_n	o	uart3 modem control request to send output	gpio_ext_porta[31]	io	gpio	-	-	-	-		1.8V
E15	hs_uart3_rxd	i_uart_3_SIO_sin	i	uart3 received data	gpio_ext_porta[30]	io	gpio	-	-	-	-		1.8V
E14	hs_uart3_txd	i_uart_3_SIO_sout	o	uart3 transmitted data	gpio_ext_porta[29]	io	gpio	-	-	-	-		1.8V
A13	irda_rxd	i_uart_1_sir_in	i	uart1 IrDA SIR input	gpio_ext_portb[6]	io	gpio	-	-	-	-		1.8V
A12	irda_txd	i_uart_1_sir_out_n	o	uart1 IrDA SIR output	gpio_ext_portb[5]	io	gpio	-	-	-	-		1.8V
GPIO													
E8	GPIO0	gpio_ext_porta[0]	io	core gpio0	-	-	-	-	-	-	-	3	1.8V/3.3V
D8	GPIO1	gpio_ext_porta[1]	io	core gpio1	-	-	-	-	-	-	-	3	1.8V/3.3V
C8	GPIO2	gpio_ext_porta[2]	io	core gpio2	-	-	-	-	-	-	-	3	1.8V/3.3V
E7	GPIO3	gpio_ext_porta[3]	io	core gpio3	-	-	-	-	-	-	-	3	1.8V/3.3V
D7	GPIO4	gpio_ext_porta[4]	io	core gpio4	-	-	-	-	-	-	-	3	1.8V/3.3V
C7	GPIO5	gpio_ext_porta[5]	io	core gpio5	-	-	-	-	-	-	-	3	1.8V/3.3V
E6	GPIO6	gpio_ext_porta[6]	io	core gpio6	-	-	-	-	-	-	-	3	1.8V/3.3V
D6	GPIO7	gpio_ext_porta[7]	io	core gpio7	-	-	-	-	-	-	-	3	1.8V/3.3V
F21	GPIO8	freq_mode[0]	i	freq mode 0	gpio_ext_porta[8]	io	core gpio8	-	-	-	-		1.8V
F22	GPIO9	freq_mode[1]	i	freq mode 1	gpio_ext_porta[9]	io	core gpio9	-	-	-	-		1.8V
F23	GPIO10	freq_mode[2]	i	freq mode 2	gpio_ext_porta[10]	io	core gpio10	-	-	-	-		1.8V
E19	GPIO11	freq_mode[3]	i	freq mode 3	gpio_ext_porta[11]	io	core gpio11	-	-	-	-		1.8V
E20	GPIO12	freq_mode[4]	i	freq mode 4	gpio_ext_porta[12]	io	core gpio12	-	-	-	-		1.8V
E21	GPIO13	boot_mode[0]	i	boot mode 0	gpio_ext_porta[13]	io	core gpio13	-	-	-	-		1.8V

E22	GPIO14	boot_mode[1]	i	boot mode 1	gpio_ext_porta[14]	io	core gpio14	-	-	-	-		1.8V
E23	GPIO15	boot_mode[2]	i	boot mode 2	gpio_ext_porta[15]	io	core gpio15	-	-	-	-		1.8V
D19	GPIO16	gpio_ext_porta[16]	io	core gpio16	-	-	-	-	-	-	-		1.8V
D20	GPIO17	gpio_ext_porta[17]	io	core gpio17	-	-	-	-	-	-	-		1.8V
D21	GPIO18	gpio_ext_porta[18]	io	core gpio18	dat_s3_i[0]	io	SDMMC slot3 data signal	i2s_1_rsck_i	io	I2s1 bit clock for rx.	-		1.8V
D22	GPIO19	gpio_ext_porta[19]	io	core gpio19	dat_s3_i[1]	io	SDMMC slot3 data signal	i2s_1_tsck_i	io	I2s1 bit clock for tx.	-		1.8V
D23	GPIO20	gpio_ext_porta[20]	io	core gpio20	dat_s3_i[2]	io	SDMMC slot3 data signal	i2s_1_rws_i	io	I2s1 channel select for rx.	-		1.8V
C19	GPIO21	gpio_ext_porta[21]	io	core gpio21	dat_s3_i[3]	io	SDMMC slot3 data signal	i2s_1_tws_i	io	I2s1 channel select for tx.	-		1.8V
B19	GPIO22	gpio_ext_porta[22]	io	core gpio22	sdclk_s3	o	SDMMC slot3 interface clock	i2s_1_sd_i[0]	i	I2s1 serial data for rx.	-		1.8V
C20	GPIO23	gpio_ext_porta[23]	io	core gpio23	cmd_s3_i	io	SDMMC slot3 command signal	i2s_1_sd_o[1]	o	I2s1 serial data for tx.	-		1.8V
C21	GPIO24	gpio_ext_porta[24]	io	core gpio24	-	-	-	-	-	-	-		1.8V
C23	GPIO25	gpio_ext_porta[25]	io	core gpio25	-	-	-	-	-	-	-		1.8V
A21	GPIO26	gpio_ext_porta[26]	io	core gpio26	-	-	-	-	-	-	-		1.8V
Jatg													
E10	jtag_mode	test_jtag_mode	i	jtag mode select	-	-	-	-	-	-	-		1.8V
E11	tck	cs_tck	i	coresight jtag tck	bs_tck	i	boundary scan jtag tck	-	-	-	PD w/o en		1.8V
B10	tdi	cs_tdi	i	coresight jtag tdi	bs_tdi	i	boundary scan jtag tdi	-	-	-	PU w/o en		1.8V
D9	tdo	cs_tdo	o	coresight jtag tdo	bs_tdo	o	boundary scan jtag tdo	-	-	-	-		1.8V
C9	tms	cs_tms	i	coresight jtag tms	bs_tms	i	boundary scan jtag tms	-	-	-	PU w/o en		1.8V
C10	trst	cs_ntrst	i	coresight jtag ntrst	bs_ntrst	i	boundary scan jtag ntrst	-	-	-	PD w/o en		1.8V
SYSTEM													
W7	chip_mode_0	chip_mode[0]	i	chip mode 0	-	-	-	-	-	-	PD w/o en	4	1.8V
Y7	chip_mode_1	chip_mode[1]	i	chip mode 1	-	-	-	-	-	-	PD w/o en	4	1.8V
AA7	chip_mode_2	chip_mode[2]	i	chip mode 0	-	-	-	-	-	-	PD w/o en	4	1.8V

AA10	mclk	mclk	o	Clock output for audio codec.	-	-	-	-	-	-	-	4	1.8V
AA6	pwrok	pwrok	i	Power ok.	-	-	-	-	-	-	-	4	1.8V
Y8	sus_s3_ack_n	sus_s3_ack_n	o	Suspend acknowledge.	-	-	-	-	-	-	-	4	1.8V
AA8	sus_s3_n	sus_s3_n	i	Suspend request.	-	-	-	-	-	-	PU w/o en	4	1.8V
AC3	sysclk_12m_xi	sysclk_12m_xi	i	System 12M clock crystal XI.	-	-	-	-	-	-	-	4	1.8V
AC4	sysclk_12m_xo	sysclk_12m_xo	o	System 12M clock crystal XO.	-	-	-	-	-	-	-	4	1.8V
W6	sysclk_32k	sysclk_32k	i	System 32K clock.	-	-	-	-	-	-	-	4	1.8V
W10	wakeup_gpio0	wakeup_gpio0	I/O	wakeup gpio0	-	-	-	-	-	-	-	4	1.8V
Y10	wakeup_gpio1	wakeup_gpio1	I/O	wakeup gpio1	-	-	-	-	-	-	-	4	1.8V
W9	wakeup_gpio2	wakeup_gpio2	I/O	wakeup gpio2	-	-	-	-	-	-	-	4	1.8V
Y9	wakeup_gpio3	wakeup_gpio3	I/O	wakeup gpio3	-	-	-	-	-	-	-	4	1.8V
W8	wakeup_gpio4	wakeup_gpio4	I/O	wakeup gpio4	-	-	-	-	-	-	-	4	1.8V
AB9	wakeup_gpio5	wakeup_gpio5	I/O	wakeup gpio5	-	-	-	-	-	-	-	4	1.8V
W11	wakeup_gpio6	wakeup_gpio6	I/O	wakeup gpio6	-	-	-	-	-	-	-	5	1.8/3.3V
Y11	wakeup_gpio7	wakeup_gpio7	I/O	wakeup gpio7	-	-	-	-	-	-	-	5	1.8/3.3V
PWM													
B7	pwm0	pwm_out[0]	o	PWM0 signal.	gpio_ext_porta[28]	io	gpio	-	-	-	-	3	1.8/3.3V
B8	pwm1	pwm_out[1]	o	PWM1 signal.	gpio_ext_porta[27]	io	gpio	-	-	-	-	3	1.8/3.3V
Power													
R14	AVDD_FUSE			High voltage for fuse programming, ground for read.									
AB13	AVDD_hdmi			Analog voltage for HDMI PHY									
W18	AVDD_hsic			1.2V Transmitter Power Supply									
AC9	AVDD_PLL0			PLL0 Analog VDD									
AC8	AVDD_PLL1			PLL1 Analog VDD									

AB8	AVDD_PLL2	PLL2 Analog VDD
AB7	AVDD_PLL3	PLL3 Analog VDD
AB6	AVDD_PLL4	PLL4 Analog VDD
AC7	AVDD_PLL5	PLL5 Analog VDD
AC6	AVDD_PLL6	PLL6 Analog VDD
W15	AVDD_usb	3.3V analog power pad
P11	VDD_2D	Digital Power Supply for 2D
R11	VDD_2D	Digital Power Supply for 2D
H14	VDD_CORE	Digital Power Supply for CORE
H15	VDD_CORE	Digital Power Supply for CORE
J13	VDD_CORE	Digital Power Supply for CORE
J14	VDD_CORE	Digital Power Supply for CORE
K13	VDD_CORE	Digital Power Supply for CORE
K14	VDD_CORE	Digital Power Supply for CORE
K15	VDD_CORE	Digital Power Supply for CORE
L9	VDD_CORE	Digital Power Supply for CORE
L14	VDD_CORE	Digital Power Supply for CORE
M17	VDD_CORE	Digital Power Supply for CORE
N10	VDD_CORE	Digital Power Supply for CORE
N14	VDD_CORE	Digital Power Supply for CORE
P9	VDD_CORE	Digital Power Supply for CORE
P13	VDD_CORE	Digital Power Supply for CORE

P16	VDD_CORE	Digital Power Supply for CORE
R12	VDD_CORE	Digital Power Supply for CORE
R13	VDD_CORE	Digital Power Supply for CORE
T10	VDD_CORE	Digital Power Supply for CORE
T11	VDD_CORE	Digital Power Supply for CORE
T13	VDD_CORE	Digital Power Supply for CORE
T14	VDD_CORE	Digital Power Supply for CORE
T15	VDD_CORE	Digital Power Supply for CORE
T16	VDD_CORE	Digital Power Supply for CORE
U12	VDD_CORE	Digital Power Supply for CORE
G12	VDD_CPU	Digital Power Supply for CPU
H8	VDD_CPU	Digital Power Supply for CPU
H9	VDD_CPU	Digital Power Supply for CPU
H10	VDD_CPU	Digital Power Supply for CPU
H11	VDD_CPU	Digital Power Supply for CPU
J8	VDD_CPU	Digital Power Supply for CPU
J10	VDD_CPU	Digital Power Supply for CPU
J11	VDD_CPU	Digital Power Supply for CPU
J12	VDD_CPU	Digital Power Supply for CPU
K8	VDD_CPU	Digital Power Supply for CPU
K9	VDD_CPU	Digital Power Supply for CPU
K10	VDD_CPU	Digital Power Supply for CPU
K11	VDD_CPU	Digital Power Supply for CPU
L10	VDD_CPU	Digital Power Supply for CPU
M9	VDD_CPU_RAM	Digital Power Supply for CPU RAM

N9	VDD_CPU_RAM	Digital Power Supply for CPU RAM
P10	VDD_DEC	Digital Power Supply for Video Decoder
R10	VDD_DEC	Digital Power Supply for Video Decoder
L15	VDD_ENC	Digital Power Supply for Video Encoder
M15	VDD_ENC	Digital Power Supply for Video Encoder
P14	VDD_ISP	Digital Power Supply for ISP
P15	VDD_ISP	Digital Power Supply for ISP
H16	VDD_MALI	Digital Power Supply for GPU
J16	VDD_MALI	Digital Power Supply for GPU
K16	VDD_MALI	Digital Power Supply for GPU
L16	VDD_MALI	Digital Power Supply for GPU
T9	VDD_WAKEUP	Digital Power Supply for Wakeup Domain
N15	VDD_ZSP	Digital Power Supply for DSP
N16	VDD_ZSP	Digital Power Supply for DSP
A3	VDDIO_DDR	IO Power Supply for DDR
C6	VDDIO_DDR	IO Power Supply for DDR
D4	VDDIO_DDR	IO Power Supply for DDR
E2	VDDIO_DDR	IO Power Supply for DDR
G4	VDDIO_DDR	IO Power Supply for DDR
H2	VDDIO_DDR	IO Power Supply for DDR

K4	VDDIO_DDR	IO Power Supply for DDR
L2	VDDIO_DDR	IO Power Supply for DDR
L8	VDDIO_DDR	IO Power Supply for DDR
M7	VDDIO_DDR	IO Power Supply for DDR
N4	VDDIO_DDR	IO Power Supply for DDR
N8	VDDIO_DDR	IO Power Supply for DDR
P2	VDDIO_DDR	IO Power Supply for DDR
P8	VDDIO_DDR	IO Power Supply for DDR
R8	VDDIO_DDR	IO Power Supply for DDR
T4	VDDIO_DDR	IO Power Supply for DDR
T8	VDDIO_DDR	IO Power Supply for DDR
U2	VDDIO_DDR	IO Power Supply for DDR
W4	VDDIO_DDR	IO Power Supply for DDR
Y2	VDDIO_DDR	IO Power Supply for DDR
AB3	VDDIO_DDR	IO Power Supply for DDR
B14	VDDIO_GPIO	IO Power Supply for GPIO
B20	VDDIO_GPIO	IO Power Supply for GPIO
B21	VDDIO_GPIO	IO Power Supply for GPIO
C22	VDDIO_GPIO	IO Power Supply for GPIO
D10	VDDIO_GPIO	IO Power Supply for GPIO
E17	VDDIO_GPIO	IO Power Supply for GPIO
H13	VDDIO_GPIO	IO Power Supply for GPIO
R22	VDDIO_GPIO	IO Power Supply for GPIO
V19	VDDIO_GPIO	IO Power Supply for GPIO
AA22	VDDIO_GPIO	IO Power Supply for GPIO

T19	VDDIO_GPIO2		IO Power Supply for GPIO group2 (IO Ring2)
E9	VDDIO_GPIO3		IO Power Supply for GPIO group3 (IO Ring3)
AB20	VDDIO_ISP		IO Power Supply for ISP
F19	VDDIO_LCD		IO Power Supply for LCD (IO Ring 1)
J22	VDDIO_LCD		IO Power Supply for LCD (IO Ring 1)
M19	VDDIO_LCD		IO Power Supply for LCD (IO Ring 1)
Y12	VDDIO_WAKEUP		IO Power Supply for Wakeup 1.8v Domain (IO Ring4)
AB10	VDDIO_WAKEUP33		IO Power Supply for Wakeup 3.3v Domain (IO Ring5)
R16	VDDL_USB		1.1V digital power pad
M5	VREF_DDR		Voltage Reference for DDR
GND			
Y18	AVSS_HSIC		Transmitter Ground Supply
AC5	AVSS_PLL		Analog VSS for PLL
AC18	AVSS_USB		Analog VSS for USB
A1	GND		ground
A2	GND		ground
A8	GND		ground
A14	GND		ground
A20	GND		ground
A22	GND		ground

A23	GND	ground
B1	GND	ground
B2	GND	ground
B6	GND	ground
B22	GND	ground
B23	GND	ground
D3	GND	ground
D11	GND	ground
D17	GND	ground
E1	GND	ground
F20	GND	ground
G3	GND	ground
G7	GND	ground
G8	GND	ground
G9	GND	ground
G10	GND	ground
G11	GND	ground
G13	GND	ground
G14	GND	ground
G15	GND	ground
G16	GND	ground
G17	GND	ground
H1	GND	ground
H7	GND	ground
H12	GND	ground

H17	GND	ground
J7	GND	ground
J9	GND	ground
J15	GND	ground
J17	GND	ground
J23	GND	ground
K3	GND	ground
K7	GND	ground
K12	GND	ground
K17	GND	ground
L1	GND	ground
L7	GND	ground
L11	GND	ground
L12	GND	ground
L13	GND	ground
L17	GND	ground
M8	GND	ground
M10	GND	ground
M11	GND	ground
M12	GND	ground
M13	GND	ground
M14	GND	ground
M16	GND	ground
M20	GND	ground
N5	GND	ground

N7	GND	ground
N11	GND	ground
N12	GND	ground
N13	GND	ground
N17	GND	ground
P1	GND	ground
P7	GND	ground
P12	GND	ground
P17	GND	ground
R7	GND	ground
R9	GND	ground
R15	GND	ground
R17	GND	ground
R19	GND	ground
R23	GND	ground
T3	GND	ground
T7	GND	ground
T12	GND	ground
T17	GND	ground
U1	GND	ground
U7	GND	ground
U8	GND	ground
U9	GND	ground
U10	GND	ground
U11	GND	ground

U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
V20	GND
W3	GND
W12	GND
W14	GND
Y1	GND
Y6	GND
Y15	GND
AA9	GND
AA15	GND
AB1	GND
AB2	GND
AB4	GND
AB22	GND
AB23	GND
AC1	GND
AC2	GND
AC10	GND
AC13	GND
AC16	GND
AC20	GND

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AC22	GND		ground	
AC23	GND		ground	

Note:

PU w/ en: Pull-up Resistor with enable controlled by software register.

PU w/o en: Pull-up Resistor without enable control

PD w/ en: Pull-down Resistor with enable controlled by software register.

PD w/o en: Pull-down Resistor without enable control

3.2 Chip Mode Selection Table

3.2.1 Chip Frequency Mode

Some clocks frequency should be certain on power on, which can be decided by STRAP PIN – FREQ_MODE [3:0] – {BUS_MODE [1:0], CPU_MODE [1:0]}.

Table 18 CPU Power on Frequency

CPU_MODE[1:0]	00	01	10	11
CPU_FREQ (MHz)	1200	1000	800	600

Table 19 BUS Power on Frequency

BUS_MODE[1:0]	00	01	10	11
DDR_FREQ (MHz)	400	333	266	200
L3M_FREQ (MHz)	400	333	266	200
L3_FREQ (MHz)	200	166	133	100
L4_FREQ (MHz)	100	83	66.5	50
L5_FREQ (MHz)	50	41.6	33.25	25

Table 20 Relationship between STRAP PIN and IO

STRAP PIN	IO
FREQ_MODE[0]	GPIO8
FREQ_MODE[1]	GPIO9
FREQ_MODE[2]	GPIO10
FREQ_MODE[3]	GPIO11
BOOT_MODE[0]	GPIO13
BOOT_MODE[1]	GPIO14
BOOT_MODE[2]	GPIO15

3.2.2 Boot Mode

Table 21 Boot Mode descriptions

boot_mode[2]	boot_mode[1]	boot_mode[0]	Description
x	0	0	1. first boot from SD/MMC slot0/1; 2. if fail, then from USB device port
x	0	1	1. first boot from SPI-0; 2. if fail, then from SD/MMC slot0/1; 3. if fail, then from USB device

			port;
x	1	0	boot from USB device port
x	1	1	boot from UART-0

Note: x -- don't care.

3.2.3 Chip Mode

Table 22 Chip Mode descriptions

jtag_mode	chip_mode[2]	chip_mode[1]	chip_mode[0]	Description
0	0	0	0	function Mode (normal mode); Jtag port is used as CoreSight debug

Note: The settings other than function mode (jtag_mode = 1'b0 && chip_mode [2:0] = 3'b000) are reserved.

Chapter 4 System Memory Mapping

Table 23 System Memory Mapping

NuSmart3 Memory Address Mapping (Core)			
Interface	**Address Range**	**Size**	**Base Address**
Internal Memory			
BootROM	0x00008000	32KB	0x00000000
SARRAM	0x00001000	4K	0x05800000
ZSPMEM	0x00080000	512KB	0x07000000
External Memory			
LPDDR2/DDR3	0xF0000000	4G(minus 256M)	0x10000000
Debug APB			
Debug ROM	0x00001000	4K	0x04000000
Reserved(ETB)	0x00001000	4K	0x04001000
CTI	0x00001000	4K	0x04002000
TPIU	0x00001000	4K	0x04003000
FUNNEL	0x00001000	4K	0x04004000
Reserved(ITM)	0x00001000	4K	0x04005000
Reserved(SWO)	0x00001000	4K	0x04006000
Reserved	0x00109000	1M (minus 36K)	0x04007000
A9 Debug ROM	0x00001000	4K	0x04100000
Reserved	0x0000F000	60K	0x04101000
CoreDbg0	0x00001000	4K	0x04110000
PMU0	0x00001000	4K	0x04111000
CoreDbg1	0x00001000	4K	0x04112000
PMU1	0x00001000	4K	0x04113000
Reserved	0x00004000	16K	0x04114000
CTI0	0x00001000	4K	0x04118000
CTI1	0x00001000	4K	0x04119000
Reserved	0x00002000	8K	0x0411A000
PTM0	0x00001000	4K	0x0411C000
PTM1	0x00001000	4K	0x0411D000
Reserved	0x00002000	8K	0x0411E000
Reserved	0x00EE0000	15M(minus 128K)	0x04120000
ARM MPU			
MPCore-A9	0x00002000	8K	0x05040000
PL310	0x00001000	4K	0x05042000

L4_CFG(0x05000000~0x05800000)			
DISP_CTRL0	0x00001000	4K	0x05010000
DISP_CTRL1	0x00001000	4K	0x05011000
DMA_330	0x00001000	4K	0x05020000
DMA_330_S	0x00001000	4K	0x05021000
MALI	0x00010000	64K	0x05030000
SD/MMC	0x00010000	64K	0x05070000
USB OHCI	0x00010000	64K	0x05080000
USB EHCI	0x00010000	64K	0x05090000
USBOTG	0x00010000	64K	0x050A0000
ON2 Decoder	0x00010000	64K	0x050C0000
ON2 Encoder	0x00010000	64K	0x050D0000
DRAM_CTR0	0x00001000	4K	0x050E0000
HDMI	0x00010000	64K	0x05110000
GC300	0x00040000	256K	0x05140000
CamerIC	0x00020000	128K	0x05180000
L4_CFG_WAKEUP(0x05800000~0x05A00000)			
SARRAM	0x00001000	4K	0x05800000
SARRAM_CTRL	0x00001000	4K	0x05820000
PRCM	0x00001000	4K	0x05821000
SCM	0x00001000	4K	0x05822000
GPIO_WAKEUP	0x00001000	4K	0x05823000
TIME0	0x00001000	4K	0x05824000
L4_PER(0x06000000~0x07000000)			
I2S0	0x00001000	4K	0x06060000
I2S1	0x00001000	4K	0x06061000
UART0	0x00010000	64K	0x06090000
UART1	0x00010000	64K	0x060A0000
UART2	0x00010000	64K	0x060B0000
UART3	0x00010000	64K	0x060C0000
SPI0	0x00010000	64K	0x060D0000
SPI1	0x00010000	64K	0x060E0000
SPI2	0x00010000	64K	0x060F0000
I2C0	0x00010000	64K	0x06100000
I2C1	0x00010000	64K	0x06110000
I2C2	0x00010000	64K	0x06120000
I2C3	0x00010000	64K	0x06130000
GPIO1	0x00010000	64K	0x06140000
TIME1	0x00010000	64K	0x06150000

AUX	0x00001000	4K	0x06160000
SPI3	0x00010000	64K	0x06170000
L3(0x07000000~0x08000000)			
BootROM	0x00008000	32KB	0x00000000
ROM_CTRL	0x00010000	64K	0x03000000
ZSPMEM	0x00080000	512KB	0x07000000
L3_ISS_CFG	0x00010000	64K	0x07100000
L3M(0x08000000~0x09000000)			
MemMax0	0x00000400	1K	0x08008000
NuSmart3 Interconnect Register Module Mapping			
Interface	**Address Range**	**Size**	**Base Address**
L3M			
ia_cpu0.ia	0x00000400	1K	0x08000000
ia_cpu1.ia	0x00000400	1K	0x08000400
ia_l3.ia	0x00000400	1K	0x08000800
ta_mem0.ta	0x00000400	1K	0x08001000
ta_l3.ta	0x00000400	1K	0x08001800
l3m_reg.si	0x00000400	1K	0x08002000
l3m_reg.rt	0x00000400	1K	0x08002400
L3			
ia_DISP0.ia	0x00000400	1K	0x07200000
ia_DISP1.ia	0x00000400	1K	0x07200400
ia_iss.ia	0x00000400	1K	0x07200800
ia_mali.ia	0x00000400	1K	0x07200C00
ia_twod.ia	0x00000400	1K	0x07201000
ia_vpu_dec.ia	0x00000400	1K	0x07201400
ia_vpu_enc.ia	0x00000400	1K	0x07201800
ia_dma.ia	0x00000400	1K	0x07201C00
ia_zspm.ia	0x00000400	1K	0x07202000
ia_sd.ia	0x00000400	1K	0x07202400
ia_cs.ia	0x00000400	1K	0x07202C00
ia_usbotg.ia	0x00000400	1K	0x07203000
ia_usbohci.ia	0x00000400	1K	0x07203400
ia_usbehci.ia	0x00000400	1K	0x07203800
ia_l3m.ia	0x00000400	1K	0x07203C00
ta_per_cpu.ta	0x00000400	1K	0x07205000
ta_per_other.ta	0x00000400	1K	0x07205400
ta_l4_cfg.ta	0x00000400	1K	0x07205800
ta_l3_iss.ta	0x00000400	1K	0x07205C00

ta_zspmem.ta	0x00000400	1K	0x07206000
ta_l3m.ta	0x00000400	1K	0x07206400
ta_rom.ta	0x00000400	1K	0x07206800
l3_reg.si	0x00000400	1K	0x07207000
l3_reg.rt	0x00000400	1K	0x07207400
L3_ISS			
iss_r.ia	0x00000400	1K	0x07100000
iss_w0.ia	0x00000400	1K	0x07100400
iss_w1.ia	0x00000400	1K	0x07100800
cfg.ia	0x00000400	1K	0x07101000
mem.ta	0x00000400	1K	0x07101400
l3iss.si	0x00000400	1K	0x07101800
l3iss.rt	0x00000400	1K	0x07101C00
L5_PER			
l5_per.ap	0x00001000	4K	0x06C00000
l5_per.la	0x00000400	1K	0x06C01000
l5_per.ip0(cpu)	0x00000400	1K	0x06C01400
l5_per.ip1(other)	0x00000400	1K	0x06C01800
aux.ta	0x00000400	1K	0x06C03400
i2s0.ta	0x00000400	1K	0x06C03800
i2s1.ta	0x00000400	1K	0x06C03C00
uart0.ta	0x00000400	1K	0x06C04000
uart1.ta	0x00000400	1K	0x06C04400
uart2.ta	0x00000400	1K	0x06C04800
uart3.ta	0x00000400	1K	0x06C04C00
spi0.ta	0x00000400	1K	0x06C05000
spi1.ta	0x00000400	1K	0x06C05400
spi2.ta	0x00000400	1K	0x06C05800
gpio1.ta	0x00000400	1K	0x06C05C00
i2c0.ta	0x00000400	1K	0x06C06000
i2c1.ta	0x00000400	1K	0x06C06400
i2c2.ta	0x00000400	1K	0x06C06800
i2c3.ta	0x00000400	1K	0x06C06C00
timer1.ta	0x00000400	1K	0x06C07000
spi3.ta	0x00000400	1K	0x06C07400
L4_CFG			
l4_cfg.ap	0x00001000	4K	0x05400000
l4_cfg.la	0x00000400	1K	0x05401000
l4_cfg.ip0	0x00000400	1K	0x05401400

cs.ta	0x00000400	1K	0x05403000
sd.ta	0x00000400	1K	0x05403400
dma330.ta	0x00000400	1K	0x05403800
dma330_s.ta	0x00000400	1K	0x05403C00
hdmi.ta	0x00000400	1K	0x05404000
mali.ta	0x00000400	1K	0x05404400
disp0.ta	0x00000400	1K	0x05404800
disp1.ta	0x00000400	1K	0x05404C00
pctl0.ta	0x00000400	1K	0x05405000
usbohci.ta	0x00000400	1K	0x05405C00
usbehci.ta	0x00000400	1K	0x05406000
usgotg.ta	0x00000400	1K	0x05406400
vpu_dec.ta	0x00000400	1K	0x05406800
vpu_enc.ta	0x00000400	1K	0x05406C00
twod.ta	0x00000400	1K	0x05407000
wakeup.ta	0x00000400	1K	0x05407400
cameric.ta	0x00000400	1K	0x05407C00
L5_WAKEUP			
l5_wk.ap	0x00001000	4K	0x058C0000
l5_wk.la	0x00000400	1K	0x058C1000
l5_wk.ip0	0x00000400	1K	0x058C1400
gpio_wk.ta	0x00000400	1K	0x058C1800
prcm.ta	0x00000400	1K	0x058C1C00
scm.ta	0x00000400	1K	0x058C2000
timer0.ta	0x00000400	1K	0x058C2400
sarram.ta	0x00000400	1K	0x058C2800

Chapter 5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 24 Absolute Maximum Ratings

Power Supply	Description	Min.	Nom.	Max.
VDDIO_DDR	IO Power Supply for DDR	-0.3v	1.5v	1.65v
VDDIO_WAKEUP	IO Power Supply for Wakeup 1.8v Domain	-0.3v	1.8v	1.98v
VDDIO_LCD	IO Power Supply for LCD	-0.3v	3.3/1.8v	3.63/1.98v
VDDIO_GPIO	IO Power Supply for GPIO	-0.3v	1.8v	1.98v
VDDIO_GPIO2	IO Power Supply for GPIO IO Ring2	-0.3v	3.3/1.8v	3.63/1.98v
VDDIO_GPIO3	IO Power Supply for GPIO IO Ring3	-0.3v	3.3/1.8v	3.63/1.98v
VDDIO_ISP	IO Power Supply for ISP	-0.3v	3.3/1.8v	3.63/1.98v
VDDIO_WAKEUP33	IO Power Supply for Wakeup 3.3v Domain	-0.3v	3.3/1.8v	3.63/1.98v
VREF_DDR	Voltage Reference for DDR	-0.3v	0.75v	0.825v
VDD_CORE	Digital Power Supply for CORE	-0.3v	1.1v	1.21v
VDD_CPU	Digital Power Supply for CPU	-0.3v	0.9~1.1v	0.99/1.21v
VDD_CPU_RAM	Digital Power Supply for CPU RAM	-0.3v	1.1v	1.21v
VDD_MALI	Digital Power Supply for GPU	-0.3v	1.1v	1.21v
VDD_2D	Digital Power Supply for 2D	-0.3v	1.1v	1.21v
VDD_ISP	Digital Power Supply for ISP	-0.3v	1.1v	1.21v
VDD_DEC	Digital Power Supply for Video Decoder	-0.3v	1.1v	1.21v
VDD_ENC	Digital Power Supply for Video Encoder	-0.3v	1.1v	1.21v
VDD_ZSP	Digital Power Supply for DSP	-0.3v	1.1v	1.21v
VDD_WAKEUP	Digital Power Supply for Wakeup Domain	-0.3v	1.1v	1.21v
VDDL_USB	1.1V digital power pad	-0.3v	1.1v	1.21v
AVDD_PLL0	PLL0 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL1	PLL1 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL2	PLL2 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL3	PLL3 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL4	PLL4 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL5	PLL5 Analog VDD	-0.3v	1.1v	1.21v
AVDD_PLL6	PLL6 Analog VDD	-0.3v	1.1v	1.21v
AVDD_HDMI	Analog voltage for HDMI PHY	-0.3v	1.1v	1.21v
AVDD_USB	3.3V analog power pad	-0.3v	3.3v	3.63v
AVDD_EFUSE	High voltage for fuse programming, ground for read.	-0.3v	2.5v	2.75v

AVDD_HSIC	1.2V Transmitter Power Supply	-0.3v	1.2v	1.32v

5.2 Operating Range

TBD

5.3 Power Supplies Sequencing

Power Up Sequence

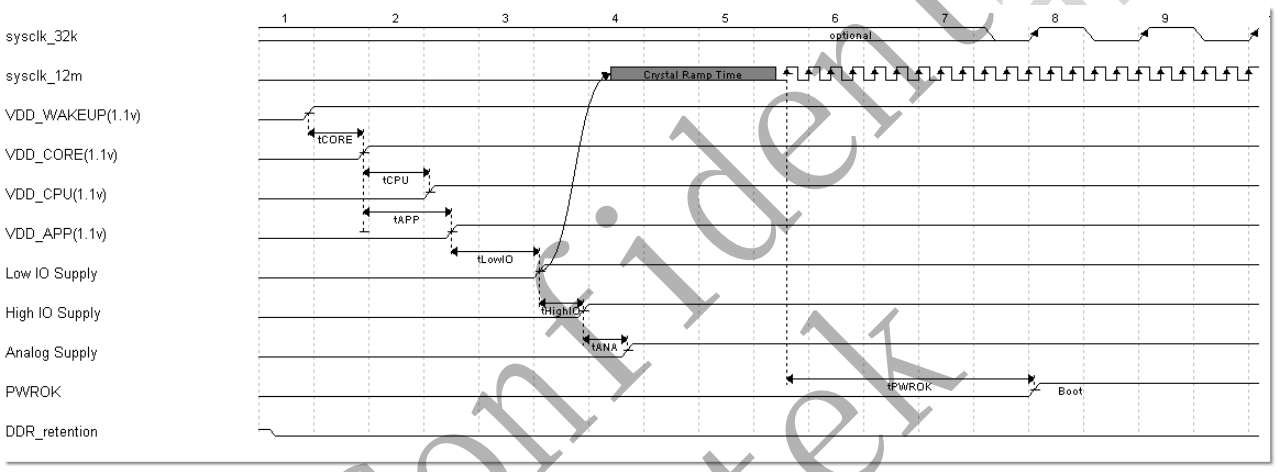


Figure 2 Power Up Sequence

Table 25 Power Up Sequence Parameters

Symbol	Description	Min	Typ	Max	Unit
tCORE	Delay from VDD_WAKEUP to VDD_CORE	0			ms
tCPU	Delay from VDD_CORE to VDD_CPU and VDD_CPU_RAM	0			ms
tAPP	Delay from VDD_CPU to VDD_APP, VDD_APP is including VDD_ZSP, VDD_2D, VDD_MALI, VDD_ISP, VDD_ENC, VDD_DEC. No timing requirement between them.	0			ms
tLowIO	Delay from VDD_APP to low voltage IO supply, including the 1.8v VDDIO_WAKEUP, VDDIO_DDR, …	1			ms
tHighIO	Delay from low voltage IO supply to high voltage IO supply	1			ms
tANA	Delay from IO supply to analog supply, including the AVDD_PLL, AVDD_HDMI, AVDD_USB, …	1			ms
tPWROK	Delay from sysclk_12m stable to pwrok deassert	2			ms

Note:

1. During power up sequence, the 32K system clock is not necessary, which is optional.

2. There is no strict order between the application supplies, which are including VDD_ZSP, VDD_ISP, VDD_2D, VDD_MALI, VDD_ENC, and VDD_DEC.
3. VDDL_USB is recommended to power with VDD_CORE together.

Power Down Sequence

When completely powering down the whole chip, the sequence is basically opposite with the power up sequence. It is recommended to be as follows:

1. Deassert the PWROK.
2. Remove the higher voltage IO supply and analog supply.
3. Remove the lower voltage IO supply.
4. Remove the 1.1v digital core supply.

Note: The power down sequence is not strictly required. It is acceptable as long as the duration of any changes from the recommended sequence are not longer than 10ms.

Suspend/Wakeup Sequence

When suspend, the VDD_WAKEUP, VDDIO_WAKEUP (1.8V), VDDIO_WAKEUP (3.3V), VDDIO_DDR (1.5V), VREF_DDR (0.75V) should be still on, other supplies can be shut off.

When wakeup, the VDD_CORE, VDDL_USB, VDD_CPU, and VDD_CPU_RAM must to be power, other power, such as application supplies, are decided by software.

5.4 I/O DC Parameters

5.4.1 Analog IO

Table 26 1.8V Analog IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units
V_{DD}	Pre_Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post_Driver Voltage	1.62	1.8	1.98	V
T_J	Junction Temperature	-40	25	125	℃
$V_{I(core)}$	Input Voltage Range for the Cell with Thin Device	-0.3		1.21	V
$V_{I(IO)}$	Input Voltage Range for the Cell with Thick Device	-0.3		1.98	V

Table 27 3.3V Analog IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units
V_{DD}	Pre_Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post_Driver Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	-40	25	125	℃
$V_{I(core)}$	Input Voltage Range for the Cell with Thin Device	-0.3		1.21	V
$V_{I(IO)}$	Input Voltage Range for the Cell with Thick Device	-0.3		3.6	V

5.4.2 Digital IO

Table 28 1.8V Digital IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units
V_{DD}	Pre-Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post-Driver Voltage	1.62	1.8	1.98	V
T_J	Junction Temperature	-40	25	125	℃
V_{IMAX}	Maximum Input Voltage			3.6	V
V_{IL}	Schmitt Trigger High to Low Threshold Point	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		3.6	V
V_T	Threshold Point	0.79	0.87	0.94	V
V_{T^+}	Schmitt Trigger Low to High Threshold Point	1	1.12	1.22	V
V_{T^-}	Schmitt Trigger High to Low Threshold Point	0.61	0.71	0.8	V
$V_{T_{PU}}$	Threshold Point with Pull-up Resistor Enabled	0.79	0.86	0.93	V
$V_{T_{PD}}$	Threshold Point with Pull-down Resistor Enabled	0.8	0.87	0.95	V
$V_{T^+_{PU}}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1	1.12	1.21	V
$V_{T^-_{PU}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.61	0.7	0.8	V
$V_{T^+_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	1.01	1.13	1.23	V
$V_{T^-_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.62	0.72	0.81	V
I_I	Input Leakage Current @ V_I =1.8V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O=1.8V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	56K	89K	148K	Ω
R_{PD}	Pull-down Resistor	52K	90K	167K	Ω
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_{OL}	Low Level Output Current @V_{OL}(max)				
	02:02mA	1.2	2.2	3.6	mA
	04:04mA	2.3	4.3	7.1	mA
	08:08mA	4.6	8.6	14.3	mA
	12:12mA	6.9	12.9	21.4	mA
	16:16mA	9.3	17.3	28.5	mA
	24:24mA	13.9	25.9	42.8	mA
I_{OH}	High Level Output Current @V_{OH} (min)				
	02:02mA	1.0	2.4	4.6	mA
	04:04mA	2.0	4.7	9.2	mA
	08:08mA	4.0	9.4	18.4	mA
	12:12mA	5.9	14.2	27.6	mA

	16:16mA	7.9	18.9	36.8	mA
	24:24mA	10.6	25.2	49.0	mA

Table 29 3.3V Digital IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units
V_{DD}	Pre-Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post-Driver Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	-40	25	125	℃
V_{IMAX}	Maximum Input Voltage			3.6	V
V_{IL}	Schmitt Trigger High to Low Threshold Point	-0.3		0.8	V
V_{IH}	Input High Voltage	2		3.6	V
V_T	Threshold Point	1.36	1.46	1.58	V
V_{T^+}	Schmitt Trigger Low to High Threshold Point	1.71	1.84	1.94	V
V_{T^-}	Schmitt Trigger High to Low Threshold Point	1.18	1.27	1.4	V
$V_{T_{PU}}$	Threshold Point with Pull-up Resistor Enabled	1.33	1.43	1.56	V
$V_{T_{PD}}$	Threshold Point with Pull-down Resistor Enabled	1.38	1.48	1.6	V
$V_{T^+_{PU}}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	1.69	1.81	1.92	V
$V_{T^-_{PU}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	1.15	1.25	1.38	V
$V_{T^+_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	1.72	1.86	1.98	V
$V_{T^-_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	1.2	1.3	1.41	V
I_I	Input Leakage Current @ V_I =3.3V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O=3.3V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	29K	41K	62K	Ω
R_{PD}	Pull-down Resistor	30K	44K	72K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @V_{OL}(max)				
	02:02mA	2.2	3.5	4.8	mA
	04:04mA	4.4	7.0	9.5	mA
	08:08mA	8.9	14.0	19.1	mA
	12:12mA	13.3	20.9	28.6	mA
	16:16mA	17.8	27.9	38.2	mA
	24:24mA	26.7	41.9	57.2	mA
I_{OH}	High Level Output Current @V_{OH} (min)				
	02:02mA	3.9	7.7	13.1	mA
	04:04mA	7.8	15.5	26.1	mA
	08:08mA	15.7	31.0	52.3	mA
	12:12mA	23.5	46.5	78.5	mA

	16:16mA	31.3	62.0	104.6	mA
	24:24mA	41.8	82.6	139.5	mA

5.4.3 SD/MMC Port0 IO

Table 30 SD/MMC Port0 1.8V IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units
V_{DD}	Pre-Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post-Driver Voltage	1.62	1.8	1.98	V
T_J	Junction Temperature	-40	25	125	℃
V_{IMAX}	Maximum Input Voltage			3.6	V
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		3.6	V
V_T	Threshold Point	0.79	0.88	0.98	V
V_{T^+}	Schmitt Trigger Low to High Threshold Point	-	-	-	V
V_{T^-}	Schmitt Trigger High to Low Threshold Point	-	-	-	V
$V_{T_{PU}}$	Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T_{PD}}$	Threshold Point with Pull-down Resistor Enabled	-	-	-	V
$V_{T^+_{PU}}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T^-_{PU}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T^+_{PD}}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	-	-	V
$V_{T^-_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	-	-	V
I_I	Input Leakage Current @ V_I =1.8V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O=1.8V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	43K	55K	67K	Ω
R_{PD}	Pull-down Resistor	43K	54K	66K	Ω
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_{OL}	Low Level Output Current @V_{OL}(max)				
	1216:12mA	11.3	20.4	32.8	mA
	1216:16mA	27.2	49.1	78.7	mA
I_{OH}	High Level Output Current @V_{OH} (min)				
	1216:12mA	7.4	17.6	34.2	mA
	1216:16mA	15.4	36.6	71.3	mA

Table 31 SD/MMC Port0 3.3V IO DC Parameters

Parameter	Description	Min.	Nom.	Max.	Units

V_{DD}	Pre-Driver Voltage	0.99	1.1	1.21	V
V_{DDPST}	Post-Driver Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	-40	25	125	℃
V_{IMAX}	Maximum Input Voltage			3.6	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage	2		3.6	V
V_T	Threshold Point	1.46	1.61	1.79	V
V_{T^+}	Schmitt Trigger Low to High Threshold Point	-	-	-	V
V_{T^-}	Schmitt Trigger High to Low Threshold Point	-	-	-	V
$V_{T_{PU}}$	Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T_{PD}}$	Threshold Point with Pull-down Resistor Enabled	-	-	-	V
$V_{T^+_{PU}}$	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T^-_{PU}}$	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	-	-	V
$V_{T^+_{PD}}$	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	-	-	V
$V_{T^-_{PD}}$	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	-	-	V
I_I	Input Leakage Current @ V_I=3.3V or 0V			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O=3.3V or 0V			±10μ	A
R_{PU}	Pull-up Resistor	43K	55K	66K	Ω
R_{PD}	Pull-down Resistor	43K	54K	66K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @V_{OL}(max)				
	1216:12mA	21.3	33.0	44.7	mA
	1216:16mA	51.2	79.2	107.2	mA
I_{OH}	High Level Output Current @V_{OH} (min)				
	1216:12mA	29.2	57.7	97.4	mA
	1216:16mA	60.8	120.2	203.0	mA

5.4.4 DDR

Table 32 DDR Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{DD}	Core supply voltage	0.99	1.1	1.21	V
V_{DDQ}	SSTL output supply voltage (DDR3)	1.425	1.50	1.575	V
V_{DDQ}	SSTL output supply voltage (DDR3L)	1.283	1.35	1.45	V

V_{DDQ}	HSUL output supply voltage (LPDDR2)	1.14	1.20	1.30	V
V_{REF}	SSTL reference supply voltage	0.49 * V_{DDQ}	0.5 * V_{DDQ}	0.5 1* V_{DDQ}	V
V_{TT}	External termination voltage	V_{REF} - 40mV	V_{REF}	V_{REF} + 40mV	V
T_J	Junction temperature	-40	25	125	℃

DDR3 Mode DC Specifications

The following table provides input and output DC threshold values and On-DIE-Termination (ODT) recommended values. The conditions for the output threshold values are unterminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table 33 DDR3 Mode DC Parameters

Symbol	Parameter	Min	Nom	Max	Units
$V_{IH(DC)}$	DC input voltage High	V_{REF} + 0.1		V_{DDQ}	**V**
$V_{IL(DC)}$	DC input voltage Low	V_{SSQ} - 0.3		V_{REF} - 0.1	**V**
V_{OH}	DC output logic High	0.8 * V_{DDQ}			**V**
V_{OL}	DC output logic Low			0.2 * V_{DDQ}	**V**
R_{TT}	Input termination resistance (ODT) to VDDQ/2	100 54 36	120 60 40	140 66 44	Ω

DDR3L Mode DC Specifications

The following table provides input and output DC threshold values and On-DIE-Termination (ODT) recommended values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table 34 DDR3L Mode DC Parameters

Symbol	Parameter	Min	Nom	Max	Units
VIH(DC)	DC input voltage High	V_{REF} + 0.09		V_{DDQ}	V
VIL(DC)	DC input voltage Low	V_{SSQ} -0.3		V_{REF} -0.09	V
VOH	DC output logic High	0.8 * V_{DDQ}			V
VOL	DC output logic Low			0.2 *V_{DDQ}	V
RTT	Input termination resistance (ODT) to VDDQ/2	100 54 36	120 60 40	140 66 44	ohm

LPDDR2 Mode DC Specifications

Table 35 LPDDR2 Mode DC Parameters

Symbol	Parameter	Min	Nom	Max	Units

$V_{IH(DC)}$	DC input voltage high	V_{REF} + 0.3		V_{DDQ}	V
$V_{IL(DC)}$	DC input voltage Low	V_{SSQ}		V_{REF} -0.3	V
$V_{OH(DC)}$	DC output voltage high	0.9 * V_{DDQ}			V
$V_{OL(DC)}$	DC output low voltage			0.1 *V_{DDQ}	V

5.4.5 USB

USB OTG PHY

Table 36 USB Low-/Full-Speed DC Parameters

Symbol	Parameter	Conditions	Min	Nom	Max
V_{IH}	Pad input high voltage		2.0V		
V_{IL}	Pad input low voltage				0.8V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2V		
V_{CM}	Common mode voltage range	Include V_{DI} range	0.8V		2.5V
V_{SE}	Single-ended receiver threshold		0.8V		2.0V
V_{OL}	Pad output low voltage		0V		0.3V
V_{OH}	Pad output high voltage		2.8V		3.6V
V_{CRS}	Differential output signal cross-point voltage		1.3V		2.0V
R_{PU}	Pull-up resistor	Bus idle	900Ω		1575Ω
		Receiving	1425Ω		3090Ω
R_{PD}	Pull-down resistor		14.25KΩ		24.80KΩ
C_{IN}	Transceiver pad capacitance	Pad to ground			20pF

Table 37 USB High-Speed DC Parameters

Symbol	Parameter	Conditions	Min	Nom	Max
V_{HSDI}	High-speed differential input signal level	|PADP-PADM|	150mV		
V_{HSSQ}	High-speed SQ detection threshold	|PADP-PADM|	100 mV		150 mV
V_{HSCM}	High-speed common mode voltage range		-50 mV		500 mV
V_{HSOH}	High-speed data signaling high		360 mV		440 mV
V_{HSOL}	High-speed data signaling low		-10 mV		10 mV
V_{CHIRPJ}	Chirp J level		700 mV		1100 mV
V_{CHIRPK}	Chirp K level		-900 mV		-500 mV
Z_{HSDV}	High-speed driver output resistance			45Ω	

USB HSIC PHY

Table 38 USB HSIC DC Parameters

Design Implementation	Value
Digital power supply (DVDD)	1.1 V (+ 10%, – 10%) at the macro pins with respect to DVSS
Transmitter power supply	1.2V (+8.4%, -8.4%) at the macro pins with respect to VSS12
Junction temperature	– 40 ºC through +125 ºC

5.4.6 HDMI

Table 39 HDMI DC Parameters

Category	Group	Value	Variation	Unit
Supply Voltage	AVCC	1.1	-5% to +5%	V
	DVCC	1.1	-5% to +5%	V
Frequency			25 to 225	MHz
Temperature			0 to 100 Junction temperature	C

5.5 System Clock Specifications

Table 40 System Clock Input Source Descriptions

Clock PIN	Frequency	Voltage	Source	Description
sysclk_32k	32KHz	1.8V	32KHz CMOS digital clock	The 32-kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode.
sysclk_12m_xi, sysclk_12m_xo	12MHz	1.8V	12MHz Crystal/OSC	sysclk_12m is used to generate the main source clock of the device. It supplies the PLLs reference clock as well as several other modules. The system clock input can be connected to either: – A crystal oscillator clock managed by sysclk_12m_xi and sysclk_12m_xo. – A CMOS digital clock through the sysclk_12m_xi pin.

Table 41 sysclk_32k Clock Specifications

sysclk_32k	Requirement	Description
Frequency	32768Hz	From off-chip PMIC or RTC output.

Rise time	< 20ns	Maximum rise time 20ns
Fall time	< 20ns	Maximum fall time 20ns
Frequency tolerance	±200ppm	Maximum ±200ppm

Table 42 sysclk_12m Clock Specifications

sysclk_12m_xi/sysclk_12m_xo	**Requirement**	**Description**
frequency tolerance	±500 ppm	required by USB ref clock
Ref. input jitter (long-term, P-P) (max)	2% div. reference	required by PLL ref clock
Reference H/L pulse width (min)	330ps	required by PLL ref clock
Crystal **-- CL**	12pF	Crystal load capacitance
Crystal **-- Maximum ESR**	80 Ohm	Crystal equivalent series resistance

Table 43 System Clock Output Descriptions

Clock PIN	**Frequency**	**Voltage**	**Description**
mclk	12MHz	1.8V	12MHz always on clock; could be used as audio CODEC reference clock.
alt_clk0	24MHz/12MHz/…	1.8V	Alternative Clock output, frequency is programmable (could be natural number divided by 480MHz, such as 24MHz, 12MHz, …)
alt_clk1	24MHz/12MHz/…/32KHz	1.8V	Alternative Clock output, frequency is programmable (could be natural number divided by 480MHz, such as 24MHz, 12MHz, … and also 32KHz.)

Chapter 6 External Peripheral Interfaces Timing Parameters

6.1 SD/MMC Interface Timing

Table 44 SDMMC Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0	5	ns
t_F	Input signal fall time	0	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

Table 45 SDMMC Interface Default Mode Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	40		ns	
t_{wh}	Duration time, SD_CLK high	19.5	20.5	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	3		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		11	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	5.4		ns	

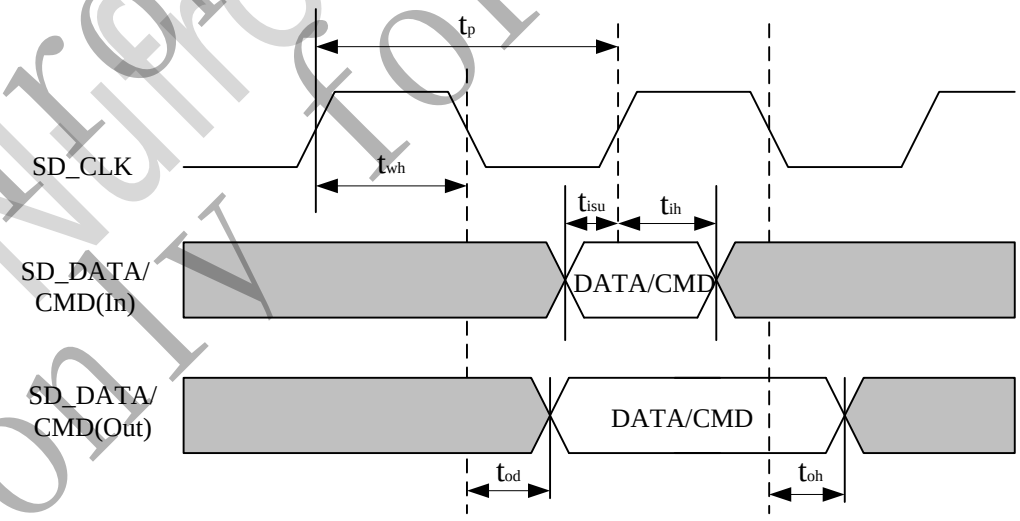


Figure 3 SDMMC Interface Default Mode Timing

Table 46 SDMMC Interface High Speed Mode Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	20		ns	
t_{wh}	Duration time, SD_CLK high	9.5	10.5	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	5.2		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		8.7	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	3.0		ns	

Table 47 SDMMC Interface SDR12 Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	40		ns	
t_{wh}	Duration time, SD_CLK high	19.5	20.5	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	5.2		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		8.7	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	3.0		ns	

Table 48 SDMMC Interface SDR25 Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	20		ns	
t_{wh}	Duration time, SD_CLK high	9.5	10.5	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	5.2		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		8.7	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	3.0		ns	

Table 49 SDMMC Interface SDR50 Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	12.5		ns	

t_{wh}	Duration time, SD_CLK high	5.75	6.75	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	5.2		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		9.3	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	3.5		ns	

Table 50 SDMMC Interface MMC Electrical Characteristics

Parameter		**MIN**	**MAX**	**Unit**	**Notes**
t_p	Cycle time, SD_CLK period	20		ns	
t_{wh}	Duration time, SD_CLK high	9.5	10.5	ns	
t_{isu}	required Setup time, input data valid before SD_CLK active edge	5.2		ns	
t_{ih}	required Hold time, input data valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to data output transition		8.6	ns	
t_{oh}	Hold Time, data output valid after SD_CLK active edge	3.6		ns	

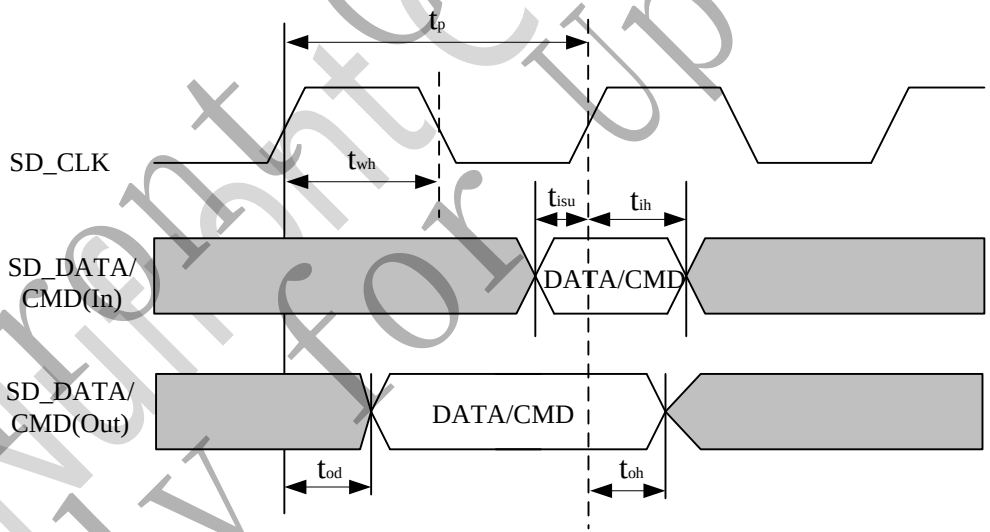


Figure 4 SDMMC Interface High Speed/SDR12/SDR25/SDR50/MMC Timing

Table 51 SDMMC Interface DDR50 Electrical Characteristics

Parameter		**MIN**	**MAX**	**Unit**	**Notes**
t_p	Cycle time, SD_CLK period	25		ns	
t_{isu}	Setup time, input CMD valid before SD_CLK active edge	5.2		ns	

t_{ih}	Hold time, input CMD valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to CMD output transition		9.3	ns	
t_{oh}	Hold Time, CMD output valid after SD_CLK active edge	3.5		ns	
t_{isu2x}	required Setup time, input DATA valid before SD_CLK active edge	5.2		ns	
t_{ih2x}	required Hold time, input DATA valid after SD_CLK active edge	0		ns	
t_{od2x}	Delay time, SD_CLK active edge to DATA output transition		9.3	ns	
t_{oh2x}	Hold Time, DATA output valid after SD_CLK active edge	3.5		ns	

Table 52 SDMMC Interface MMC DDR Electrical Characteristics

Parameter		**MIN**	**MAX**	**Unit**	**Notes**
t_p	Cycle time, SD_CLK period	25		ns	
t_{isu}	Setup time, input CMD valid before SD_CLK active edge	5.2		ns	
t_{ih}	Hold time, input CMD valid after SD_CLK active edge	0		ns	
t_{od}	Delay time, SD_CLK active edge to CMD output transition		9.2	ns	
t_{oh}	Hold Time, CMD output valid after SD_CLK active edge	4.2		ns	
t_{isu2x}	required Setup time, input DATA valid before SD_CLK active edge	5.2		ns	
t_{ih2x}	required Hold time, input DATA valid after SD_CLK active edge	0		ns	
t_{od2x}	Delay time, SD_CLK active edge to DATA output transition		9.2	ns	
t_{oh2x}	Hold Time, DATA output valid after SD_CLK active edge	4.2		ns	

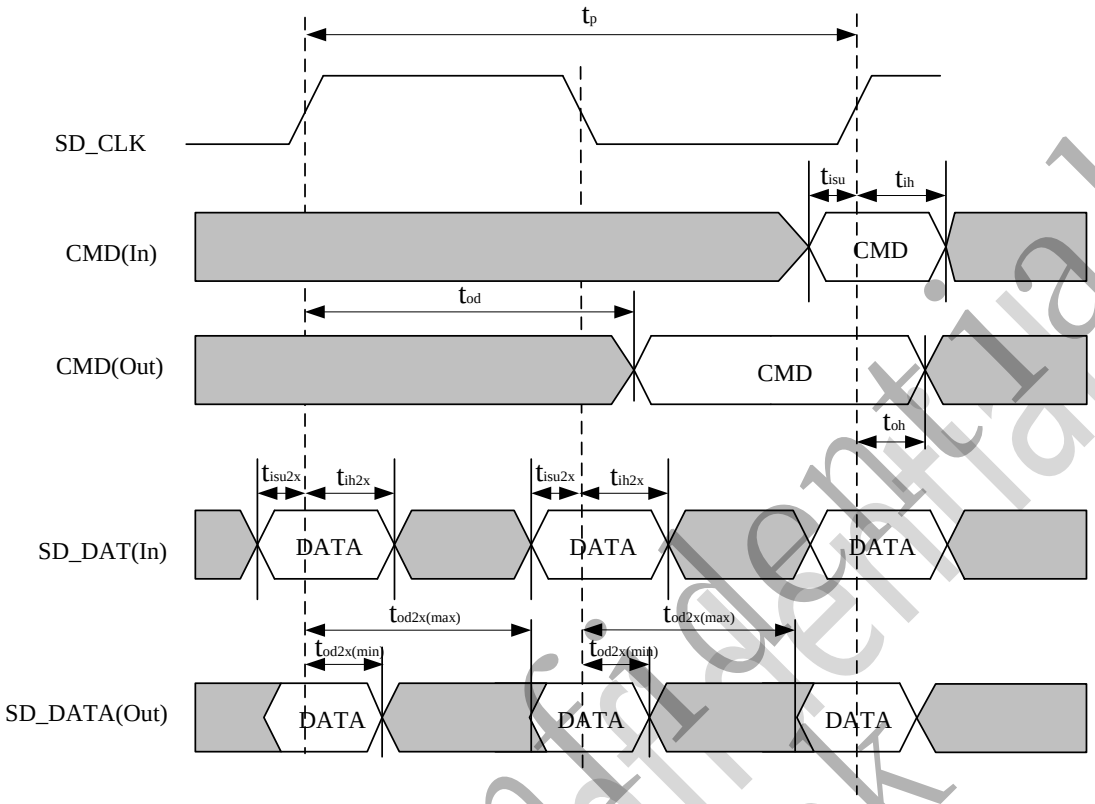


Figure 5 SDMMC Interface DDR50/MMC DDR Timing

6.2 SPI interface timing

Table 53 SPI Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0	5	ns
t_F	Input signal fall time	0	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

SPI slave interface timing

Table 54 SPI Slave Mode Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SPI_SCLK period	50		ns	
t_{ss}	required SPI_CS active to SPI_SCLK first edge	25		ns	
t_{sh}	required SPI_SCLK last edge to SPI_CS inactive	25		ns	
t_{od}	Delay time, SPI_SCLK active edge to SPI_MISO shifted		14.5	ns	
t_{oh}	Hold time, SPI_MISO valid after SPI_SCLK active edge	8.6		ns	

t_{ds}	required Setup time, SPI_MOSI valid before SPI_SCLK active edge	0		ns	
t_{dh}	required Hold time, SPI_MOSI valid after SPI_SCLK active edge	7.2		ns	

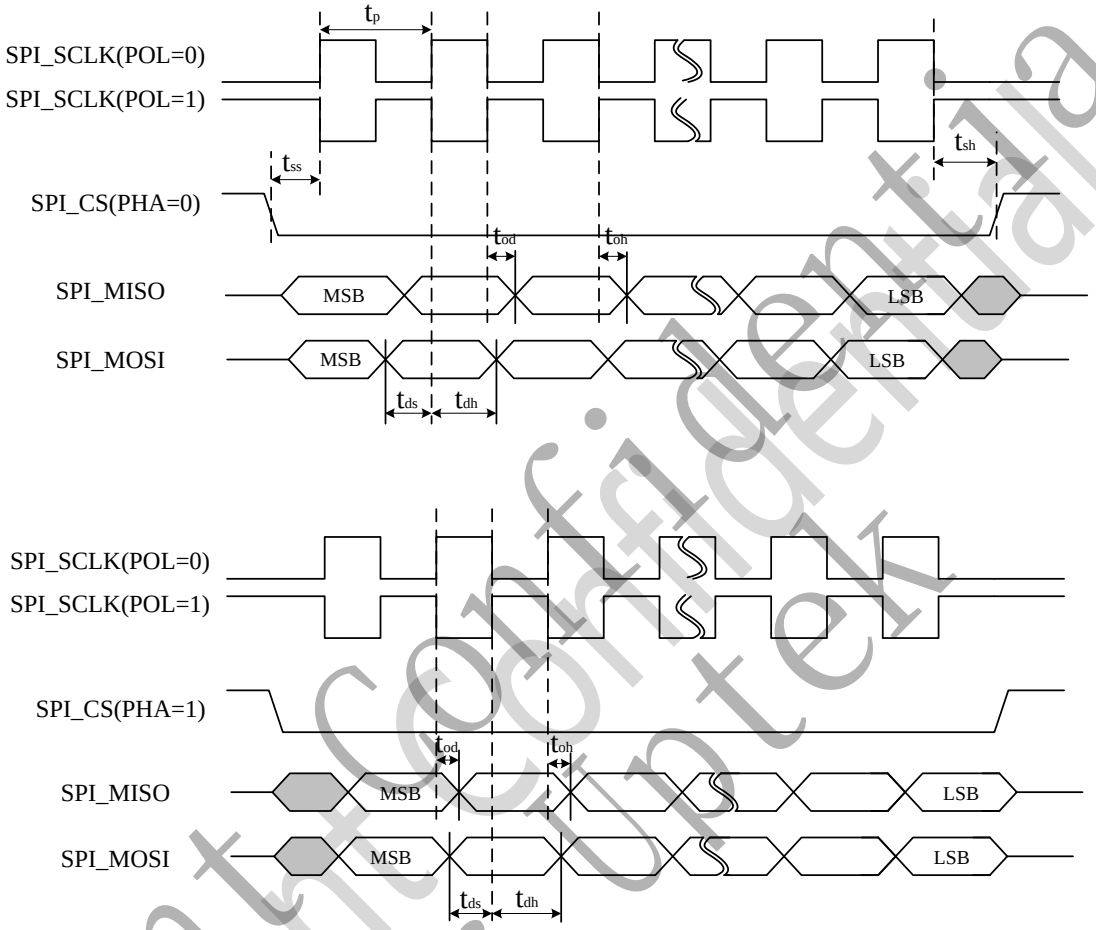


Figure 6 SPI Slave Mode Interface Timing

SPI master interface timing

Table 55 SPI Master Mode Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SPI_SCLK period	50		ns	
t_{ss}	SPI_CS active to SPI_SCLK first edge	23		ns	
t_{sh}	SPI_SCLK last edge to SPI_CS inactive	25		ns	
t_{od}	Delay time, SPI_SCLK active edge to SPI_MOSI shifted		2.5	ns	
t_{oh}	Hold time, SPI_MOSI valid after SPI_SCLK active edge	0.9		ns	
t_{ds}	required Setup time, SPI_MISO valid before SPI_SCLK active edge	9		ns	

t_{dh}	required Hold time, SPI_MISO valid after SPI_SCLK active edge	-2		ns	

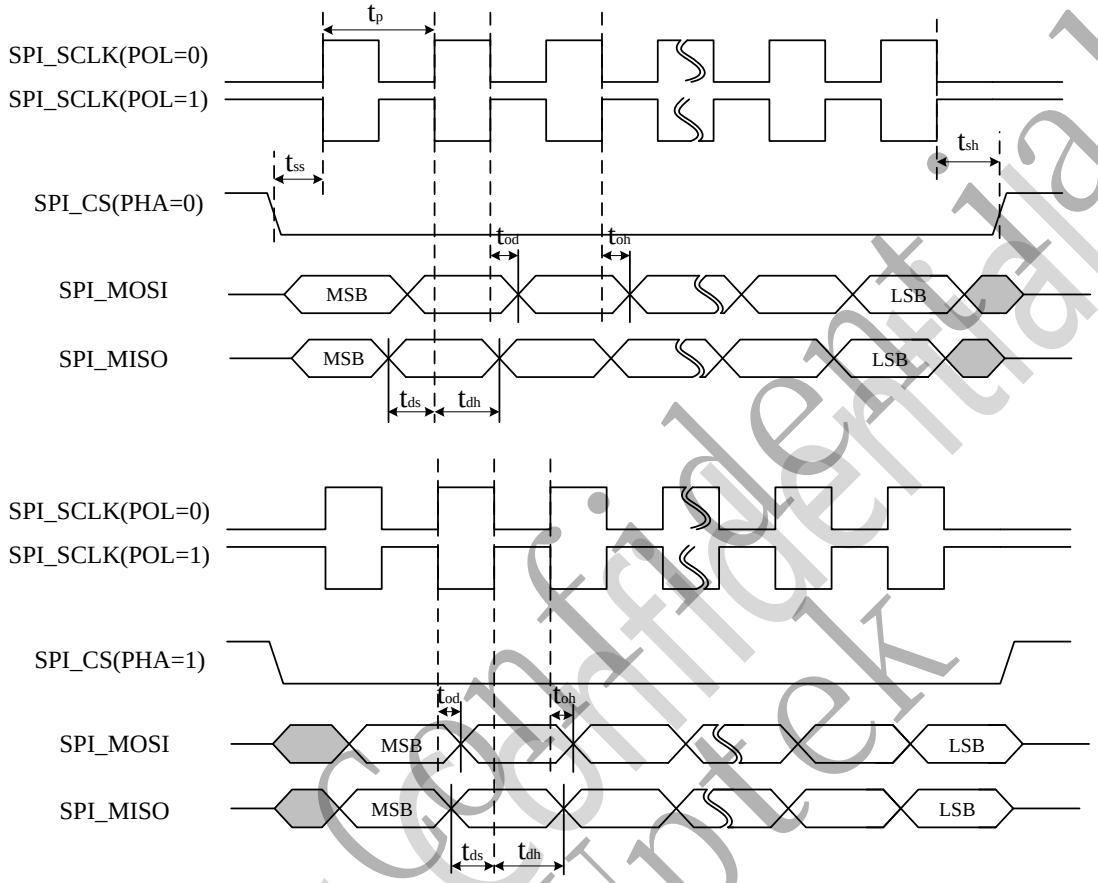


Figure 7 SPI Master Mode Interface Timing

6.3 I2C interface timing

Table 56 I2C Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0	5	ns
t_F	Input signal fall time	0	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

Table 57 I2C Interface Electrical Characteristics (Standard Mode)

Parameter		MIN	MAX	Unit	Notes
f_{SCL}	SCL clock frequency	0	100	kHZ	
t_{HIGH}	SCL high pulse width	4.0		us	
t_{LOW}	SCL low pulse width	4.7		us	

$t_{SU;STO}$	Setup time, SDA low to high when SCL high for stop bit	4.0		us	
$t_{HD;STA}$	Hold time, SDA high to low when SCL high for start bit	4.0		us	
t_{BUF}	I2C bus free time	4.7		us	
$T_{SU;DAT}$	SDA setup time	250		ns	
$T_{HD;DAT}$	SDA hold time	0		ns	

Table 58 I2C Interface Electrical Characteristics (Fast Mode)

Parameter		**MIN**	**MAX**	**Unit**	**Notes**
f_{SCL}	SCL clock frequency	0	400	kHZ	
t_{HIGH}	SCL high pulse width	0.6		us	
t_{LOW}	SCL low pulse width	1.3		us	
$t_{SU;STO}$	Setup time, SDA low to high when SCL high for stop bit	0.6		us	
$t_{HD;STA}$	Hold time, SDA high to low when SCL high for start bit	0.6		us	
t_{BUF}	I2C bus free time	1.3		us	
$T_{SU;DAT}$	SDA setup time	100		ns	
$T_{HD;DAT}$	SDA hold time	0		ns	

Table 59 I2C Interface Electrical Characteristics (High Speed Mode)

Parameter		**MIN**	**MAX**	**Unit**	**Notes**
f_{SCL}	SCL clock frequency	0	3.4	MHZ	
t_{HIGH}	SCL high pulse width	60		ns	
t_{LOW}	SCL low pulse width	160		ns	
$t_{SU;STO}$	Setup time, SDA low to high when SCL high for stop bit	160		ns	
$t_{HD;STA}$	Hold time, SDA high to low when SCL high for start bit	160		ns	
$T_{SU;DAT}$	SDA setup time	10		ns	
$T_{HD;DAT}$	SDA hold time	0	70	ns	

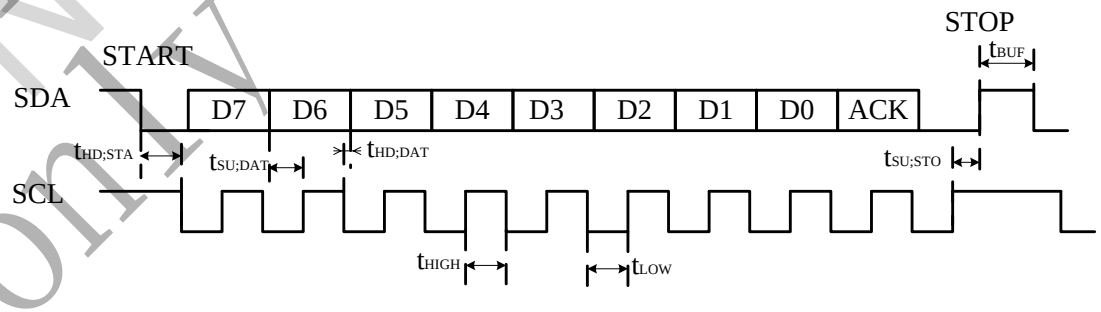


Figure 8 I2C Interface Timing

6.4 I2S Interface Timing

Table 60 I2S Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_R	Input signal fall time	0.5	5	ns
Output Conditions				
C_{load}	Output load capacitance		20	pf

Table 61 I2S Interface Electrical Characteristics

Parameter		MIN	MAX	Unit
t_{sck}	I2S SCK period	162	1953	ns
t_{wsdly}	Delay time, SCK active edge to WS transition	1	5	ns
t_{sdodly}	Delay time, SCK active edge to SDO transition	1	5	ns
t_{sdist}	SDI setup time	2	8	ns
t_{sdihd}	SDI hold time	1	9	ns

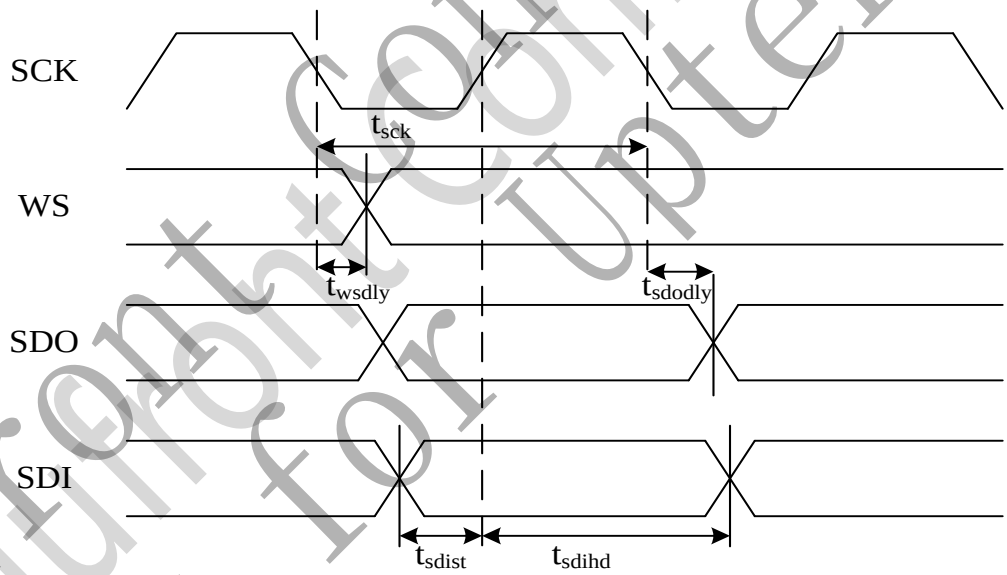


Figure 9 I2S Interface Timing

6.5 LCD Interface Timing

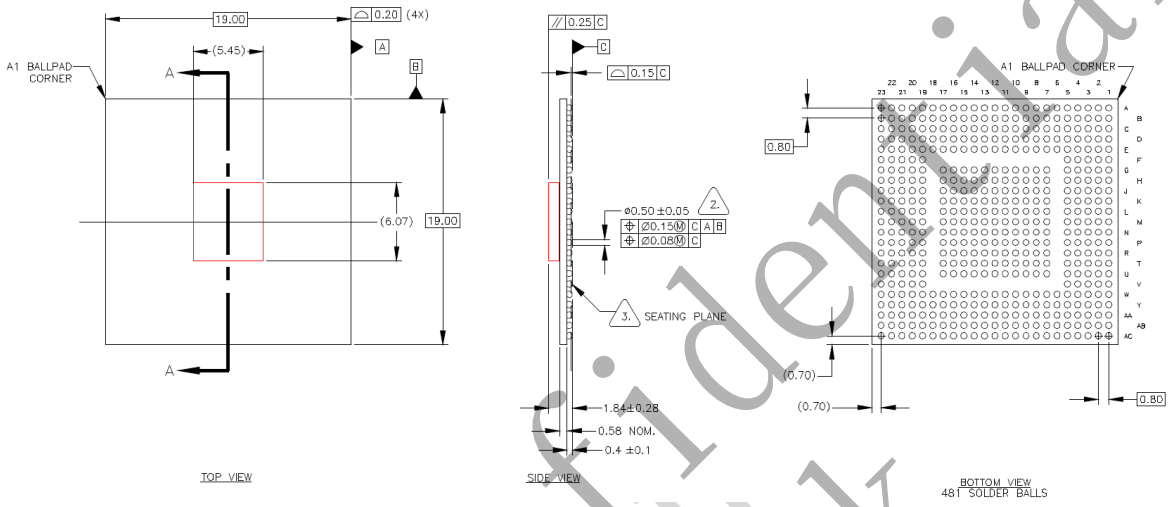
Table 62 LCD Interface Electrical Characteristics

Parameter	Min	Max	Unit	Note
Pixel Clock Period	6.734	-	ns	-
Pixel Clock Duty	45%	55%	ns	-

Setup time: Data valid to clock rising edge	-	2.5	ns	-
Setup time: Data valid to clock falling edge	-	3.0	ns	-
Hold time: Data valid after pixel clock rising edge	0.8	-	ns	-
Hold time: Data valid after pixel clock falling edge	0.8	-	ns	-

Chapter 7 Ballout and Package Information

7.1 Package Information



4. REFERENCE SPECIFICATIONS:
   A. AWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE
   B. AWW SPEC #001-0519-2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 10 Package Information

Table 63 Package Parameters

Package Type	Body X	Body Y	Body Z
FCBGA	19.00	19.00	1.84 NOM
Ball Pitch	**RAW Ball Size**	**Ball Count**	**Ball Matrix**
0.80	0.50	481	23x23

Note: Unless otherwise specified, dimensions are in millimeters.

7.2 Thermal Information

TBD

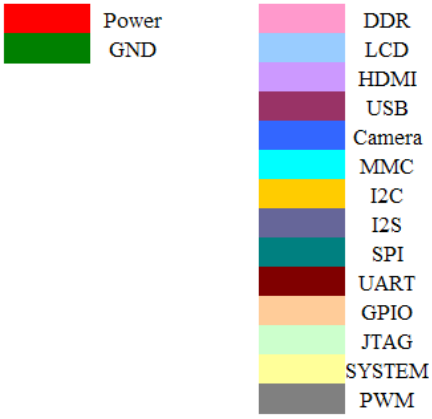
7.3 Reflow Profile

TBD

7.4 Ball Location

Note: package body size:19mmx19mm
Note: ball pitch 0.8mm, ball size 0.5mm
Note: TOP view(Die face down)

Legend



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	GND	GND	VDDIO_DDR	ddr_ds3n	ddr_dm3	sda2	scl2	GND	sda3	uart0_rxd	uart0_txd	irda_txd	irda_rxd	GND	i2s0_sdo	i2s0_ws1	i2s0_sck1	spi0_mosi	spi0_cs_n	GND	GPIO26	GND	GND
B	GND	GND	ddr_dq31	ddr_ds3p	ddr_dq29	GND	pwm0	pwm1	scl3	tdi	uart0_rts	uart1_cts	hs_uart2_rts	VDDIO_GPIO	i2s0_sdi	sda1	spi0_miso	spi0_clk	GPIO22	VDDIO_GPIO	VDDIO_GPIO	GND	GND
C	ddr_dq26	ddr_dq27	ddr_dq30	ddr_dq28	ddr_dq25	VDDIO_DDR	GPIO5	GPIO2	tms	trst	uart0_cts	uart1_rxd	hs_uart2_cts	hs_uart3_rts	i2s0_sck0	scl1	spi1_miso	spi1_clk	GPIO21	GPIO23	GPIO24	VDDIO_GPIO	GPIO25
D	ddr_ds2p	ddr_ds2n	GND	VDDIO_DDR	ddr_dq24	GPIO7	GPIO4	GPIO1	tdo	VDDIO_GPIO	GND	uart1_txd	hs_uart2_txd	hs_uart3_cts	i2s0_ws0	sda0	GND	spi1_cs_n	GPIO16	GPIO17	GPIO18	GPIO19	GPIO20
E	GND	VDDIO_DDR	ddr_dq21	ddr_dm2	ddr_dq23	GPIO6	GPIO3	GPIO0	VDDIO_GPIO	jtag_mode	tck	uart1_rts	hs_uart2_rxd	hs_uart3_txd	hs_uart3_rxd	scl0	VDDIO_GPIO	spi1_mosi	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15
F	ddr_dq18	ddr_dq19	ddr_dq17	ddr_dq20	ddr_dq22														VDDIO_LCD	GND	GPIO8	GPIO9	GPIO10
G	ddr_ba1	ddr_ba0	GND	VDDIO_DDR	ddr_dq16		GND	GND	GND	GND	GND	VDD_CPU	GND	GND	GND	GND	GND		lcd_sync	lcd_de	lcd_hsync	lcd_vsync	lcd_pclk
H	GND	VDDIO_DDR	ddr_ca15	ddr_ca14	ddr_ba2		GND	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	GND	VDDIO_GPIO	VDD_CORE	VDD_CORE	VDD_MALI	GND		lcd_data4	lcd_data3	lcd_data2	lcd_data1	lcd_data0
J	ddr_ca11	ddr_ca12	ddr_ca10	ddr_ca13	ddr_ca9		GND	VDD_CPU	GND	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CORE	VDD_CORE	GND	VDD_MALI	GND		lcd_data7	lcd_data6	lcd_data5	VDDIO_LCD	GND
K	ddr_ca8	ddr_ca6	GND	VDDIO_DDR	ddr_ca5		GND	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	GND	VDD_CORE	VDD_CORE	VDD_CORE	VDD_MALI	GND		lcd_data12	lcd_data11	lcd_data10	lcd_data9	lcd_data8
L	GND	VDDIO_DDR	ddr_ca1	ddr_ca4	ddr_ca7		GND	VDDIO_DDR	VDD_CORE	VDD_CPU	GND	GND	GND	VDD_CORE	VDD_ENC	VDD_MALI	GND		lcd_data17	lcd_data16	lcd_data15	lcd_data14	lcd_data13
M	ddr_ca3	ddr_ca2	ddr_cs1_n	ddr_ca0	VREF_DDR		VDDIO_DDR	GND	VDD_CPU_RAM	GND	GND	GND	GND	GND	VDD_ENC	GND	VDD_CORE		VDDIO_LCD	GND	lcd_data20	lcd_data19	lcd_data18
N	ddr_ck_c	ddr_ck_t	ddr_zq	VDDIO_DDR	GND		GND	VDDIO_DDR	VDD_CPU_RAM	VDD_CORE	GND	GND	GND	VDD_CORE	VDD_ZSP	VDD_ZSP	GND		mmc0_dat2	mmc0_clk	lcd_data23	lcd_data22	lcd_data21
P	GND	VDDIO_DDR	ddr_cas_n	ddr_ras_n	ddr_odt0		GND	VDDIO_DDR	VDD_CORE	VDD_DEC	VDD_2D	GND	VDD_CORE	VDD_ISP	VDD_ISP	VDD_CORE	GND		mmc0_dat3	mmc0_cmd	mmc0_dat0	mmc0_dat1	mmc0_wp
R	ddr_cke	ddr_odt1	ddr_retention	ddr_rst_n	ddr_dq15		GND	VDDIO_DDR	GND	VDD_DEC	VDD_2D	VDD_CORE	VDD_CORE	AVDD_FUSE	GND	VDDL_USB	GND		GND	mmc0_psw	mmc0_cd_n	VDDIO_GPIO	GND
T	ddr_cs0_n	ddr_we_n	GND	VDDIO_DDR	ddr_dq14		GND	VDDIO_DDR	VDD_WAKEUP	VDD_CORE	VDD_CORE	GND	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	GND		VDDIO_GPIO	mmc1_dat0	mmc1_dat5	mmc1_dat4	mmc1_clk
U	GND	VDDIO_DDR	ddr_dm1	ddr_dq13	ddr_dq12		GND	GND	GND	GND	GND	VDD_CORE	GND	GND	GND	GND	GND		mmc2_dat0	mmc2_dat1	mmc1_dat1	mmc1_dat6	mmc1_cmd
V	ddr_ds1p	ddr_dq8	ddr_dq9	ddr_dq10	ddr_dq11														VDDIO_GPIO	GND	mmc2_dat2	mmc1_dat2	mmc1_dat7
W	ddr_ds1n	ddr_dq7	GND	VDDIO_DDR	ddr_dq5	sysclk_32k	chip_mode_0	wakeup_gpio4	wakeup_gpio2	wakeup_gpio0	wakeup_gpio6	GND	hdmi_ext_swing	GND	AVDD_usb	cam_data7	cam_data8	AVDD_hsic	cam_data9	alt_clk0	alt_clk1	mmc2_dat3	mmc1_dat3
Y	GND	VDDIO_DDR	ddr_dq6	ddr_dq3	ddr_dq4	GND	chip_mode_1	sus_s3_ack_n	wakeup_gpio3	wakeup_gpio1	wakeup_gpio7	VDDIO_WAKEUP	hdmi_hpd	usb0_vres	GND	hsic_strobe	cam_data2	AVSS_HSIC	cam_data3	cam_data4	cam_data10	mmc2_cmd	mmc2_clk
AA	ddr_ds0n	ddr_ds0p	ddr_dm0	ddr_dq1	ddr_dq2	pwrok	chip_mode_2	sus_s3_n	GND	mclk	hdmi_cec	hdmi_ddc_scl	hdmi_ddc_sda	usb1_vres	GND	hsic_data	cam_pclk	cam_vsync	cam_hsync	cam_data5	cam_data6	VDDIO_GPIO	cam_data11
AB	GND	GND	VDDIO_DDR	GND	ddr_dq0	AVDD_PLL4	AVDD_PLL3	AVDD_PLL2	wakeup_gpio5	VDDIO_WAKEUP	hdmi_data2_n	hdmi_data1_n	AVDD_hdmi	hdmi_data0_n	hdmi_clock_n	usb1_vbus	usb1_padm	usb0_vbus	usb0_padm	VDDIO_ISP	cam_data1	GND	GND
AC	GND	GND	sysclk_12m_in	sysclk_12m_out	AVSS_PLL	AVDD_PLL6	AVDD_PLL5	AVDD_PLL1	AVDD_PLL0	GND	hdmi_data2_p	hdmi_data1_p	GND	hdmi_data0_p	hdmi_clock_p	GND	usb1_padp	AVSS_USB	usb0_padp	GND	cam_data0	GND	GND

Figure 11 Ball Location Mapping

Table 64 Ball Location Mapping table

Ball Location	Ball Name	Ball Location	Ball Name
W20	alt_clk0	AA11	hdmi_cec
W21	alt_clk1	AC15	hdmi_clock_p
R14	AVDD_FUSE	AB15	hdmi_clock_n
AB13	AVDD_hdmi	AB14	hdmi_data0_p
W18	AVDD_hsic	AC14	hdmi_data0_n
AC9	AVDD_PLL0	AB12	hdmi_data1_p
AC8	AVDD_PLL1	AC12	hdmi_data1_n
AB8	AVDD_PLL2	AB11	hdmi_data2_p
AB7	AVDD_PLL3	AC11	hdmi_data2_n
AB6	AVDD_PLL4	AA13	hdmi_ddc_scl
AC7	AVDD_PLL5	AA12	hdmi_ddc_sda
AC6	AVDD_PLL6	W13	hdmi_ext_swing
W15	AVDD_usb	Y13	hdmi_hpd
Y18	AVSS_HSIC	C13	hs_uart2_cts
AC5	AVSS_PLL	B13	hs_uart2_rts
AC18	AVSS_USB	E13	hs_uart2_rxd
AC21	cam_data0	D13	hs_uart2_txd
AB21	cam_data1	D14	hs_uart3_cts
Y21	cam_data10	C14	hs_uart3_rts
AA23	cam_data11	E15	hs_uart3_rxd
Y17	cam_data2	E14	hs_uart3_txd
Y19	cam_data3	AA16	hsic_data
Y20	cam_data4	Y16	hsic_strobe
AA20	cam_data5	C15	i2s0_sck0
AA21	cam_data6	A17	i2s0_sck1
W16	cam_data7	B15	i2s0_sdi
W17	cam_data8	A15	i2s0_sdo
W19	cam_data9	D15	i2s0_ws0
AA19	cam_hsync	A16	i2s0_ws1
AA17	cam_pclk	A13	irda_rxd
AA18	cam_vsync	A12	irda_txd
W7	chip_mode_0	E10	jtag_mode
Y7	chip_mode_1	H23	lcd_data0
AA7	chip_mode_2	H22	lcd_data1
G2	ddr_ba0	K21	lcd_data10
G1	ddr_ba1	K20	lcd_data11
H5	ddr_ba2	K19	lcd_data12
M4	ddr_ca0	L23	lcd_data13
L3	ddr_ca1	L22	lcd_data14

J3	ddr_ca10	L21	lcd_data15
J1	ddr_ca11	L20	lcd_data16
J2	ddr_ca12	L19	lcd_data17
J4	ddr_ca13	M23	lcd_data18
H4	ddr_ca14	M22	lcd_data19
H3	ddr_ca15	H21	lcd_data2
M2	ddr_ca2	M21	lcd_data20
M1	ddr_ca3	N23	lcd_data21
L4	ddr_ca4	N22	lcd_data22
K5	ddr_ca5	N21	lcd_data23
K2	ddr_ca6	H20	lcd_data3
L5	ddr_ca7	H19	lcd_data4
K1	ddr_ca8	J21	lcd_data5
J5	ddr_ca9	J20	lcd_data6
P3	ddr_cas_n	J19	lcd_data7
N1	ddr_ck_c	K23	lcd_data8
N2	ddr_ck_t	K22	lcd_data9
R1	ddr_cke	G20	lcd_de
T1	ddr_cs0_n	G21	lcd_hsync
M3	ddr_cs1_n	G23	lcd_pclk
AA3	ddr_dm0	G19	lcd_sync
U3	ddr_dm1	G22	lcd_vsync
E4	ddr_dm2	AA10	mclk
A5	ddr_dm3	R21	mmc0_cd_n
AB5	ddr_dq0	N20	mmc0_clk
AA4	ddr_dq1	P20	mmc0_cmd
V4	ddr_dq10	P21	mmc0_dat0
V5	ddr_dq11	P22	mmc0_dat1
U5	ddr_dq12	N19	mmc0_dat2
U4	ddr_dq13	P19	mmc0_dat3
T5	ddr_dq14	R20	mmc0_psw
R5	ddr_dq15	P23	mmc0_wp
G5	ddr_dq16	T23	mmc1_clk
F3	ddr_dq17	U23	mmc1_cmd
F1	ddr_dq18	T20	mmc1_dat0
F2	ddr_dq19	U21	mmc1_dat1
AA5	ddr_dq2	V22	mmc1_dat2
F4	ddr_dq20	W23	mmc1_dat3
E3	ddr_dq21	T22	mmc1_dat4
F5	ddr_dq22	T21	mmc1_dat5
E5	ddr_dq23	U22	mmc1_dat6
D5	ddr_dq24	V23	mmc1_dat7

C5	ddr_dq25	Y23	mmc2_clk
C1	ddr_dq26	Y22	mmc2_cmd
C2	ddr_dq27	U19	mmc2_dat0
C4	ddr_dq28	U20	mmc2_dat1
B5	ddr_dq29	V21	mmc2_dat2
Y4	ddr_dq3	W22	mmc2_dat3
C3	ddr_dq30	B7	pwm0
B3	ddr_dq31	B8	pwm1
Y5	ddr_dq4	AA6	pwrok
W5	ddr_dq5	E16	scl0
Y3	ddr_dq6	C16	scl1
W2	ddr_dq7	A7	scl2
V2	ddr_dq8	B9	scl3
V3	ddr_dq9	D16	sda0
AA1	ddr_ds0n	B16	sda1
AA2	ddr_ds0p	A6	sda2
W1	ddr_ds1n	A9	sda3
V1	ddr_ds1p	B18	spi0_clk
D2	ddr_ds2n	A19	spi0_cs_n
D1	ddr_ds2p	B17	spi0_miso
A4	ddr_ds3n	A18	spi0_mosi
B4	ddr_ds3p	C18	spi1_clk
P5	ddr_odt0	D18	spi1_cs_n
R2	ddr_odt1	C17	spi1_miso
P4	ddr_ras_n	E18	spi1_mosi
R3	ddr_retention	Y8	sus_s3_ack_n
R4	ddr_rst_n	AA8	sus_s3_n
T2	ddr_we_n	AC3	sysclk_12m_xi
N3	ddr_zq	AC4	sysclk_12m_xo
A1	GND	W6	sysclk_32k
A2	GND	E11	tck
A8	GND	B10	tdi
A14	GND	D9	tdo
A20	GND	C9	tms
A22	GND	C10	trst
A23	GND	C11	uart0_cts
B1	GND	B11	uart0_rts
B2	GND	A10	uart0_rxd
B6	GND	A11	uart0_txd
B22	GND	B12	uart1_cts
B23	GND	E12	uart1_rts
D3	GND	C12	uart1_rxd

D11	GND	D12	uart1_txd
D17	GND	AB19	usb0_padm
E1	GND	AC19	usb0_padp
F20	GND	AB18	usb0_vbus
G3	GND	Y14	usb0_vres
G7	GND	AB17	usb1_padm
G8	GND	AC17	usb1_padp
G9	GND	AB16	usb1_vbus
G10	GND	AA14	usb1_vres
G11	GND	P11	VDD_2D
G13	GND	R11	VDD_2D
G14	GND	H14	VDD_CORE
G15	GND	H15	VDD_CORE
G16	GND	J13	VDD_CORE
G17	GND	J14	VDD_CORE
H1	GND	K13	VDD_CORE
H7	GND	K14	VDD_CORE
H12	GND	K15	VDD_CORE
H17	GND	L9	VDD_CORE
J7	GND	L14	VDD_CORE
J9	GND	M17	VDD_CORE
J15	GND	N10	VDD_CORE
J17	GND	N14	VDD_CORE
J23	GND	P9	VDD_CORE
K3	GND	P13	VDD_CORE
K7	GND	P16	VDD_CORE
K12	GND	R12	VDD_CORE
K17	GND	R13	VDD_CORE
L1	GND	T10	VDD_CORE
L7	GND	T11	VDD_CORE
L11	GND	T13	VDD_CORE
L12	GND	T14	VDD_CORE
L13	GND	T15	VDD_CORE
L17	GND	T16	VDD_CORE
M8	GND	U12	VDD_CORE
M10	GND	G12	VDD_CPU
M11	GND	H8	VDD_CPU
M12	GND	H9	VDD_CPU
M13	GND	H10	VDD_CPU
M14	GND	H11	VDD_CPU
M16	GND	J8	VDD_CPU
M20	GND	J10	VDD_CPU

N5	GND	J11	VDD_CPU
N7	GND	J12	VDD_CPU
N11	GND	K8	VDD_CPU
N12	GND	K9	VDD_CPU
N13	GND	K10	VDD_CPU
N17	GND	K11	VDD_CPU
P1	GND	L10	VDD_CPU
P7	GND	M9	VDD_CPU_RAM
P12	GND	N9	VDD_CPU_RAM
P17	GND	P10	VDD_DEC
R7	GND	R10	VDD_DEC
R9	GND	L15	VDD_ENC
R15	GND	M15	VDD_ENC
R17	GND	P14	VDD_ISP
R19	GND	P15	VDD_ISP
R23	GND	H16	VDD_MALI
T3	GND	J16	VDD_MALI
T7	GND	K16	VDD_MALI
T12	GND	L16	VDD_MALI
T17	GND	T9	VDD_WAKEUP
U1	GND	N15	VDD_ZSP
U7	GND	N16	VDD_ZSP
U8	GND	A3	VDDIO_DDR
U9	GND	C6	VDDIO_DDR
U10	GND	D4	VDDIO_DDR
U11	GND	E2	VDDIO_DDR
U13	GND	G4	VDDIO_DDR
U14	GND	H2	VDDIO_DDR
U15	GND	K4	VDDIO_DDR
U16	GND	L2	VDDIO_DDR
U17	GND	L8	VDDIO_DDR
V20	GND	M7	VDDIO_DDR
W3	GND	N4	VDDIO_DDR
W12	GND	N8	VDDIO_DDR
W14	GND	P2	VDDIO_DDR
Y1	GND	P8	VDDIO_DDR
Y6	GND	R8	VDDIO_DDR
Y15	GND	T4	VDDIO_DDR
AA9	GND	T8	VDDIO_DDR
AA15	GND	U2	VDDIO_DDR
AB1	GND	W4	VDDIO_DDR
AB2	GND	Y2	VDDIO_DDR

AB4	GND
AB22	GND
AB23	GND
AC1	GND
AC2	GND
AC10	GND
AC13	GND
AC16	GND
AC20	GND
AC22	GND
AC23	GND
E8	GPIO0
D8	GPIO1
F23	GPIO10
E19	GPIO11
E20	GPIO12
E21	GPIO13
E22	GPIO14
E23	GPIO15
D19	GPIO16
D20	GPIO17
D21	GPIO18
D22	GPIO19
C8	GPIO2
D23	GPIO20
C19	GPIO21
B19	GPIO22
C20	GPIO23
C21	GPIO24
C23	GPIO25
A21	GPIO26
E7	GPIO3
D7	GPIO4
C7	GPIO5
E6	GPIO6
D6	GPIO7
F21	GPIO8
F22	GPIO9

AB3	VDDIO_DDR
B14	VDDIO_GPIO
B20	VDDIO_GPIO
B21	VDDIO_GPIO
C22	VDDIO_GPIO
D10	VDDIO_GPIO
E17	VDDIO_GPIO
H13	VDDIO_GPIO
R22	VDDIO_GPIO
V19	VDDIO_GPIO
AA22	VDDIO_GPIO
T19	VDDIO_GPIO2
E9	VDDIO_GPIO3
AB20	VDDIO_ISP
F19	VDDIO_LCD
J22	VDDIO_LCD
M19	VDDIO_LCD
Y12	VDDIO_WAKEUP
AB10	VDDIO_WAKEUP33
R16	VDDL_USB
M5	VREF_DDR
W10	wakeup_gpio0
Y10	wakeup_gpio1
W9	wakeup_gpio2
Y9	wakeup_gpio3
W8	wakeup_gpio4
AB9	wakeup_gpio5
W11	wakeup_gpio6
Y11	wakeup_gpio7