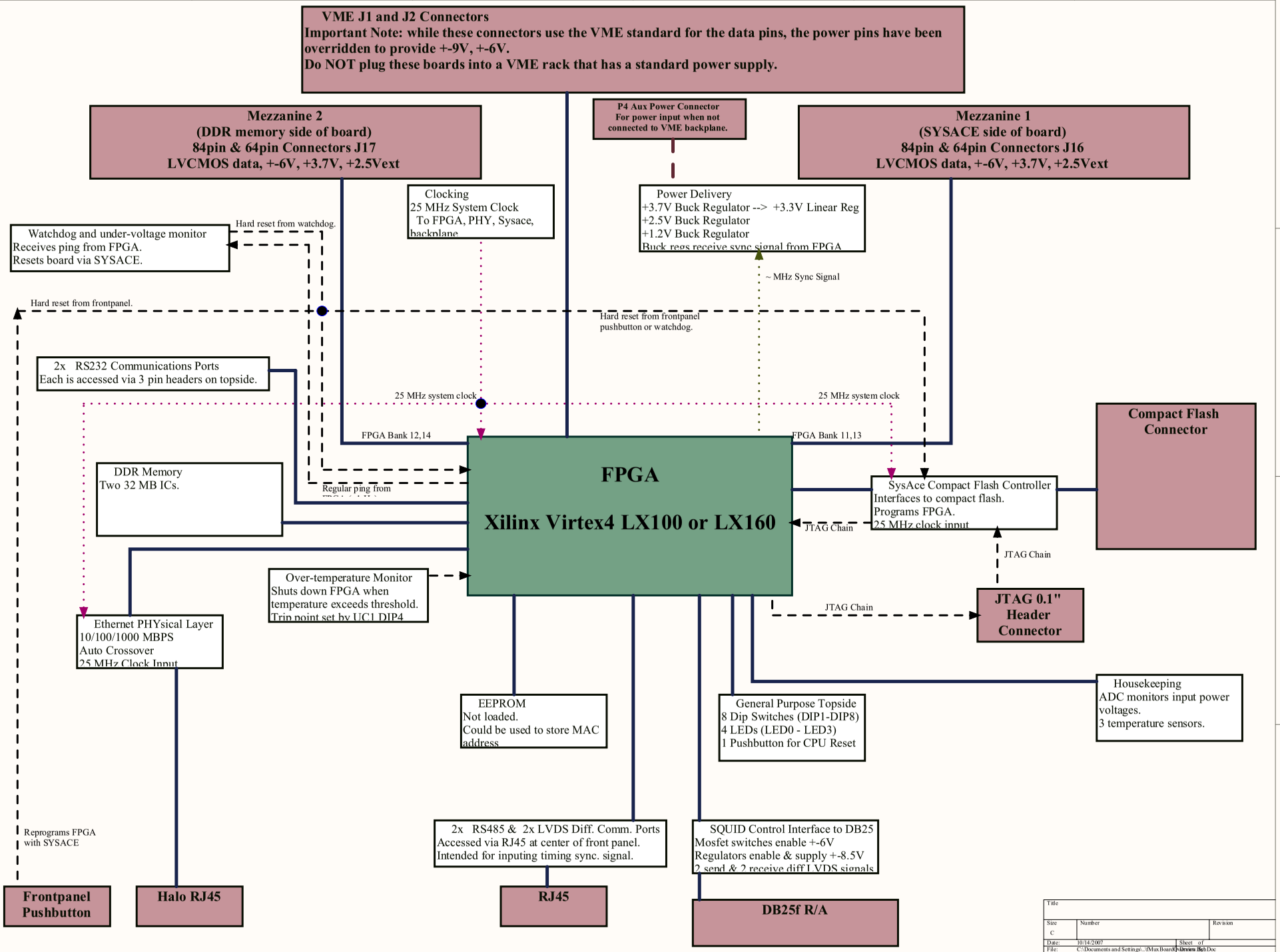
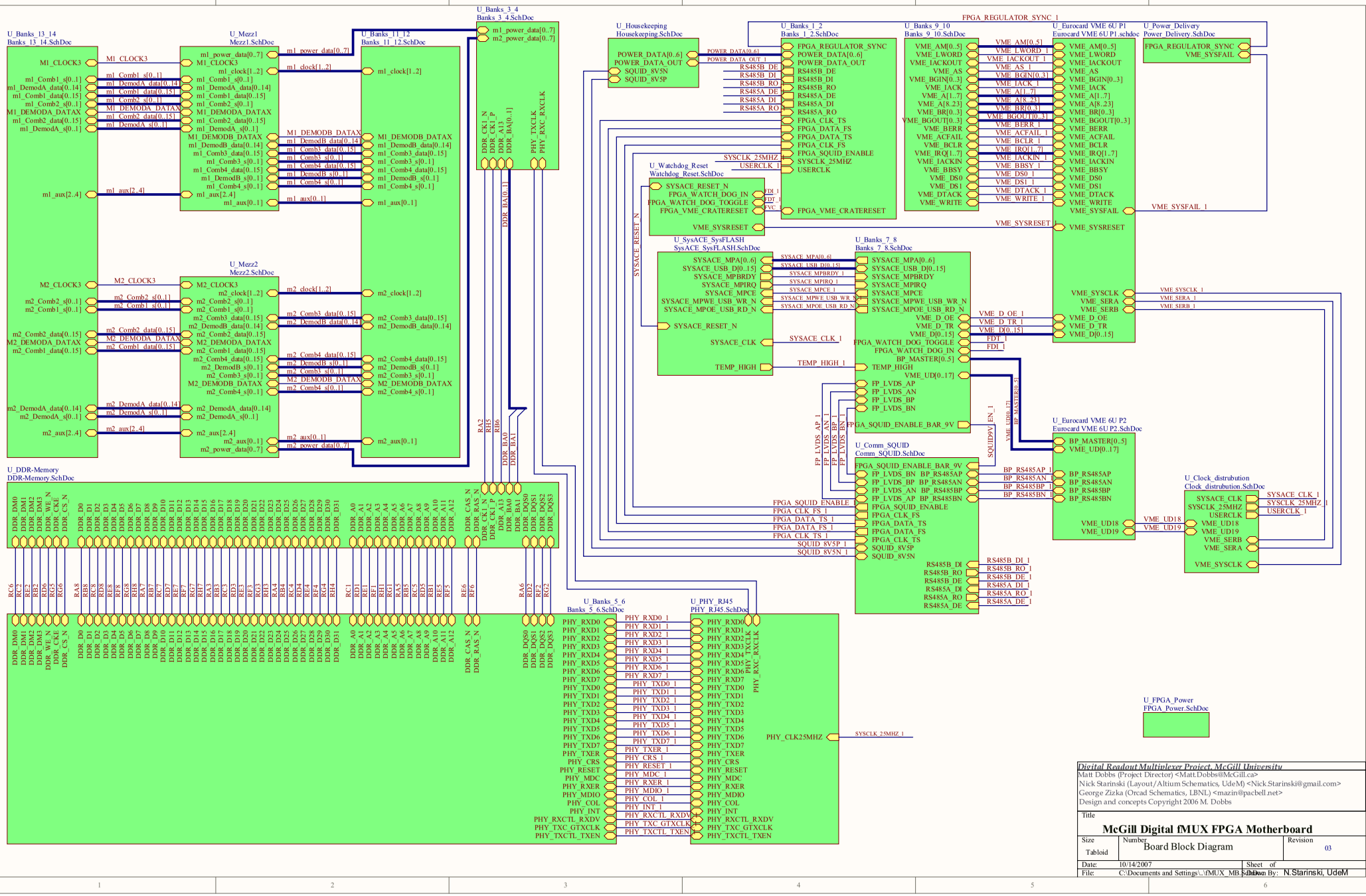

VME J1 and J2 Connectors
Important Note: while these connectors use the VME standard for the data pins, the power pins have been overridden to provide +-9V, +-6V.
Do NOT plug these boards into a VME rack that has a standard power supply.
Mezzanine 2
(DDR memory side of board)
84pin & 64pin Connectors J17
LVCMOS data, +-6V, +3.7V, +2.5Vext
P4 Aux Power Connector
For power input when not connected to VME backplane.
Mezzanine 1
(SYSACE side of board)
84pin & 64pin Connectors J16
LVCMOS data, +-6V, +3.7V, +2.5Vext
Clocking
25 MHz System Clock
To FPGA, PHY, Sysace, backplane
Power Delivery
+3.7V Buck Regulator --> +3.3V Linear Reg
+2.5V Buck Regulator
+1.2V Buck Regulator
Buck regs receive sync signal from FPGA
Watchdog and under-voltage monitor
Receives ping from FPGA.
Resets board via SYSACE.
Hard reset from watchdog.
~ MHz Sync Signal
Hard reset from frontpanel.
Hard reset from frontpanel pushbutton or watchdog.
2x RS232 Communications Ports
Each is accessed via 3 pin headers on topside.
25 MHz system clock
25 MHz system clock
FPGA Bank 12,14
FPGA Bank 11,13
Compact Flash Connector
DDR Memory
Two 32 MB ICs.
Regular ping from
FPGA
Xilinx Virtex4 LX100 or LX160
SysAce Compact Flash Controller
Interfaces to compact flash.
Programs FPGA.
25 MHz clock input
JTAG Chain
JTAG Chain
Over-temperature Monitor
Shuts down FPGA when temperature exceeds threshold.
Trip point set by UC1 DIP4
JTAG Chain
JTAG 0.1" Header Connector
Ethernet PHYsical Layer
10/100/1000 MBPS
Auto Crossover
25 MHz Clock Input
Housekeeping
ADC monitors input power voltages.
3 temperature sensors.
EEPROM
Not loaded.
Could be used to store MAC address
General Purpose Topside
8 Dip Switches (DIP1-DIP8)
4 LEDs (LED0 - LED3)
1 Pushbutton for CPU Reset
Reprograms FPGA with SYSACE
2x RS485 & 2x LVDS Diff. Comm. Ports
Accessed via RJ45 at center of front panel.
Intended for inputing timing sync. signal.
SQUID Control Interface to DB25
Mosfet switches enable +-6V
Regulators enable & supply +-8.5V
2 send & 2 receive diff LVDS signals
Frontpanel Pushbutton
Halo RJ45
RJ45
DB25f R/A
Title
Size
C
Number
Revision
Date: 10/14/2007
Sheet of
File: C:\Documents and Settings\...\MuxBoard\Drawing.SchDoc
Drawn By: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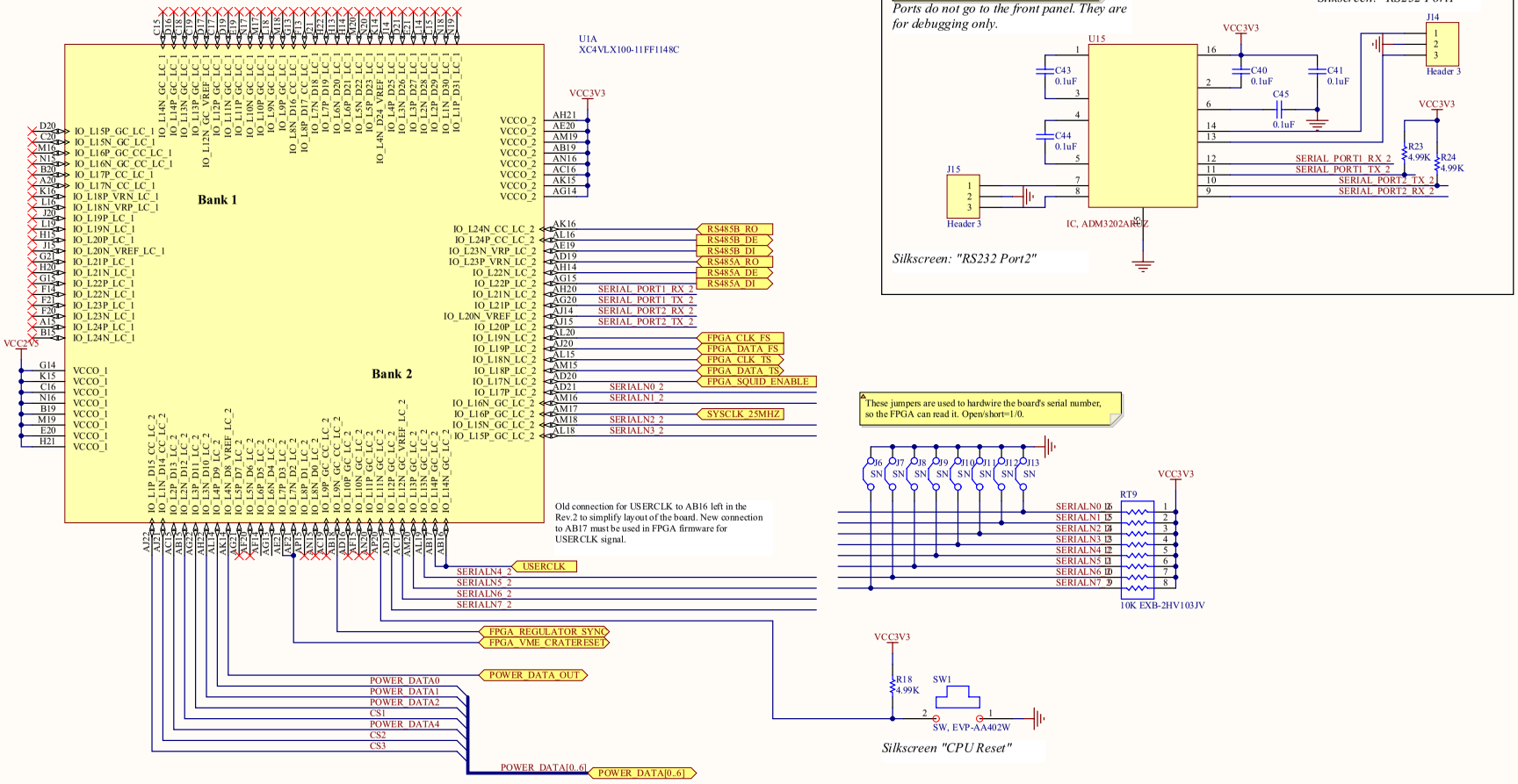
Banks_13_14.SchDoc
U_Mezz1
Mezz1.SchDoc
U_Banks_11_12
Banks_11_12.SchDoc
U_Banks_3_4
Banks_3_4.SchDoc
U_Housekeeping
Housekeeping.SchDoc
U_Banks_1_2
Banks_1_2.SchDoc
FPGA_REGULATOR_SYNC_1
U_Banks_9_10
Banks_9_10.SchDoc
U_Eurocard VME 6U P1
Eurocard VME 6U P1.schdoc
U_Power_Delivery
Power_Delivery.SchDoc
U_Watchdog_Reset
Watchdog_Reset.SchDoc
U_SysACE_SysFLASH
SysACE_SysFLASH.SchDoc
U_Banks_7_8
Banks_7_8.SchDoc
U_Mezz2
Mezz2.SchDoc
U_Eurocard VME 6U P2
Eurocard VME 6U P2.SchDoc
U_DDR-Memory
DDR-Memory.SchDoc
U_Comm_SQUID
Comm_SQUID.SchDoc
U_Clock_distrubution
Clock_distrubution.SchDoc
U_Banks_5_6
Banks_5_6.SchDoc
U_PHY_RJ45
PHY_RJ45.SchDoc
U_FPGA_Power
FPGA_Power.SchDoc
Digital Readout Multiplexer Project, McGill University
Matt Dobbs (Project Director) <Matt.Dobbs@McGill.ca>
Nick Starinski (Layout/Altium Schematics, UdeM) <Nick.Starinski@gmail.com>
George Zizka (Orcad Schematics, LBNL) <mazin@pacbell.net>
Design and concepts Copyright 2006 M. Dobbs
Title
McGill Digital fMUX FPGA Motherboard
Size
Tabloid
Number
Board Block Diagram
Revision
03
Date: 10/14/2007
Sheet of
File: C:\Documents and Settings\...\fMUX_MB.SchDoc
Drawn By: N.Starinski, UdeM



Title	**McGill Digital fMUX FPGA Motherboard**	
Size: Tabloid	Number: Banks 1, 2 and RS232	Revision: 03
Date: 10/14/2007	Sheet of	
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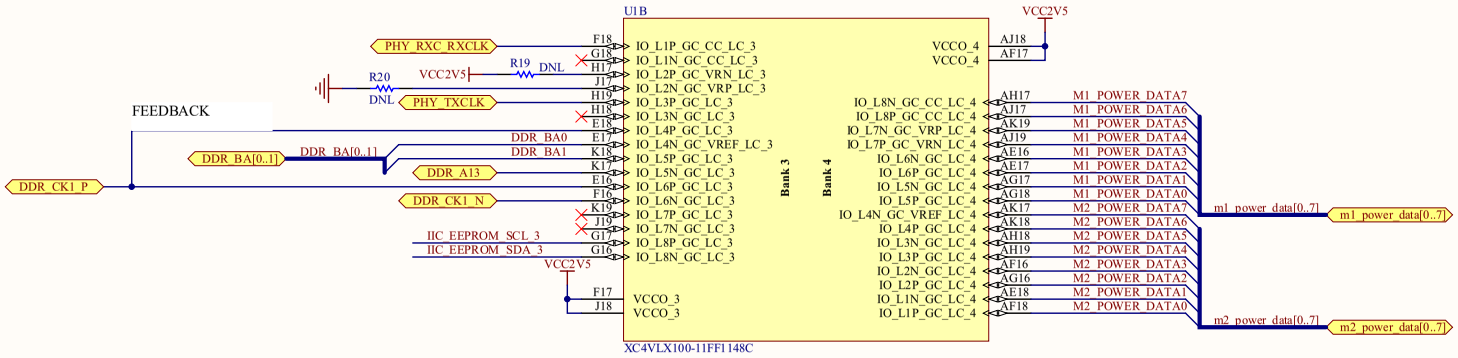
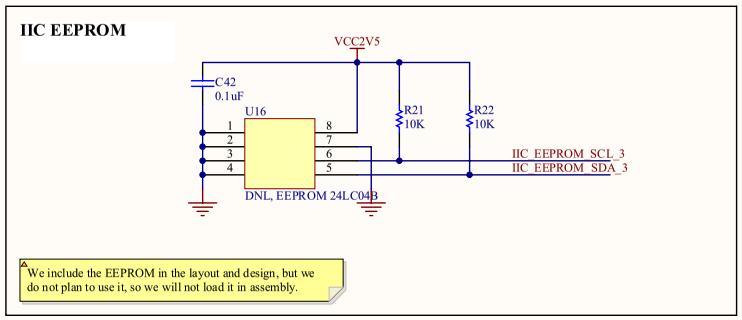
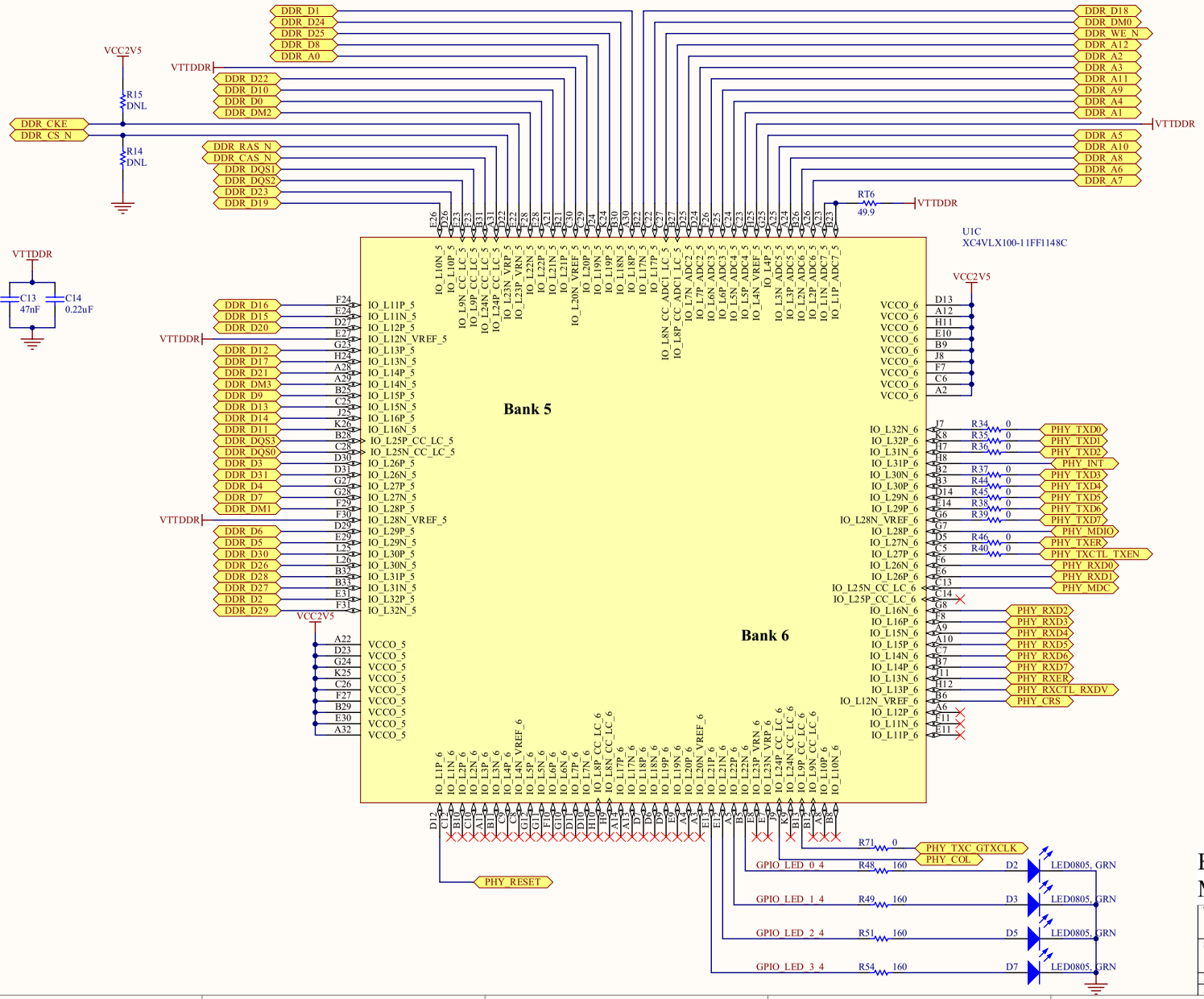


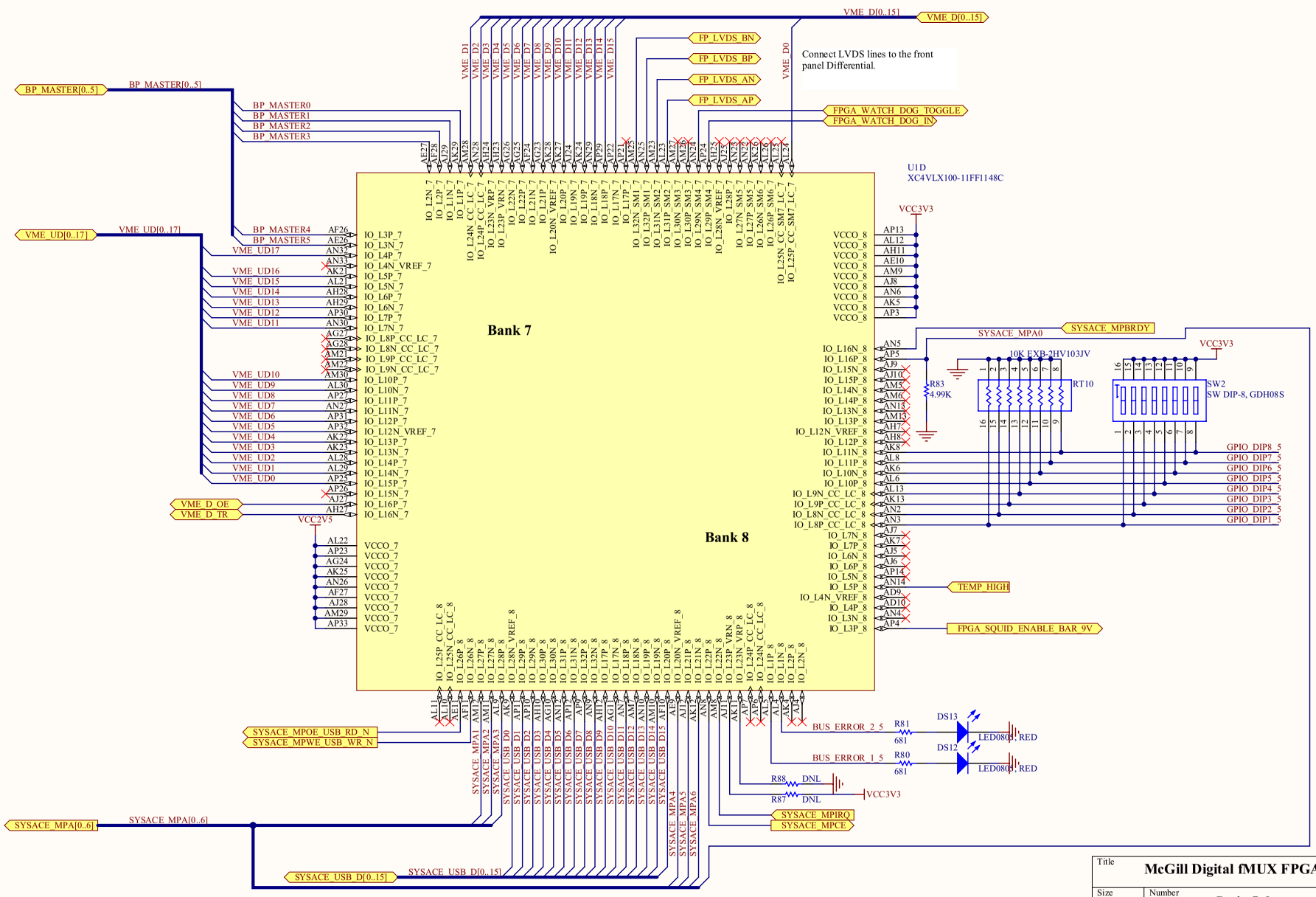


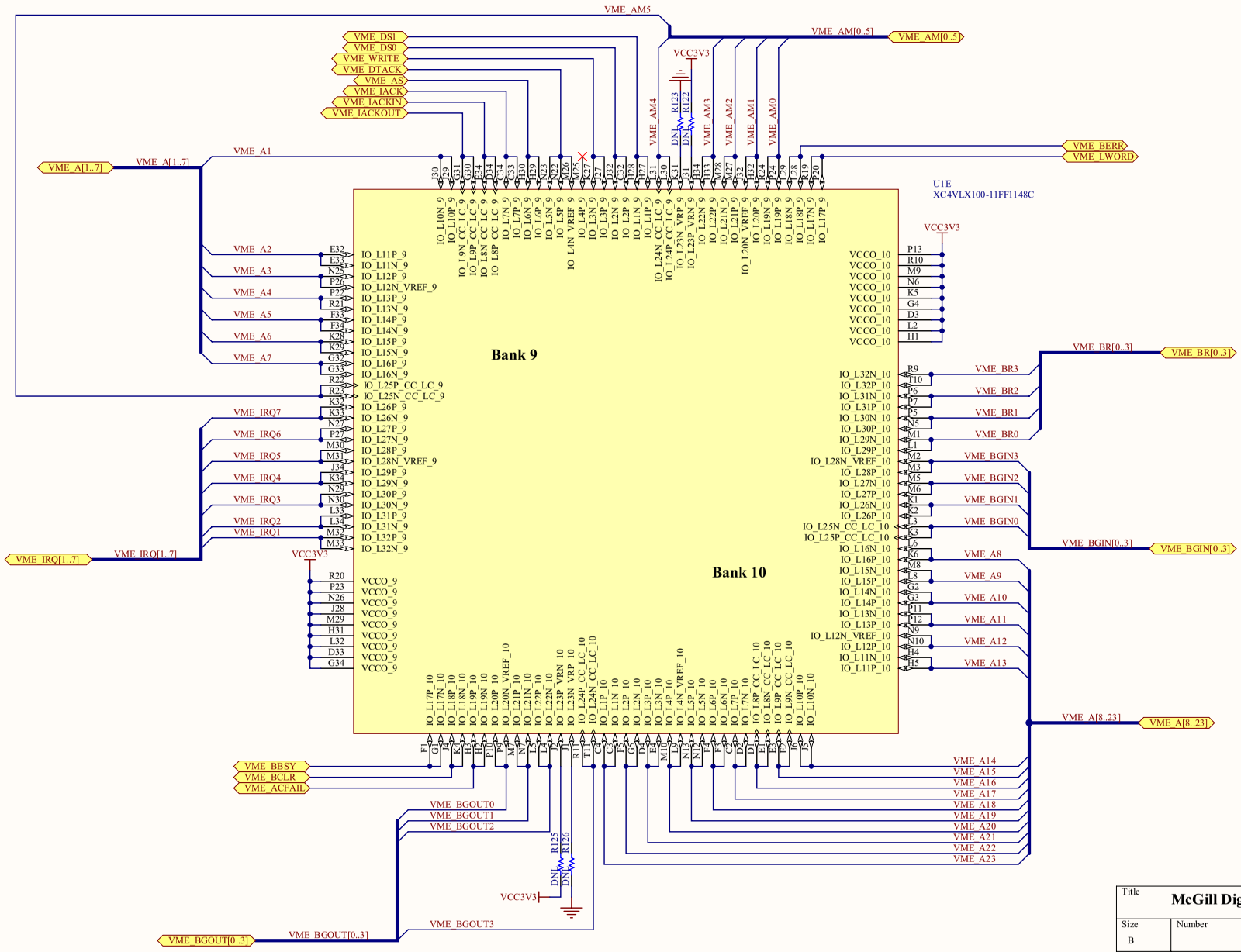
Title: **McGill Digital fMUX FPGA Motherboard**		
Size: B	Number: Banks 3, 4 and EEPROM	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Banks_3_4.SchDoc	Drawn By: N.Starinski, UdeM	



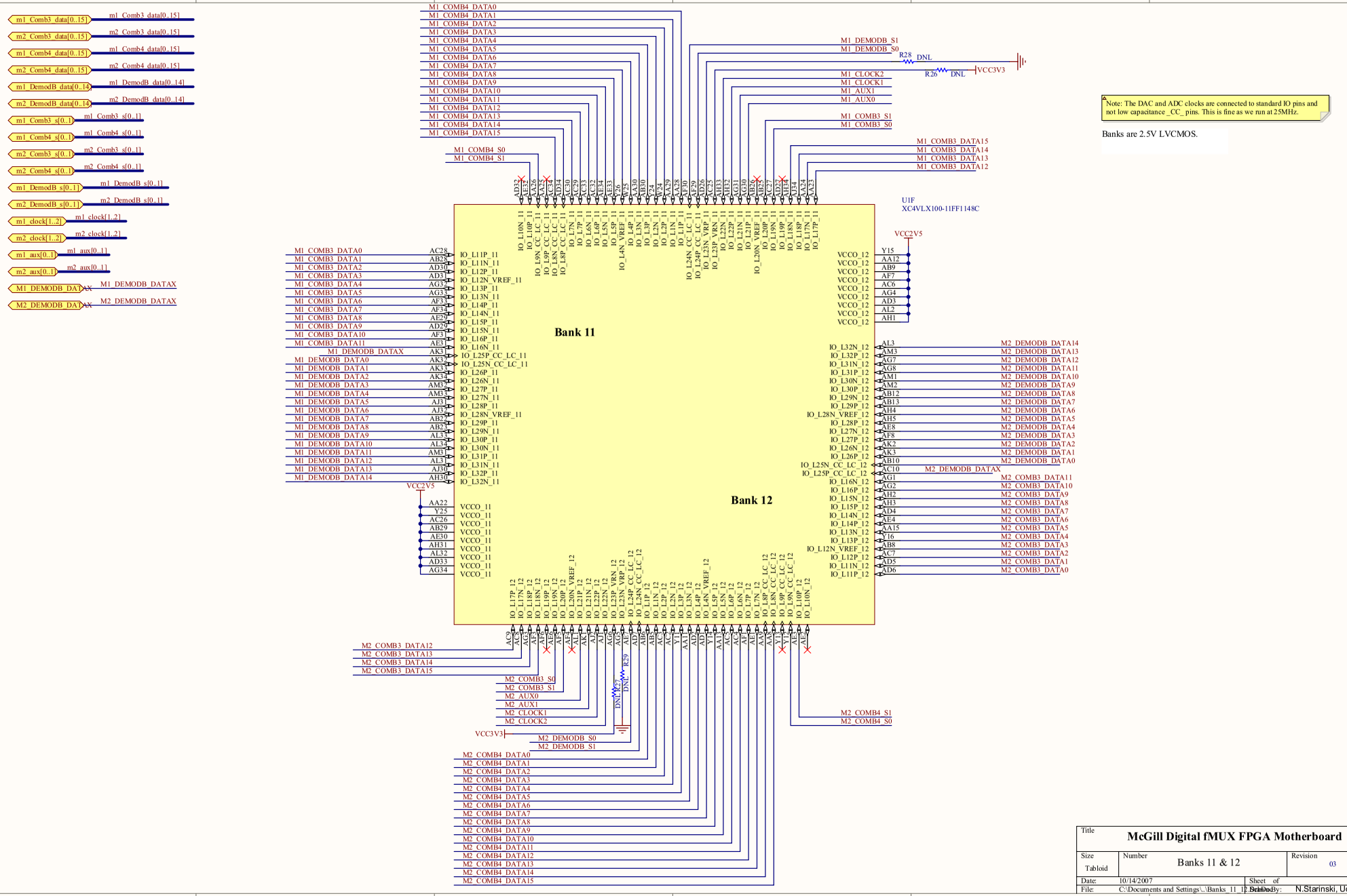
Bank 5 is used for DDR Memory.

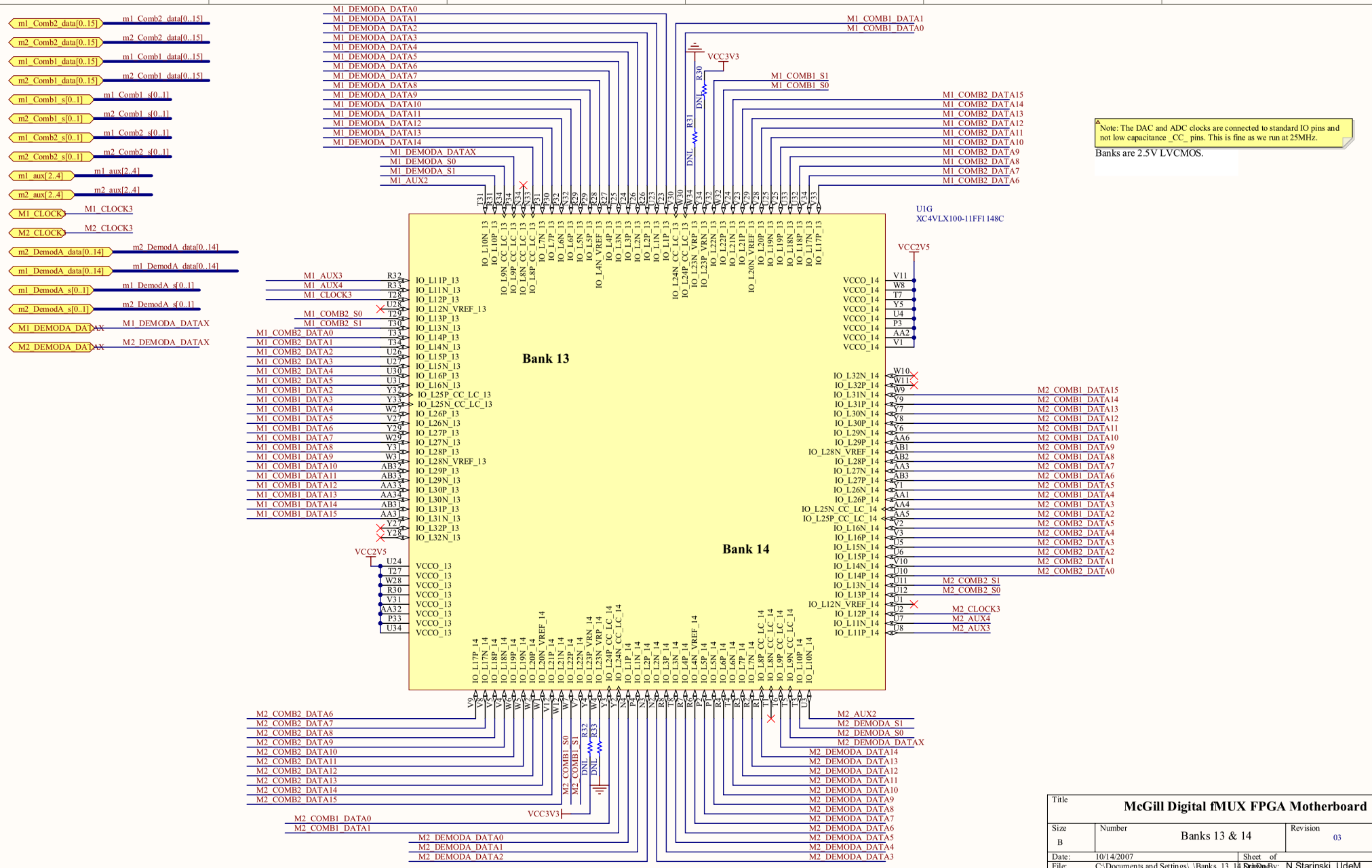
Title: **McGill Digital fMUX FPGA Motherboard**		
Size: B	Number: Banks 5 & 6	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Banks_5_6.SchDoc	Drawn By: N.Starinski, UdeM	


VME_D[0..15]
VME_D[0..15]
Connect LVDS lines to the front panel Differential.
FP_LVDS_BN
FP_LVDS_BP
FP_LVDS_AN
FP_LVDS_AP
FPGA_WATCH_DOG_TOGGLE
FPGA_WATCH_DOG_IN
BP_MASTER[0..5]
BP_MASTER[0..5]
BP_MASTER0
BP_MASTER1
BP_MASTER2
BP_MASTER3
U1D
XC4VLX100-11FF1148C
Bank 7
Bank 8
VCC3V3
VME_UD[0..17]
VME_UD[0..17]
BP_MASTER4
BP_MASTER5
VME_UD17
VME_UD16
VME_UD15
VME_UD14
VME_UD13
VME_UD12
VME_UD11
VME_UD10
VME_UD9
VME_UD8
VME_UD7
VME_UD6
VME_UD5
VME_UD4
VME_UD3
VME_UD2
VME_UD1
VME_UD0
VME_D_OE
VME_D_TR
VCC2V5
SYSACE_MPA0
SYSACE_MPBRDY
10K_EXB-2HV103JV
RT10
R83
4.99K
SW2
SW DIP-8, GDH08S
GPIO_DIP8_5
GPIO_DIP7_5
GPIO_DIP6_5
GPIO_DIP5_5
GPIO_DIP4_5
GPIO_DIP3_5
GPIO_DIP2_5
GPIO_DIP1_5
TEMP_HIGH
FPGA_SQUID_ENABLE_BAR_9V
SYSACE_MPOE_USB_RD_N
SYSACE_MPWE_USB_WR_N
BUS_ERROR_2_5
BUS_ERROR_1_5
R81
681
R80
681
DS13
DS12
LED0805_RED
R88
DNL
R87
DNL
SYSACE_MPIRQ
SYSACE_MPCE
SYSACE_MPA[0..6]
SYSACE_MPA[0..6]
SYSACE_USB_D[0..15]
SYSACE_USB_D[0..15]
Title
McGill Digital fMUX FPGA Motherboard
Size
B
Number
Banks 7, 8
Revision
03
Date:
10/14/2007
Sheet of
File:
C:\Documents and Settings\..\Banks_7_8.SchDoc
Drawn By:
N.Starinski, UdeM



Title	McGill Digital fMUX FPGA Motherboard	
Size: B	Number: Banks 9, 10	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Banks_9_10.SchDoc	Drawn By: N.Starinski, UdeM	


m1_Comb3_data[0..15]
m2_Comb3_data[0..15]
m1_Comb4_data[0..15]
m2_Comb4_data[0..15]
m1_DemodB_data[0..14]
m2_DemodB_data[0..14]
m1_Comb3_s[0..1]
m1_Comb4_s[0..1]
m2_Comb3_s[0..1]
m2_Comb4_s[0..1]
m1_DemodB_s[0..1]
m2_DemodB_s[0..1]
m1_clock[1..2]
m2_clock[1..2]
m1_aux[0..1]
m2_aux[0..1]
M1_DEMODB_DATAX
M2_DEMODB_DATAX
M1_COMB4_DATA0
M1_COMB4_DATA1
M1_COMB4_DATA2
M1_COMB4_DATA3
M1_COMB4_DATA4
M1_COMB4_DATA5
M1_COMB4_DATA6
M1_COMB4_DATA7
M1_COMB4_DATA8
M1_COMB4_DATA9
M1_COMB4_DATA10
M1_COMB4_DATA11
M1_COMB4_DATA12
M1_COMB4_DATA13
M1_COMB4_DATA14
M1_COMB4_DATA15
M1_COMB4_S0
M1_COMB4_S1
M1_DEMODB_S1
M1_DEMODB_S0
R28
DNL
R26
DNL
VCC3V3
M1_CLOCK2
M1_CLOCK1
M1_AUX1
M1_AUX0
M1_COMB3_S1
M1_COMB3_S0
M1_COMB3_DATA15
M1_COMB3_DATA14
M1_COMB3_DATA13
M1_COMB3_DATA12
U1F
XC4VLX100-11FF1148C
VCC2V5
Bank 11
Bank 12
M1_COMB3_DATA0
M1_COMB3_DATA1
M1_COMB3_DATA2
M1_COMB3_DATA3
M1_COMB3_DATA4
M1_COMB3_DATA5
M1_COMB3_DATA6
M1_COMB3_DATA7
M1_COMB3_DATA8
M1_COMB3_DATA9
M1_COMB3_DATA10
M1_COMB3_DATA11
M1_DEMODB_DATAX
M1_DEMODB_DATA0
M1_DEMODB_DATA1
M1_DEMODB_DATA2
M1_DEMODB_DATA3
M1_DEMODB_DATA4
M1_DEMODB_DATA5
M1_DEMODB_DATA6
M1_DEMODB_DATA7
M1_DEMODB_DATA8
M1_DEMODB_DATA9
M1_DEMODB_DATA10
M1_DEMODB_DATA11
M1_DEMODB_DATA12
M1_DEMODB_DATA13
M1_DEMODB_DATA14
M2_DEMODB_DATA14
M2_DEMODB_DATA13
M2_DEMODB_DATA12
M2_DEMODB_DATA11
M2_DEMODB_DATA10
M2_DEMODB_DATA9
M2_DEMODB_DATA8
M2_DEMODB_DATA7
M2_DEMODB_DATA6
M2_DEMODB_DATA5
M2_DEMODB_DATA4
M2_DEMODB_DATA3
M2_DEMODB_DATA2
M2_DEMODB_DATA1
M2_DEMODB_DATA0
M2_DEMODB_DATAX
M2_COMB3_DATA11
M2_COMB3_DATA10
M2_COMB3_DATA9
M2_COMB3_DATA8
M2_COMB3_DATA7
M2_COMB3_DATA6
M2_COMB3_DATA5
M2_COMB3_DATA4
M2_COMB3_DATA3
M2_COMB3_DATA2
M2_COMB3_DATA1
M2_COMB3_DATA0
M2_COMB3_DATA12
M2_COMB3_DATA13
M2_COMB3_DATA14
M2_COMB3_DATA15
M2_COMB3_S0
M2_COMB3_S1
M2_AUX0
M2_AUX1
M2_CLOCK1
M2_CLOCK2
M2_COMB4_S1
M2_COMB4_S0
M2_DEMODB_S0
M2_DEMODB_S1
M2_COMB4_DATA0
M2_COMB4_DATA1
M2_COMB4_DATA2
M2_COMB4_DATA3
M2_COMB4_DATA4
M2_COMB4_DATA5
M2_COMB4_DATA6
M2_COMB4_DATA7
M2_COMB4_DATA8
M2_COMB4_DATA9
M2_COMB4_DATA10
M2_COMB4_DATA11
M2_COMB4_DATA12
M2_COMB4_DATA13
M2_COMB4_DATA14
M2_COMB4_DATA15
R29
DNL
R27
DNL
Note: The DAC and ADC clocks are connected to standard IO pins and not low capacitance _CC_ pins. This is fine as we run at 25MHz.
Banks are 2.5V LVCMOS.
Title
McGill Digital fMUX FPGA Motherboard
Size
Tabloid
Number
Banks 11 & 12
Revision
03
Date:
10/14/2007
Sheet of
File:
C:\Documents and Settings\...\Banks_11_12.SchDoc
Drawn By:
N.Starinski, UdeM


m1_Comb2_data[0..15]
m2_Comb2_data[0..15]
m1_Comb1_data[0..15]
m2_Comb1_data[0..15]
m1_Comb1_s[0..1]
m2_Comb1_s[0..1]
m1_Comb2_s[0..1]
m2_Comb2_s[0..1]
m1_aux[2..4]
m2_aux[2..4]
M1_CLOCK
M2_CLOCK
m2_DemodA_data[0..14]
m1_DemodA_data[0..14]
m1_DemodA_s[0..1]
m2_DemodA_s[0..1]
M1_DEMODA_DATAX
M2_DEMODA_DATAX
M1_DEMODA_DATA0
M1_DEMODA_DATA1
M1_DEMODA_DATA2
M1_DEMODA_DATA3
M1_DEMODA_DATA4
M1_DEMODA_DATA5
M1_DEMODA_DATA6
M1_DEMODA_DATA7
M1_DEMODA_DATA8
M1_DEMODA_DATA9
M1_DEMODA_DATA10
M1_DEMODA_DATA11
M1_DEMODA_DATA12
M1_DEMODA_DATA13
M1_DEMODA_DATA14
M1_DEMODA_DATAX
M1_DEMODA_S0
M1_DEMODA_S1
M1_AUX2
M1_COMB1_DATA1
M1_COMB1_DATA0
M1_COMB1_S1
M1_COMB1_S0
M1_COMB2_DATA15
M1_COMB2_DATA14
M1_COMB2_DATA13
M1_COMB2_DATA12
M1_COMB2_DATA11
M1_COMB2_DATA10
M1_COMB2_DATA9
M1_COMB2_DATA8
M1_COMB2_DATA7
M1_COMB2_DATA6
VCC3V3
DNL
R30
R31
U1G
XC4VLX100-11FF1148C
VCC2V5
Bank 13
Bank 14
M1_AUX3
M1_AUX4
M1_CLOCK3
M1_COMB2_S0
M1_COMB2_S1
M1_COMB2_DATA0
M1_COMB2_DATA1
M1_COMB2_DATA2
M1_COMB2_DATA3
M1_COMB2_DATA4
M1_COMB2_DATA5
M1_COMB1_DATA2
M1_COMB1_DATA3
M1_COMB1_DATA4
M1_COMB1_DATA5
M1_COMB1_DATA6
M1_COMB1_DATA7
M1_COMB1_DATA8
M1_COMB1_DATA9
M1_COMB1_DATA10
M1_COMB1_DATA11
M1_COMB1_DATA12
M1_COMB1_DATA13
M1_COMB1_DATA14
M1_COMB1_DATA15
M2_COMB1_DATA15
M2_COMB1_DATA14
M2_COMB1_DATA13
M2_COMB1_DATA12
M2_COMB1_DATA11
M2_COMB1_DATA10
M2_COMB1_DATA9
M2_COMB1_DATA8
M2_COMB1_DATA7
M2_COMB1_DATA6
M2_COMB1_DATA5
M2_COMB1_DATA4
M2_COMB1_DATA3
M2_COMB1_DATA2
M2_COMB1_DATA1
M2_COMB1_DATA0
M2_COMB2_S1
M2_COMB2_S0
M2_CLOCK3
M2_AUX4
M2_AUX3
M2_COMB2_DATA6
M2_COMB2_DATA7
M2_COMB2_DATA8
M2_COMB2_DATA9
M2_COMB2_DATA10
M2_COMB2_DATA11
M2_COMB2_DATA12
M2_COMB2_DATA13
M2_COMB2_DATA14
M2_COMB2_DATA15
M2_COMB1_S0
M2_COMB1_S1
M2_AUX2
M2_DEMODA_S1
M2_DEMODA_S0
M2_DEMODA_DATAX
M2_DEMODA_DATA14
M2_DEMODA_DATA13
M2_DEMODA_DATA12
M2_DEMODA_DATA11
M2_DEMODA_DATA10
M2_DEMODA_DATA9
M2_DEMODA_DATA8
M2_DEMODA_DATA7
M2_DEMODA_DATA6
M2_DEMODA_DATA5
M2_DEMODA_DATA4
M2_DEMODA_DATA3
M2_DEMODA_DATA0
M2_DEMODA_DATA1
M2_DEMODA_DATA2
Note: The DAC and ADC clocks are connected to standard IO pins and not low capacitance _CC_ pins. This is fine as we run at 25MHz.
Banks are 2.5V LVCMOS.
Title
McGill Digital fMUX FPGA Motherboard
Size
B
Number
Banks 13 & 14
Revision
03
Date:
10/14/2007
Sheet of
File:
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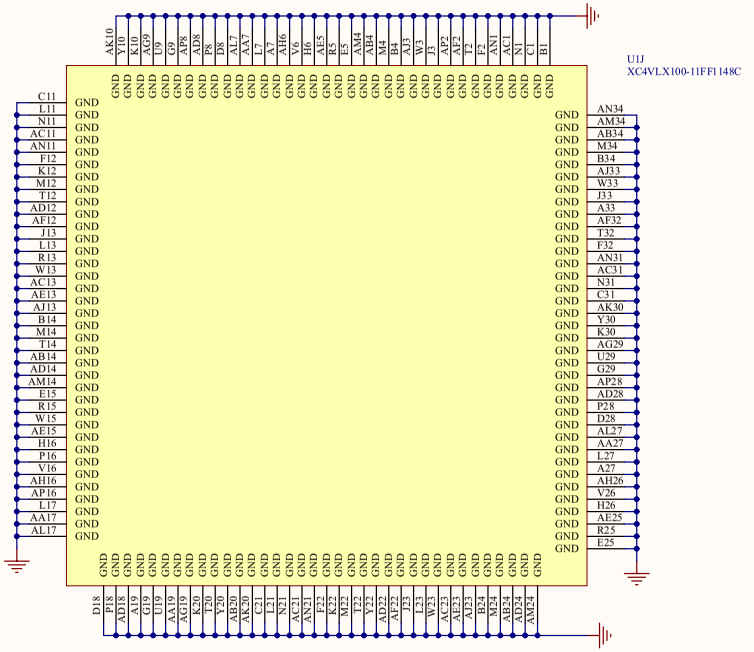
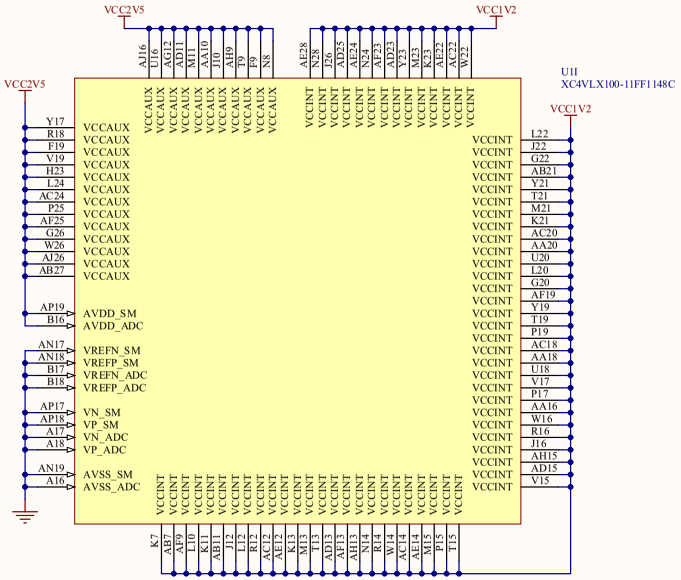
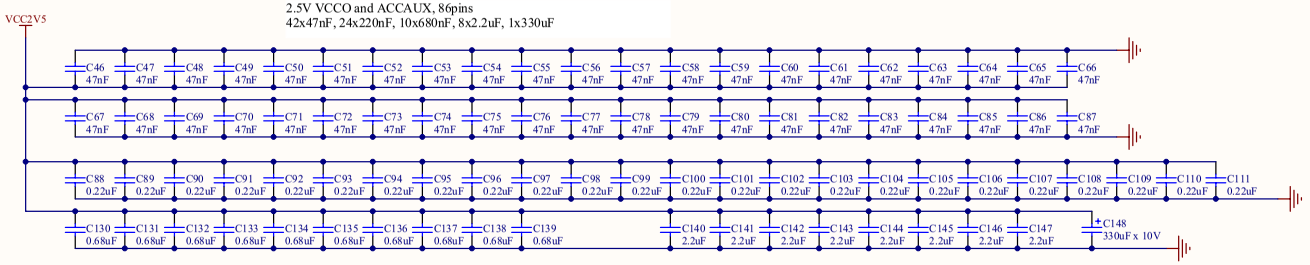
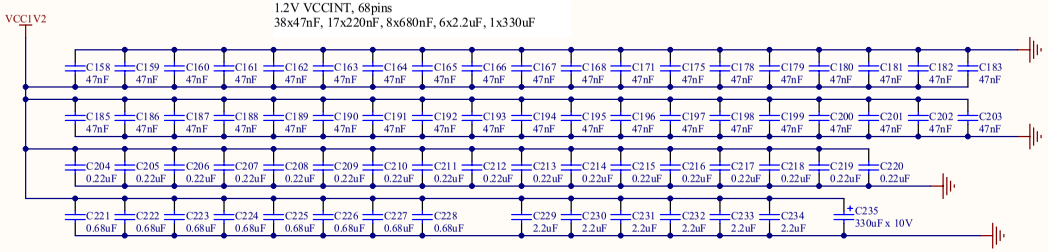
Drawn By:
N.Starinski, UdeM

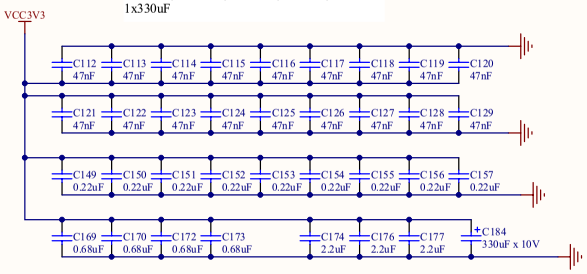




These _SM, _ADC pins connected according to p.16 of V4 pinout guide.

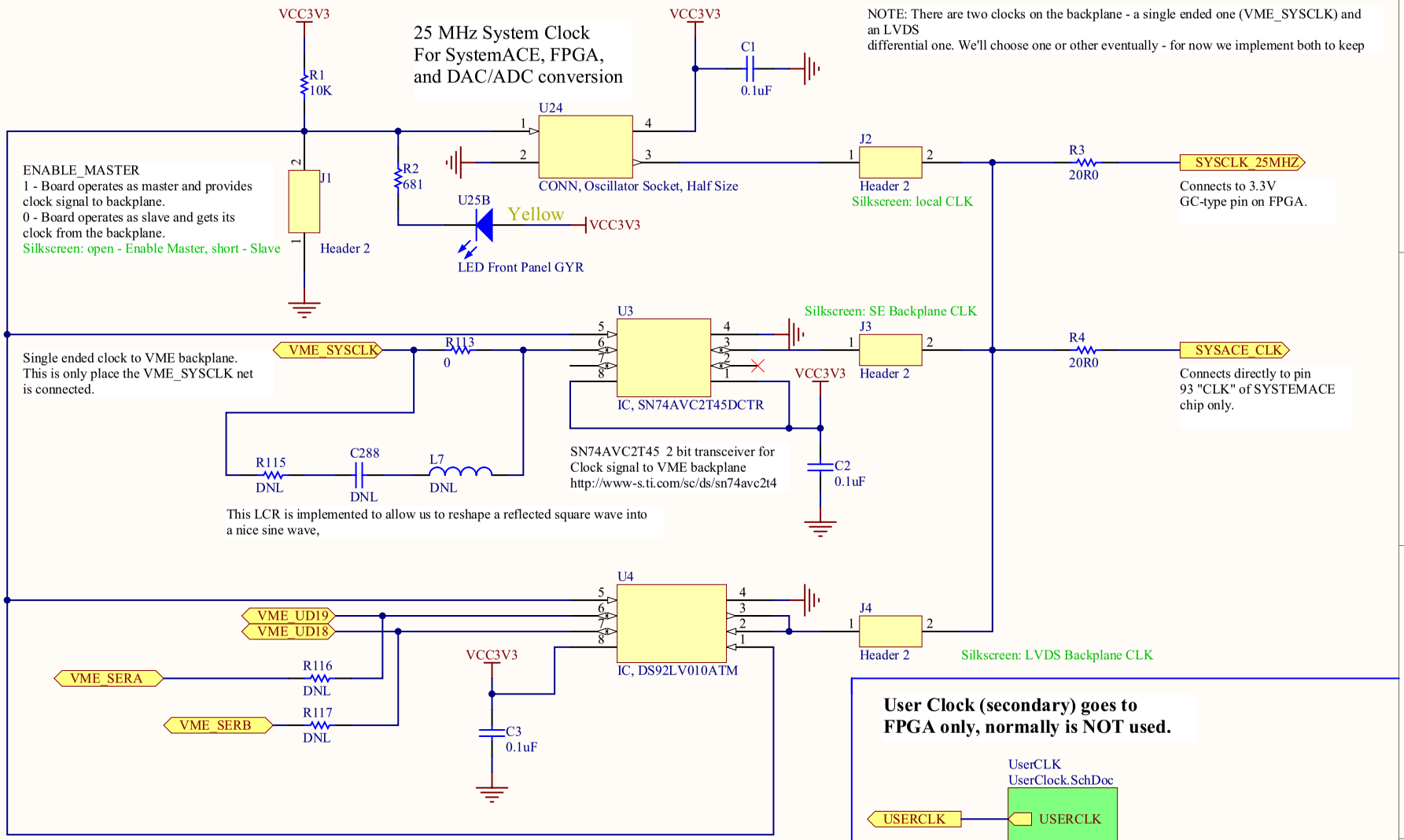




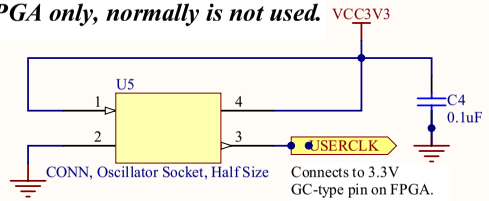


Note: To estimate the number of bypass caps needed of each type, I have scaled up the number of bypass caps used on the ML402 demo board by the ratio of power pins for each voltage. Layout Note: ALL 47nF CAPS are placed under the FPGA between pads.

Title	McGill Digital fMUX FPGA Motherboard		
Size: Tabloid	Number: FPGA Power, GND, Bypass		Revision: 03
Date: 10/14/2007		Sheet of	
File: C:\Documents and Settings\..\FPGA_Power_Bypass....		Drawn By: N.Starinski, UdeM	


25 MHz System Clock
For SystemACE, FPGA,
and DAC/ADC conversion
NOTE: There are two clocks on the backplane - a single ended one (VME_SYSCLK) and an LVDS
differential one. We'll choose one or other eventually - for now we implement both to keep
VCC3V3
R1
10K
C1
0.1uF
U24
CONN, Oscillator Socket, Half Size
J2
Header 2
Silkscreen: local CLK
R3
20R0
SYSCLK_25MHZ
Connects to 3.3V
GC-type pin on FPGA.
ENABLE_MASTER
1 - Board operates as master and provides clock signal to backplane.
0 - Board operates as slave and gets its clock from the backplane.
Silkscreen: open - Enable Master, short - Slave
J1
Header 2
R2
681
U25B
Yellow
LED Front Panel GYR
Silkscreen: SE Backplane CLK
U3
IC, SN74AVC2T45DCTR
J3
Header 2
R4
20R0
SYSACE_CLK
Connects directly to pin
93 "CLK" of SYSTEMACE
chip only.
VME_SYSCLK
R113
0
Single ended clock to VME backplane.
This is only place the VME_SYSCLK net is connected.
R115
DNL
C288
DNL
L7
DNL
This LCR is implemented to allow us to reshape a reflected square wave into a nice sine wave,
SN74AVC2T45 2 bit transceiver for
Clock signal to VME backplane
http://www-s.ti.com/sc/ds/sn74avc2t4
C2
0.1uF
U4
IC, DS92LV010ATM
J4
Header 2
Silkscreen: LVDS Backplane CLK
VME_UD19
VME_UD18
VME_SERA
VME_SERB
R116
DNL
R117
DNL
C3
0.1uF
User Clock (secondary) goes to
FPGA only, normally is NOT used.
UserCLK
UserClock.SchDoc
USERCLK
USERCLK
Title
McGill Digital fMUX FPGA Motherboard
Size
A
Number
Clock Distribution
Revision
03
Date:
10/14/2007
Sheet of
File:
C:\Documents and Settings\..\Clock_distrubution.SchDoc
Drawn By:
N.Starinski, UdeM

User Clock (secondary) goes to FPGA only, normally is not used.



Oscillator socket: Aries 1108800 (Digikey A463-ND)
http://rocky.digikey.com/WebLib/Aries/Web%20Data/1107741%20and%201108800.pdf

Title: McGill Digital fMUX FPGA Motherboard		
Size: Letter	Number: User Clock	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\UserClock.SchDoc	Drawn By: N.Starinski, UdeM	

Pin-to-Pin MAPPING

PIN	BIT[2..0]
VCC2V5	111
PHY_LED_LINK10	110
PHY_LED_LINK100	101
PHY_LED_LINK1000	100
PHY_LED_DUPLEX	011
PHY_LED_RX	010
PHY_LED_TXT	001
GND	000

Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the Pause bit.
CONFIG1	ENA_PAUSE	PHY_ADR[4]	PHY_ADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[0]	111	Auto-Neg enable, advertise all capabilities; prefer slave. Auto crossover enable. 125 CLK option disable.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111	GMII to GU mode. Fiber/copper auto-detect disable Sleep mode disable.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Actile Low Interrupt. 500 OHM SERDES option.

All datasheet rec'd 10uF tantalum caps have been changed to 33uF ceramic (lower ESR, but could buzz at microphonic freq - verify).

Layout note: Place these four LEDs anywhere they would be visible when the mezz cards are mounted, but the board is not in a rack.

The comparator "trips" at 0V, so we bias the -ve reference up to 3.3V * 1/ 3.49K = 0.95V to define a low. Likewise, at the output we divide down from 3.3V to 2.5V. (also changed datasheet rec'd 100n bypass cap to 47n against datasheet.)

Silkscreen: "ETHERNET"

Title	McGill Digital fMUX FPGA Motherboard		
Size: Letter	Number: PHY		Revision: 03
Date: 10/14/2007		Sheet of	
File: C:\Documents and Settings\..\PHY_RJ45.SchDoc		Drawn By: N.Starinski, UdeM	

Update Notes:
Some signals connected to the FPGA differently than on the original OrCAD scgematic.

N.Starinski 2006/10/30

This circuit connects the external DDR memory to the FPGA.
The memory uses 2.5V CMOC logic level, and is powered from the VCC2V5 power.
The memory is used exclusively by the embedded soft processor in the FPGA.

DDR_CK1_N
DDR_CK1_P
DDR_CKE
DDR_CS_N
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_BA1
DDR_BA0

DDR_DQS3
DDR_DQS2
DDR_DQS1
DDR_DQS0
DDR_DM3
DDR_DM2
DDR_DM1
DDR_DM0

DDR_A13
DDR_A12
DDR_A11
DDR_A10
DDR_A9
DDR_A8
DDR_A7
DDR_A6
DDR_A5
DDR_A4
DDR_A3
DDR_A2
DDR_A1
DDR_A0

DDR_D31
DDR_D30
DDR_D29
DDR_D28
DDR_D27
DDR_D26
DDR_D25
DDR_D24
DDR_D23
DDR_D22
DDR_D21
DDR_D20
DDR_D19
DDR_D18
DDR_D17
DDR_D16
DDR_D15
DDR_D14
DDR_D13
DDR_D12
DDR_D11
DDR_D10
DDR_D9
DDR_D8
DDR_D7
DDR_D6
DDR_D5
DDR_D4
DDR_D3
DDR_D2
DDR_D1
DDR_D0

RA2 RH5 RG5 RG6 RF6 RE6 RD6 DDR_B DDR_BA0 RG2 RF2 RD2 RA6 RB2 RE2 RC2 RC6 RB6 RF5 RE5 RB1 RD5 RC5 RB5 RA5 RG1 RH1 RF1 RE1 RD1 RC1 RH4 RG4 RF4 RE4 RD4 RC4 RB4 RA4 RH3 RG3 RF3 RE3 RD3 RC3 RB3 RA3 RH7 RG7 RF7 RE7 RD7 RC7 RB7 RA7 RH8 RG8 RF8 RE8 RD8 RC8 RB8 RA8

U12 IC, DDR SDRAM MT46V16M16P-6T IT:F TR

U13 IC, DDR SDRAM MT46V16M16P-6T IT:F TR

Vref

VCC2V5

C32 0.1uF
C33 0.1uF
C34 0.1uF
C35 0.1uF
C27 100uF x 10V
C30 0.1uF
C31 0.1uF
C36 0.1uF
C37 0.1uF
C38 0.1uF
C39 0.1uF
C28 100uF x 10V

Sink / Source DDR Termination Regulator

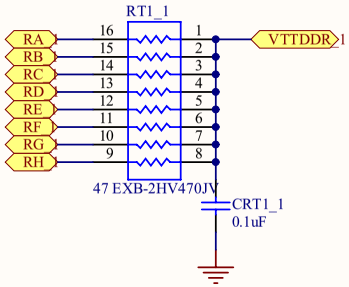
Note: the ML402 used http://focus.ti.com/lit/ds/symlink/tps51100.pdf, we have switched to the LP2996M because it allows VIN=2.5V and it is available from Digikey. http://www.national.com/pf/LP/LP2996.html

VCC2V5
VTTDDR
Vref
U28
REG, LP2996M, DDR Termination
C29 100uF x 10V
C289 100uF x 10V
C290 100uF x 10V

VTTDDR
C17 100uF x 10V
C20 100uF x 10V
C23 100uF x 10V
C26 100uF x 10V

Repeat(RTerm,1,8)
RTerm.SchDoc
Ra[1..8] Rb[1..8] Rc[1..8] Rd[1..8] Re[1..8] Rf[1..8] Rg[1..8] Rh[1..8]
Repeat(Ra) Repeat(Rb) Repeat(Rc) Repeat(Rd) Repeat(Re) Repeat(Rf) Repeat(Rg) Repeat(Rh)
VTTDDR

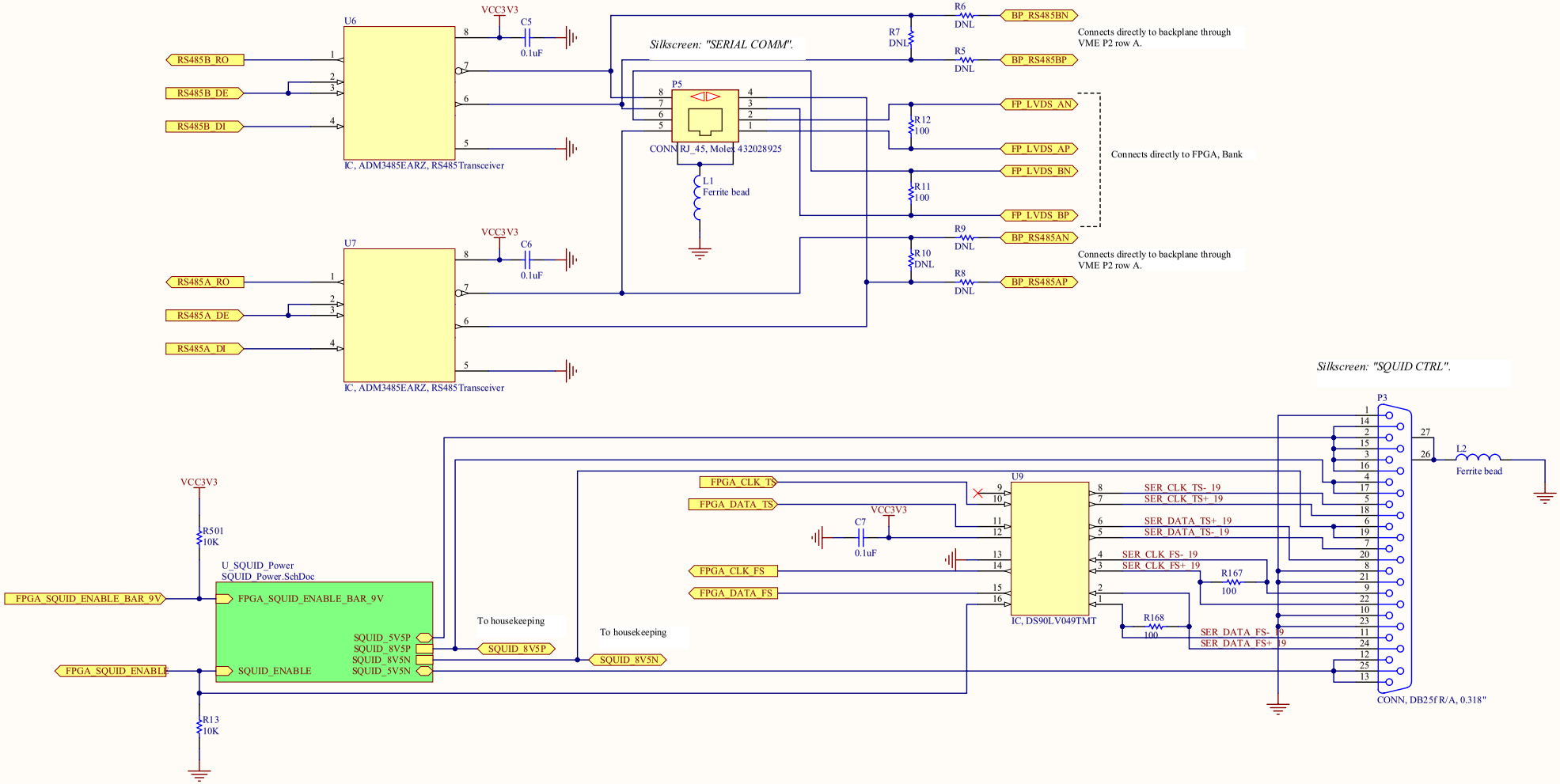
Title	**McGill Digital fMUX FPGA Motherboard**	
Size: B	Number: DDR Memory	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\DDR-Memory.SchDoc	Drawn By: N.Starinski, UdeM	



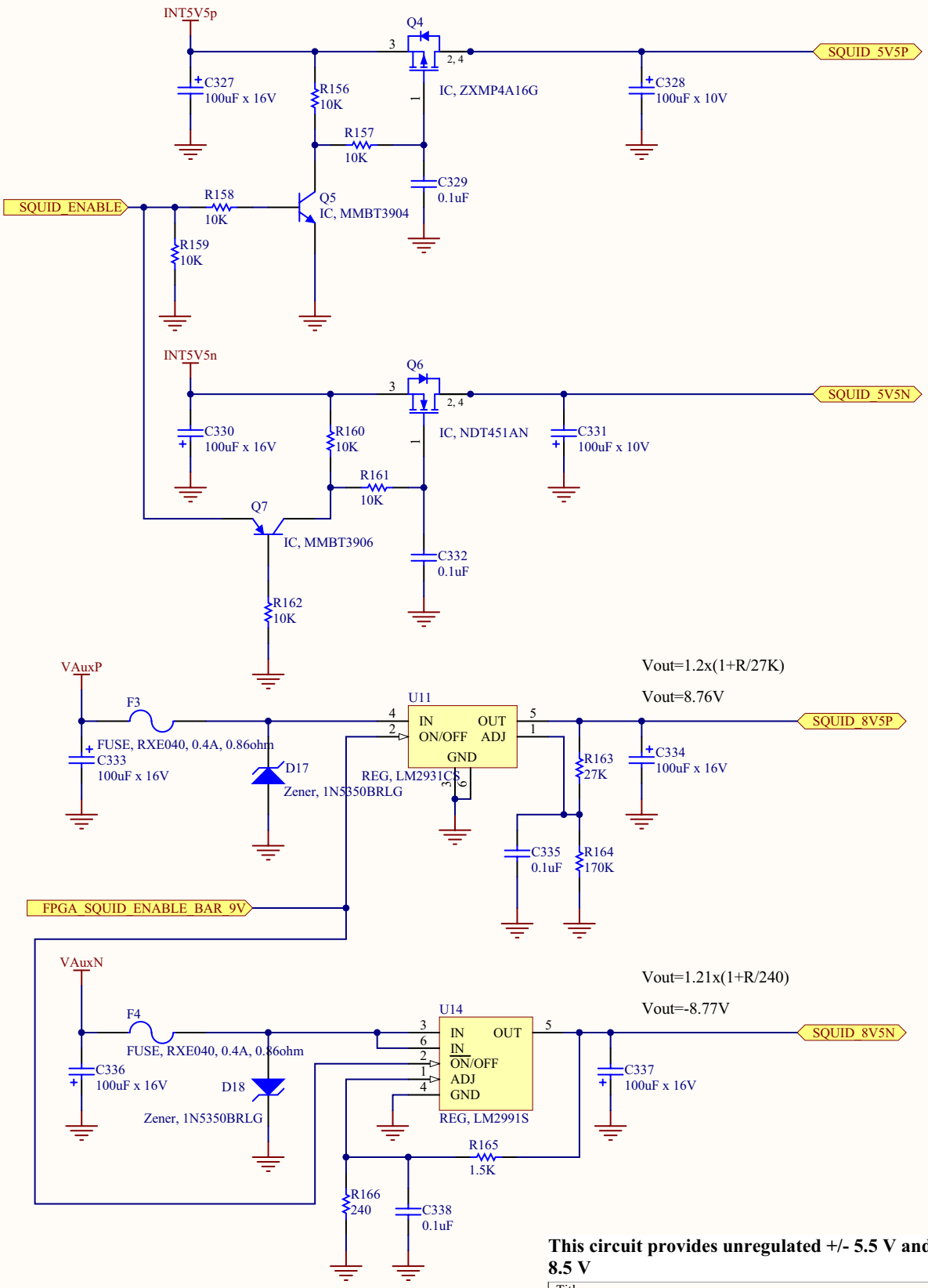
For updates and general information contact:

Matt Dobbs at McGill University: matt.dobbs@mcgill.ca
Nick Starinski at UdeM: starinsky@lps.umontreal.ca
or nick.starinsky@gmail.com

Title	**McGill Digital fMUX FPGA Motherboard**		
Size: Letter	Number: Pullup Resistors for DDR Memory		Revision: 03
Date: 10/14/2007		Sheet of	
File: C:\Documents and Settings\...\RTerm.SchDoc		Drawn By:	N.Starinski, UdeM

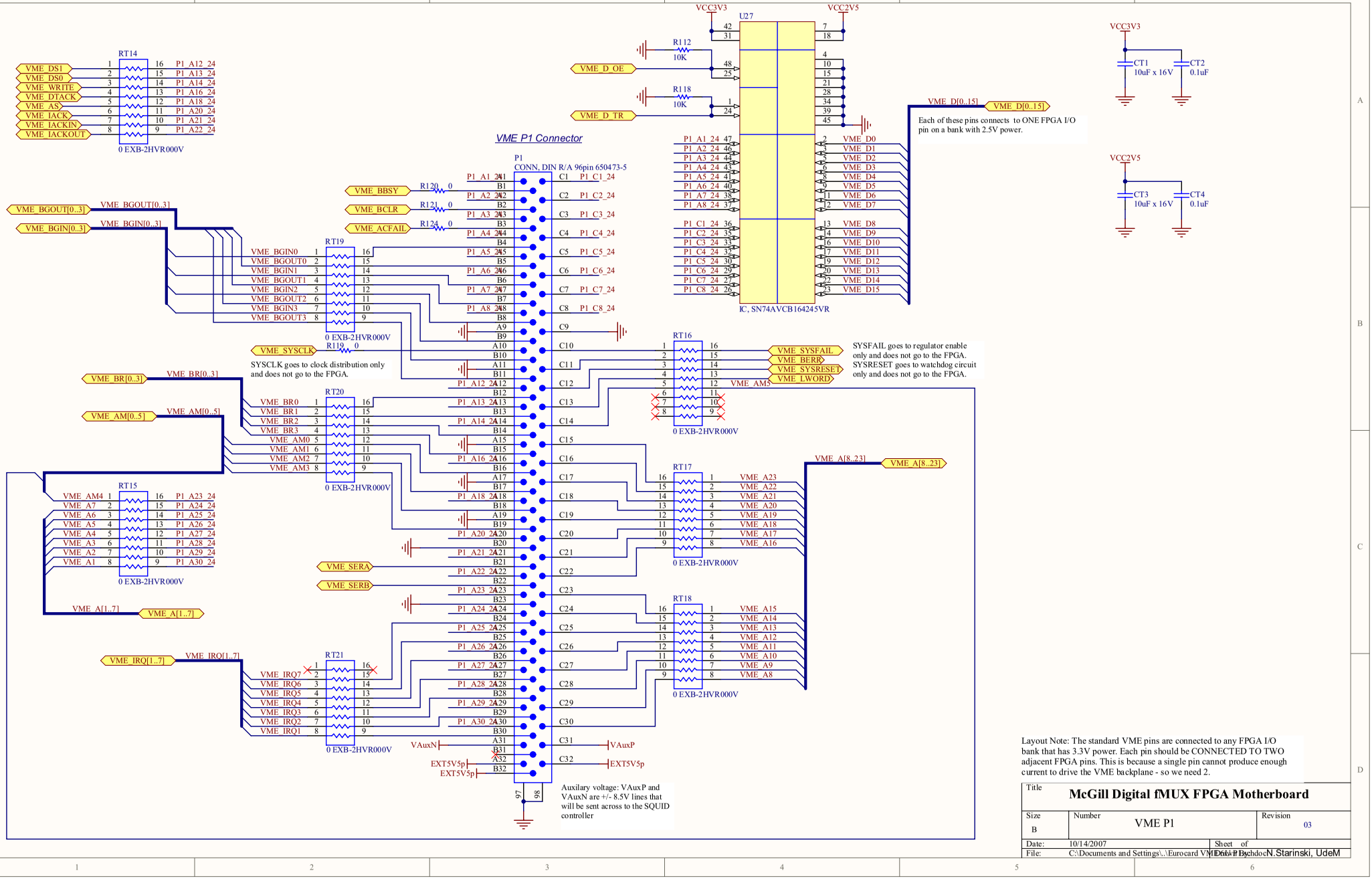


Title	**McGill Digital fMUX FPGA Motherboard**	
Size: B	Number: Communication and SQUID	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Comm_SQUID.SchDoc	Drawn By: N.Starinski, UdeM	



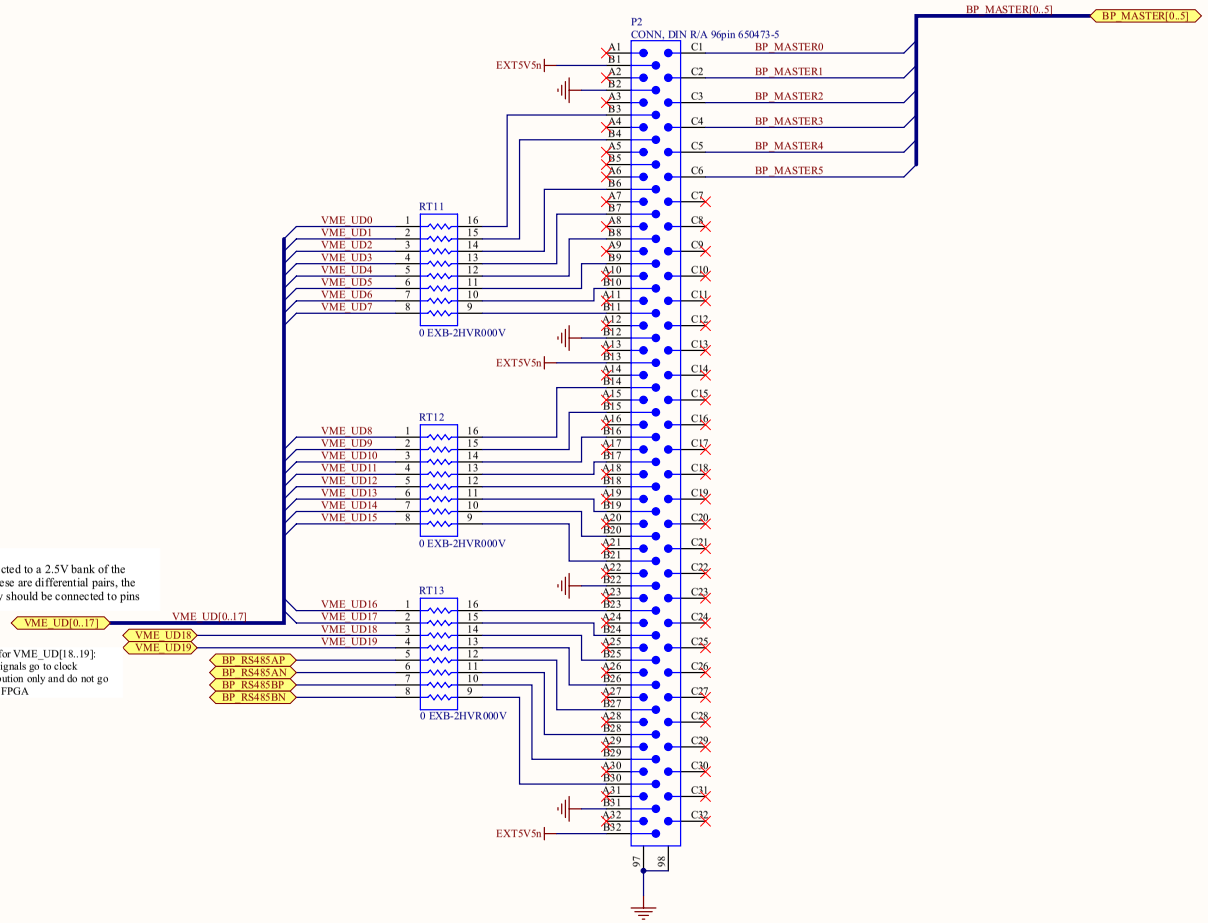
This circuit provides unregulated +/- 5.5 V and regulated +/- 8.5 V

Title: **McGill Digital fMUX FPGA Motherboard**		
Size: A	Number: **SQUID Power**	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\SQUID_Power.SchDoc	Drawn By: N.Starinski, UdeM	


VME P1 Connector
P1
CONN, DIN R/A 96pin 650473-5
U27
IC, SN74AVCB164245VR
VCC3V3
VCC2V5
RT14
RT15
RT16
RT17
RT18
RT19
RT20
RT21
0 EXB-2HVR000V
VME_DS1
VME_DS0
VME_WRITE
VME_DTACK
VME_AS
VME_IACK
VME_IACKIN
VME_IACKOUT
VME_BBSY
VME_BCLR
VME_ACFAIL
VME_BGOUT[0..3]
VME_BGIN[0..3]
VME_SYSCLK
VME_BR[0..3]
VME_AM[0..5]
VME_IRQ[1..7]
VME_A[1..7]
VME_A[8..23]
VME_SERA
VME_SERB
VME_D_OE
VME_D_TR
VME_D[0..15]
VME_SYSFAIL
VME_BERR
VME_SYSRESET
VME_LWORD
VAuxN
VAuxP
EXT5V5p
Each of these pins connects to ONE FPGA I/O pin on a bank with 2.5V power.
SYSCLK goes to clock distribution only and does not go to the FPGA.
SYSFAIL goes to regulator enable only and does not go to the FPGA.
SYSRESET goes to watchdog circuit only and does not go to the FPGA.
Auxilary voltage: VAuxP and VAuxN are +/- 8.5V lines that will be sent across to the SQUID controller
Layout Note: The standard VME pins are connected to any FPGA I/O bank that has 3.3V power. Each pin should be CONNECTED TO TWO adjacent FPGA pins. This is because a single pin cannot produce enough current to drive the VME backplane - so we need 2.
Title
McGill Digital fMUX FPGA Motherboard
Size
B
Number
VME P1
Revision
03
Date:
10/14/2007
Sheet of
File:
C:\Documents and Settings\..\Eurocard VME P1.SchDoc
Drawn By:
N.Starinski, UdeM

VME P2 Connector

P2 is the LOWER connector in the 6U rack. Looking at the top-side of the board, with the connectors at the BACK, this is on the RIGHT side.



Note for VME_UD[0..17]:
These LVDS pins are connected to a 2.5V bank of the FPGA (any bank is fine). These are differential pairs, the pairs are (0,1) (2,3) etc. They should be connected to pins with P N

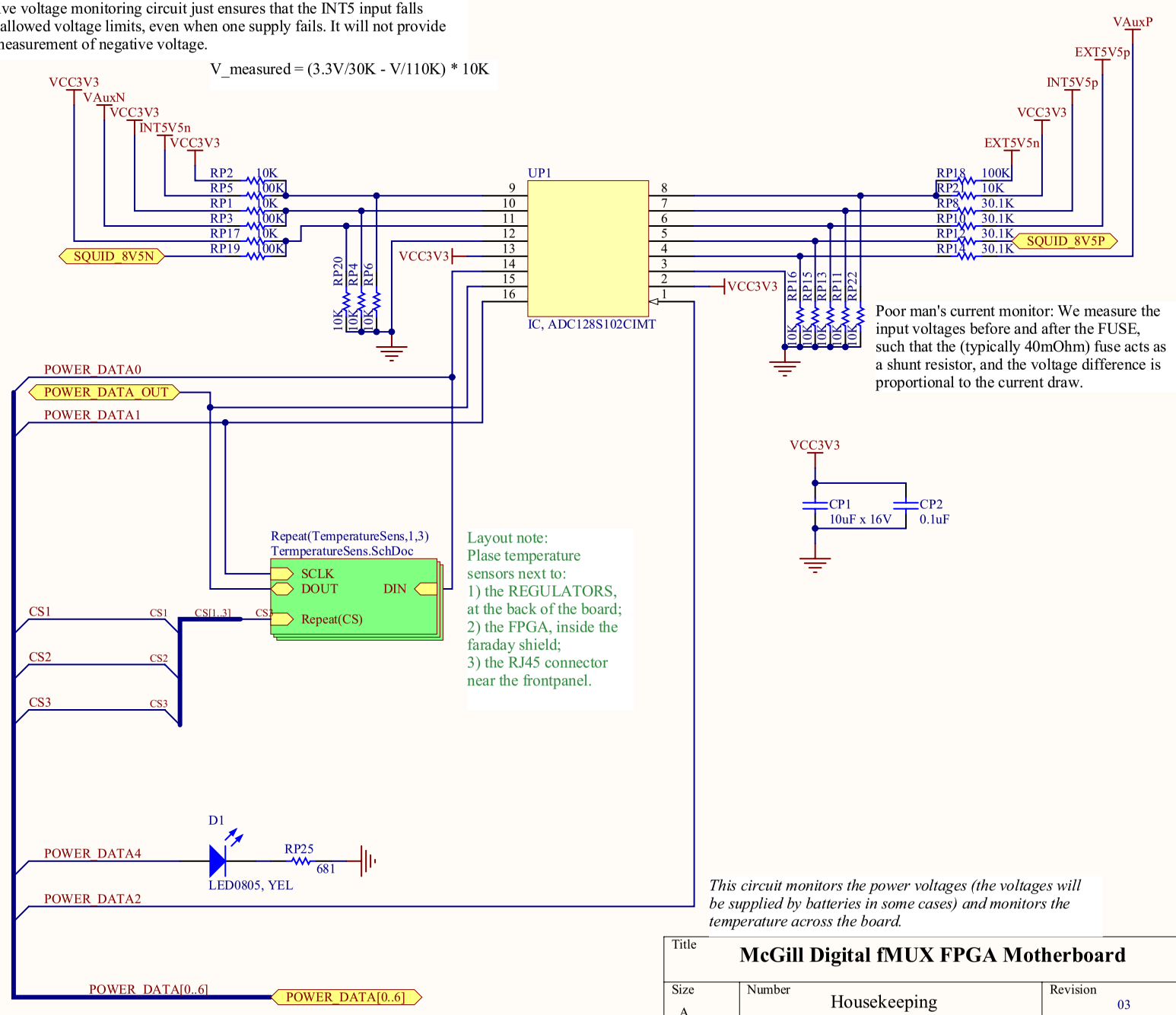
Note for VME_UD[18..19]:
This signals go to clock distribution only and do not go to the FPGA

The standard VME pins are connected to any FPGA I/O bank that has 3.3V power. Each pin should be CONNECTED TO TWO adjacent FPGA pins. This is because a single pin cannot produce enough current to drive the VME backplane - so we need 2.

Title	**McGill Digital fMUX FPGA Motherboard**	
Size: Tabloid	Number: VME P2	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Eurocard VME P2.SchDoc	Drawn By: N.Starinski, UdeM	

The funny negative voltage monitoring circuit just ensures that the INT5 input falls withing the max allowed voltage limits, even when one supply fails. It will not provide a very accurate measurement of negative voltage.

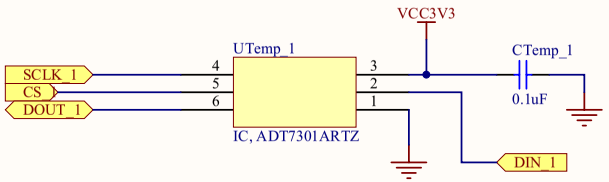
V_measured = (3.3V/30K - V/110K) * 10K



This circuit monitors the power voltages (the voltages will be supplied by batteries in some cases) and monitors the temperature across the board.

Title: **McGill Digital fMUX FPGA Motherboard**		
Size: A	Number: Housekeeping	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Housekeeping.SchDoc	Drawn By: N.Starinski, UdeM	

Layout note:
Plase temperature sensors next to:
1) the REGULATORS, at the back of the board;
2) the FPGA, inside the faraday shield;
3) the RJ45 connector near the frontpanel.



Title	**McGill Digital fMUX FPGA Motherboard**	
Size: Letter	Number: Temperature Sensor	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Termperature Sensor.SchDoc	Drawn By: N.Starinski, UdeM	

m1_Comb4_data[0..15] — m1_Comb4_data[0..15]
m1_Comb3_data[0..15] — m1_Comb3_data[0..15]
m1_Comb4_s[0..1] — m1_Comb4_s[0..1]
m1_Comb3_s[0..1] — m1_Comb3_s[0..1]
M1_DEMODB_DATAX — M1_DEMODB_DATAX
m1_DemodB_s[0..1] — m1_DemodB_s[0..1]
m1_DemodB_data[0..14] — m1_DemodB_data[0..14]

M1_CLOCK — M1_CLOCK3
m1_clock[1..2] — m1_clock[1..2]
m1_aux[0..1] — m1_aux[0..1]
m1_aux[2..4] — m1_aux[2..4]

m1_power_data[0..7] — m1_power_data[0..7]
m1_DemodA_data[0..14] — m1_DemodA_data[0..14]
m1_Comb2_data[0..15] — m1_Comb2_data[0..15]
m1_Comb1_data[0..15] — m1_Comb1_data[0..15]
M1_DEMODA_DATAX — M1_DEMODA_DATAX
m1_DemodA_s[0..1] — m1_DemodA_s[0..1]
m1_Comb2_s[0..1] — m1_Comb2_s[0..1]
m1_Comb1_s[0..1] — m1_Comb1_s[0..1]

VCC2V5

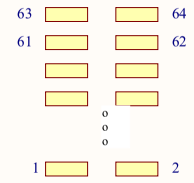
J16_1

M1_COMB4_DATA0	3	4		M1_COMB4_DATA1
M1_COMB4_DATA2	5	6		M1_COMB4_DATA3
M1_COMB4_DATA4	7	8		M1_COMB4_DATA5
M1_COMB4_DATA6	9	10		M1_COMB4_DATA7
M1_COMB4_DATA8	11	12		M1_COMB4_DATA9
M1_COMB4_DATA10	13	14		M1_COMB4_DATA11
M1_COMB4_DATA12	15	16		M1_COMB4_DATA13
M1_COMB4_DATA14	17	18		M1_COMB4_DATA15
	19	20		
M1_COMB4_S0	21	22		M1_COMB4_S1
M1_COMB3_DATA0	23	24		M1_COMB3_DATA1
M1_COMB3_DATA2	25	26		M1_COMB3_DATA3
M1_COMB3_DATA4	27	28		M1_COMB3_DATA5
M1_COMB3_DATA6	29	30		M1_COMB3_DATA7
M1_COMB3_DATA8	31	32		M1_COMB3_DATA9
M1_COMB3_DATA10	33	34		M1_COMB3_DATA11
M1_COMB3_DATA12	35	36		M1_COMB3_DATA13
M1_COMB3_DATA14	37	38		M1_COMB3_DATA15
M1_COMB3_S0	39	40		M1_COMB3_S1
M1_AUX0	41	42		M1_AUX1
M1_CLOCK1	43	44		M1_CLOCK2
	45	46		
M1_DEMODB_S0	47	48		M1_DEMODB_S1
M1_DEMODB_DATAX	49	50		M1_DEMODB_DATA0
M1_DEMODB_DATA1	51	52		M1_DEMODB_DATA2
M1_DEMODB_DATA3	53	54		M1_DEMODB_DATA4
M1_DEMODB_DATA5	55	56		M1_DEMODB_DATA6
M1_DEMODB_DATA7	57	58		M1_DEMODB_DATA8
M1_DEMODB_DATA9	59	60		M1_DEMODB_DATA10
M1_DEMODB_DATA11	61	62		M1_DEMODB_DATA12
M1_DEMODB_DATA13	63	64		M1_DEMODB_DATA14

CONN, 120603-1 IEEE1386 64pin Receptacle
To Bank11

Board to board spacing between this connector and its mate is 12 mm.

Layout note: the amp data sheet for these Mezz connector DOES NOT specify the pin numbers. AS such I have chosen my own convention. When building this part for layout, the pin locations need to be mirrored vertically for all four IEEE connectors in order for this to be consistent with the mezz board. Please TRIPLE check



This is what the layout should look like looking down from the top of the board

VCC2V5

J16_2

M1_DEMODA_DATA0	3	4		M1_DEMODA_DATA1
M1_DEMODA_DATA2	5	6		M1_DEMODA_DATA3
M1_DEMODA_DATA4	7	8		M1_DEMODA_DATA5
M1_DEMODA_DATA6	9	10		M1_DEMODA_DATA7
M1_DEMODA_DATA8	11	12		M1_DEMODA_DATA9
M1_DEMODA_DATA10	13	14		M1_DEMODA_DATA11
M1_DEMODA_DATA12	15	16		M1_DEMODA_DATA13
M1_DEMODA_DATA14	17	18		M1_DEMODA_DATAX
M1_DEMODA_S0	19	20		M1_DEMODA_S1
M1_AUX2	21	22		M1_AUX3
M1_AUX4	23	24		M1_CLOCK3
	25	26		
M1_COMB2_S0	27	28		M1_COMB2_S1
M1_COMB2_DATA0	29	30		M1_COMB2_DATA1
M1_COMB2_DATA2	31	32		M1_COMB2_DATA3
M1_COMB2_DATA4	33	34		M1_COMB2_DATA5
M1_COMB2_DATA6	35	36		M1_COMB2_DATA7
M1_COMB2_DATA8	37	38		M1_COMB2_DATA9
M1_COMB2_DATA10	39	40		M1_COMB2_DATA11
M1_COMB2_DATA12	41	42		M1_COMB2_DATA13
M1_COMB2_DATA14	43	44		M1_COMB2_DATA15
	45	46		
M1_COMB1_S0	47	48		M1_COMB1_S1
M1_COMB1_DATA0	49	50		M1_COMB1_DATA1
M1_COMB1_DATA2	51	52		M1_COMB1_DATA3
M1_COMB1_DATA4	53	54		M1_COMB1_DATA5
M1_COMB1_DATA6	55	56		M1_COMB1_DATA7
M1_COMB1_DATA8	57	58		M1_COMB1_DATA9
M1_COMB1_DATA10	59	60		M1_COMB1_DATA11
M1_COMB1_DATA12	61	62		M1_COMB1_DATA13
M1_COMB1_DATA14	63	64		M1_COMB1_DATA15
	65	66		
M1_POWER_DATA0	67	68		M1_POWER_DATA1
M1_POWER_DATA2	69	70		M1_POWER_DATA3
M1_POWER_DATA4	71	72		M1_POWER_DATA5
M1_POWER_DATA6	73	74		M1_POWER_DATA7
	75	76		
	77	78		
MEZZ5V5p	79	80		MEZZ5V5p
MEZZ3V7p	81	82		MEZZ3V7p
MEZZ5V5n	83	84		MEZZ5V5n

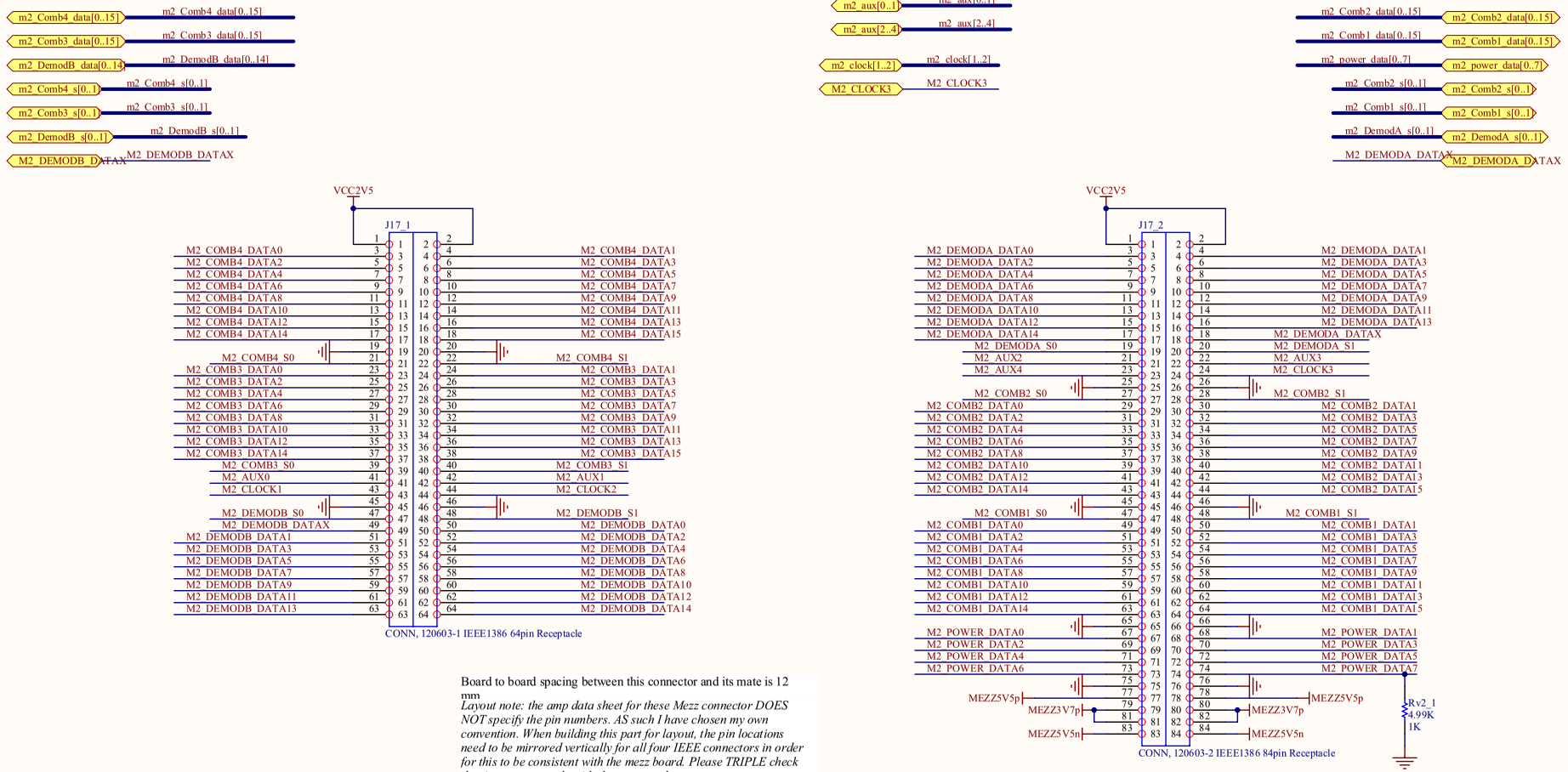
Rv2_2
4.99K
1K

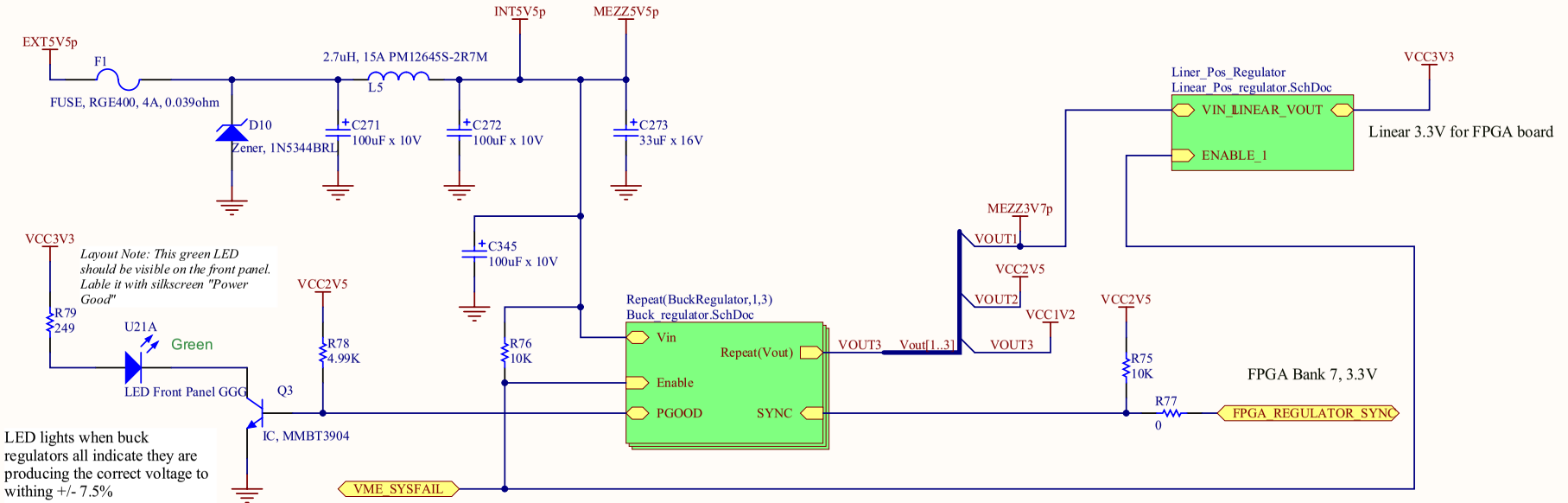
CONN, 120603-2 IEEE1386 84pin Receptacle

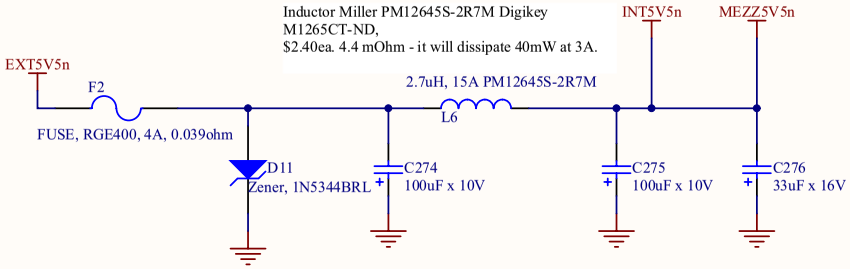
Note: power_data[5] is data out from mezz, power_data[6] is not used, and power_data[7] is the mezz regulator enable.

Mezz Module 1
Connects to FPGA banks 11 and 13.
Located on SYSACE side of board.

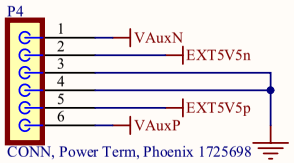
Title: **McGill Digital fMUX FPGA Motherboard**		
Size: B	Number: Mezz Connector Pair 1	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Mezz1.SchDoc	Drawn By: N.Starinski, UdeM	


m2_Comb4_data[0..15]
m2_Comb4_data[0..15]
m2_Comb3_data[0..15]
m2_Comb3_data[0..15]
m2_DemodB_data[0..14]
m2_DemodB_data[0..14]
m2_Comb4_s[0..1]
m2_Comb4_s[0..1]
m2_Comb3_s[0..1]
m2_Comb3_s[0..1]
m2_DemodB_s[0..1]
m2_DemodB_s[0..1]
M2_DEMODB_DATAX
M2_DEMODB_DATAX
m2_aux[0..1]
m2_aux[0..1]
m2_aux[2..4]
m2_aux[2..4]
m2_clock[1..2]
m2_clock[1..2]
M2_CLOCK3
M2_CLOCK3
m2_DemodA_data[0..14]
m2_DemodA_data[0..14]
m2_Comb2_data[0..15]
m2_Comb2_data[0..15]
m2_Comb1_data[0..15]
m2_Comb1_data[0..15]
m2_power_data[0..7]
m2_power_data[0..7]
m2_Comb2_s[0..1]
m2_Comb2_s[0..1]
m2_Comb1_s[0..1]
m2_Comb1_s[0..1]
m2_DemodA_s[0..1]
m2_DemodA_s[0..1]
M2_DEMODA_DATAX
M2_DEMODA_DATAX
VCC2V5
J17_1
M2_COMB4_DATA0
M2_COMB4_DATA1
M2_COMB4_DATA2
M2_COMB4_DATA3
M2_COMB4_DATA4
M2_COMB4_DATA5
M2_COMB4_DATA6
M2_COMB4_DATA7
M2_COMB4_DATA8
M2_COMB4_DATA9
M2_COMB4_DATA10
M2_COMB4_DATA11
M2_COMB4_DATA12
M2_COMB4_DATA13
M2_COMB4_DATA14
M2_COMB4_DATA15
M2_COMB4_S0
M2_COMB4_S1
M2_COMB3_DATA0
M2_COMB3_DATA1
M2_COMB3_DATA2
M2_COMB3_DATA3
M2_COMB3_DATA4
M2_COMB3_DATA5
M2_COMB3_DATA6
M2_COMB3_DATA7
M2_COMB3_DATA8
M2_COMB3_DATA9
M2_COMB3_DATA10
M2_COMB3_DATA11
M2_COMB3_DATA12
M2_COMB3_DATA13
M2_COMB3_DATA14
M2_COMB3_DATA15
M2_COMB3_S0
M2_COMB3_S1
M2_AUX0
M2_AUX1
M2_CLOCK1
M2_CLOCK2
M2_DEMODB_S0
M2_DEMODB_S1
M2_DEMODB_DATAX
M2_DEMODB_DATA0
M2_DEMODB_DATA1
M2_DEMODB_DATA2
M2_DEMODB_DATA3
M2_DEMODB_DATA4
M2_DEMODB_DATA5
M2_DEMODB_DATA6
M2_DEMODB_DATA7
M2_DEMODB_DATA8
M2_DEMODB_DATA9
M2_DEMODB_DATA10
M2_DEMODB_DATA11
M2_DEMODB_DATA12
M2_DEMODB_DATA13
M2_DEMODB_DATA14
CONN, 120603-1 IEEE1386 64pin Receptacle
VCC2V5
J17_2
M2_DEMODA_DATA0
M2_DEMODA_DATA1
M2_DEMODA_DATA2
M2_DEMODA_DATA3
M2_DEMODA_DATA4
M2_DEMODA_DATA5
M2_DEMODA_DATA6
M2_DEMODA_DATA7
M2_DEMODA_DATA8
M2_DEMODA_DATA9
M2_DEMODA_DATA10
M2_DEMODA_DATA11
M2_DEMODA_DATA12
M2_DEMODA_DATA13
M2_DEMODA_DATA14
M2_DEMODA_DATAX
M2_DEMODA_S0
M2_DEMODA_S1
M2_AUX2
M2_AUX3
M2_AUX4
M2_CLOCK3
M2_COMB2_S0
M2_COMB2_S1
M2_COMB2_DATA0
M2_COMB2_DATA1
M2_COMB2_DATA2
M2_COMB2_DATA3
M2_COMB2_DATA4
M2_COMB2_DATA5
M2_COMB2_DATA6
M2_COMB2_DATA7
M2_COMB2_DATA8
M2_COMB2_DATA9
M2_COMB2_DATA10
M2_COMB2_DATA11
M2_COMB2_DATA12
M2_COMB2_DATA13
M2_COMB2_DATA14
M2_COMB2_DATA15
M2_COMB1_S0
M2_COMB1_S1
M2_COMB1_DATA0
M2_COMB1_DATA1
M2_COMB1_DATA2
M2_COMB1_DATA3
M2_COMB1_DATA4
M2_COMB1_DATA5
M2_COMB1_DATA6
M2_COMB1_DATA7
M2_COMB1_DATA8
M2_COMB1_DATA9
M2_COMB1_DATA10
M2_COMB1_DATA11
M2_COMB1_DATA12
M2_COMB1_DATA13
M2_COMB1_DATA14
M2_COMB1_DATA15
M2_POWER_DATA0
M2_POWER_DATA1
M2_POWER_DATA2
M2_POWER_DATA3
M2_POWER_DATA4
M2_POWER_DATA5
M2_POWER_DATA6
M2_POWER_DATA7
MEZZ5V5p
MEZZ3V7p
MEZZ5V5n
MEZZ5V5p
MEZZ3V7p
MEZZ5V5n
Rv2_1
4.99K
1K
CONN, 120603-2 IEEE1386 84pin Receptacle
Board to board spacing between this connector and its mate is 12 mm
Layout note: the amp data sheet for these Mezz connector DOES NOT specify the pin numbers. AS such I have chosen my own convention. When building this part for layout, the pin locations need to be mirrored vertically for all four IEEE connectors in order for this to be consistent with the mezz board. Please TRIPLE check that it mates properly with the mezz cards.
63
64
61
62
1
2
This is what the layout should look like looking down from the top of the board
Module 2
Connects to FPGA banks 12 and 14.
Located on DDR side of board.
Title
McGill Digital fMUX FPGA Motherboard
Size
B
Number
Mezz Connector Pair 2
Revision
03
Date:
10/14/2007
Sheet of
File:
C:\Documents and Settings\...\Mezz2.SchDoc
Drawn By:
N.Starinski, UdeM

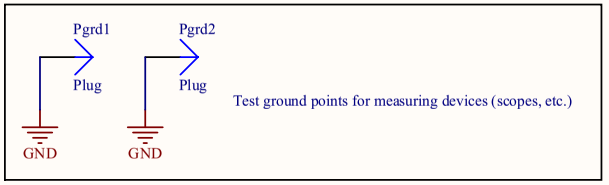




Auxillary Power Connector

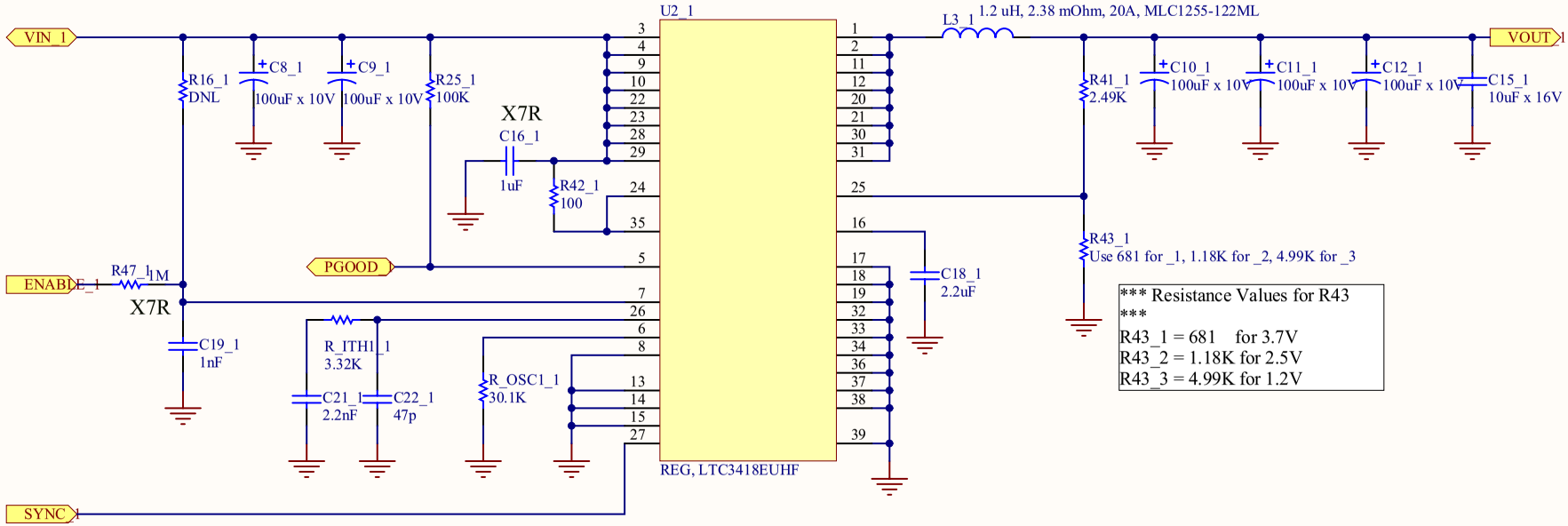


This power can be used when the board is run stand-alone whithout a backplane. Place this part near the VME commectors.

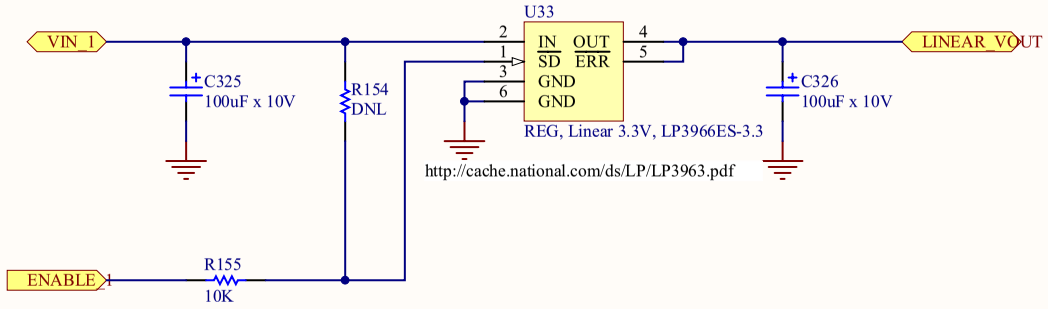


Layout Note: If the input power LC filter is really challenging to fit on the board, we can probably survive without it. Instead of the inductor/caps, we could use: Murata BNX002-01 50V, 10A maxm 30dB at 100KHz, 60dB 5-1000MHz. Datasheet: http://www.murata.com/catalog/c31e.pdf page 145.

Title	**McGill Digital fMUX FPGA Motherboard**	
Size: Letter	Number: Power Delivery	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Power_Delivery.SchDoc	Drawn By: N.Starinski, UdeM	

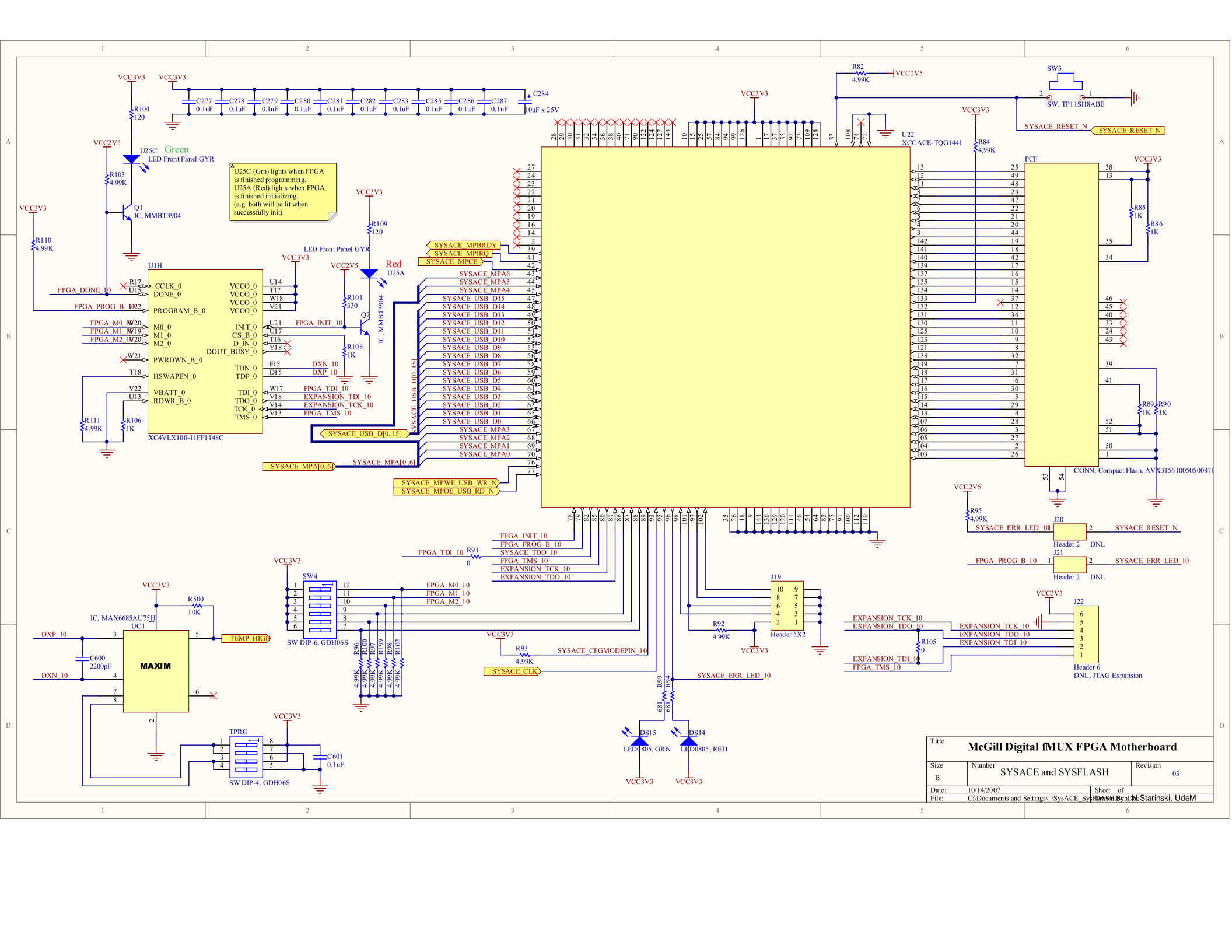


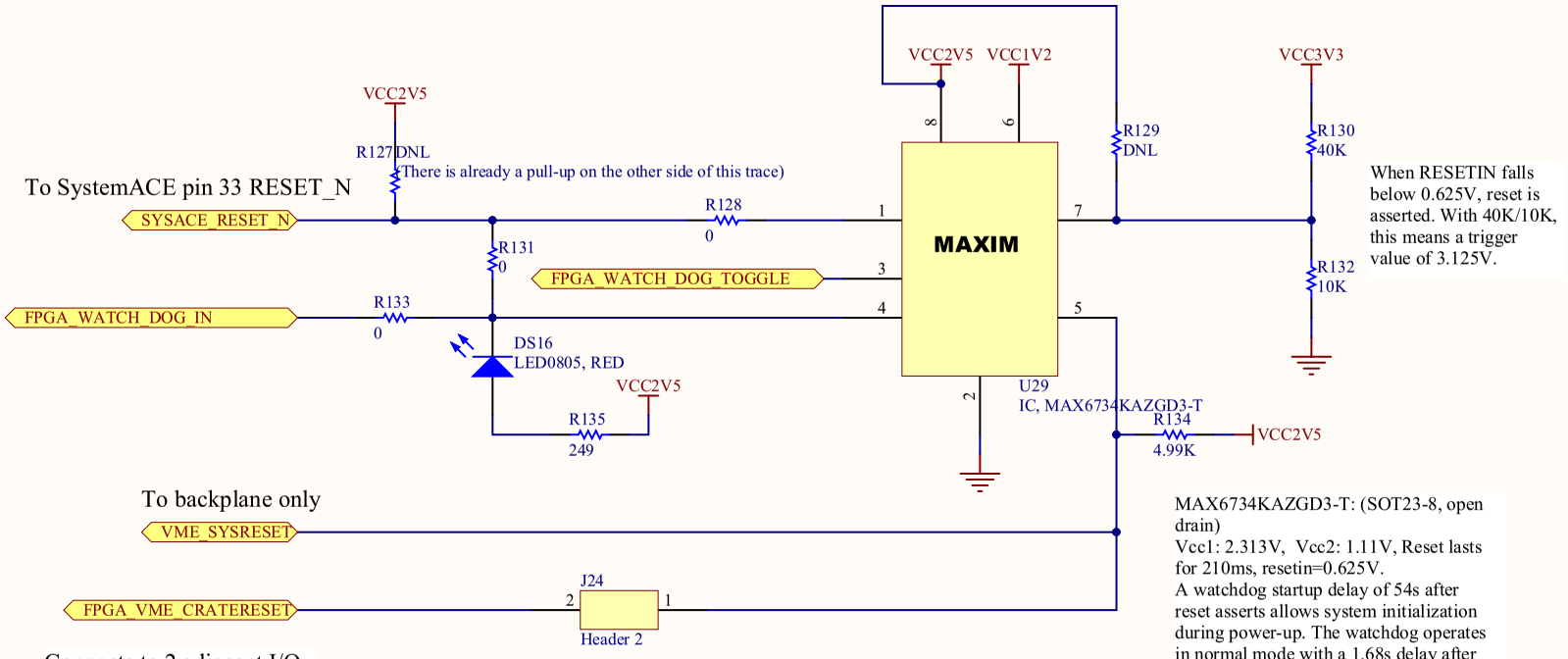
Title	**McGill Digital fMUX FPGA Motherboard**	
Size: A	Number: Buck Regulator	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\...\Buck_regulator.SchDoc	Drawn By: N.Starinski, UdeM	



Layout Note: pay special attention to thermal heat sinking for all regulators to the ground plane.
Kelvin connect the input/output caps to the device leads.

Title	**McGill Digital fMUX FPGA Motherboard**	
Size: A	Number: Linear Positive Regulator	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Linear_Pos_regulator.SchDoc	Drawn By: N.Starinski, UdeM	


U25C (Grn) lights when FPGA is finished programming.
U25A (Red) lights when FPGA is finished initializing.
(e.g. both will be lit when successfully init)
XC4VLX100-11FF1148C
XCCACE-TQG1441
CONN, Compact Flash, AVX31561005050087
SW DIP-6, GDH06S
SW DIP-4, GDH06S
Header 5X2
Header 2
Header 6
DNL, JTAG Expansion
LED0805, GRN
LED0805, RED
SW, TP11SH8ABE
IC, MMBT3904
IC, MAX6685AU75H
MAXIM
McGill Digital fMUX FPGA Motherboard
SYSACE and SYSFLASH
Size B
Number
Revision 03
Date: 10/14/2007
Sheet of
File: C:\Documents and Settings\...\SysACE_SysFlash.SchDoc
Drawn By: N.Starinski, UdeM



This RESET circuit complements the reset circuit on page 7 of the ML402 schematic.
Replace the pushbutton switch on that page with the TP11SH8ABE, wich goes to the front panel.

Title	**McGill Digital fMUX FPGA Motherboard**	
Size: A	Number: Watchdog and Reset	Revision: 03
Date: 10/14/2007	Sheet of	
File: C:\Documents and Settings\..\Watchdog_Reset.SchDoc	Drawn By: N.Starinski, UdeM	