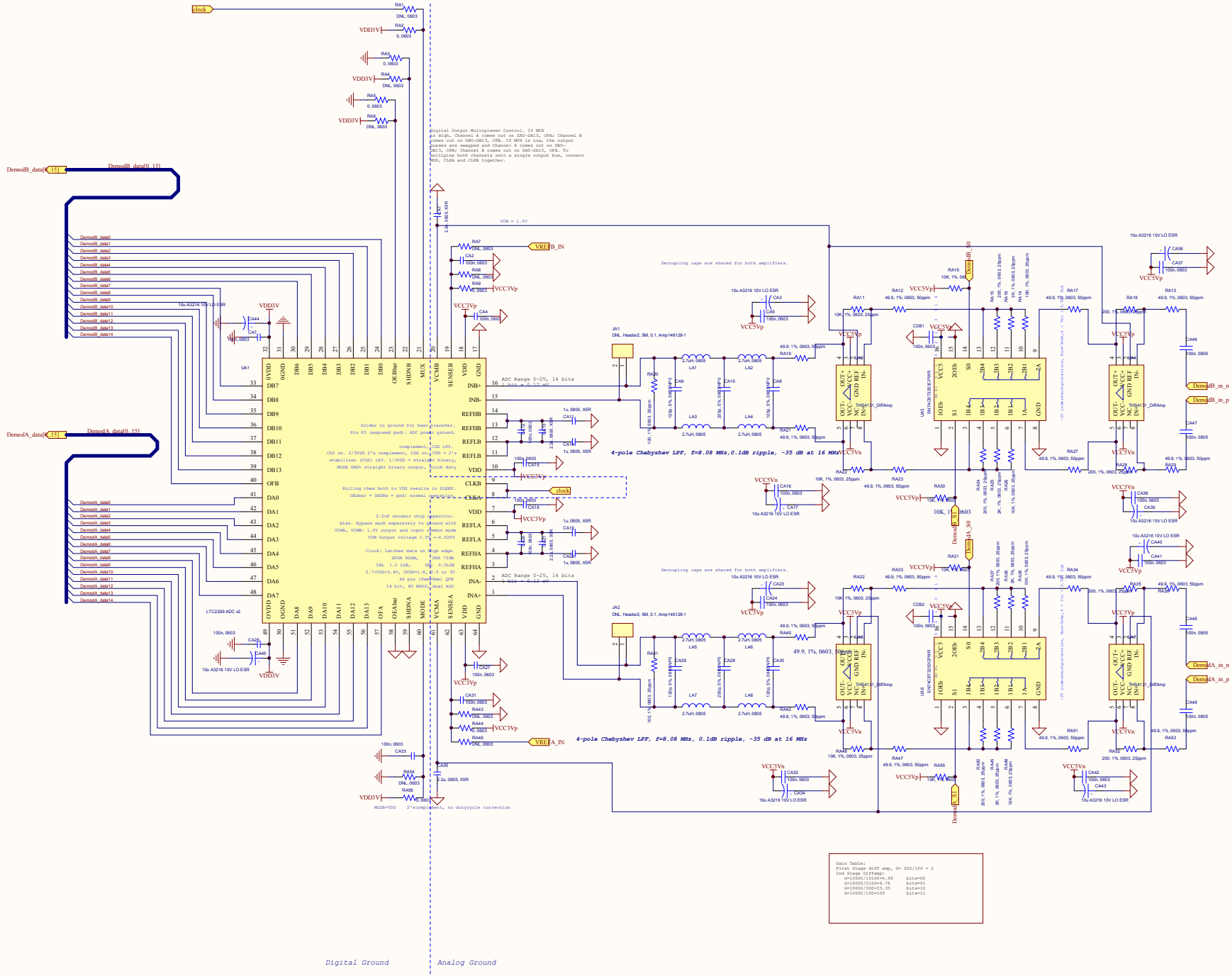
clock
VDD3V
DemodB_data[15]
DemodB_data[0..15]
DemodA_data[15]
DemodA_data[0..15]
LTC2299 ADC x2
Digital Ground
Analog Ground
VCC5Vp
VCC5Vn
VCC3Vp
VREFB_IN
VREFA_IN
4-pole Chebyshev LPF, f=8.08 MHz,0.1dB ripple, -35 dB at 16 MHz
4-pole Chebyshev LPF, f=8.08 MHz, 0.1dB ripple, -35 dB at 16 MHz
Digital Output Multiplexer Control. If MUX is High, Channel A comes out on DA0-DA13, OFA; Channel B comes out on DB0-DB13, OFB. If MUX is Low, the output busses are swapped and Channel A comes out on DB0-DB13, OFB; Channel B comes out on DA0-DA13, OFA. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together.
Solder to ground for heat transfer. Pin 65 (exposed pad): ADC power ground.
complement. CDS off. CDS on, 2/3VDD 2's complement, CDS on, VDD = 2's stabilizer (CDS) off, 1/3VDD = straight binary, MODE GND= straight binary output, clock duty
Pulling them both to VDD results in SLEEP. OExbar = SHDNx = gnd: normal operation.
2.2uF ceramic chip capacitor. bias. Bypass each separately to ground with VCMA, VCMB: 1.5V output and input common mode VCM Output voltage 1.5V +-0.025V
Clock: Latches data on High edge, SFDR 95dB, SNR 73dB INL 1.2 LSB, DNL 0.5LSB 2.7-VDD=3.4V, OVDD=1.8, 2.5 or 3V 64 pin (9mmx9mm) QFN 14 bit, 80 MSPS, dual ADC
ADC Range 0-2V, 14 bits 0.12 mV
Decoupling caps are shared for both amplifiers.
Gain Table:
First Stage diff amp, G= 200/100 = 2
2nd Stage Diffamp:
G=10000/10100=0.99 bits=00
G=10000/2100=4.76 bits=01
G=10000/300=33.33 bits=10
G=10000/100=100 bits=11
Title
Digital fMUX Mezzanine - ADC
Size
A
Number
M.Dobbs, McGill U.
Revision
4
Date:
18/02/2010
File:
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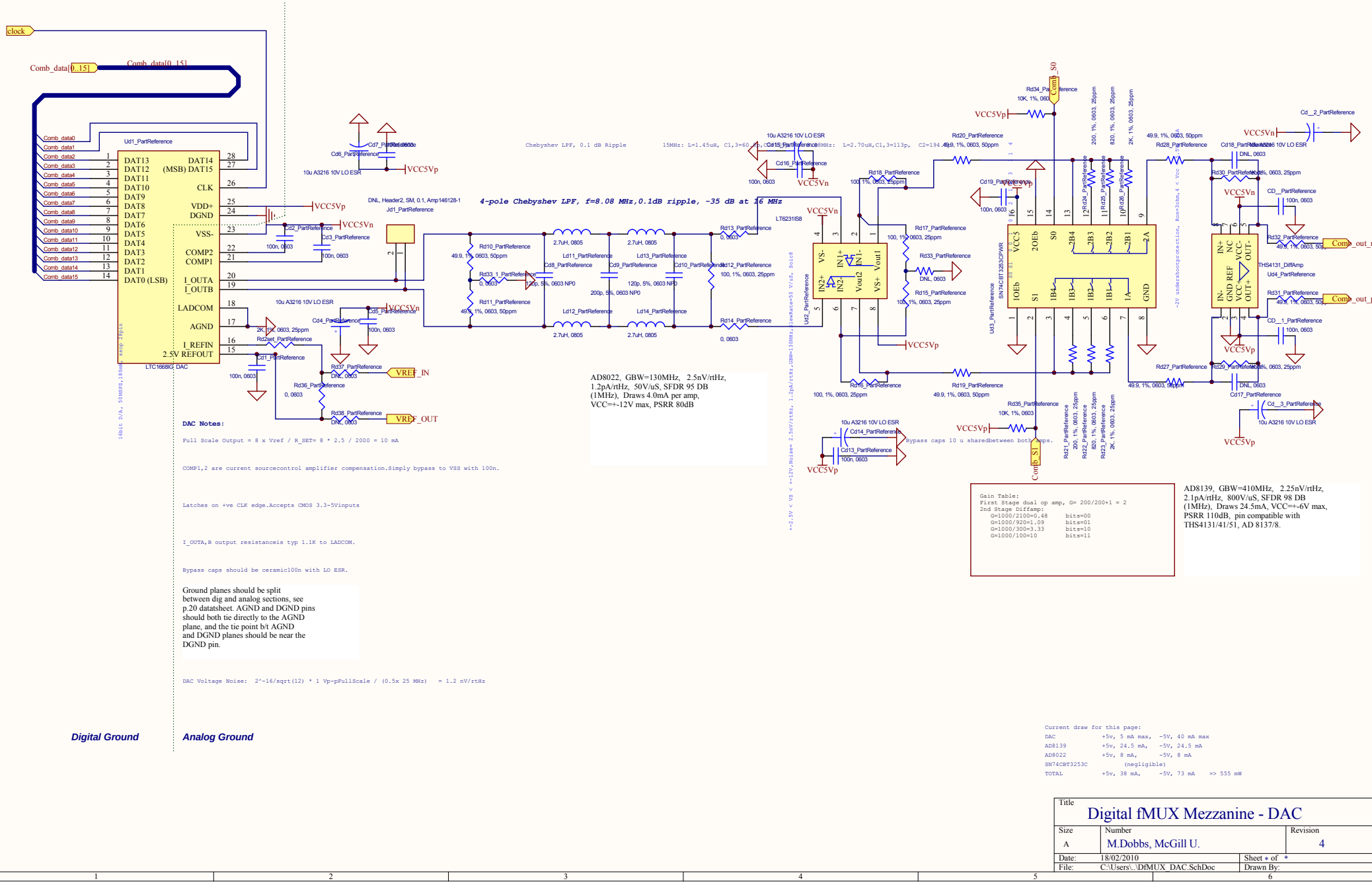
Drawn By:


clock
Comb_data[0..15]
Comb_data[0..15]
Ud1_PartReference
DAT13
DAT12
DAT11
DAT10
DAT9
DAT8
DAT7
DAT6
DAT5
DAT4
DAT3
DAT2
DAT1
DAT0 (LSB)
DAT14
(MSB) DAT15
CLK
VDD+
DGND
VSS-
COMP2
COMP1
I_OUTA
I_OUTB
LADCOM
AGND
I_REFIN
2.5V REFOUT
LTC1668IG DAC
VCC5Vp
VCC5Vn
Cd2_PartReference
Cd3_PartReference
100n, 0603
Cd6_PartReference
Cd7_PartReference
10u A3216 10V LO ESR
Cd4_PartReference
Cd5_PartReference
2K, 1%, 0603, 25ppm
Rd2set_PartReference
Cd1_PartReference
Rd37_PartReference
Rd36_PartReference
0, 0603
DNL, 0603
VREF_IN
VREF_OUT
DNL, Header2, SM, 0.1, Amp146128-1
Jd1_PartReference
4-pole Chebyshev LPF, f=8.08 MHz,0.1dB ripple, -35 dB at 16 MHz
Rd10_PartReference
Rd33_1_PartReference
Rd11_PartReference
49.9, 1%, 0603, 50ppm
2.7uH, 0805
Ld11_PartReference
Ld12_PartReference
Ld13_PartReference
Ld14_PartReference
Cd8_PartReference
Cd9_PartReference
Cd10_PartReference
120p, 5%, 0603 NP0
200p, 5%, 0603 NP0
Rd13_PartReference
Rd12_PartReference
Rd14_PartReference
100, 1%, 0603, 25ppm
LT6231IS8
Ud2_PartReference
Rd17_PartReference
Rd33_PartReference
Rd15_PartReference
Rd16_PartReference
Rd19_PartReference
Rd18_PartReference
Rd20_PartReference
Cd19_PartReference
Ud3_PartReference
SN74CBT3253CPWR
Rd21_PartReference
Rd22_PartReference
Rd23_PartReference
Rd24_PartReference
Rd25_PartReference
Rd26_PartReference
Rd27_PartReference
Rd28_PartReference
Rd29_PartReference
Rd30_PartReference
Rd31_PartReference
Rd32_PartReference
Rd34_PartReference
Rd35_PartReference
10K, 1%, 0603
Comb_S0
Comb_S1
Cd14_PartReference
Cd13_PartReference
Cd15_PartReference
Cd16_PartReference
Cd18_PartReference
Cd__1_PartReference
Cd__2_PartReference
Cd__3_PartReference
THS4131_DiffAmp
Ud4_PartReference
Comb_out_n
Comb_out_p
Chebyshev LPF, 0.1 dB Ripple
15MHz: L=1.45uH, C1,3=60.7p, C2=194.8p
8MHz: L=2.70uH,C1,3=113p, C2=194.8p
AD8022, GBW=130MHz, 2.5nV/rtHz, 1.2pA/rtHz, 50V/uS, SFDR 95 DB (1MHz), Draws 4.0mA per amp, VCC=+-12V max, PSRR 80dB
AD8139, GBW=410MHz, 2.25nV/rtHz, 2.1pA/rtHz, 800V/uS, SFDR 98 DB (1MHz), Draws 24.5mA, VCC=+-6V max, PSRR 110dB, pin compatible with THS4131/41/51, AD 8137/8.
Gain Table:
First Stage dual op amp, G= 200/200+1 = 2
2nd Stage Diffamp:
G=1000/2100=0.48 bits=00
G=1000/920=1.09 bits=01
G=1000/300=3.33 bits=10
G=1000/100=10 bits=11
DAC Notes:
Full Scale Output = 8 x Vref / R_SET= 8 * 2.5 / 2000 = 10 mA
COMP1,2 are current sourcecontrol amplifier compensation.Simply bypass to VSS with 100n.
Latches on +ve CLK edge.Accepts CMOS 3.3-5Vinputs
I_OUTA,B output resistanceis typ 1.1K to LADCOM.
Bypass caps should be ceramic100n with LO ESR.
Ground planes should be split between dig and analog sections, see p.20 datatsheet. AGND and DGND pins should both tie directly to the AGND plane, and the tie point b/t AGND and DGND planes should be near the DGND pin.
DAC Voltage Noise: 2^-16/sqrt(12) * 1 Vp-pFullScale / (0.5x 25 MHz) = 1.2 nV/rtHz
Bypass caps 10 u sharedbetween both opamps.
Current draw for this page:
DAC +5v, 5 mA max, -5V, 40 mA max
AD8139 +5v, 24.5 mA, -5V, 24.5 mA
AD8022 +5v, 8 mA, -5V, 8 mA
SN74CBT3253C (negligible)
TOTAL +5v, 38 mA, -5V, 73 mA => 555 mW
Digital Ground
Analog Ground
Title
Digital fMUX Mezzanine - DAC
Size
A
Number
M.Dobbs, McGill U.
Revision
4
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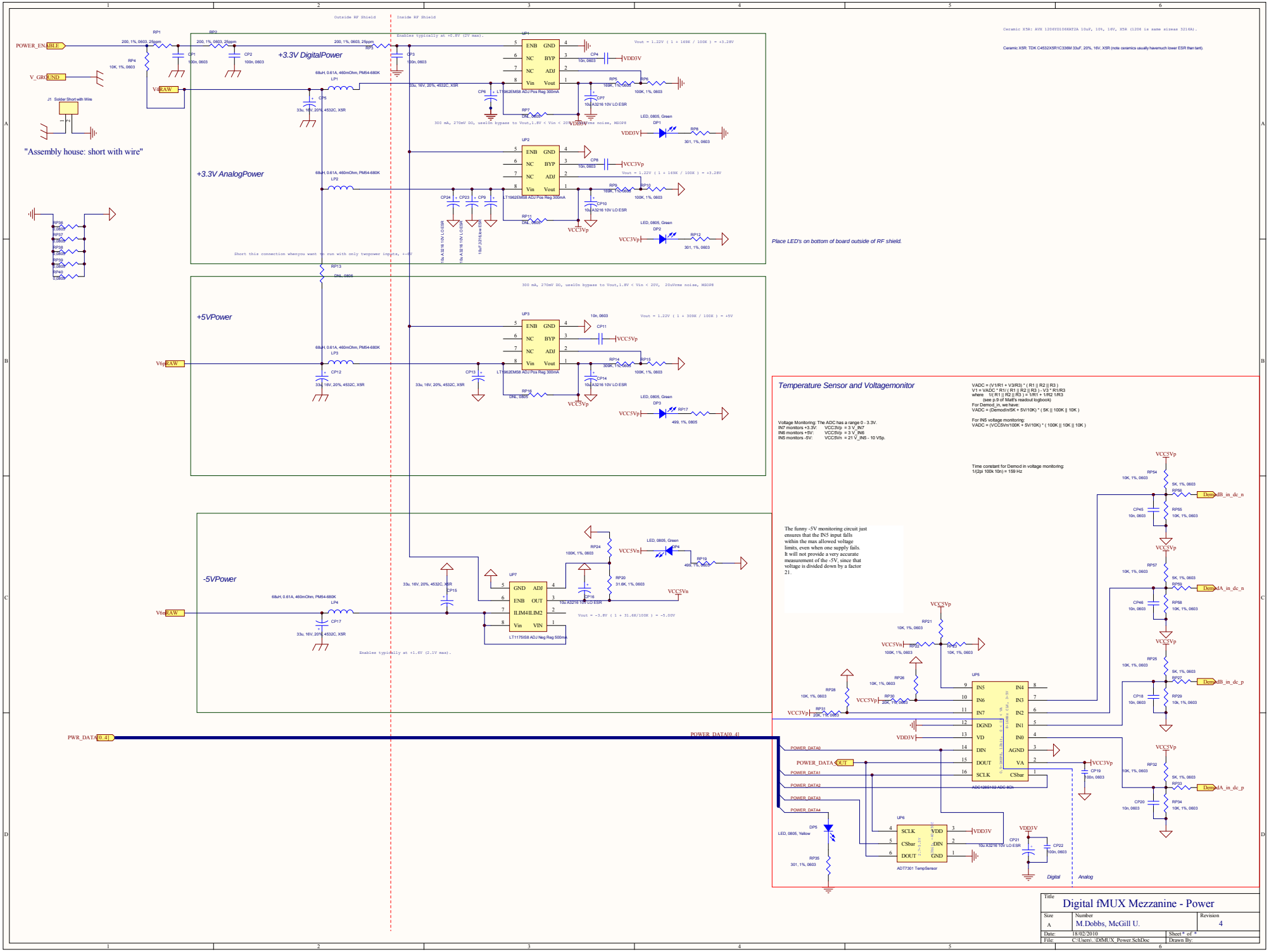
Outside RF Shield
Inside RF Shield
+3.3V DigitalPower
+3.3V AnalogPower
+5VPower
-5VPower
"Assembly house: short with wire"
Place LED's on bottom of board outside of RF shield.
Temperature Sensor and Voltagemonitor
The funny -5V monitoring circuit just ensures that the IN5 input fails within the max allowed voltage limits, even when one supply fails. It will not provide a very accurate measurement of the -5V, since that voltage is divided down by a factor 21.
Digital
Analog
Digital fMUX Mezzanine - Power
M.Dobbs, McGill U.
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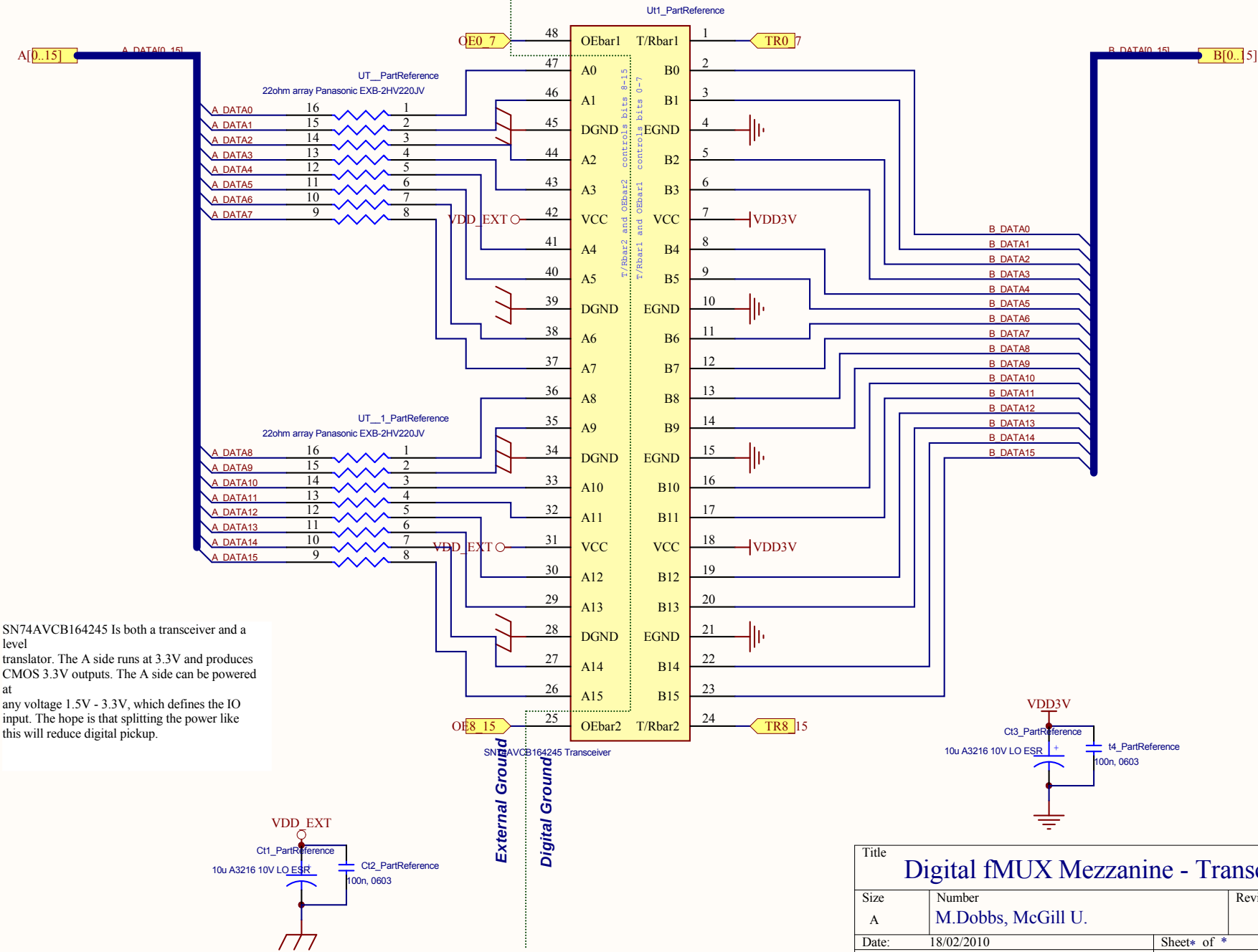
Ut1_PartReference
A[0..15]
A_DATA[0..15]
B[0..15]
B_DATA[0..15]
OE0_7
OE8_15
TR0_7
TR8_15
OEbar1
T/Rbar1
OEbar2
T/Rbar2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
DGND
EGND
VCC
VDD_EXT
VDD3V
T/Rbar2 and OEbar2 controls bits 8-15
T/Rbar1 and OEbar1 controls bits 0-7
SN74AVCB164245 Transceiver
UT__PartReference
22ohm array Panasonic EXB-2HV220JV
UT__1_PartReference
22ohm array Panasonic EXB-2HV220JV
A_DATA0
A_DATA1
A_DATA2
A_DATA3
A_DATA4
A_DATA5
A_DATA6
A_DATA7
A_DATA8
A_DATA9
A_DATA10
A_DATA11
A_DATA12
A_DATA13
A_DATA14
A_DATA15
B_DATA0
B_DATA1
B_DATA2
B_DATA3
B_DATA4
B_DATA5
B_DATA6
B_DATA7
B_DATA8
B_DATA9
B_DATA10
B_DATA11
B_DATA12
B_DATA13
B_DATA14
B_DATA15
SN74AVCB164245 Is both a transceiver and a level
translator. The A side runs at 3.3V and produces
CMOS 3.3V outputs. The A side can be powered at
any voltage 1.5V - 3.3V, which defines the IO
input. The hope is that splitting the power like
this will reduce digital pickup.
External Ground
Digital Ground
VDD_EXT
Ct1_PartReference
10u A3216 10V LO ESR
Ct2_PartReference
100n, 0603
VDD3V
Ct3_PartReference
10u A3216 10V LO ESR
t4_PartReference
100n, 0603
Title
Digital fMUX Mezzanine - Transceiver
Size
A
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Layer Stackup Suggestion

Silkscreen, Solder Mask

1. Top signal Traces
2. Ground (closes the RF shield)
3. +3V Analog plane, inner Signals for gain select, etc.
4. Power planes: VDD_EXT, +3VDigital, +5V analog
5. signal traces for clock and some voltage references. -5V power plane
6. Bottom signal traces

Silkscreen, Solder Mask

All traces should be 100 +-10 ohm controlledimpedance. Differential pairs should be runtogether.

Try to make the layout compatible with the www.pcbexpress.com specifications:

Allowed Drill sizes: 0.008 .0135 .020 .025 .029 .035 .040 .046 .052 .061 .067 .079 .093 .11 .125 .15 .192

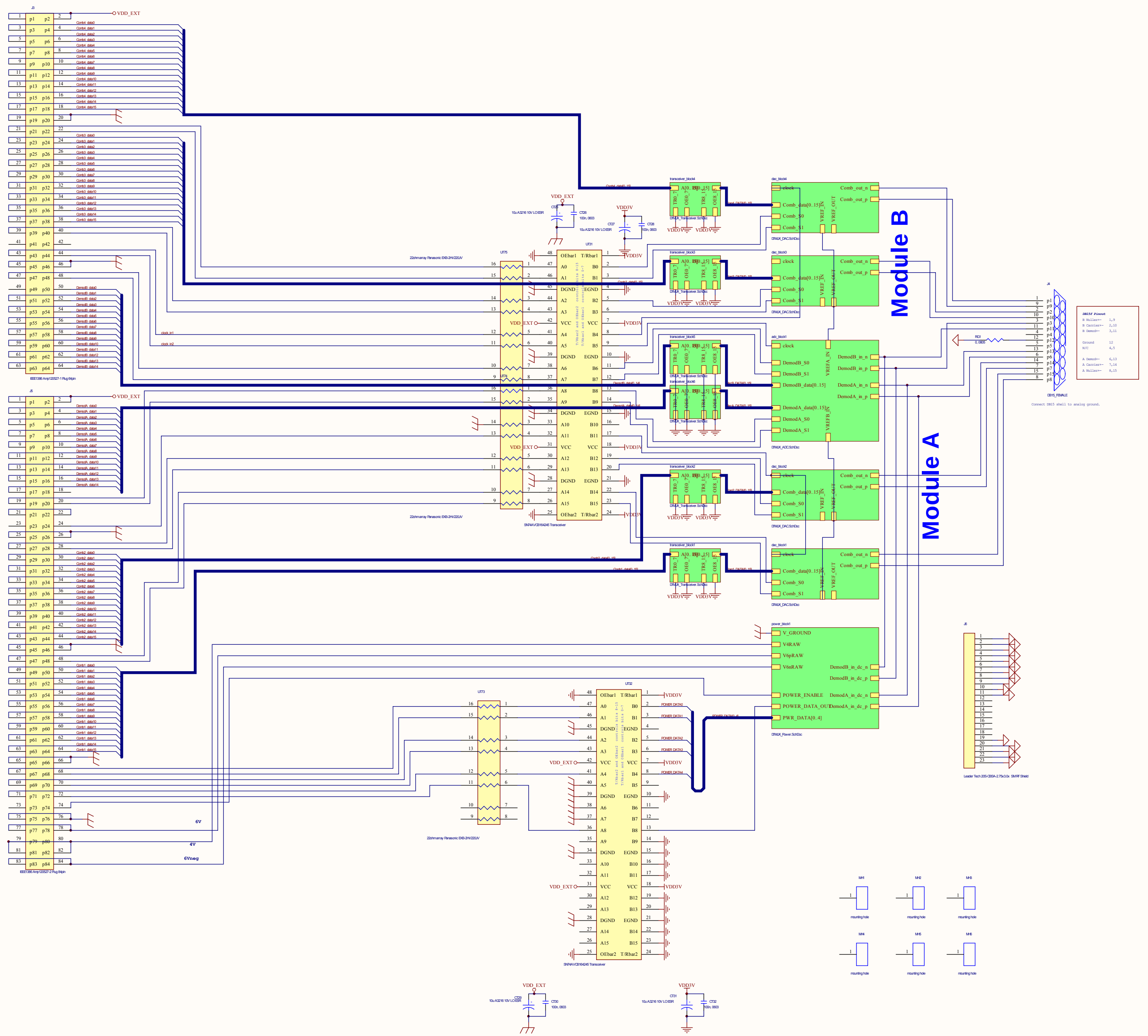
All spaces/traces are a minimum of .007 (7 mil) or larger.

Mount Holes: 4-40, back of board are connected to external ground, front of board are floating.

RF Shield (build this partcarefully!). All mounting pointsare connected to ANALOG ground.

RF Shield outer dimensions are 80x73mm.

This connection pf p21 to p22 is for Rev3 only. The FPGA will toggle p21 high then low, and if it sees this signal on p22, it will know it is talking to a Rev 3 board.



Title	Digital fMUX Mezzanine - TOP	
Size: A	Number: M.Dobbs, McGill U.	Revision: 4
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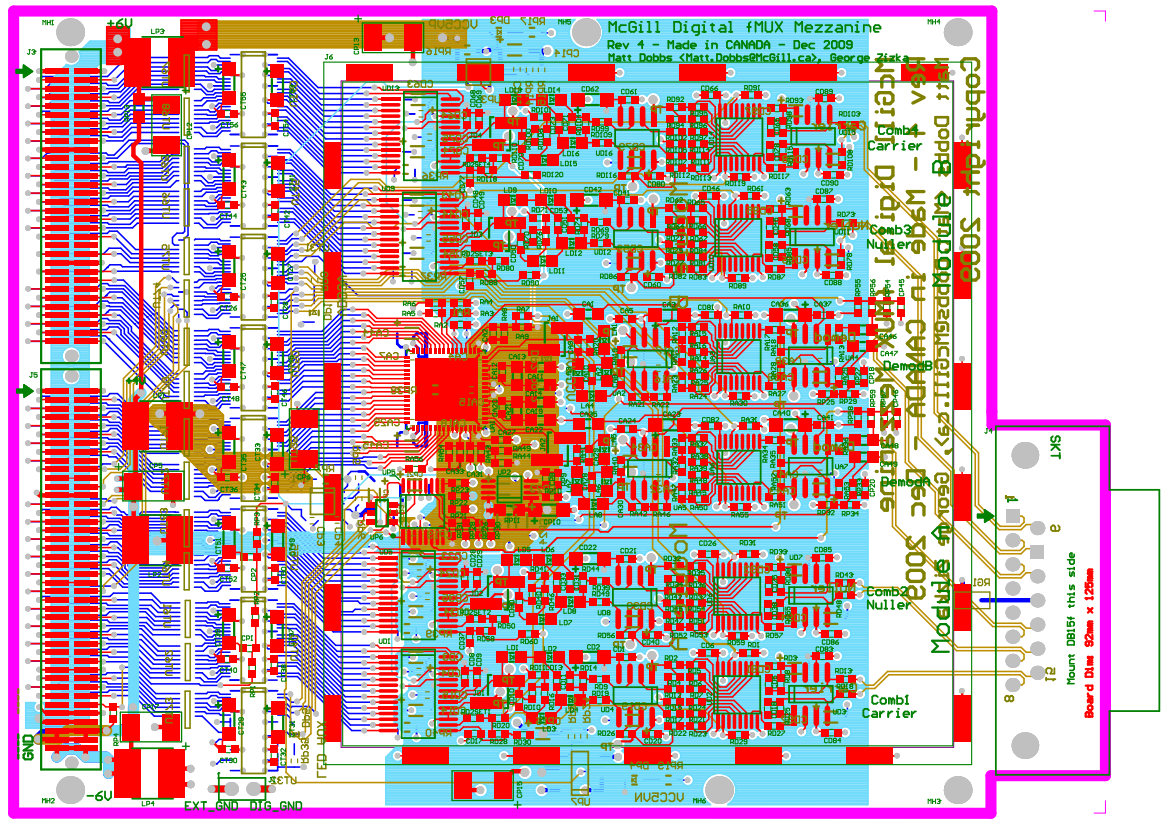
McGill: DfMux Mezzanine Board Rev4

Nominal Size: 4.920 x 3.625 inches

FINISHED BOARD: 0.062 (Nom) 370HR

ARRANGE LAYERS SEQUENTIALLY: L1-L6

Thieving Copper Dots CAN be added to INNER layers if needed



L1 (TOP) .GTL

TOP IDENT (.GTO)

L3 (ML1) .G1

L5 (ML2) .G2

L6 (BOT) .GBL

BOARD OUTLINE KEEPOUT