

# CSCI370 Computer Architecture: Homework 1

**Due date: On or before Monday, February 13, 2023**

**Absolutely no copying others' works**

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- Upload the completed homework to the section of "COVID-19 Exams, Homeworks, & Programming Exercises" of [Blackboard](#).
- The purpose of homeworks is for students to practice for the exams without others' help, so the penalty of mistakes will be minor.
- Without practicing for the exams properly, students will not be able to do well on the exams.

1. (55% total) Consider two different implementations of the same instruction set architecture. The instructions can be divided into three classes according to their CPI (class A, B, and C). The clock rate and CPI of each implementation are given in the following table:

	Clock rate	CPI Class A	CPI Class B	CPI Class C
P1	4.0 GHz	3	4	3
P2	3.0 GHz	3	2	2

- a. (25%) Given a program with a ~~dynamic instruction count~~ of  $10^5$  instructions divided into classes as follows: 30% class A, 30% class B, and 40% Class C, which implementation is faster?

<sup>†</sup>Hint: You have to find the execution times.

Ans>

$$P1: (3 * 10^5 * 0.3) + (4 * 10^5 * 0.3) + (3 * 10^5 * 0.4) = 330000 / 4.0 * 10^9 = 82.5 * 10^{-6} \text{ sec}$$

$$P2: (3 * 10^5 * 0.3) + (2 * 10^5 * 0.3) + (2 * 10^5 * 0.4) = 230000 / 3.0 * 10^9 = 76.6 * 10^{-6} \text{ sec}$$

P2 is faster than P1

- b. (15%) What is the global CPI for each implementation?

<sup>†</sup>Hint:  $\text{global CPI} = \frac{\text{execution time} \times \text{clock rate}}{\text{number of instructions}}$ , where the execution time can be found from the solution of the previous question.

Ans>

$$\blacksquare \text{CPI}_{P1} = (82.5 * 10^{-6} \text{ sec} * 4.0) / 10^5 = 3.3$$

$$\blacksquare \text{CPI}_{P2} = (76.6 * 10^{-6} \text{ sec} * 3.0) / 10^5 = 2.29$$

- c. (15%) Find the clock cycles required in both cases.

Ans>

$$\blacksquare \text{clock cycles}_{P1} = 330000 \text{ Cycles}$$

$$\blacksquare \text{clock cycles}_{P2} = 230000 \text{ Cycles}$$

2. (15%) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 2.5 GHz and voltage of 1.5 V. Assume that, on average, it consumed 12 W of static power and 80 W of dynamic power. Find the average capacitive load.

Ans> 
$$CL = 80 / (0.5 * 1.5^2 * 2.5 * 10^9) = 2.84 \times 10^{-8}$$

Capacitive load  $\cong$  
$$CL = 12 / (0.5 * 1.5^2 * 2.5 * 10^9) = 4.26 \times 10^{-9}$$

Average =  $1.63 \times 10^{-8}$

3. (30% total) The following table shows manufacturing data of a processor:

Wafer diameter	Dies per wafer	Defects per unit area	Cost per wafer	# of critical steps
30 cm	90	0.03 defects/cm <sup>2</sup>	30	3

- a. (10%) Find the yield.

Ans> 
$$1 / (1 + (0.03 * (3.14 * 15 * 15) / 90))^{*3} = 0.53$$

Yield = 0.53

- b. (10%) Find the cost per die.

Ans> 
$$30 / (90 * 0.53) = 0.62$$

Cost per die = 0.62

- c. (10%) If the number of dies per wafer is increased by 15% and the defects per area unit increase by 20%, find the die area and yield.

Ans>