ADAM TABACK

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EDUCATION

University of Toronto September 2022 - May 2026
B.A.Sc in Computer Engineering + PEY *GPA: 3.9/4*

- **Awards:** Top 30 Average in Computer Engineering, Dean's List, Danny Goldberg Memorial Scholarship
- **Relevant Courses:** Data Structures and Algorithms (**C**), Final Mark: 100%, Programming Fundamentals (**C++**), Final Mark: 92%, Introduction to Deep Learning (**Pytorch**), Computer Organization (**Assembly, C, Verilog**): 96%

SKILLS

Computer Languages	Python, C, C++, Verilog, CUDA, Nios II Assembly
Operating Systems	Linux, Mac OS, Windows
Packages	Scikit-Learn, Pytorch, Numpy, Pandas, Matplotlib, CMake
Tools	High Performance Computing (HPC), Quartus, Modelsim, LaTeX, Github, Git, Llama, Hugging Face, CUDA

WORK EXPERIENCE

Deep Learning Architecture Research Intern May 2024 - September 2024
Moshovos Lab - University of Toronto

- Implemented Entropy Compression technique, Asymmetric Numeral Systems, in **Python** and **C**, using lookup tables
- Achieved compression rates of $1.5-2.3\times$ when applied to weights and activations of pretrained **Pytorch** models, speeding up transfer of data from memory to CPU
- Wrote optimized code in **C** using bit-level operations in preparation for digital logic implementation
- Created **PyPi** package for Asymmetric Numeral Systems, from the code I developed
- **Patent Pending** for work done

Teaching Assistant Fall 2023 - Present
*Introduction to Computer Programming (**Python**) & Data Structures and Algorithms (**C**)*

- Ran weekly labs, helping students complete lab assignments and assessing their performance
- Received positive feedback from students for clear communication and quick debugging

PROJECTS

Cartoon Image Generation Using Generative AI May - August 2024
Introduction to Deep Learning (APS360) - University of Toronto

- Developed a Generative Adversarial Network and Variational Autoencoder to generate images of cartoon emojis, using **PyTorch**
- Achieved realistic new images that closely matched training images with the Variational Autoencoder architecture, with dimensions 128x128

FPGA Processor January - May 2024
Computer Organization (ECE243) - University of Toronto

- Created RTL design for a 16 bit processor in **Verilog** to run on a FPGA, with associated **Assembly language** and **Python** parser
- Ran **Assembly** programs on the processor to add up numbers from 1 to 30 and find biggest element in an array

INTERESTS/COMMITMENTS

Write, Record and Produce original music; Latest Release: **Don't Know - Adam Taback** (Apple Music/Spotify)