Project VLSI System Design Project

The Design Project is a group assignment. Students are obliged to form groups of four until May 4th.

Milestones and Presentations

For each **milestone** please submit the following at the day of the milestone (preferably by e-mail).

- Short written report (approx. 2 pages including figures)
- VHDL code/assembler code of required components

At each milestone a demonstration of the working components is expected (during exercises).

Project Kick-off: 16.5.2018

Each group will give a short presentation (10 min + 5 min Q&A) that shows that they understood the challenges of the upcoming project. We recommend considering the following points:

- Project partitioning: Which major system components were defined? Who is responsible for the implementation of which part?
- Interfaces: How exactly is the data transferred between the system components? How do the components communicate?
- System level design: What is the system level design approach for each component? Which sub-components will be necessary?

Milestone 1: 30.5.2018

ALU

- ALU from “Processor Exercise 1” completed
- The testbench runs without errors

Processor

- Processor from “Processor Exercise 2” completed
- Processor runs successful with debugger module in hardware
- Unlike the other milestones, a written report is **not** required for this milestone.

Milestone 2: 13.6.2018

PS2 interface

- PS2 interface capable of reading scan codes from keyboard, operational in simulation
- Successful test on FPGA board using given test environment

Processor

- Implementation of LOADI*/STOREI* commands, all registers (basic load/store functionality)
- Correct functionality of PSW register
- Change software of debug module to test implemented functionality in hardware

VGA Interface

- VGA Interface outputting a test picture with correct timing
- Successful test on the FPGA board
- It should become obvious how the design can be extended for character output.

Software

- Extend the test program of the debugger module so that the new functions of the processor can be tested
- Successful test of the processor in hardware with the modified debugger module

Milestone 3: 27.6.2018

PS2 interface

- Interface to processor (via interrupt)
- Conversion from scan codes to characters either implemented in software or hardware

Processor

- Implementation of CALL/RET
- Implementation of Interrupt handling (IEN, IFLAG registers), RETI
- Change software of debug module to test implemented functionality in hardware

VGA Interface

- VGA component capable of outputting data from a character memory
- Interface to write character memory from processor
- Successful test on FPGA board

Software

- Interrupt service routine for PS2 interface, successfully tested in simulation (Debugger)

Milestone 4: 11.7.2018

- Software interface for VGA component
- Integration of all components
- Successful test of complete design (hardware + software) on FPGA board

Final Presentation: 18.7.2018 (approx. 15 minutes)