ALBERT-LUDWIGS-
UNIVERSITÄT FREIBURG

IMTEK

VLSI System Design
Project Introduction

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Course plan

- Module “VLSI System Design” consists of two sub-modules: lecture and practical exercises.

VLSI System Design module

Lecture

- Written exam
  - Participation requirements:
    - 70% in written reports and source code
    - Final presentation passed
  - Determines the final grade of the course

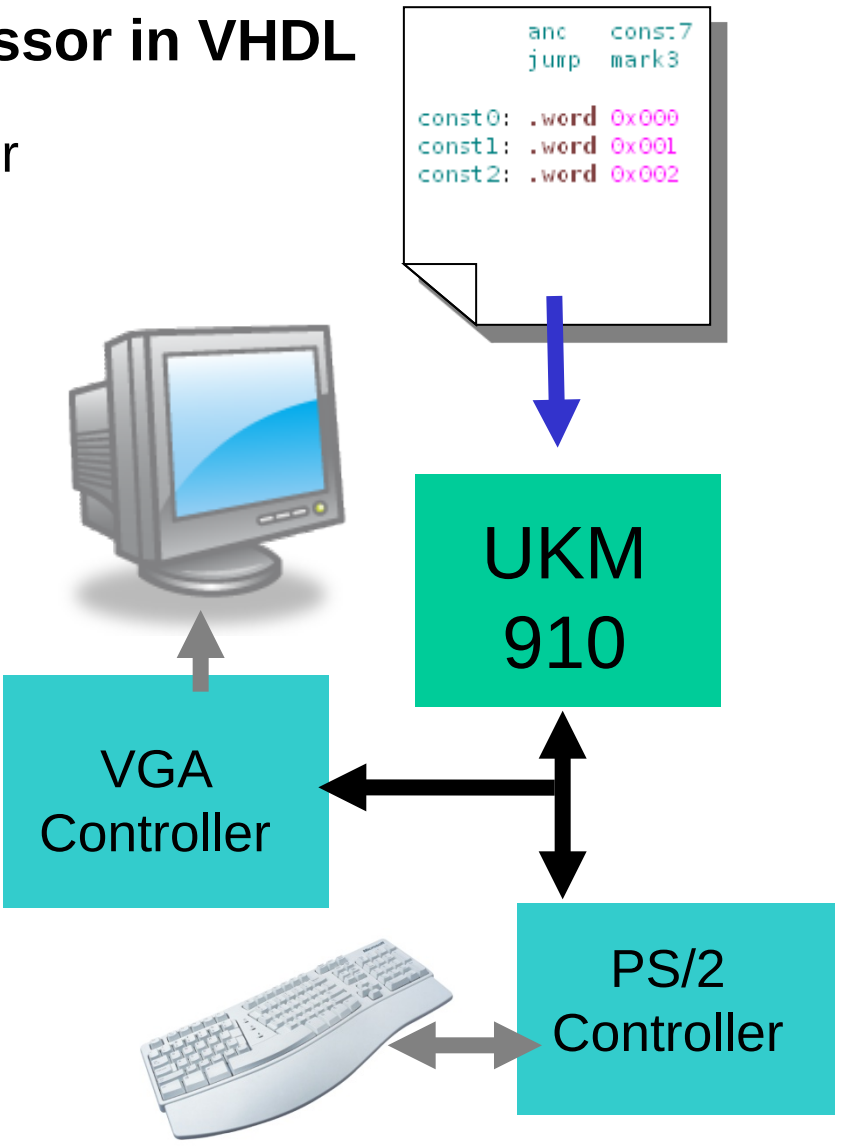
Project

- Written reports: one per Milestone, plus one final report
- Milestone sign-off (checklist)
- Commented VHDL and assembler source code
- Final presentation 18.07.2018

The Project – Goal

Implementation of an advanced processor in VHDL

- Based on the simpler “UKM901” processor presented in the lecture
- Improved architecture and instruction set:
  - indirect addressing
  - calling of subroutines
  - interrupts
- Communication with the outside world:
  - VGA controller
  - PS/2 (keyboard) controller
  - …
- Must be synthesizable to an actual FPGA
  - Run a useful program
  - Example: Calculator



Overview – What will we do?

- **VHDL Course – Lecture and practical exercises (not graded)**
  - VHDL: a Hardware description language
  - Goal: Give you a basic understanding of VHDL
- **Project preparation – Processor exercise**
  - Implement the simple processor from the lecture in VHDL
  - Your first “big” VHDL project
  - Serves as a base for the real project
- **Project Support**
  - We help you with problems/questions regarding your project

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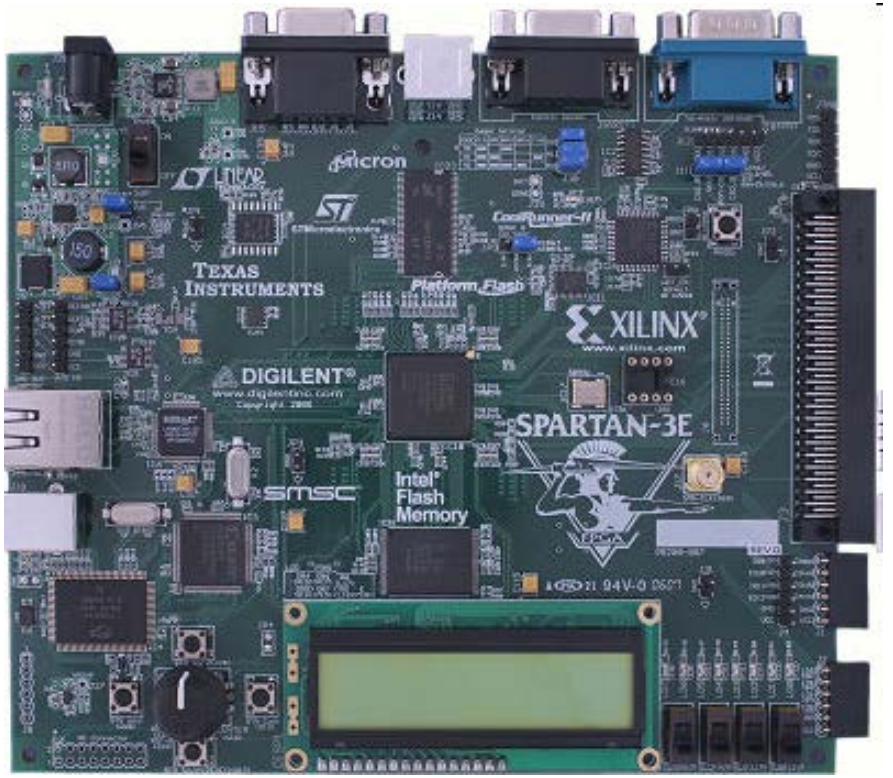
Project – Tools

Documentation

- UKM 910 Datasheet

Software provided by us

- Xilinx ISE
  - Installed in the computer pool
  - “WebPack” version available for free (www.xilinx.com)
- CPU Simulator, assembler, debugger



Hardware provided by us

- Xilinx Spartan 3E Evaluation Board
- One board per group of students

Miscellaneous

The project is a *team effort!*

- Teams of **4** students
- There is a lot to do
  - You will **not** be able to complete the project on your own
  - You will have to **distribute** tasks inside your team
  - You will have to **keep track** of the progress of different groups inside your team to avoid bottlenecks
  - Careful **planning** of the **interfaces** between components is paramount, **before** you start with the implementation
- Consider using tools like version control, or project management techniques

Project Milestones

Project Kick-off

- Takes place before the actual implementation of the project starts
- Short presentation by each group on their overall design and implementation choices
- Discussion, suggestions

Project milestones

- Dates at which a specific component should be fully implemented
- Check-list of features
- Written report

Final review

- Submit source code
- Demonstrate working calculator on the FPGA board
- Final presentation

Grading of the project

- Teams of 4 students: **One grade per group**.

- Grading of the project is as follows:
  - 30% Milestones → 10% each
    checklist, code, report
  - 20% Final source code
    structure, readability, commentary
  - 50% Final project review
    implementation (success, finesse),
    presentation, questions and answers
  - During the Milestones the whole group has to be present!
- Any form of **plagiarism** will lead to failing the project for the whole group!

Preliminary course plan

Date	10:00 – 11:30 Lecture Room	12:00 – 13:30 MST Pool
18.04.2018	Introduction	Overview of Exercises and Project VHDL 1 and Exercise: VHDL 1
25.04.2018	VHDL 2 and Exercise: VHDL 1	Exercise: VHDL 2 Introduction of Project
02.05.2018	Processor Design 1	Exercise: Processor Implementation in VHDL 1 Student groups are final
09.05.2018	Processor Design 2	Exercise: Processor Implementation in VHDL 2
16.05.2018	Project Kick-off: Students present their approach to the project, Introduction to FPGA evaluation boards	Project “Support”
23.05.2018	Pentecost holidays – Pfingstferien	
30.05.2018	Logic Synthesis	Project Milestone 1
06.06.2018	Timing in Combinatorial Logic Circuits	Project “Support”
13.06.2018	Timing in Combinatorial Logic Circuits 2	Project Milestone 2
20.06.2018	Interconnect	Exercise: Timing Combinatorial (Lecture Room) Project “Support”
27.06.2018	Timing in Sequential Logic Circuits	Project Milestone 3
04.07.2018	Design for Test	Exercise: Test and Timing Sequential (Lecture Room) Project “Support”
11.07.2018	Low Power Digital Design	Project Milestone 4
18.07.2018	Final Project Presentation and Review (Lecture Room)	Final Project Presentation and Review (Lecture Room)