Analysis of HK-MASH Delta-Sigma Modulators with and without Dithering

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***Abstract*—This report presents a spectral analysis of HK-MASH (Hildebrand-Kaiser MASH) Delta-Sigma Modulators (DSMs) implemented with varying accumulator bit-widths (4-bit, 9-bit, 20-bit). We also compare performance with and without dithering applied to the quantization stages. Time-domain and power spectral density (PSD) results are analyzed to determine the impact on quantization noise shaping and spurious suppression.**

***Index Terms*—Delta-Sigma Modulation, HK-MASH, Dithering, Quantization Noise, Power Spectral Density**

I. Introduction

Delta-Sigma Modulators (DSMs) are widely used in digital signal processing and communication systems to perform high-resolution analog-to-digital or digital-to-analog conversion. Among these, the Multi-stage Noise Shaping (MASH) topology enables high-order noise shaping using a modular approach. The HK-MASH implementation uses high-precision feedback methods and is robust against non-idealities. Dithering is often employed in DSMs to decorrelate quantization noise and signal, helping to suppress tonal spurs in the output spectrum. This work compares the spectral performance of HK-MASH modulators across varying accumulator resolutions and evaluates the effectiveness of dithering.

A. Theory and Background

The quantization process in DSMs introduces error that can be modeled as additive noise. In standard DSMs, this noise is shaped by the modulator's transfer function, pushing quantization noise power to higher frequencies outside the signal band of interest. The noise transfer function (NTF) of an L-order DSM can be expressed as:

$$\text{NTF}(z) = (1 - z^{-1})^L \tag{1}$$

For a MASH architecture with cascaded first-order stages, the effective NTF becomes increasingly steeper, resulting in better in-band noise suppression.

B. HK-MASH Architecture

The Hildebrand-Kaiser MASH architecture introduces high-precision feedback mechanisms that improve stability and robustness. A key advantage is the ability to maintain performance even with lower bit-width accumulators, which can reduce hardware complexity and power consumption.

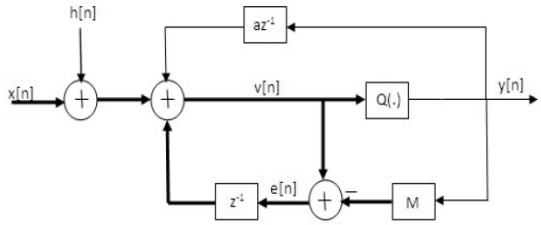

Fig. 1: EFM Block diagram of the implemented HK-MASH 1-1-1 architecture

II. Design Overview

The following Verilog modules and testbenches are used:

- RTL Files: `dff.v`, `hk_efm.v`, `hk_mash111.v`, `hk_mash111_dithered.v`, `ncl.v`
- Testbenches: `tb_hk_mash111.v`, `tb_dither.v`
- Output Datasets: Simulation output text files for 4-bit, 9-bit, 20-bit, and 24-bit configurations (with and without dither)
- Analysis Script: `PSD.m` (used to compute and plot PSD and time domain plots)

A. Implemented Architecture

The implemented HK-MASH modulator consists of a 1-1-1 cascade of first-order stages. Each stage includes:

- First-order accumulator with variable bit-width
- Single-bit quantizer
- Error feedback path
- (Optional) dithering input to the quantizer

The overall architecture is shown in Figure **??**.

III. Simulation Setup

Each simulation produces a text file with raw modulator output data, which is analyzed using MATLAB. The script `PSD.m` generates PSD plots and time-domain signal plots. Dithering is applied using a pseudorandom binary sequence as additive input to the second stage of the efm.

IV. Results and Analysis

A. Bit-width Comparison (No Dither)

Figures 2, 3, and 4 show the PSDs for 4-bit, 9-bit, and 20-bit MASH implementations without dither. Increasing

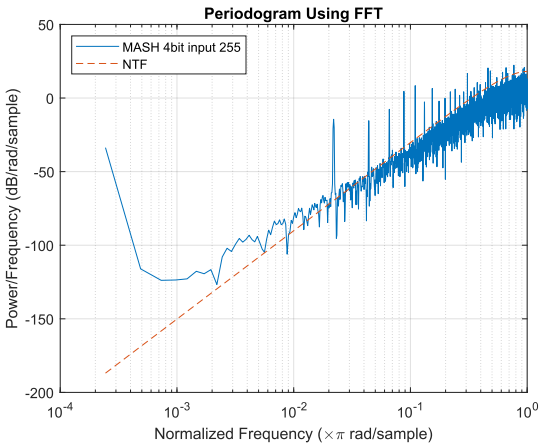

Fig. 2: PSD of 4-bit HK-MASH DSM (no dither)

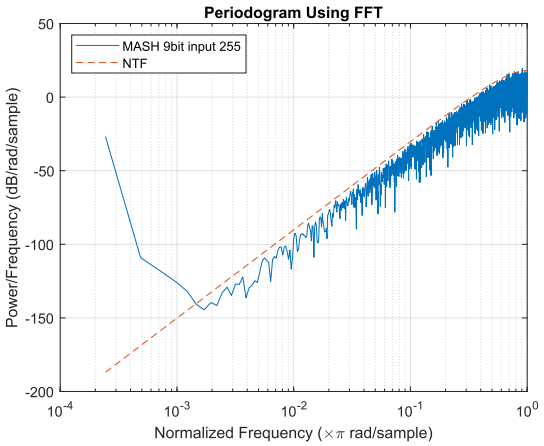

Fig. 3: PSD of 9-bit HK-MASH DSM (no dither)

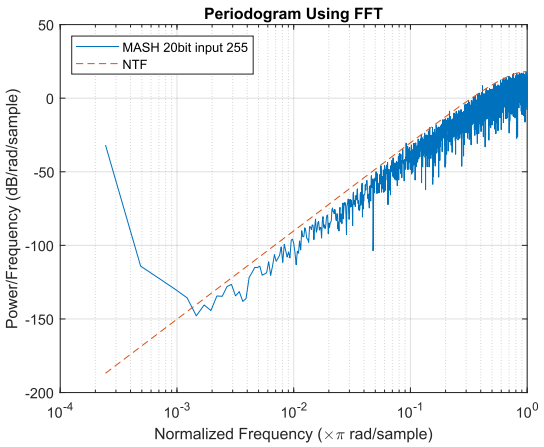

Fig. 4: PSD of 20-bit HK-MASH DSM (no dither)

the bit-width improves noise shaping and reduces in-band noise. The 20-bit version provides significantly better spurious suppression and dynamic range. From the PSD plots, we observe:

- 4-bit implementation shows visible tonal spurs and limited noise shaping
- 9-bit implementation demonstrates improved noise floor with some residual tonality
- 20-bit implementation achieves near-ideal third-order noise shaping with a clean 18 dB/octave slope

B. Effect of Dithering

Figures 5 and 6 compare PSDs with dither applied.

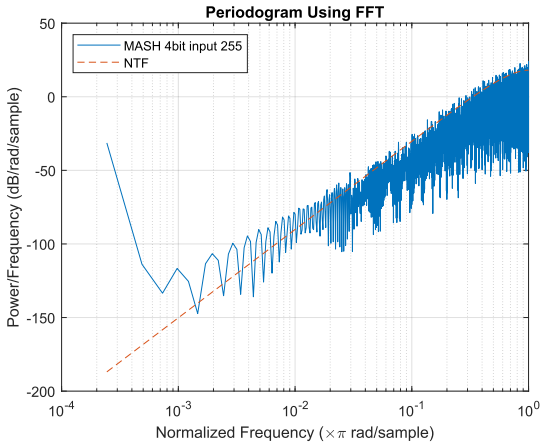

Fig. 5: PSD of 4-bit HK-MASH DSM with dither

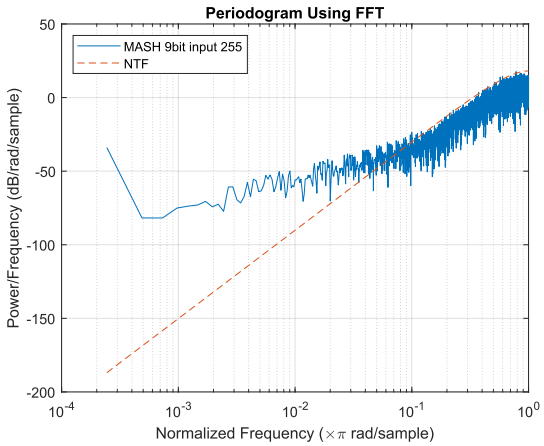

Fig. 6: PSD of 9-bit HK-MASH DSM with dither

Dithering improves the spectral purity by removing tonal spurs. This effect is more prominent at lower bit-widths, where quantization error dominates. The most significant improvements occur in the 9-bit implementation, where dithering effectively randomizes the pattern of quantization error. The application of dithering introduces a slight noise floor increase but significantly improves the overall spectral characteristics by:

- Breaking up pattern dependencies between input signal and quantizer output
- Whitening the quantization noise spectrum
- Reducing harmonic distortion components

C. Time-Domain Behavior

Figures 7 and 8 show the time-domain output of the 20-bit MASH design with and without dither. Dithered output appears more randomized, confirming the de-correlation of signal and quantization noise. The time-domain analysis reveals:

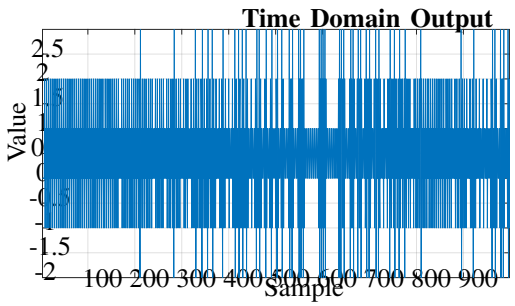

Fig. 7: Time-domain output: 20-bit HK-MASH DSM (no dither)

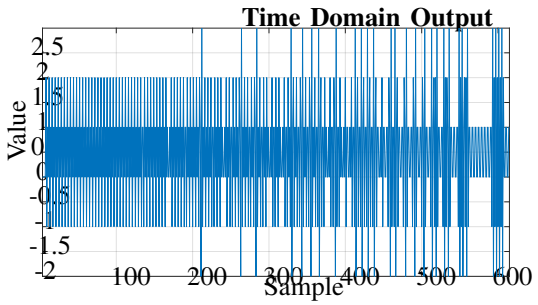

Fig. 8: Time-domain output: 20-bit HK-MASH DSM with dither

- Non-dithered output exhibits repeating patterns, indicating potential tonal behavior
- Dithered output shows more random transitions, consistent with whitened quantization noise
- Both outputs maintain the underlying sinusoidal pattern of the input signal

V. Hardware Implementation Considerations

The HK-MASH architecture offers several advantages for hardware implementation. The modular structure allows for efficient pipeline design, and the first-order stages are inherently stable. Key implementation considerations include:

A. Clock Domain Considerations

The modulator performance is sensitive to clock jitter, particularly in high-resolution implementations. The simulations assume ideal clocking conditions, but practical implementations require careful clock domain management.

VI. Conclusion

The HK-MASH DSM exhibits improved performance with increased accumulator bit-width. Dithering effectively reduces tonal spurs and enhances spectral flatness. For high-fidelity applications, a dithered 20-bit configuration provides the best overall performance, achieving near-theoretical third-order noise shaping. The key findings of this study are:

- Bit-width scaling provides significant performance improvements, with diminishing returns beyond 20 bits
- Dithering is most effective at lower bit-widths but beneficial at all resolutions
- The HK-MASH architecture achieves excellent noise shaping and spurious suppression even at moderate bit-widths
- The combination of optimal bit-width selection and dithering allows for efficient hardware implementation with excellent performance

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Code Repository

The project structure is preserved for reproducibility. Please refer to the original folder structure uploaded in Overleaf. `\HK-MASH-DDSM \PSD`