a

b

I0

I1

y_i

O

RTL_XOR

y

Name Value

y 1

a 1

b 0

41.667 ns

10 ns   20 ns   30 ns   40 ns   50 ns

m1

a   cout

b   s

half_addr

a

b

cin

m2

a   cout

b   s

half_addr

I0

I1

m3_i

O

RTL_OR

cout

sum

a

b

I0

I1

cout_i

O

RTL_AND

cout

I0

I1

s_i

O

RTL_XOR

s

Name	Value
a	1
b	1
cin	1
s	1
cout	1

0 ns   10 ns   20 ns   30 ns   40 ns   50 ns   60 ns   70 ns   80 ns

Name	Value
a	1
b	1
s	0
cout	1

0 ns   10 ns   20 ns   30 ns   40 ns   50 ns   60 ns

a[3:0]

b[3:0]

cin

m0

a

b

cin

full_addr

cout

s

m1

a

b

cin

full_addr

cout

s[3:0]

m2

a

b

cin

full_addr

cout

s

m3

a

b

cin

full_addr

cout

s

cout

Name	Value	0 ns	5 ns	10 ns	15 ns	20 ns	25 ns	30 ns	35 ns	40 ns	45 ns	50 ns	55 ns	60 ns	65 ns
s[3:0]	15		15			0						15			
cin	0														
a[3:0]	7		13			5						7			
b[3:0]	8		2			10						8			
cout	0														

i[0:7]

s[2:0]

m1

i[0:3]

s[1:0]

mux_4x1

y

m2

i[0:3]

s[1:0]

mux_4x1

y

m3

i[0:1]

s

mux_2x1

y

y

Untitled 1

Name	Value	0 ns	20 ns	40 ns	60 ns	80 ns
i[0:7]	00101101				00101101	
s[2:0]	110	101	100	001		110
y	0					

Untitled 2

Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 ns	80 ns	90 ns
y[0:7]	01000000	00100000		00000100		00000001				01000000	
i	1										
s[2:0]	001	010		101		111				001	

y_i

i

S=3'b000 I0[7:0]
S=3'b001 I1[7:0]
S=3'b010 I2[7:0]
S=3'b011 I3[7:0]
S=3'b100 I4[7:0]
S=3'b101 I5[7:0]
S=3'b110 I6[7:0]
S=3'b111 I7[7:0]

O[7:0] → y[0:7]

Net: <const0>
Type: GROUND
Cell pin count: 57
Number of ports: 0.

S[2:0] RTL_MUX

s[2:0]

temp_i

i[7:0] → A[7:0] O[2:0]

RTL_ROM

temp_i__0

S=1'b1 I0[2:0]
S=default I1[2:0]

O[2:0] → y[3:0]

S RTL_MUX

s

Untitled 2

Name	Value	20 ns	40 ns	60 ns	80 ns	100 ns	120
y[3:0]	0011	0100	0001	0111			0011
i[7:0]	00001000	00010000	00000010	10000000			00001000
s	1						

temp_i

i[2:0] → A[2:0] O[7:0]

RTL_ROM

temp_i__0

S=1'b1 I0[7:0]
S=default I1[7:0]

O[7:0] → y[7:0]

S RTL_MUX

s

Untitled 1

Name	Value	0 ns	20 ns	40 ns	60 ns	80 ns	100 ns	120 ns	140
y[7:0]	00000010	01000000	00000100	10000000				00000010	
i[2:0]	001	110	010	111				001	
s	1								

RTL_REG_SYNC (schematic)

clk, clr, q_reg[3:0], RST, SET, C, D, Q, q[3:0], n/c

Arithmetic unit (schematic)

a[3:0], b[3:0], op[1:0], y[7:0]

temp0_i — I0[3:0], I1[3:0], O[4:0], RTL_ADD (+)
temp0_i__0 — I0[3:0], I1[3:0], O[7:0], RTL_SUB (-)
temp0_i__1 — I0[3:0], I1[3:0], O[7:0], RTL_MULT (*)
temp0_i__2 — I0[3:0], I1[3:0], O[3:0], RTL_DIV (/)

temp_i (RTL_MUX):
S=2'b00 I0[4:0]
S=2'b01 I1[7:0]
S=2'b10 I2[7:0]
S=2'b11 I3[3:0]
O[7:0], S[1:0]

Untitled 1 (waveform)

Name	Value
q[3:0]	0001
clr	0
clk	0

q[3:0]: 0001 1000 0100 0010 0001 1000 0100 0010 0001 1000 0100 0010 0001 1000 0100 0010 0001 1000 0100 0010 0001 1000

Untitled 2 (waveform)

Name	Value
y[7:0]	00000010
op[1:0]	11
a[3:0]	1100
b[3:0]	0110

y[7:0]: 00001101, 00001001, 00010100, 00000010
op[1:0]: 00, 01, 10, 11
a[3:0]: 1011, 1100, 1010, 1100
b[3:0]: 0010, 0011, 0010, 0110

RTL_ROM (schematic)

in[3:0], y_i, A[3:0], O[6:0], y[6:0]

Untitled 3 (waveform)

Name	Value
y[6:0]	1111011
in[3:0]	1001
i[31:0]	0000000000000000...

y[6:0]: 1111110, 0110000, 1101101, 1111001, 0110011, 1011011, 1011111, 1110000, 1111111, 1111011
in[3:0]: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001